10kHz to 150kHz Digitally Controlled Antialiasing Filter and 4-Bit P.G.A.

FEATURES

- **4-Bit Digitally Controlled 8th-Order Lowpass Filter**
  - **f_{CUTOFF} Adjustable from 10kHz to 150kHz in 10kHz Steps**
  - **100dB Attenuation at 2.5 × f_{CUTOFF}**
- **4-Bit Digitally Controlled Programmable Gain Amplifier**
  - **G = 1 to 16 in 1V/V Steps**
- Miniature 16-Pin SSOP Package
- No External Components
- 122dB Total System Dynamic Range
- Rail-to-Rail Input and Output Range
- 2.7V to 10V Operation
- Low Noise Mute Mode
- Low Power Shutdown Mode
- Available in 16-Lead Plastic SSOP Package

APPLICATIONS

- Antialias or Reconstruction Filtering
- DSP Systems
- Communications Systems
- Scientific Instruments
- High Resolutions (16 Bits to 20 Bits)
- Processing Signals Buried in Noise
- Audio Signal Processing
- Programmable Data Rates
- Automatic Gain Control (AGC)
- Single Part Replacing Multiple Filters

DESCRIPTION

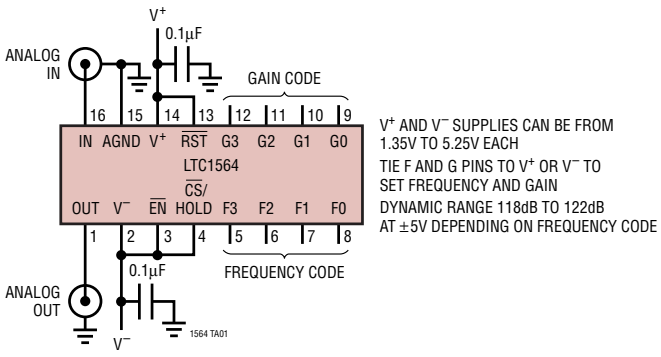
The LTC®1564 is a new type of continuous time filter for antialiasing, reconstruction and other band-limiting applications. No other analog components or filter expertise are needed to use it. There is one analog input pin and one analog output pin. The cutoff frequency (f_C) and gain are programmable while the shape of the lowpass response is fixed. A latching digital interface stores f_C and gain settings or it can be bypassed for control directly from the pins. The LTC1564 operates from 2.7V to 10V total (single or split supplies) and comes in a 16-pin surface mount SSOP.

The LTC1564 is a rail-to-rail high resolution 8th-order lowpass filter with two stopband notches, giving approximately 100dB attenuation at 2.5 times the passband cutoff frequency f_C (a de-facto standard for DSP front ends). Signals with low or variable levels can be normalized with the built-in variable gain that reduces input-referred noise with increasing gain for a typical dynamic range (maximum signal level to minimum noise) of 122dB (20 equivalent bits) with 20kHz f_C and 118dB at 100kHz f_C on a ±5V supply.

Other frequency-response shapes can be provided upon request. Please contact LTC Marketing.

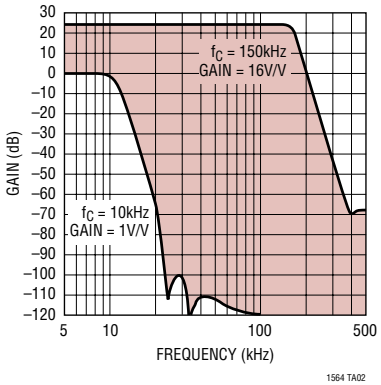
TYPICAL APPLICATION

Low Noise Programmable Filter with Variable Gain



V+ AND V– SUPPLIES CAN BE FROM 1.35V TO 5.25V EACH
TIE F AND G PINS TO V+ OR V– TO SET FREQUENCY AND GAIN
DYNAMIC RANGE 118dB TO 122dB AT ±5V DEPENDING ON FREQUENCY CODE

LTC1564 Programmable Range

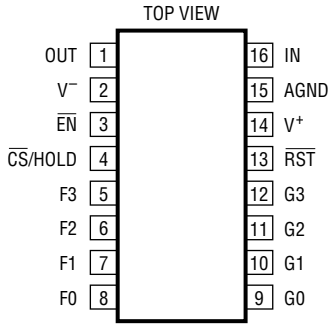


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 11V
Input Voltage ..... $V^+ + 0.3V$ to $V^- - 0.3V$
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
LTC1564C ..... 0°C to 70°C
LTC1564I ..... –40°C TO 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC1564CG
LTC1564IG

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±2.375V, f_C = 10kHz, gain = 1, R_L = 10k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Voltage			2.7		10.5	V
Supply Current	V_S = ±1.35V, V_{IN} = 0V V_S = ±2.375V, V_{IN} = 0V V_S = ±5V, V_{IN} = 0V	● ● ●		15 16 22	17 18.5 25	mA mA mA
Output Voltage Swing	R_L = 10k to 0V	●	4.5	4.65		V_{P-P}
Output Short-Circuit Current	V_S = ±5V	●		±10		mA
DC Offset Voltage Magnitude (Referred to Input)	Gain = 1, 0°C to 70°C Gain = 1, –40°C to 85°C Gain = 10, 0°C to 70°C Gain = 10, –40°C to 85°C	● ● ● ●		3 3 1 1	13 16 5 6	mV mV mV mV
DC AGND Reference Voltage	V_S = Single 5V Supply			2.5		V
Passband Gain	f_C = 50kHz, f_{IN} = 10kHz, Gain = 1 f_C = 50kHz, f_{IN} = 10KHz, Gain = 16	● ●	–0.1 23.5	0.3 24.2	0.8 25.3	dB dB
Passband Ripple	f_C = 10kHz, 0 ≤ f_{IN} ≤ 9kHz (Notes 2, 3) f_C = 150kHz, 0 ≤ f_{IN} ≤ 135kHz (Notes 2, 3)	● ●	–0.5 –0.6		0.5 1.6	dB dB
Roll Off at Cutoff Frequency (f_C) (Note 3)	f_C = 10kHz (F = 0001) f_C = 150kHz (F = 1111)	● ●	–1.2 –1.5	–0.7 –0.5	–0.3 0.6	dB dB
Roll Off at $2f_C$ (Note 3)	f_C = 10kHz	●	–67	–63	–59	dB
Roll Off at $2.5f_C$ (Note 3)	f_C = 10kHz			–99		dB
Wideband Noise (Referred to Input)	BW = 20kHz, f_C = 10kHz, Gain = 1 BW = 20kHz, f_C = 10kHz, Gain = 16 BW = 200kHz, f_C = 100kHz, Gain = 1			33 2.5 50		μV_{RMS} μV_{RMS} μV_{RMS}
Total Harmonic Distortion	f_C = 100kHz, f_{IN} = 10kHz, V_{IN} = $1V_{RMS}$			–86		dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±2.375V, f_C = 10kHz, gain = 1, R_L = 10k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Impedance	Gain = 1, DC V_{IN} = 0V Gain = 16, DC V_{IN} = 0V			10 625		kΩ Ω
Output Impedance	f_C = 10kHz, f = 10kHz			30		Ω
Mute State (F = 0000) Gain	F = 0000, f_{IN} = 20kHz, V_{IN} = 1V_{RMS}			–103		dB
Mute State Output Noise	F = 0000, BW = 200kHz			5.4		μV_{RMS}
Shutdown Supply Current	V_S = ±1.35V, $\overline{EN}$ to V^+ V_S = ±1.35V, $\overline{EN}$ to V^+	 ●		45	75 150	µA µA
	V_S = ±2.375V, $\overline{EN}$ to V^+ V_S = ±2.375V, $\overline{EN}$ to V^+	 ●		100	150 180	µA µA
	V_S = ±5V, $\overline{EN}$ to V^+ (Note 4)			175		µA
Digital Input "High" Voltage	V_S = ±1.35V V_S = ±2.375V V_S = ±5V		1.08 1.90 4.50			V V V
Digital Input "Low" Voltage	V_S = ±1.35V V_S = ±2.375V V_S = ±5V				–1.08 –1.90 0.50	V V V
Digital Input Pull-Up or Pull-Down Current (Note 5) (Digital Inputs Other than $\overline{EN}$)	V_S = ±1.35V V_S = ±5V	● ●		3.5 13	6 20	µA µA
Digital Input Pull-Up Current ($\overline{EN}$ Input)	V_S = ±1.35V V_S = ±5V	● ●		1 10	2 20	µA µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Response is tested in production at discrete frequencies f_{IN} of 0.1, 0.5, 0.8 and 0.9 times f_C.

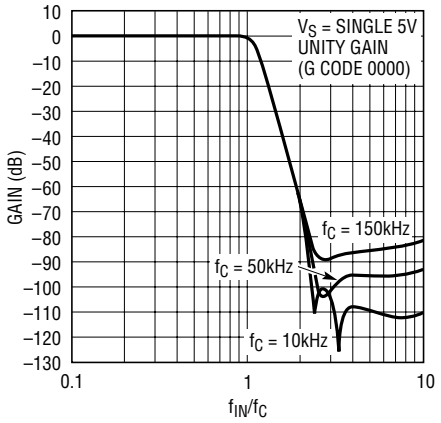
Note 3: Relative to gain at 0.1f_C.

Note 4: All digital inputs driven rail-to-rail. When driving digital inputs with 0V and 5V levels, the shutdown current will increase to 3.5mA (typ).

Note 5: Each digital input includes a small positive or negative current source to float the CMOS input to V^+ or $V^–$ potential if it is unconnected. The table shows the current due to this source when the input is driven at the supply voltage opposite from the float potential. Pins $\overline{CS}$/HOLD, F3, F2, F0 and G3 to G0 float to the $V^–$ voltage, pins $\overline{RST}$, $\overline{EN}$ and F1 to the V^+ voltage. See "Floatable Digital Inputs" in Applications Information section.

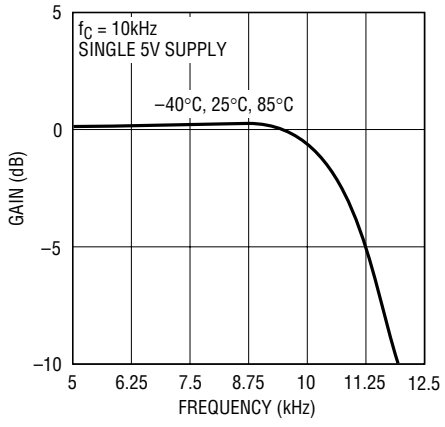
TYPICAL PERFORMANCE CHARACTERISTICS

Overall Frequency Response (Frequency Scales Normalized to f_C)



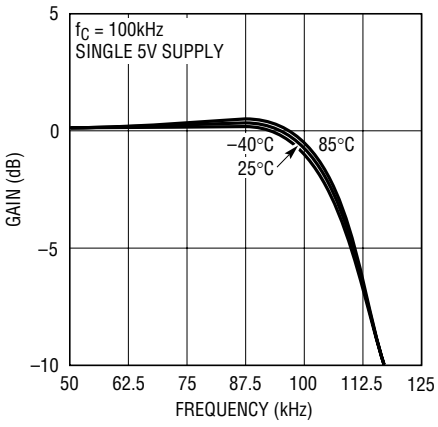
1564 G01

Roll-Offs Over Temperature (f_C = 10kHz)



1564 G02

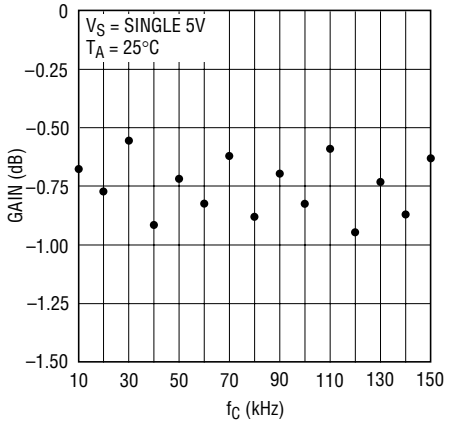
Roll-Offs Over Temperature (f_C = 100kHz)



1564 G03

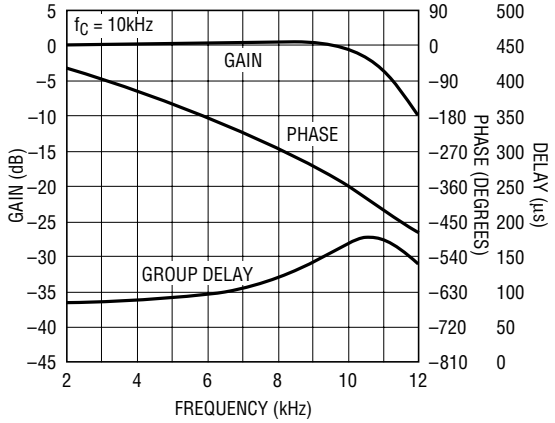
TYPICAL PERFORMANCE CHARACTERISTICS

Passband Roll-Off at $f_{IN} = f_C$ vs f_C



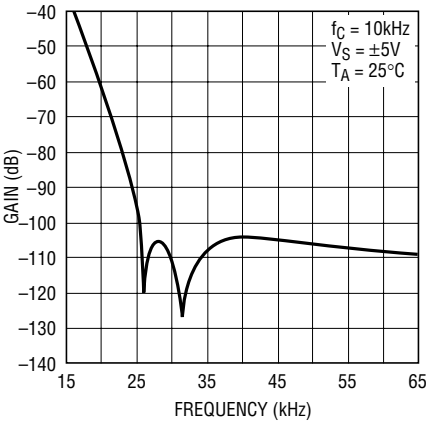
1564 G04

Passband Gain, Phase and Group Delay



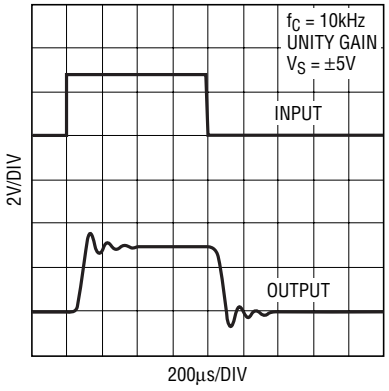
1546 G06

Detail of Stopband Response



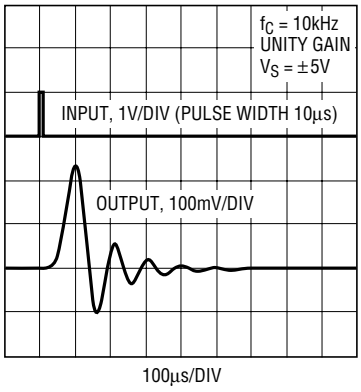
1564 G05

Rectangular Pulse Response



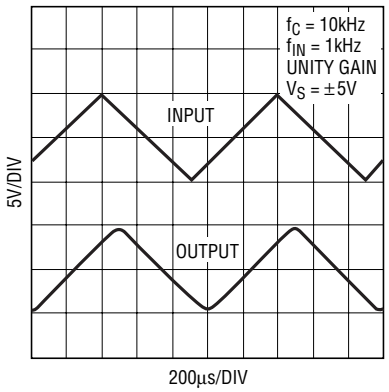
1564 G07

Short-Pulse Response



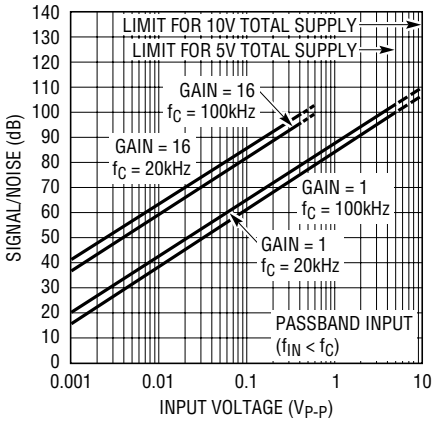
1564 G08

Triangular-Wave Time Response



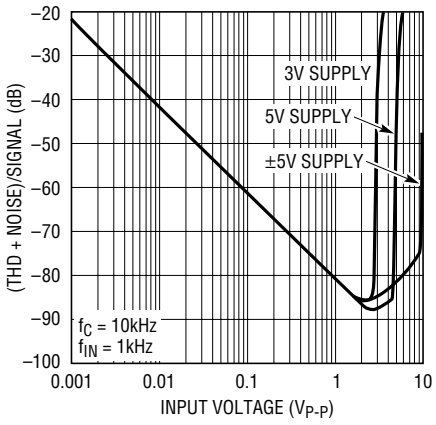
1564 G09

SNR vs Input Voltage



1564 G10

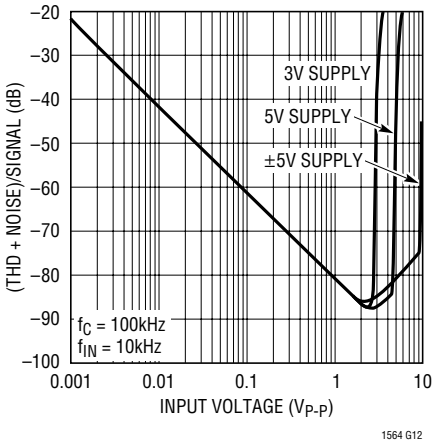
THD + Noise vs Input Voltage (f_C = 10kHz)



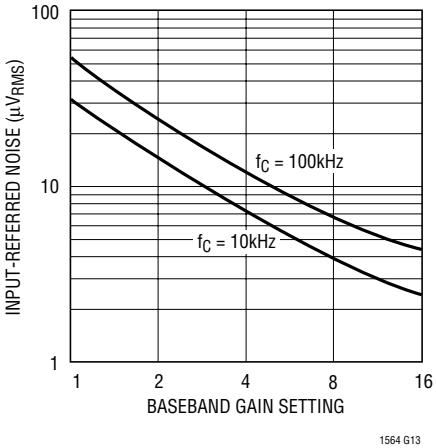
1564 G11

TYPICAL PERFORMANCE CHARACTERISTICS

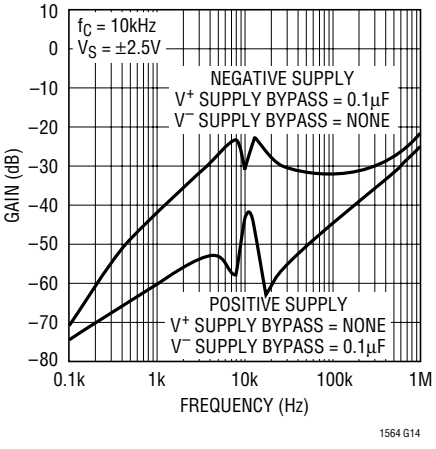
THD + Noise vs Input Voltage (f_C = 100kHz)



Noise vs Frequency and Gain Settings



Power Supply Rejection vs Frequency



PIN FUNCTIONS

OUT (Pin 1): Analog Output. In normal filtering, this is the output of an internal operational amplifier and is capable of swinging essentially to any voltage between the power supply rails (that is, between V^+ and V^-). This output is designed to drive a nominal load of 5k and 50pF. For lowest signal distortion it should be loaded as lightly as possible. The output can drive lower resistances than 5k, but distortion may increase, and the output current will limit at approximately ±10mA. Capacitances higher than 50pF should be isolated by a series resistor of 500Ω to preserve AC stability. In the Mute state (F code 0000 or $\overline{RST}$ = 0), the output operates as in normal filtering but the gain from the IN pin becomes zero and the output noise is reduced. In the shutdown state ($\overline{EN}$ = 1 or $\overline{EN}$ open circuited), most of the circuitry in the LTC1564 shuts off and the OUT pin assumes a high impedance state.

V^-, V^+ (Pins 2, 14): Power Supply Pins. The V^+ and V^- pins should be bypassed with 0.1μF capacitors to an adequate analog ground plane using the shortest possible wiring. Electrically clean supplies and a low impedance ground are important for the high dynamic range and high stopband suppression available from the LTC1564 (see further details under AGND). Low noise linear power supplies are recommended. Switching supplies are not recommended because of the inevitable risk of their switching noise coupling into the signal path, reducing dynamic range.

$\overline{EN}$ (Pin 3): CMOS-Level Digital Chip Enable Input. Logic 1 or open circuiting this pin causes a shutdown mode with reduced supply current. The active circuitry in the LTC1564 shuts off and its output assumes a high impedance state. If F and G bits are latched ($\overline{CS}$/HOLD = 1) during the shutdown state, the latch will retain its contents.

A small pull-up current source at the $\overline{EN}$ input causes the LTC1564 to be in shutdown state if the $\overline{EN}$ pin is left open. Therefore, the user must connect the $\overline{EN}$ pin to logic 0 (V^- or optionally 0V with ±5V supplies) for normal filter operation.

$\overline{CS}$/HOLD (Pin 4): CMOS-Level Digital Enable Input for the Latch Holding F and G Bits. Logic 0 makes the latch transparent so that the F and G inputs directly control the filter's cutoff frequency and gain. Logic 1 holds the last values of these inputs prior to the transition. This pin floats to logic 0 (V^-) when open circuited because of a small current source (see Electrical Characteristics, Note 5).

F3, F2, F1, F0 (Pins 5, 6, 7, 8): CMOS-Level Digital Frequency Control ("F Code") Inputs. F3 is the most significant bit (MSB). These pins program the LTC1564's cutoff frequency f_C through the internal latch, which

PIN FUNCTIONS

passes the bits directly when the $\overline{CS}$/HOLD input is at logic 0. When $\overline{CS}$/HOLD changes to logic 1, the F pins cease to have effect and the latch holds the previous values. The F code controls the filter's cutoff frequency f_C in 10kHz steps up to 150kHz, as summarized in Table 1.

Table 1

F3	F2	F1	F0 (AT OUTPUT OF INTERNAL LATCH)	NOMINAL F_C (CUTOFF FREQUENCY)
0	0	0	0	0 (Mute State: Filter Gain is Zero)
0	0	0	1	10kHz
0	0	1	0	20kHz
0	0	1	1	30kHz
0	1	0	0	40kHz
0	1	0	1	50kHz
0	1	1	0	60kHz
0	1	1	1	70kHz
1	0	0	0	80kHz
1	0	0	1	90kHz
1	0	1	0	100kHz
1	0	1	1	110kHz
1	1	0	0	120kHz
1	1	0	1	130kHz
1	1	1	0	140kHz
1	1	1	1	150kHz

Thus f_C is proportional to the binary value of the F code. Note that small current sources pull F1 to V^+ and F3, F2 and F0 to V^- when these pins are left unconnected (see Electrical Characteristics, Note 5). This sets an F code input of 0010 (2, in decimal form) by default, giving an f_C of 20kHz in normal filtering operation, if $\overline{CS}$/HOLD is logic 0 or is open circuited.

G0, G1, G2, G3 (Pins 9, 10, 11, 12): CMOS-Level Digital Gain Control ("G Code") Inputs. G3 is the most significant bit (MSB). These pins program the LTC1564's passband gain through the internal latch, which passes the bits directly when the $\overline{CS}$/HOLD input is at logic 0. When $\overline{CS}$/HOLD changes to logic 1, the G pins cease to have effect and the latch retains the previous input values. This gain control is linear in amplitude: nominal passband gain of the LTC1564 is the binary value of the G code, plus one as shown in Table 2.

Note that small current sources pull the G pins to V^- when these pins are left unconnected (see Electrical Characteristics, Note 5). This sets a G code input of 0000 by default, giving unity passband gain in normal filtering operation, if $\overline{CS}$/HOLD is logic 0 or is open circuited.

$\overline{RST}$ (Pin 13): CMOS-Level Asynchronous Reset Input. Logic 0 on this pin immediately resets the internal F and G latch to all zeros, regardless of the state of the $\overline{CS}$/HOLD pin or the F or G input pins. This causes the LTC1564 to enter a mute state (powered but with zero signal gain) because of the resulting F = 0000 command. Logic 1 permits the other pins to control F and G. This pin floats to logic 1 (V^+) when open circuited because of a small current source (see Electrical Characteristics, Note 5). A brief internal reset (shorter than the analog settling time of the filter) also occurs when power is first applied.

Table 2

G3	G2	G1	G0 (AT OUTPUT OF INTERNAL LATCH)	NOMINAL PASSBAND GAIN (VOLT/VOLT)	(dB)	MAXIMUM INPUT SIGNAL LEVEL (VOLTS PEAK-TO-PEAK) DUAL 5V	SINGLE 5V	SINGLE 3V	NOMINAL INPUT IMPEDANCE (kΩ)
0	0	0	0	1	0	10	5.0	3.0	10
0	0	0	1	2	6.0	5	2.5	1.5	5
0	0	1	0	3	9.5	3.33	1.67	1.0	3.33
0	0	1	1	4	12	2.5	1.25	0.75	2.5
0	1	0	0	5	14.0	2	1	0.6	2
0	1	0	1	6	15.6	1.67	0.83	0.5	1.67
0	1	1	0	7	16.9	1.43	0.71	0.43	1.43
0	1	1	1	8	18.1	1.25	0.63	0.38	1.25
1	0	0	0	9	19.1	1.1	0.56	0.33	1.11
1	0	0	1	10	20.0	1.0	0.50	0.30	1
1	0	1	0	11	20.8	0.91	0.45	0.27	0.91
1	0	1	1	12	21.6	0.83	0.42	0.25	0.83
1	1	0	0	13	22.3	0.77	0.38	0.23	0.77
1	1	0	1	14	22.9	0.71	0.36	0.21	0.71
1	1	1	0	15	23.5	0.67	0.33	0.20	0.66
1	1	1	1	16	24.1	0.63	0.31	0.19	0.63

PIN FUNCTIONS

Table 3. Summary of LTC1564 Digital Controls and Modes

$\overline{EN}$	$\overline{RST}$	$\overline{CS}$/HOLD	F3	F2	F1	F0	G3	G2	G1	G0	FUNCTION
1	1	1	X	X	X	X	X	X	X	X	Shutdown Mode. Filter Disabled. Latch Holds F and G Inputs Present when Last $\overline{CS}$/HOLD = 0
1	1	0	X	X	X	X	X	X	X	X	Shutdown Mode. Filter Disabled. Latch Accepts F and G Inputs
1	0	X	X	X	X	X	X	X	X	X	Shutdown Mode. Filter Disabled. Latch Contents (F and G) Reset to All Zeros
0	1	0	0	0	0	0	X	X	X	X	Mute Mode. Filter Active, Zero Gain, Reduced Noise
0	0	X	X	X	X	X	X	X	X	X	Mute Mode. Filter Active, Zero Gain, Reduced Noise. Latch Contents (F and G) Reset to All Zeros
0	1	1	Other Than 0000				X	X	X	X	Normal Filtering Operation. Latch Holds F and G Inputs Present when Last $\overline{CS}$/HOLD = 0
0	1	0	Other Than 0000				X	X	X	X	Normal Filtering Operation. Filter Responds Directly to F and G Input Pins (See Separate Pin Descriptions)

X = Doesn't Matter

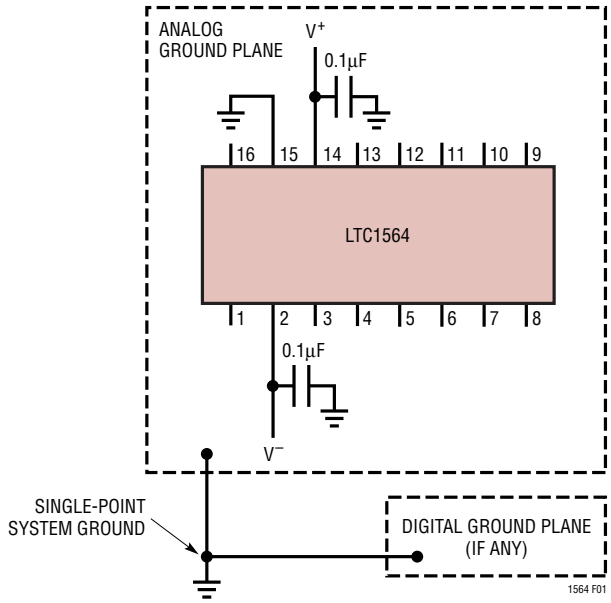


Figure 1. Dual Supply Ground Plane Connection

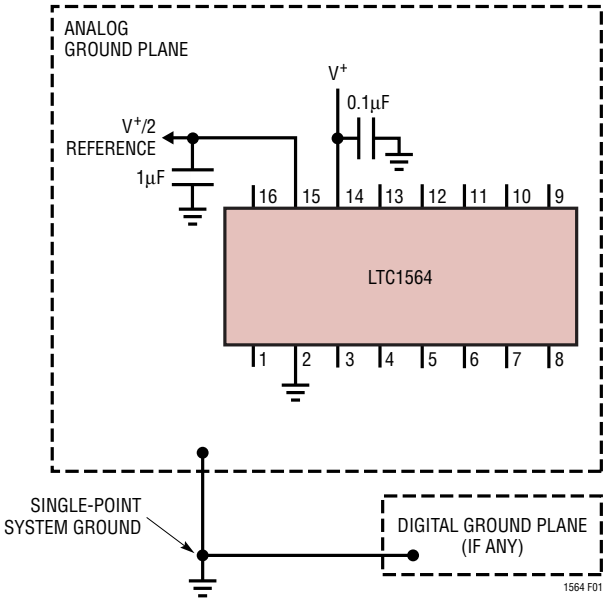


Figure 2. Single Supply Ground Plane Connection

AGND (Pin 15): Analog Ground. The AGND pin is at the midpoint of an internal resistive voltage divider, developing a potential halfway between the V^+ and V^- pins, with an equivalent series resistance to the pin of nominally 7k. (In the shutdown state, analog switch FETs interrupt the voltage-divider resistors and the AGND pin assumes a high impedance.) AGND also serves as the internal half-supply reference in the LTC1564, tied to the noninverting inputs of all internal op amps and establishing the ground reference voltage for the IN and OUT pins. Because of this, very "clean" grounding is recommended, including an analog ground plane surrounding the package. For dual supply operation, this ground plane will be tied to the 0V point and the AGND pin should connect directly to the ground plane (Figure 1). For single supply operation, in contrast, if the system signal ground is at V^-, the ground plane should tie to V^- and the AGND pin should be AC-bypassed to the ground plane by at least a 0.1µF high quality capacitor (at least 1µF for best AC performance) (Figure 2). As with all high dynamic range analog circuits, performance in an application will reflect the quality of the grounding.

PIN FUNCTIONS

IN (Pin 16): Analog Input. The filter in the LTC1564 senses the voltage difference between the IN and AGND pins. In normal filtering ($\overline{EN}$ = 0, $\overline{RST}$ = 1, F code other than 0000), the IN pin connects within the LTC1564 to a digitally controlled resistance whose other end is a current-summing point at the AGND potential. At unity gain (G code 0000), the value of this input resistance is nominally 10k and the IN voltage range is rail-to-rail (V^+ to V^-). When filtering at gain settings above unity (G code ≠ 0000), the input resistance falls as (1/gain) to nominally 625Ω at a gain of 16 (G code 1111) and the linear input range also falls in inverse proportion to gain. (The variable gain capability is designed to boost lower level input signals with good noise performance.) Input resistance does not vary significantly with the frequency-setting F code except in the mute state (F code 0000). In either the mute state (F code 0000 or $\overline{RST}$ = 0) or the shutdown state ($\overline{EN}$ = 1 or $\overline{EN}$ open circuited), analog switches disconnect the IN pin internally and this pin presents a very high input resistance. Circuitry driving the IN pin must be compatible with the LT1564's input resistance and with the variation of this resistance in the event that the LTC1564 is used in multiple modes. Signal sources with significant output resistance may introduce a gain error as the source's output resistance and the LTC1564's input resistance form a voltage divider. This is especially true at the higher gain or G code settings where the LTC1564's input resistance is lowest.

In single supply voltage applications with elevated gain settings (G code ≠ 0000) it is important to keep in mind that the LTC1564's ground reference point is AGND, not V^-. With increasing gains, the LTC1564's linear input voltage range is no longer rail-to-rail but converges toward AGND. Similarly the OUT pin swings positive or negative with respect to AGND. At unity gain (G code 0000), both IN and OUT voltages can swing from rail-to-rail.

BLOCK DIAGRAM

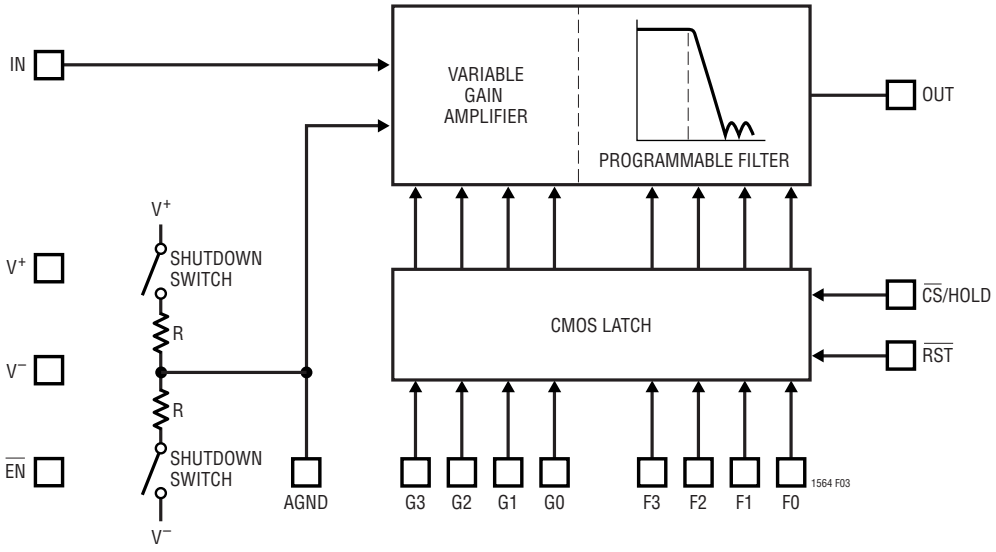


Figure 3. Block Diagram

APPLICATIONS INFORMATION

Functional Description

The LTC1564 is a self-contained, continuous time, variable gain, high order analog lowpass filter. The gain magnitude between IN and OUT pins is approximately constant for signal frequency components up to the cutoff frequency f_C and falls off rapidly for frequencies above f_C. The pins IN, OUT and AGND (analog ground) are the sole analog signal connections on the LTC1564; the others are power supplies and digital control inputs to select f_C (and to select gain if desired). The f_C range is 10kHz to 150kHz in 10kHz steps. The form of the lowpass frequency response is an 8-pole elliptic type with two stopband notches (Figure 4). This response rolls off by approximately 100dB from f_C to $2.5f_C$. The LTC1564 is laser trimmed for f_C accuracy, passband ripple, gain and offset. It delivers a combination of 100+dB stopband attenuation, 100+dB signal-to-noise ratio (SNR) and 100+kHz f_C.

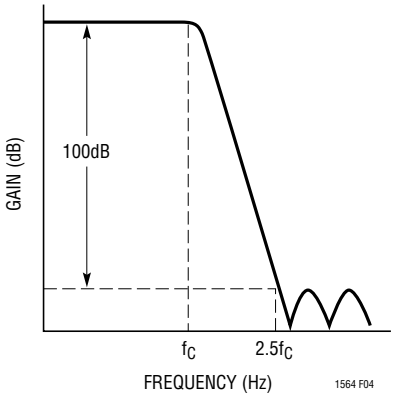


Figure 4. General Shape of Frequency Response

Figure 3 is a block diagram showing analog signal path, digital control latch, and analog ground (AGND) circuitry. A proprietary active-RC architecture filters the analog signal. This architecture limits internal noise sources to near the fundamental "kT/C" bounds for a filter of this order and power consumption. The variable gain capability at the input is an integral part of the filter, and allows boosting of low level input signals with little increase in output referred noise. This permits the input noise floor to drop steadily with increasing gain, enhancing the SNR at lower signal levels. Such a property is difficult to achieve in practice by combining separate variable gain amplifier and filter circuits.

Digital Control

Logic levels for the LTC1564 digital inputs are nominally rail-to-rail CMOS. (Logic 1 is V^+, logic 0 is V^- or alternatively 0V with ±5V supplies). The part is tested with 10% and 90% of full excursion on the inputs, thus ±1.08V at ±1.35V supplies, ±1.9V at ±2.375V and 0.5V and 4.5V at ±5V.

The f_C and gain settings are always controlled by the output of an on-chip CMOS latch. Inputs to this latch are the pins F3 through F0, G3 through G0, the latch-enable control $\overline{CS}$/HOLD and the asynchronous reset input $\overline{RST}$. A logic-0 input to $\overline{CS}$/HOLD makes the latch transparent so that the F and G input pins pass directly to the latch outputs and therefore control the filter directly. Raising $\overline{CS}$/HOLD to logic 1 freezes the latch's output so that the F and G input pins have no effect. Logic 0 at the $\overline{RST}$ input at any time resets the latch outputs to all zeros. The all-zero state, in turn, imposes a mute mode with zero gain and low output noise if the filter is powered on ($\overline{EN}$ = 0). The all-zeros condition will persist until $\overline{RST}$ is returned to logic 1, nonzero F and G inputs are set up and the latch outputs are updated by $\overline{CS}$/HOLD = 0. $\overline{EN}$ is a chip-enable input causing a shutdown state. Specific details on the digital controls appear in the Pin Functions section of this data sheet.

Floatable Digital Inputs

Every digital input of the LTC1564 includes a small current source (roughly 10µA) to float the CMOS input to V^+ or V^- potential if the pin is unconnected. Table 4 summarizes the open-circuit default levels.

Table 4. Open-Circuit Default Input Levels

INPUT	FLOATING LOGIC LEVEL	EFFECT
$\overline{EN}$	1	Shutdown State
$\overline{CS}$/HOLD	0	F and G Pins Enabled
$\overline{RST}$	1	Latch Not Reset
F3 F2 F1 F0	0 0 1 0	f_C = 20kHz
G3 G2 G1 G0	0 0 0 0	Unity Passband Gain

Note particularly that the pull-up current source at the $\overline{EN}$ pin forces the LTC1564 to the shutdown state if this pin is left open. Therefore the user *must* connect $\overline{EN}$ deliberately to a logic-0 level (V^-, or optionally 0V with ±5V supplies) for normal filter operation. The other digital inputs float to

APPLICATIONS INFORMATION

levels that program the part for enabled F and G pins ($\overline{CS}$/HOLD = 0), 20kHz f_C and unity passband gain. Therefore six connections (power pins, $\overline{EN}$ to logic 0, AGND, IN and OUT) are enough to set up a working 20kHz lowpass filter, and additional pins can be connected as necessary to select different f_C or gain.

This feature of floatable logic inputs is intended for rapid prototyping and experimentation. Floating the logic inputs is not recommended for production designs because, depending on construction details, the high impedances of these inputs may permit unwanted interference coupling and consequent erroneous digital inputs to the LTC1564.

Also, it may be necessary to consider the effect of the pull-up and pull-down current sources on the logic that drives the LTC1564. In particular, if the LTC1564 operates from ±5V but receives digital inputs from logic using 5V and 0V, CMOS logic levels will be compatible but the possibility exists of the LTC1564 pulling current out of the driving logic at those LTC1564 inputs that are capable of floating to logic 0. That is because the small current sources at these inputs return to V^-, not to 0V. If the driving logic presents a high impedance or three-state output, the LTC1564's input current may pull this output below 0V, although the current is limited to about 10μA. The system designer should be aware of this possibility and ensure that any such current flow is compatible with the driving logic.

Mute State

The Mute mode keeps the filter powered as in normal filtering but "turns off" the signal path for minimal signal transmission (approximately –100dB) and reduced output noise. This feature may be useful for gating a signal source on and off, or for system calibration procedures. Note however that the DC output in the Mute state may shift by some millivolts compared to normal filtering because the internal signal path changes. Recovery from Mute, like other transient responses in a filter, proceeds at the time scale of the filter's pole-zero time constants and therefore is faster at the higher f_C settings (that is, at the higher F codes).

The LTC1564 enters the Mute state when the F bits at the latch output (Figure 3) become 0000. (It can be remembered as a "zero-bandwidth" frequency setting.) This is achieved either by presenting a 0000 code to the F inputs and lowering the $\overline{CS}$/HOLD input to enable the latch, or alternatively at any time by lowering $\overline{RST}$, which immediately resets the latch contents to all zeroes. Such a reset also occurs normally at the application of power, unless $\overline{CS}$/HOLD is low and a nonzero pattern at the F inputs overrides the brief power-on reset. In the Mute state, the G gain-control inputs have no effect.

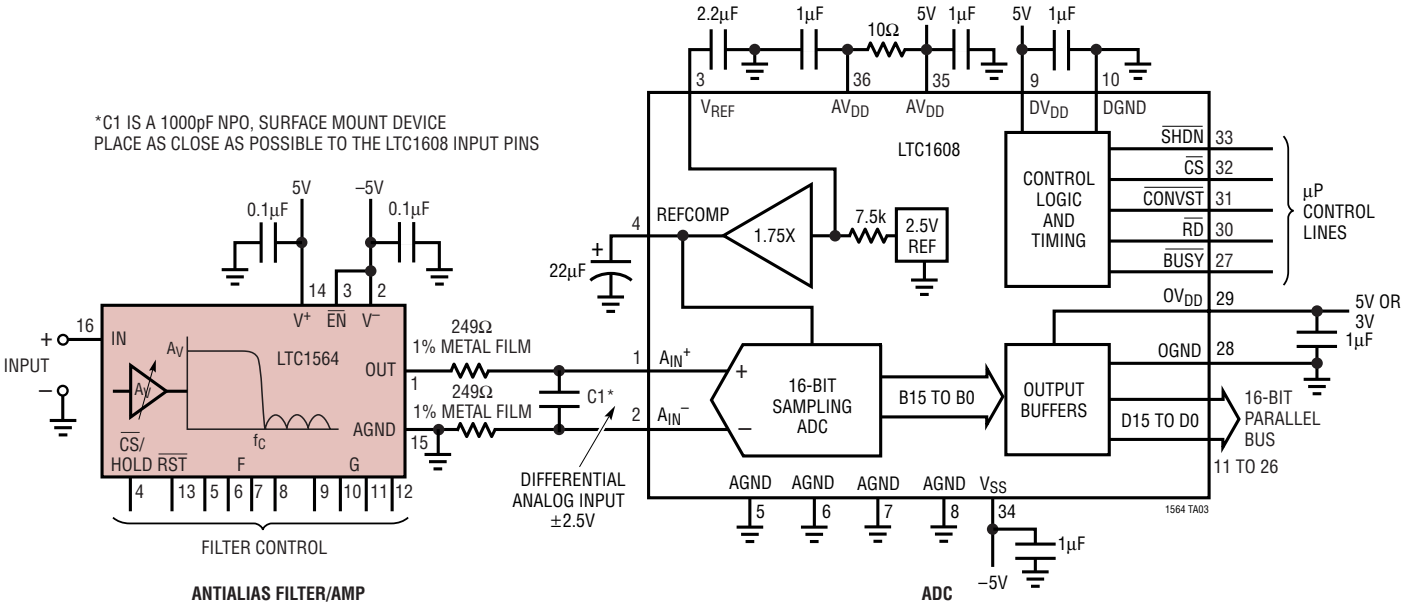
Output noise in Mute is largely thermal and wideband (unlike in normal filtering, where the filter's response affects the noise spectrum). Typical Mute-state output noise is $5.4\mu V_{RMS}$ in 200kHz measurement bandwidth and less than $3\mu V_{RMS}$ in 40kHz bandwidth. It has occasionally happened elsewhere in the electronics industry that someone would characterize a circuit or system by comparing its output level in normal operation to the noise level in a Mute state as though this were a normal signal-to-noise ratio (SNR), which it is not, because this signal and noise exist only at different times. A scrupulous name for such a measure is SMR, signal-to-mute ratio. Accordingly in a 40kHz bandwidth, the LTC1564 can exhibit an SMR exceeding 120dB.

Construction and Instrumentation Cautions

Electrically clean construction is important in applications seeking the full dynamic range or high stopband rejection of the LTC1564. Short, direct wiring will minimize parasitic capacitance and inductance. High quality supply bypass capacitors of 0.1μF near the chip provide good decoupling from a clean, low inductance power source. But several inches of wire (i.e., a few microhenrys of inductance) from the power supplies, unless decoupled by substantial capacitance (≥ 10μF) near the chip, can cause a high-Q LC resonance in the hundreds of kHz in the chip's supplies or ground reference. This may impair stopband rejection and other specifications at those frequencies. In stringent filter applications we have often found that a compact, carefully laid out printed circuit board with good ground plane makes a difference in both stopband rejection and distortion. Finally, equipment to measure filter performance can itself introduce distortion or noise floors. Checking for these limits with a wire replacing the filter is a prudent routine procedure.

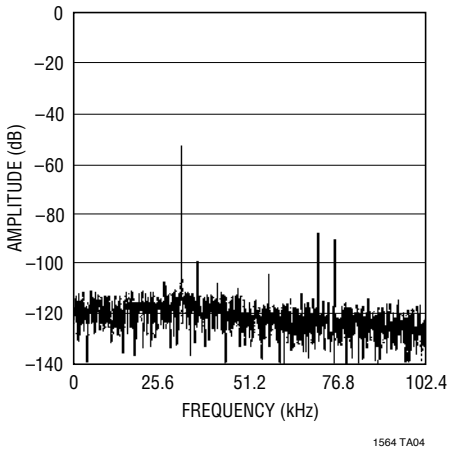
TYPICAL APPLICATIONS

2-Chip Flexible DSP Front End with Amplification, Antialias Filtering and A/D Conversion



16-Bit Output, Sampling Rate to 500ksps, Analog Bandwidth to 150kHz, Gain to 24dB. (For More Information, See *Linear Technology* Magazine, May 2001)

4096-Point FFT Spectrum with Low Level Input



Boosting a 100mV$_{RMS}$ Input Signal to Nearly Fill the Input Range of the LTC1608 ADC. Input Frequency of 40kHz, LTC1608 f$_{SAMPLE}$ = 204.8ksps, LTC1564 is Set for f$_C$ = 50kHz and Gain of 16 (F = 0101, G = 1111). Measured THD is 86dB, HD$_2$ = –88dB, SNR = 85dB with 100mV$_{RMS}$ Input. Dynamic Range of Approximately 115dB