Hot Swap Controller

FEATURES

- **Adjustable Undervoltage and Overvoltage Protection**
- **Foldback Current Limit**
- **Adjustable Current Limit Time-Out**
- **V_{CC}: 2.97V to 16.5V Normal Operation, Protected Against Surges to 33V**
- Single Channel NFET Driver
- Latch Off or Automatic Retry on Current Fault
- Driver for SCR Crowbar on Overvoltage
- Adjustable Reset Timer
- Reference Output with Uncommitted Comparator
- 16-Pin SSOP Package

APPLICATIONS

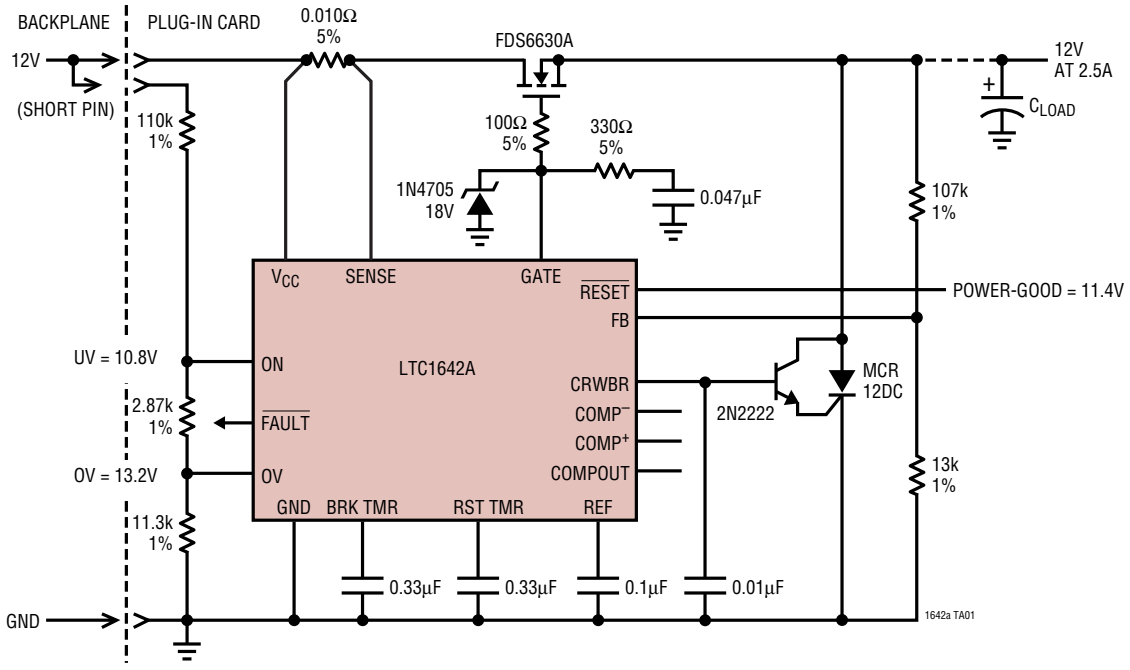
- Hot Board Insertion
- Electronic Circuit Breaker
- InfiniBand™ Systems

DESCRIPTION

The LTC®1642A is a 16-pin Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. Using an external N-Channel pass transistor, the board supply voltage can be ramped up at an adjustable rate. A high side switch driver controls the N-Channel gate for supply voltages ranging from 2.97V to 16.5V.

The SENSE pin allows foldback limiting of the load current, with circuit breaker action after an adjustable delay time. The delay allows the part to power-up in current limit. The CRWBR output can be used to trigger an SCR for crowbar protection of the load if the input supply exceeds an adjustable threshold. The $\overline{\text{RESET}}$ output can generate a system reset with adjustable delay when the supply voltage falls below an adjustable threshold. The ON pin cycles the board power. The LTC1642A is available in the 16-pin SSOP package.

TYPICAL APPLICATION

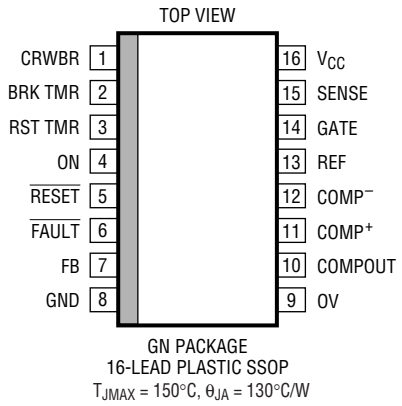


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) .....–0.3V to 33V
SENSE Pin ..... –0.3V to (V_{CC} + 0.3V)
ON, FB, OV, $COMP^+$, $COMP^-$
RESET, FAULT, COMPOUT .....–0.3V to 18.5V
Operating Temperature Range
LTC1642AC ..... 0°C to 70°C
LTC1642AI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1642ACGN LTC1642AIGN
GN PART MARKING
1642A 1642AI

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Voltage Range		●	2.97		16.5	V
I_{CC}	V_{CC} Supply Current	ON = V_{CC}	●		1.25	3.0	mA
V_{LKHI}	V_{CC} Undervoltage Lockout	V_{CC} Rising	●	2.55	2.73	2.95	V
V_{LKLO}	V_{CC} Undervoltage Lockout	V_{CC} Falling	●	2.35	2.50	2.95	V
V_{LKHYST}	V_{CC} Undervoltage Lockout Hysteresis				230		mV
V_{FB}	FB Pin Voltage Threshold	FB Falling	●	1.208	1.220	1.232	V
ΔV_{FB}	FB Pin Threshold Supply Variation	FB Falling, 2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
V_{FBHST}	FB Pin Voltage Threshold Hysteresis				3		mV
$I_{FB(IN)}$	FB Pin Input Current	V_{OV} = 5V	●		0	±1	µA
V_{OV}	OV Pin Voltage Threshold	OV Rising	●	1.208	1.220	1.232	V
ΔV_{OV}	OV Pin Threshold Supply Variation	OV Rising, 2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
V_{OVHYST}	OV Pin Voltage Theshold Hysteresis				3		mV
$I_{OV(IN)}$	OV Pin Input Current	V_{FB} = 5V	●		0	±1	µA
V_{RST}	RST TMR Pin Voltage Threshold	RST TMR Rising	●	1.200	1.220	1.250	V
ΔV_{RST}	RST TMR Pin Threshold Supply Variation	RST TMR Rising, 2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
I_{RST}	RST TMR Pin Current	Timer On Timer Off, V_{RSTTMR} = 1.5V	●	–1.5	–2.0 10	–2.5	µA mA
V_{BRK}	BRK TMR Pin Voltage Threshold	BRK TMR Rising	●	1.200	1.220	1.250	V
ΔV_{BRK}	BRK TMR Pin Threshold Supply Variation	BRK TMR Rising, 2.97V ≤ V_{CC} ≤ 16.5V	●		5	15	mV
I_{BRK}	BRK TMR Pin Current	Timer On Timer Off, V_{BRKTMR} = 1.5V	●	–15	–20 10	–30	µA mA
V_{CR}	CRWBR Pin Voltage Theshold	CRWBR Rising	●	375	410	425	mV
ΔV_{CR}	CRWBR Pin Threshold Supply Variation	2.97V ≤ V_{CC} ≤ 16.5V	●		4	15	mV
I_{CR}	CRWBR Pin Current	CRWBR On, V_{CRWBR} = 0V CRWBR On, V_{CRWBR} = 2.1V CRWBR Off, V_{CRWBR} = 1.5V	● ●	–30 –1000	–45 –1500 2.3	–60	µA µA mA

DC ELECTRICAL CHARACTERISTICS

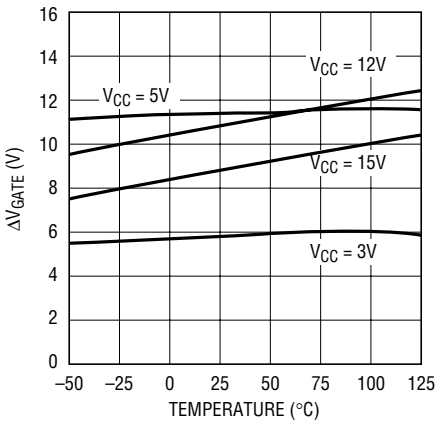
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CB}	Circuit Breaker Trip Voltage	$V_{CB} = (V_{CC} - V_{SENSE})$, V_{FB} = GND	●	15	25	36	mV
		$V_{CB} = (V_{CC} - V_{SENSE})$, V_{FB} = 1V	●	45	52.5	60	mV
		2.97V ≤ V_{CC} ≤ 16.5V,					
		$V_{CB} = (V_{CC} - V_{SENSE})$, V_{FB} = GND	●	12	25	39	mV
		$V_{CB} = (V_{CC} - V_{SENSE})$, V_{FB} = 1V	●	42	52.5	63	mV
I_{SENSE}	SENSE Pin Input Bias Current	$V_{CC} = V_{SENSE}$ = 16.5V	●			0.5	µA
I_{GATE}	GATE Pin Output Current	Charge Pump On, V_{GATE} = GND	●	–20	–25	–30	µA
		Charge Pump Off, V_{GATE} = 5V			10		mA
ΔV_{GATE}	External N-Channel Gate Drive	$V_{GATE} - V_{CC}$, V_{CC} = 2.97V	●	4.5	5.9	8.0	V
		$V_{GATE} - V_{CC}$, V_{CC} = 5V	●	10	11.5	14	V
		$V_{GATE} - V_{CC}$, V_{CC} = 15V (0°C to 70°C)	●	6.5	8.5	18	V
		$V_{GATE} - V_{CC}$, V_{CC} = 15V (–40°C to 85°C)	●	6	8.5	18	V
V_{ONHI}	ON Pin Threshold	ON Rising		1.30	1.34	1.38	V
V_{ONLO}	ON Pin Threshold	ON Falling	●	1.20	1.22	1.26	V
V_{ONHYST}	ON Pin Hysteresis				110		mV
$I_{ON(IN)}$	ON Pin Input Current	V_{ON} = 5V	●		0	±1	µA
V_{OL}	Output Low Voltage	$\overline{RESET}$, $\overline{FAULT}$, COMPOUT I_{OL} = 1.54mA	●			0.4	V
		$\overline{RESET}$, $\overline{FAULT}$ I_O = 5mA				2	V
I_{PU}	Logic Output Pull-Up Current	$\overline{RESET}$, $\overline{FAULT}$ = GND			–15		µA
V_{REF}	Reference Output Voltage	No Load	●	1.208	1.220	1.232	V
ΔV_{LNR}	Reference Supply Variation	2.97V ≤ V_{CC} ≤ 16.5V, No Load	●		5	15	mV
ΔV_{LDR}	Reference Load Regulation	I_O = 0mA to –1mA, Sourcing Only	●		2.5	7.5	mV
I_{RSC}	Reference Short-Circuit Current	V_{REF} = 0V			4.5		mA
V_{COS}	Comparator Offset Voltage	$V_{CM} = V_{REF}$	●			±10	mV
V_{CHYST}	Comparator Hysteresis	$V_{CM} = V_{REF}$			3		mV

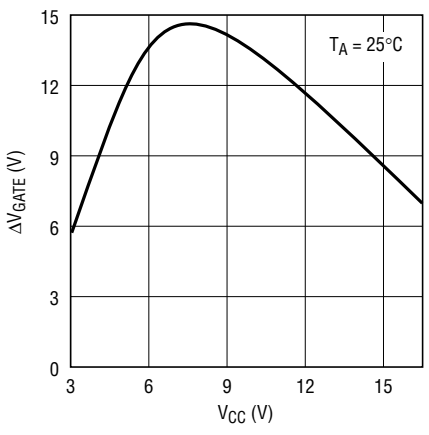
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

TYPICAL PERFORMANCE CHARACTERISTICS

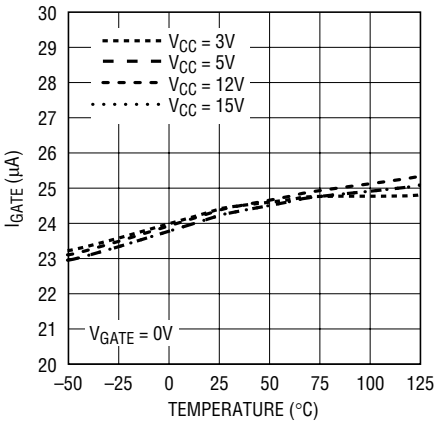
ΔV_{GATE} vs Temperature



ΔV_{GATE} vs V_{CC}

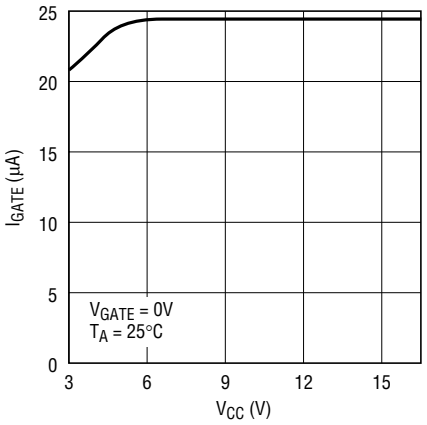


I_{GATE} vs Temperature



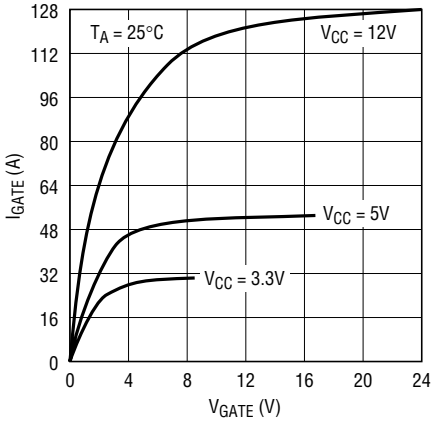
TYPICAL PERFORMANCE CHARACTERISTICS

I_{GATE} Pull-Up Current vs V_{CC}



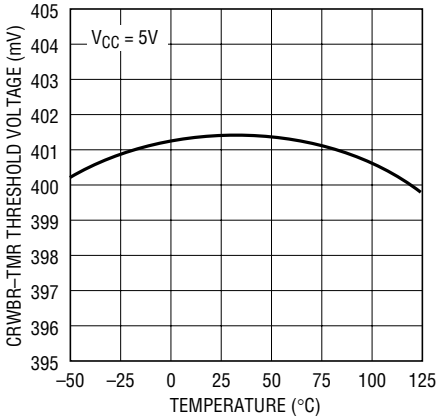
1642a G23

GATE Pull-Down Current (Current Limit Active)



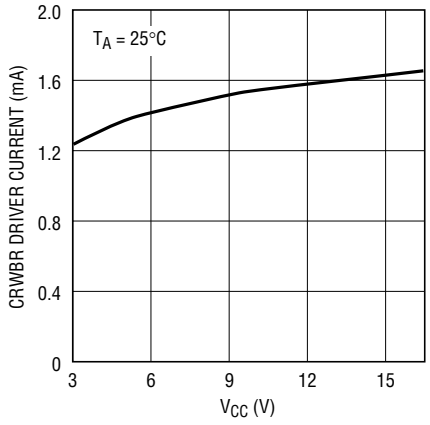
1642a G36

CRWBR-TMR Threshold Voltage vs Temperature



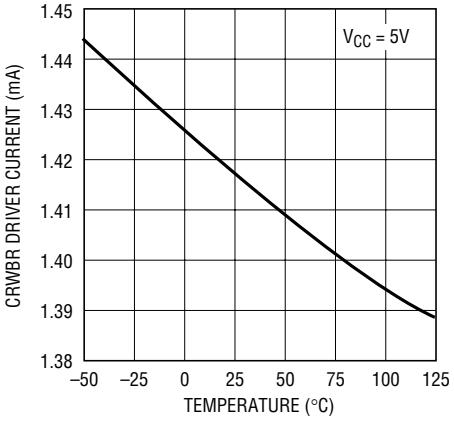
1642a G05

CRWBR Driver Current vs V_{CC}



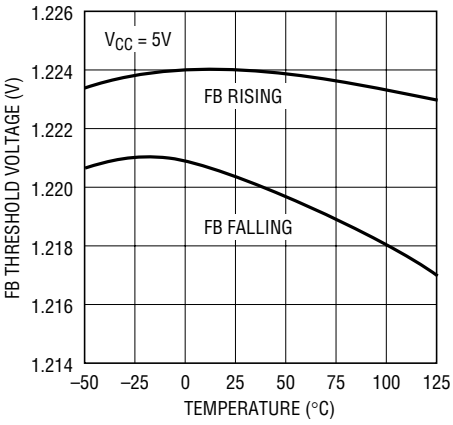
1642a G35

CRWBR Driver Current vs Temperature



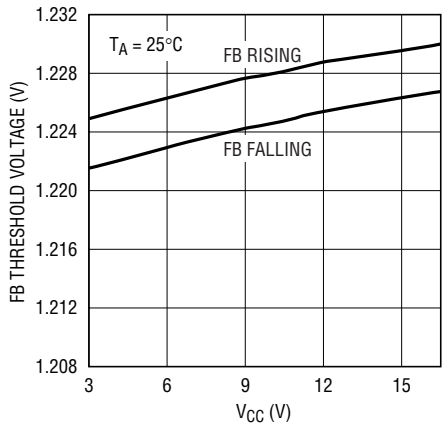
1642a G13

FB Threshold Voltage vs Temperature



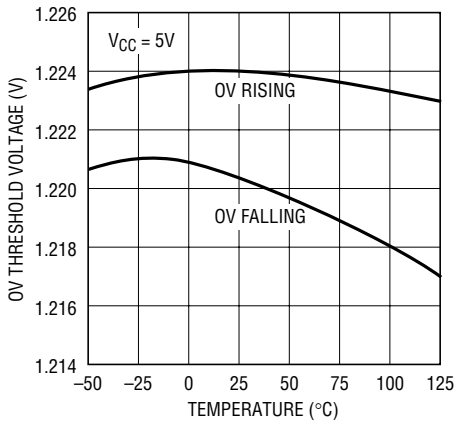
1642a G06

FB Threshold Voltage vs V_{CC}



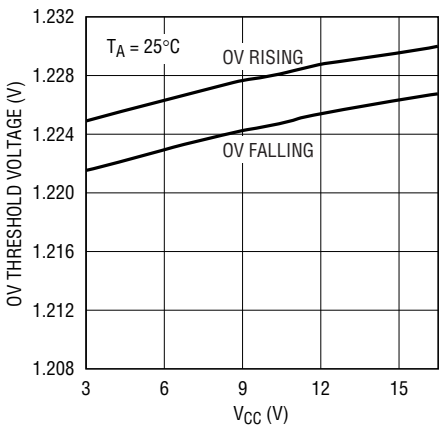
1642a G27

OV Threshold Voltage vs Temperature



1642a G07

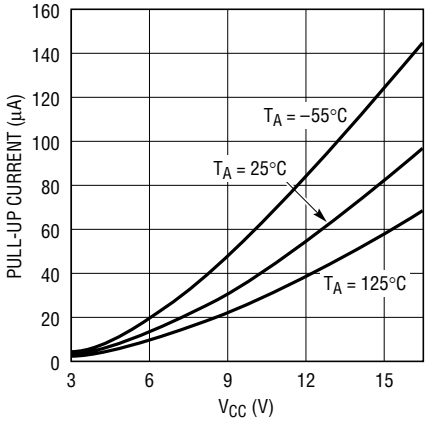
OV Threshold Voltage vs V_{CC}



1642a G28

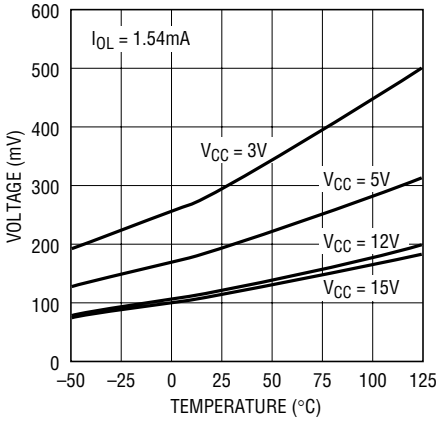
TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{FAULT}$ and $\overline{RESET}$ Pull-Up Current (I_{OH}) vs V_{CC}



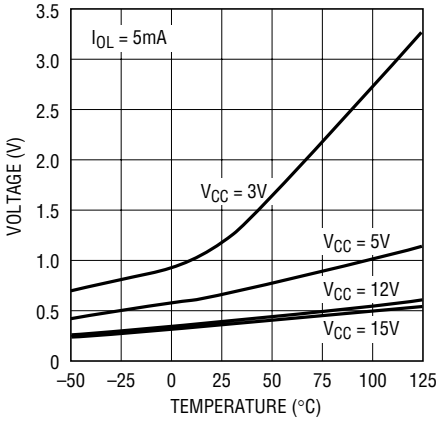
1642a G14

$\overline{FAULT}$ and $\overline{RESET}$ V_{OL} vs Temperature



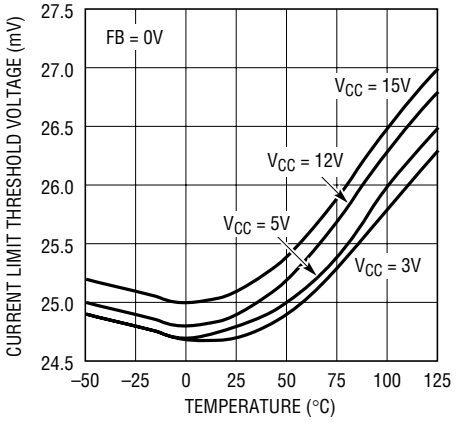
1642a G16

$\overline{FAULT}$ and $\overline{RESET}$ V_{OL} vs Temperature



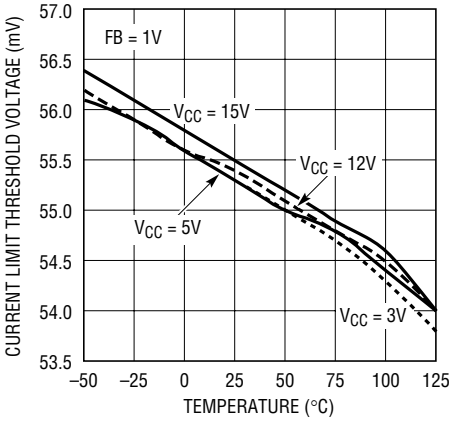
1642a G17

Current Limit Threshold Voltage (Full Foldback) vs Temperature



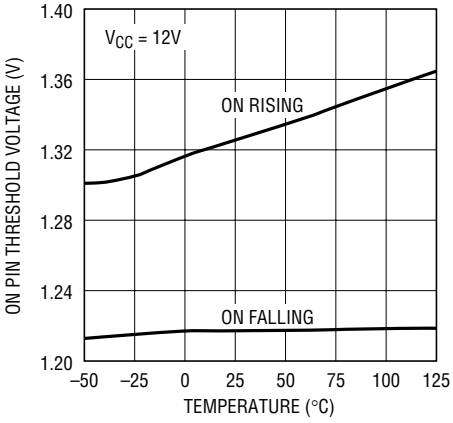
1642a G20

Current Limit Threshold Voltage (Nominal) vs Temperature



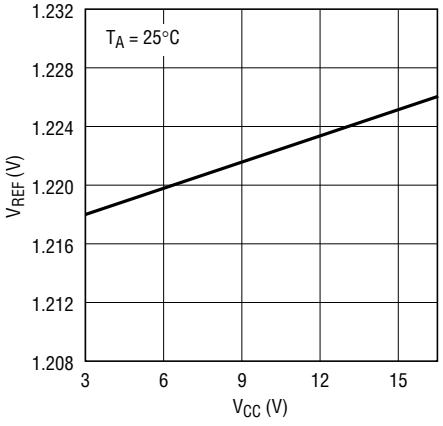
1642a G21

ON Pin Threshold Voltage vs Temperature



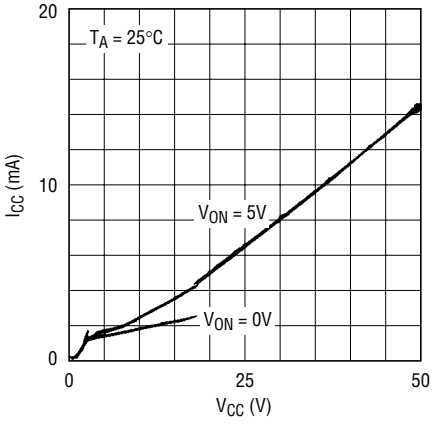
1642a G22

V_{REF} vs V_{CC}



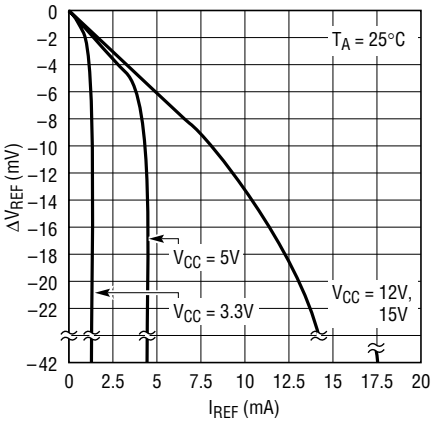
1642a G24

I_{CC} vs V_{CC}



1642a G25

Reference O/P Impedance



1642a G37

PIN FUNCTIONS

CRWBR (Pin 1): Overvoltage Crowbar Circuit Timer and Trigger. This pin controls an external overvoltage crowbar circuit. A capacitor from the pin to ground sets a 9ms/μF delay after an overvoltage occurs until an external SCR is triggered. See Applications Information. Ground the CRWBR pin if unused.

BRK TMR (Pin 2): Circuit Breaker Timer. Connect a capacitor from BRK TMR to ground to set a 60ms/μF delay from the time the sense resistor current reaches its limit until the FET is shut off. $\overline{\text{FAULT}}$ output is then asserted and the FET remains off until the chip is reset. Ground BRK TMR to allow the part to remain in current limit indefinitely.

RST TMR (Pin 3): Analog System/Reset Timer. A capacitor from this pin to ground sets a 0.6s/μF delay from the ON pin going high to the start of the GATE pin's ramp. It also sets the delay from output voltage good, as sensed by the FB pin, to $\overline{\text{RESET}}$ going high.

ON (Pin 4): ON Control Input. When ON is low the GATE pin is grounded and $\overline{\text{FAULT}}$ goes high. The GATE pin voltage starts ramping up one RST TMR timing cycle after ON goes high. Pulsing the ON pin low for at least 2μs resets the chip if it latches off after a sustained overvoltage or current limit. The threshold for a low to high transition is 1.34V with 110mV of hysteresis. A 21V zener clamp limits the voltage at this pin. The pin can be safely tied to V_{CC} > 21V through a series resistor that limits the current below 1mA.

$\overline{\text{RESET}}$ (Pin 5): Open Drain Reset Output. $\overline{\text{RESET}}$ is pulled low if the voltage at the FB pin is below its trip point. $\overline{\text{RESET}}$ goes high one RESET timing cycle after the FB voltage exceeds its trip point plus 3mV of hysteresis. $\overline{\text{RESET}}$ has a weak pull-up to one diode drop below V_{CC} and an external resistor can pull the pin above V_{CC}. A 21V zener clamp limits the voltage at this pin. The pin can be safely tied to V_{CC} > 21V through a series resistor that limits the current below 1mA.

$\overline{\text{FAULT}}$ (Pin 6): Open Drain Fault Output. $\overline{\text{FAULT}}$ is pulled low when the part turns off following a sustained overvoltage or current limit. It goes high 2μs after the ON pin goes low. $\overline{\text{FAULT}}$ has a weak pull-up to one diode drop below V_{CC} and an external resistor can pull the pin above V_{CC}. A 21V zener clamp limits the voltage at this pin. The pin can be safely tied to V_{CC} > 21V through a series resistor that limits the current below 1mA.

FB (Pin 7): Output Voltage Monitor and Foldback Input. The FB comparator can be used with an external resistive divider to monitor the output supply voltage. When the FB voltage is lower than 1.22V the $\overline{\text{RESET}}$ pin is pulled low. $\overline{\text{RESET}}$ goes high one system timing cycle after the voltage at FB exceeds its threshold by 3mV of hysteresis. A low pass filter at the comparator's output prevents negative voltage glitches from triggering a false reset.

GND (Pin 8): Chip Ground.

PIN FUNCTIONS

OV (Pin 9): Overvoltage Input. When the voltage on OV exceeds its trip point the GATE pin is pulled low immediately and the CRWBR timer starts. If OV remains above its trip point (minus 3mV of hysteresis) long enough for CRWBR to reach its trip point, then the part turns off until reset by pulsing the ON pin low. Otherwise, the GATE pin begins ramping up one RST TMR timing cycle after OV goes below its trip point. Ground the OV pin to disable overvoltage protection.

COMPOUT (Pin 10): Uncommitted Comparator's Open Drain Output.

COMP$^+$ (Pin 11): Uncommitted Comparator's Noninverting Input.

COMP$^-$ (Pin 12): Uncommitted Comparator's Inverting Input.

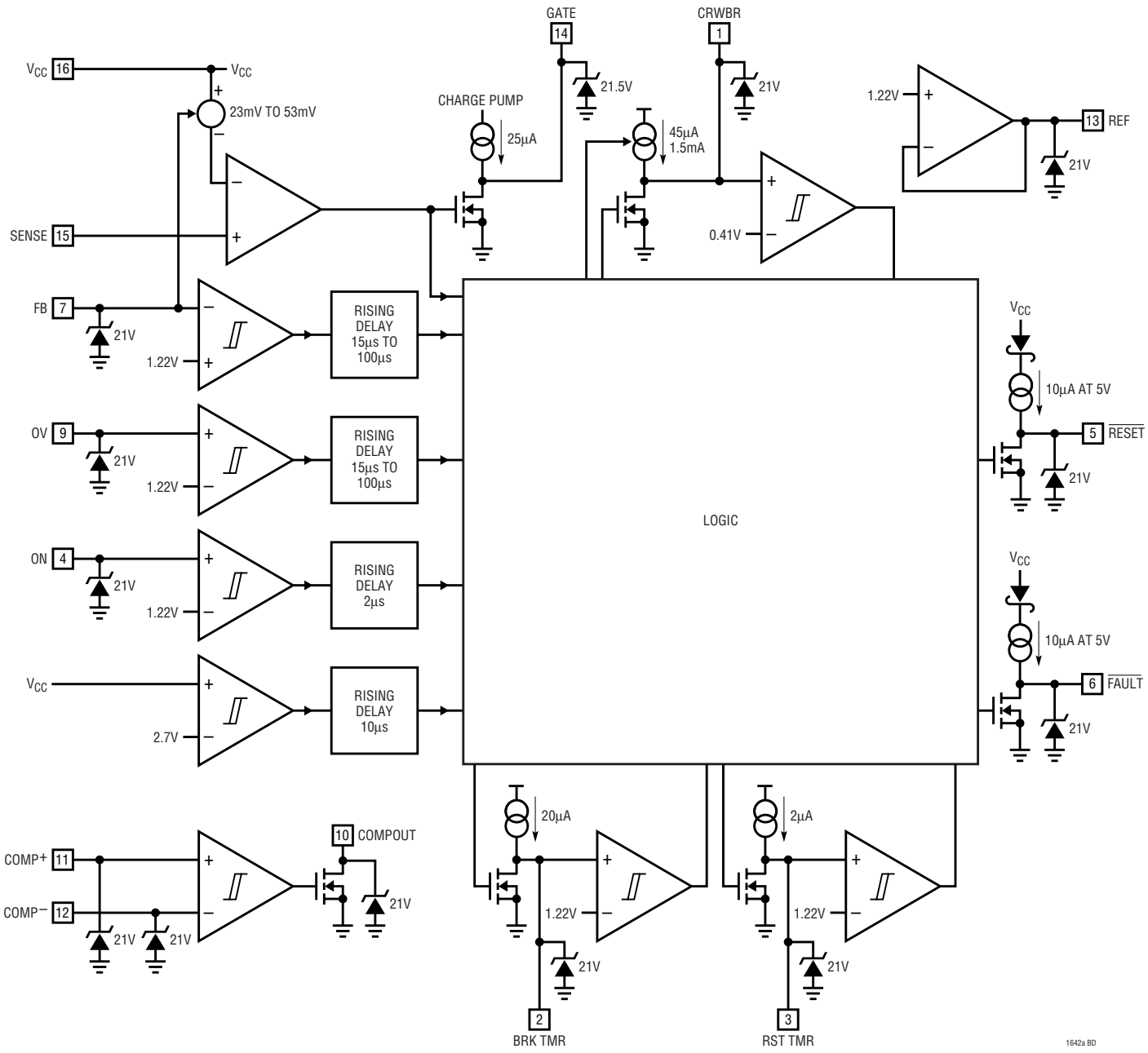
REF (Pin 13): Reference Voltage Output. The 1.22V ±1% reference should be bypassed with a 0.1μF compensation capacitor. For V_{CC} = 5V it can source 1mA.

GATE (Pin 14): Gate Drive for the External N-Channel MOSFET. An internal charge pump provides at least 4.5V of gate drive and sources 25μA. The pin requires an external series RC network to ground to compensate the current limit loop and to limit the ramp rate. A resistor of 100Ω is also recommended in series with the MOSFET gate to suppress high frequency oscillations. GATE is immediately pulled to ground when the overvoltage comparator trips or the input supply is below the undervoltage lockout trip point. During current limit the GATE voltage is adjusted to maintain constant load current until the circuit breaker timer trips. At that point GATE is pulled to ground until the chip is reset. Clamp the GATE pin with a zener diode to ground if the supply is 8V or higher. For the 8V to 12V range use an 18V zener (1N4705), and for supplies exceeding 12V use a 20V zener (TOSHIBA 02DZ20Y).

SENSE (Pin 15): Current Sense Input. To use the current limit place a sense resistor in the supply path between V_{CC} and SENSE. When the drop across the resistor exceeds a threshold voltage, the GATE pin is adjusted to maintain a constant load current and the circuit breaker timer is started. A foldback feature reduces the current limit as the voltage at FB approaches ground. Short SENSE to V_{CC} to disable the current limiting.

V_{CC} (Pin 16): Positive Supply Voltage. An internal undervoltage lockout circuit holds the GATE pin at ground until V_{CC} exceeds 2.73V. If V_{CC} exceeds 16.5V an internal shunt regulator protects the chip from V_{CC} and SENSE pin voltages up to 33V. In this case the GATE pin voltage will usually be low but this is not guaranteed; use the OV pin to ensure that the pass device is off. The V_{CC} pin also provides a high side connection to the SENSE resistor.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Hot Circuit Insertion

When a circuit board is inserted into a live backplane its supply bypass capacitors can draw large currents from the backplane power bus as they charge. These currents can permanently damage connector pins and can glitch the backplane supply, resetting other boards in the system. The LTC1642A limits the charging currents drawn by a board's capacitors, allowing safe insertion into a live backplane.

In the circuit shown in Figure 1 the LTC1642A and the external NMOS pass transistor Q1 work together to limit charging currents. Waveforms at board insertion are shown in Figure 2. When power is first applied to V_{CC} the chip holds Q1's gate at ground. After an adjustable delay a 25µA current source begins to charge the external capacitor C2, so choose C2 to limit the inrush current I_{INRUSH} charging the board's bypass capacitance C_{LOAD} according to the equation:

$$C2 = C_{LOAD} \bullet \frac{25\mu A}{I_{INRUSH}}$$

An internal charge pump supplies the 25µA gate current, ensuring sufficient gate drive to Q1. At 3V V_{CC} the minimum gate drive is 4.5V; at 5V V_{CC} the minimum is 10V; at 15V V_{CC} the minimum is again 6.5V, due to an internal zener clamp from the GATE pin to ground. Resistor R3 limits this zener's transient current during board insertion and removal and protects against high frequency oscillations in Q1. D1 provides additional protection against supply spikes.

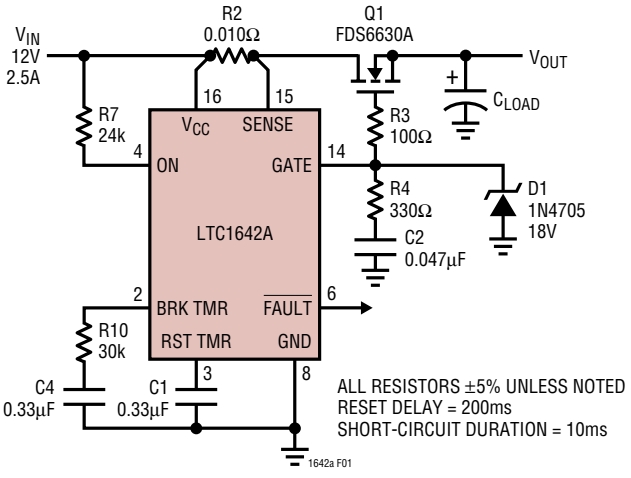


Figure 1. Supply Control Circuitry

The delay before the GATE pin voltage begins ramping is determined by the system timer. It comprises an external capacitor C1 from the RST TMR pin to ground; an internal 2µA current source feeding RST TMR from V_{CC}; an internal comparator, with the noninverting input tied to RST TMR and the inverting input tied to the 1.22V reference; and an internal NMOS pull-down. In standby, the NMOS holds RST TMR at ground. When the timer starts the NMOS turns off and the RST TMR voltage ramps up as the current source charges the capacitor. When RST TMR reaches 1.22V the timer comparator trips, the GATE voltage begins ramping up and RST TMR returns to ground. The timer delay is:

$$t_{RSTTMR} = (615ms/\mu F)\ C1.$$

The second RST TMR cycle indicates that V_{OUT} is within tolerance; it is discussed in the Undervoltage Monitor section.

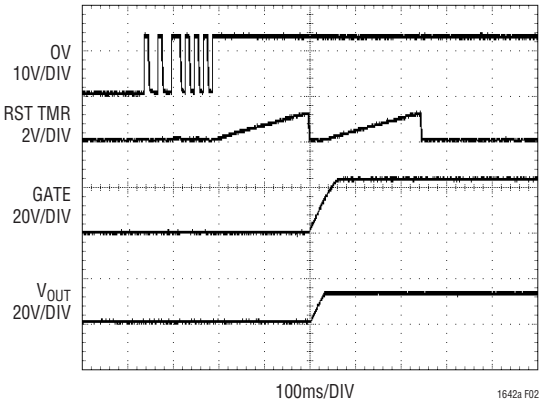


Figure 2. Timing at Board Insertion

Powering-Up in Current Limit

Ramping the GATE pin voltage limits the current to I = 25µA • C_{LOAD}/C2, where C2 is the external capacitor connected to the GATE and C_{LOAD} is the load capacitance. If the value of C_{LOAD} is uncertain, then a worst-case design can often result in needlessly long ramp times, and it may be better to limit the charging current by powering up in current limit.

Current Limiting and Solid-State Circuit Breaker

The current can be limited by connecting a sense resistor between the LTC1642A's V_{CC} and SENSE pins. When the voltage drop across this resistor reaches a limiting value,

APPLICATIONS INFORMATION

an internal servo loop adjusts the GATE pin voltage such that Q1 acts as a constant current source. The voltage limit across R2 increases as the output charges; this foldback in the current limit helps to even out Q1's power dissipation. The output is sensed at the FB pin. When FB is grounded, the sense voltage is limited to 26mV. When FB is greater than 0.7V, the limit is 56mV and the full dependence is shown in Figure 3.

When the sense resistor voltage is 3mV below its limit, the circuit breaker timer starts. Once BRK TMR reaches its threshold, the circuit breaker opens, the GATE pin is pulled to ground (cutting off Q1) and $\overline{\text{FAULT}}$ is asserted.

The parameter V_{CB} specified in the DC electrical characteristics refers to the voltage difference between the V_{CC} and SENSE pins needed to start the circuit breaker timer. The limiting value maintained by the servo loop is 3mV higher than V_{CB}.

Should the sense resistor voltage drop below its limit before the timer trips, the GATE voltage begins ramping back up immediately and the BRK TMR pin returns to ground. However, due to the slow gate ramp, Q1 continues to dissipate substantial power for some time. Connecting R10 in series with timing capacitor C4 (as shown in Figure 1) ensures that the circuit breaker trips in the event of repetitive, but brief, load shorts. The delay before the circuit breaker opens is:

$$t_{BRKTMR} = C4\ (61k\Omega - R10).$$

Once the circuit breaker trips, GATE and $\overline{\text{FAULT}}$ remain at ground until the chip is restarted. To restart, hold the ON pin low for at least 2µs and $\overline{\text{FAULT}}$ will go high. Then take ON high again and the GATE will ramp up after a system timing cycle. Or, configure the LTC1642A to restart itself after the circuit breaker trips by connecting $\overline{\text{FAULT}}$ to the ON pin, as shown in the next section.

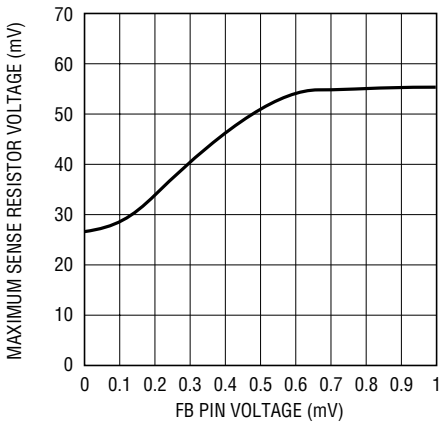


Figure 3. Foldback Current Limit

The servo loop controlling Q1 during current limit has a unity-gain frequency of about 125kHz. In Figure 1, R4 and C2 provide compensation. To ensure stability the product $1/(2 \bullet \pi \bullet R4 \bullet C2)$ should be kept below the unity-gain frequency, and C2 should be more than Q1's input capacitance C_{ISS}. A good starting point for C2 is 0.047µF and R4 is 330Ω. Keep R4 ≥ 100Ω.

Typical waveforms during a load short to ground are shown in Figure 4. The load is shorted to ground at time 1. The GATE voltage drops until the load current equals its maximum limit, and the circuit breaker timer starts. The short is cleared at time 2, before the timer trips. The BRK TMR pin returns to ground, and the GATE voltage begins ramping up. At time 3 the load is shorted again and at time 4 the timer trips, pulling the GATE to ground and asserting $\overline{\text{FAULT}}$. Although the short is cleared at time 5, $\overline{\text{FAULT}}$ doesn't go high until the ON pin is pulled low at time 6. At time 7 ON goes high and the system timer starts. When it trips at time 8 the GATE voltage begins ramping.

To disable current limit and electronic circuit breaker protection, tie the SENSE pin to V_{CC}, the BRK TMR pin to GND and omit compensating resistor R4.

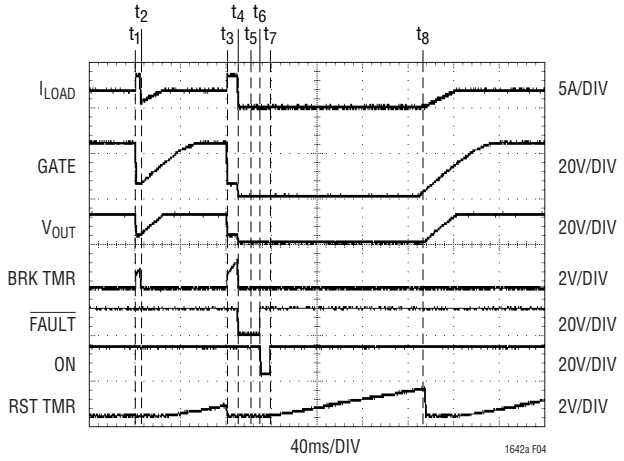


Figure 4. Current Limit and Circuit Breaker Timing

APPLICATIONS INFORMATION

Automatic Restart After the Circuit Breaker Opens

The LTC1642A will automatically attempt to restart itself after the circuit breaker opens if the $\overline{FAULT}$ output is tied to the ON pin. The circuit is shown in Figure 5. Diode D1 blocks the weak $\overline{FAULT}$ pull-up current source from unbalancing the R6-R5 divider.

During a continuous current limit such as a load short, Q1's duty cycle is equal to the circuit breaker timer period, divided by the sum of the circuit breaker and system timer periods:

$$\text{Short-Circuit Duty Cycle} = \frac{C4}{C4 + 10 \bullet C1}$$

The duty cycle is 9% for the Figure 5 circuit. Waveforms during a load short are shown in Figure 6.

Undervoltage Lockout

An internal undervoltage lockout circuit holds the charge pump off until V_{CC} exceeds 2.73V. If V_{CC} falls below 2.5V, it turns off the charge pump and clears overvoltage and current limit faults.

For higher lockout thresholds tie the ON pin to a resistor divider driven from V_{CC}, as shown in Figure 7. This circuit keeps the charge pump off until V_{CC} exceeds (1+R6/R5) • 1.34V, and also turns it off if V_{CC} falls below (1+R6/R5) • 1.22V.

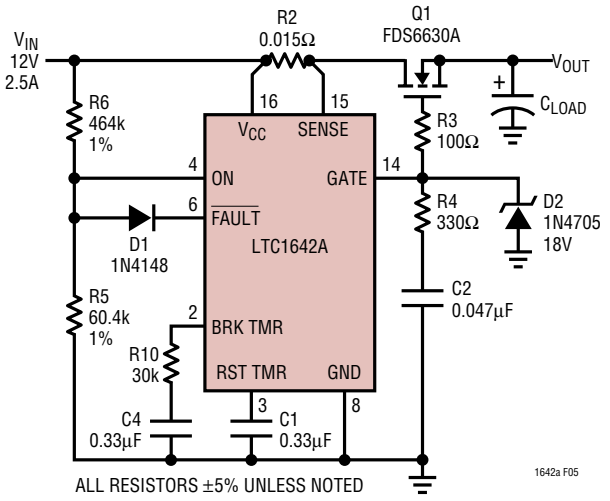


Figure 5. Automatic Restart Circuit

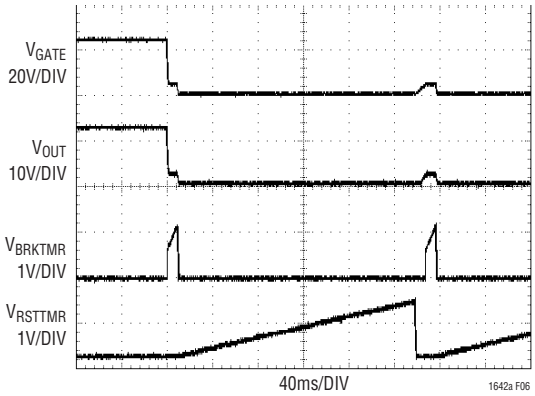


Figure 6. Automatic Retry Following a Load Short

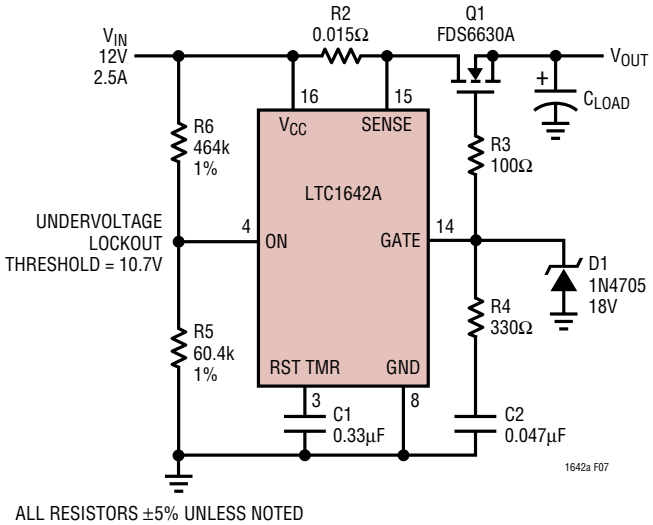


Figure 7. Setting a Higher Undervoltage Lockout

APPLICATIONS INFORMATION

Overvoltage Protection

The LTC1642A can protect a load from overvoltages by turning off the pass transistor if the supply voltage exceeds an adjustable limit, and by triggering a crowbar SCR if the overvoltage lasts longer than an adjustable time. The part can also be configured to automatically restart when the overvoltage clears.

The overvoltage protection circuitry is shown in Figure 8. The external components comprise a resistor divider driving the OV pin, timing capacitor C5, NPN emitter follower Q2, and crowbar SCR Q3. Because the MCR12DC is not a sensitive-gate device, the optional resistor shunting the SCR gate to ground is omitted. The internal components comprise a comparator, 1.22V bandgap reference, two current sources, and a timer at the CRWBR pin. When V_{CC} exceeds (1+R6/R5)•1.22V the comparator's output goes high and internal logic turns off Q1 and starts the timer. This timer has a 0.410V threshold and uses the CRWBR pin; when CRWBR reaches 0.410V the timer comparator trips, and the current sourced from V_{CC} increases to 1.5mA. Emitter follower Q2 boosts this current to trigger crowbar SCR Q3. The ramp time Δt needed to trip the comparator is:

$$t_{CRWBR} = 9.1(ms/\mu F)\ C5$$

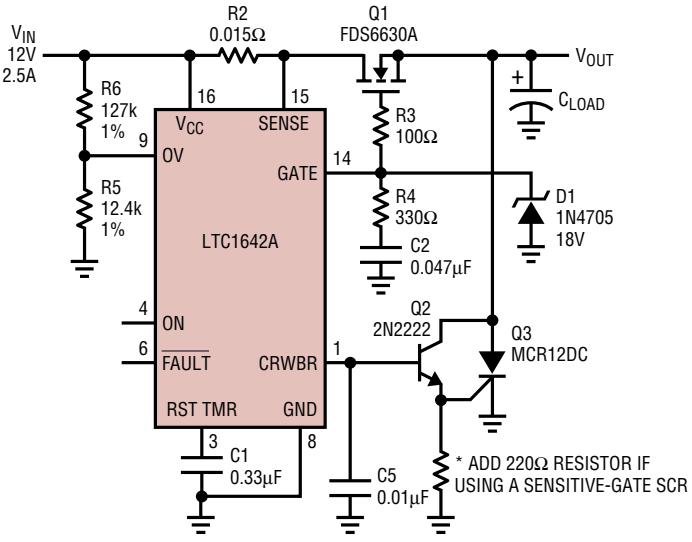


Figure 8. Overvoltage Protection Circuitry

Once the CRWBR timer trips the LTC1642A latches off: after the overvoltage clears GATE and FAULT remain at ground and CRWBR continues sourcing 1.5mA. To restart the part after the overvoltage clears, hold the ON pin low for at least 2µs and then bring it high. The GATE voltage will begin ramping up one system timing cycle later. The part will restart itself if FAULT and ON are connected.

Figure 9 shows typical waveforms when the divider is driven from V_{CC}. The OV comparator goes high at time 1, causing the chip to pull the GATE pin to ground and start the CRWBR timer. At time 2, before the timer's comparator trips, OV falls below its threshold; the timer resets and GATE begins charging one system timing cycle later at time 3. Another overvoltage begins at time 4, and at time 5 the CRWBR timer trips; FAULT goes low and the CRWBR pin begins sourcing 1.5mA. Even after OV falls below 1.22V at time 6, GATE and FAULT stay low, and CRWBR continues to source 1.5mA. FAULT goes high when ON goes low at time 7, and GATE begins charging at time 8, one RST TMR cycle after FAULT goes high.

Figure 10 shows typical waveforms when the OV divider is driven from the N-Channel's output side. Because the voltage driving the divider collapses after the OV comparator trips, FAULT stays high and CRWBR stays near ground, which prevents the pin from triggering an SCR. The GATE voltage begins ramping up after a RST TMR timing cycle.

To disable overvoltage protection completely, tie the OV and CRWBR pins to GND. For overvoltage protection at the GATE pin, but without latch off or a crowbar SCR such as Q3 in Figure 1, tie CRWBR to GND.

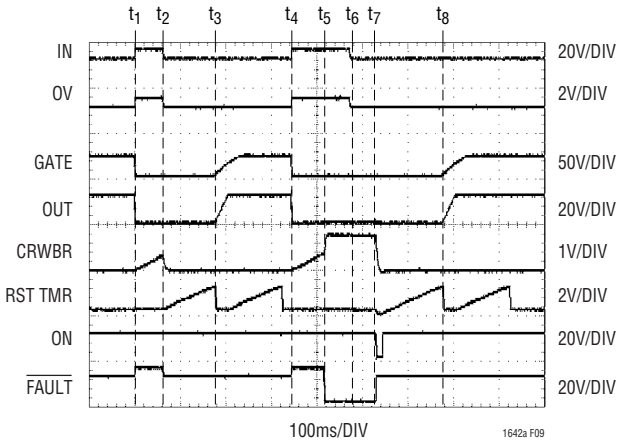


Figure 9. Overvoltage Timing (Input Side)

APPLICATIONS INFORMATION

Automatic Restart

If there is an overvoltage, and the resistor divider feeding OV is connected to the output of the N-Channel pass transistor, the LTC1642A will automatically restart even if FAULT is not tied to ON. If the divider is connected to the input side, the LTC1642A will restart itself only if FAULT is tied to ON, and only after the overvoltage clears.

The OV and FB Comparators

The propagation delay through the OV and FB comparators on low to high transitions depends strongly on the differential input voltage. The relationship is shown in Figure 11. The minimum propagation delay for large overdrives is about 20µs. In addition the comparators have 3mV of hysteresis.

Internal Voltage Clamp Protection

The LTC1642A includes a shunt regulator to protect itself from V_{CC} and SENSE pin voltages up to 33V. The regulator turns on when V_{CC} exceeds 16.5V and limits most of the chip's circuitry to 15V. When it is on the chip functions normally with one exception: if the charge pump is on, the GATE voltage is usually near ground but this is not guaranteed. Use the OV pin to ensure that GATE is grounded.

The pull-up voltage on the $\overline{RESET}$ and $\overline{FAULT}$ pins follows V_{CC} until the shunt regulator turns on. When the regulator is on the pull-up voltage is 14.4V.

Undervoltage Monitor

The LTC1642A will assert $\overline{RESET}$ if a monitored voltage falls below an adjustable minimum. When the monitored voltage has exceeded its minimum for at least one system timing cycle, $\overline{RESET}$ goes high. The monitoring circuitry comprises an internal 1.22V bandgap reference, an internal precision voltage comparator and an external resistive divider to monitor the output supply voltage.

The circuit is shown in Figure 12, and typical waveforms in Figure 13. When the voltage at the FB pin rises above its reset threshold (1.22V), the comparator output goes low and a timing cycle starts (times 1 and 5). Following the cycle $\overline{RESET}$ is pulled high. At time 2 the voltage at FB drops below the comparator's threshold and $\overline{RESET}$ is pulled low. If the FB pin rises above the reset threshold for less than a timing cycle the $\overline{RESET}$ output will remain low (time 3 to time 4). The 15µA pull-up current source to V_{CC} on $\overline{RESET}$ has a series diode so the pin can be pulled above V_{CC} by an external pull-up resistor without forcing current back into the supply.

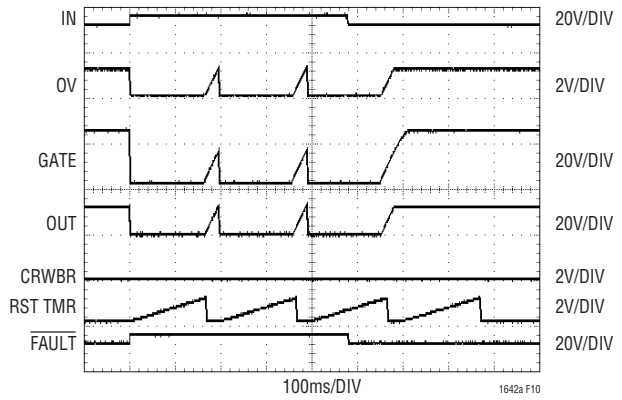


Figure 10. Overvoltage Timing (Output Side)

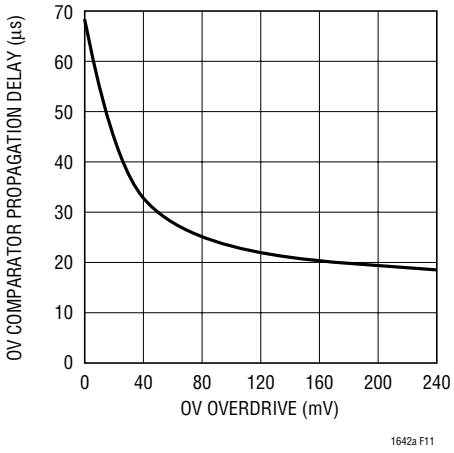


Figure 11. OV Comparator Propagation Delay vs Overdrive Voltage

APPLICATIONS INFORMATION

The undervoltage monitor behaves differently if FB is above its threshold when the GATE begins ramping: RESET goes high as soon as the GATE ramp begins.

$\overline{\text{RESET}}$ goes low immediately if V_{CC} falls below the chip's 2.5V internal undervoltage lockout threshold.

To disable the undervoltage monitor, tie FB to REF and ground $\overline{\text{RESET}}$.

Reference

The LTC1642A's internal voltage reference is buffered and brought out to the REF pin. The buffer amplifier should be compensated with a capacitor connected between REF and ground. If no DC current is drawn from REF, 0.1µF ensures an adequate phase margin, but the minimum compensation increases if REF sources a substantial DC current, as shown in Figure 14.

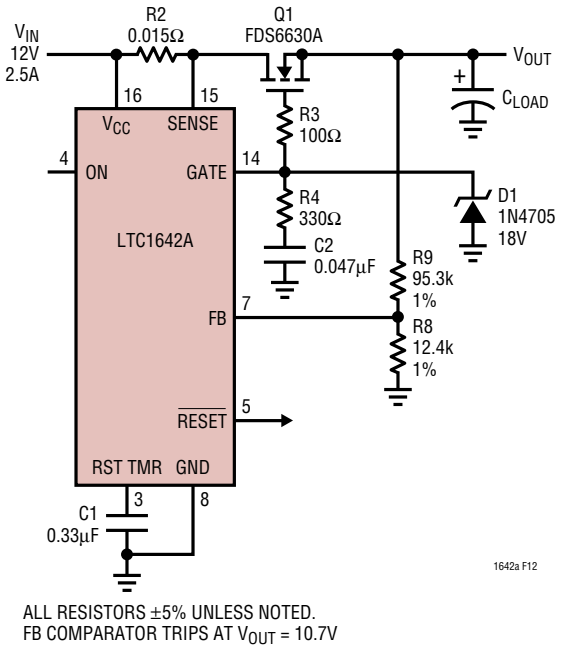


Figure 12. Undervoltage Monitoring Circuitry

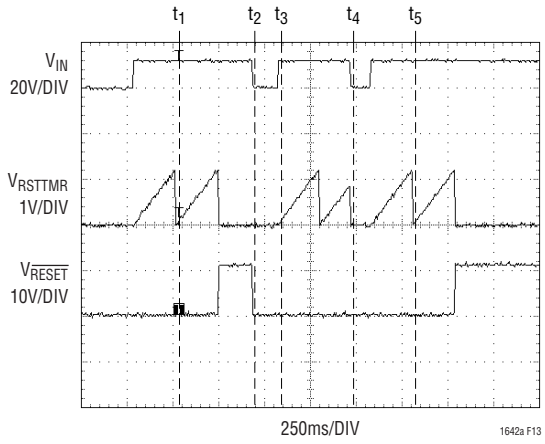


Figure 13. Supply Monitor Waveforms

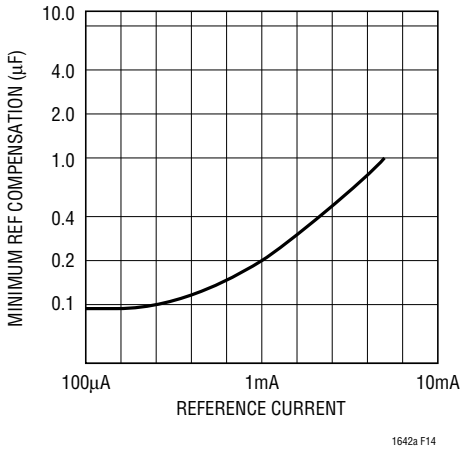


Figure 14. Minimum REF Compensation vs REF Current

APPLICATIONS INFORMATION

Uncommitted Comparator

The uncommitted comparator has an open drain output. The comparator has 3mV of hysteresis: the output goes high when the differential input voltage exceeds 1.5mV and goes low when the differential input is less than –1.5mV.

The comparator's input transistors are MOSFETs so the input bias and offset currents are very small: typically picoamps at 25°C, increasing to nanoamps at 90°C. If the auxilliary comparator is unused, the $COMP^+$, $COMP^-$ and COMPOUT pins may be left floating.

Layout Considerations

One ounce copper exhibits a sheet resistance of 530μΩ per square. To minimize self-heating, traces should be at least 0.02" wide per ampere of current and 0.03" is recommended.

In high current applications, the voltage drop along traces can be appreciable. Connect the LTC1642A's V_{CC} and SENSE pins *directly* across sense resistor R2 to prevent the power trace's resistance from adding to R2. It is also a good practice to keep the resistor divider to the ON pin close to the chip and the divider's connections to the V_{CC} and GND pins short. Figure 15 shows an example layout.

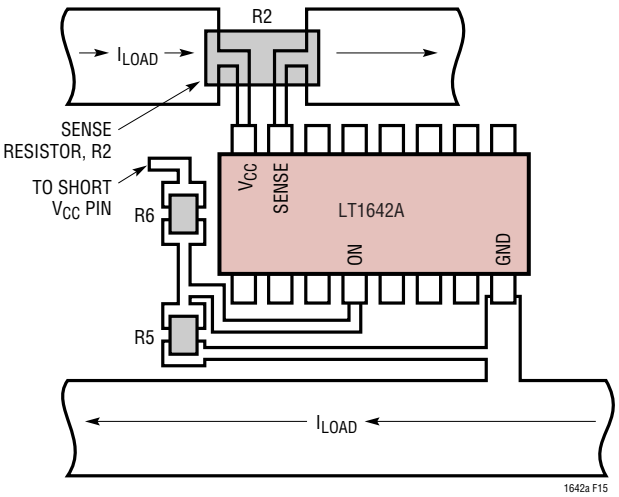


Figure 15. Recommended Layout for R1, R2 and R5