No R_{SENSE} Synchronous Step-Up DC/DC Controller

FEATURES

- **High Efficiency: Up to 95%**
- **No Current Sense Resistor Required**
- **Constant Frequency 530kHz Operation Allows Small Size, Surface Mount Inductors**
- **OPTI-LOOP® Compensation Minimizes C_{OUT}**
- **Selectable Burst Mode® Operation**
- **Minimum Start-Up Voltage as Low as 0.9V**
- Synchronizable Between 400kHz and 750kHz
- Micropower Shutdown: 10μA
- Current Mode Operation for Excellent Line and Load Transient Response
- Soft-Start Reduces Supply Current Transients
- 1.5% Output Voltage Accuracy
- Uses Low Value, Small Size, Surface Mount Inductors
- Available in 10-Lead MSOP Package

APPLICATIONS

- Cellular Telephones
- Wireless Modems
- RF Communications
- 2.5V to 3.3V, 2.5V to 5V Converters
- Battery-Powered Equipment
- Telecom/Network Systems

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Burst Mode, OPTI-LOOP are registered trademarks of Linear Technology Corporation.
No R_{SENSE} is a trademark of Linear Technology Corporation.

DESCRIPTION

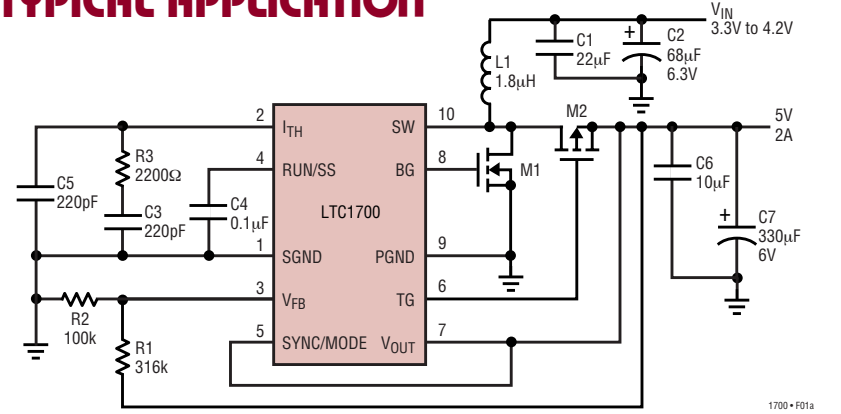
The LTC®1700 is a current mode synchronous step-up DC/DC controller that drives external N-channel and P-channel power MOSFETs using a constant frequency PWM architecture. Current limiting is provided by sensing the voltage drop across the main MOSFET, eliminating the need of a sense resistor. This No R_{SENSE}™ technique helps the LTC1700 maintain high efficiency at heavy loads while Burst Mode operation ensures high efficiency at light loads, thus providing high efficiencies over a wide range of load currents.

The LTC1700 operates at a minimum input voltage as low as 0.9V. The device boasts a ±1.5% output voltage accuracy and consumes only 200μA of quiescent current. In shutdown, it only draws 10μA.

To prevent inductor current runaway, the duty cycle is limited to 90%. Overvoltage protection is also provided which shuts both the external MOSFETs off when tripped.

High constant operating frequency of 530kHz allows the use of small inductors and output capacitors. The LTC1700 can also be synchronized between 400kHz to 750kHz. Burst Mode operation is inhibited when the device is externally clocked or when the SYNC/MODE pin is pulled low to reduce noise and RF interference.

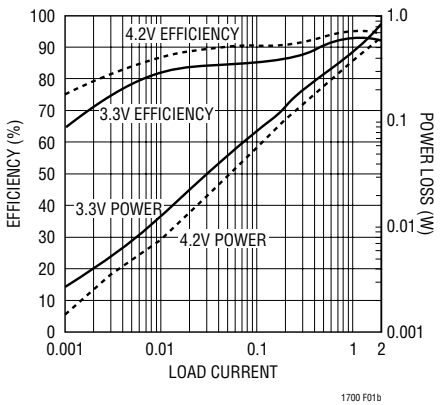
TYPICAL APPLICATION



C1: CERAMIC TAIYO YUDEN LMK432BJ226MM
C2: AVX TAJB686K006R
L1: TOKO 919AS-IR8N (D104C TYPE)
C6: CERAMIC TAIYO YUDEN JMK316BJ106ML
C7: SANYO POSCAP 6TPB330M
M1: SILICONIX Si9804
M2: SILICONIX Si9803

Figure 1. High Efficiency Step-Up Converter

Efficiency, Power Loss vs Load Current

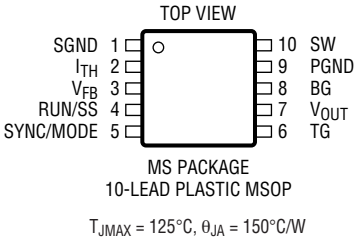


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Output Supply Voltage (V_{OUT}) .....–0.3V to 6V
RUN/SS, V_{FB} Voltages .....–0.3V to 2.4V
SYNC/MODE, I_{TH} Voltages .....–0.3V to 6V
SWITCH Voltage (SW) .....–0.3V to 6.5V
TG, BG Peak Output Current (<10μs) 1A
Operating Temperature Range (Note 2) ...–40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1700EMS
MS PART MARKING
LTLC

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = 3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SOP}	Start-Up Minimum Operating Voltage	(Note 4)			0.9	1.8	V
V_{OP}	Minimum Operating Voltage Hysteresis	(Note 5) V_{OUT} Ramping Up			2.34 90	2.6	V mV
I_S	Input DC Supply Current Normal Mode Sleep Mode Start-Up Mode Shutdown	(Note 6) V_{FB} = 1.6V, V_{MODE} = 0V, $V_{RUN/SS}$ = 3V V_{FB} = 1.6V, V_{MODE} = 3V, $V_{RUN/SS}$ = 3V V_{FB} = 0V, V_{MODE}, $V_{RUN/SS}$, V_{OUT} = 1.8V V_{FB} = 0V, V_{MODE} = 3V, $V_{RUN/SS}$ = 0V			 536 179 35 10	 620 210 45 14	 μA μA μA μA
I_{VFB}	Feedback Current	V_{FB} = 1.20V			1	50	nA
V_{FB}	Regulated Output Voltage	(Note 7)	●	1.187	1.205	1.223	V
ΔV_{OSENS}	Reference Voltage Line Regulation	V_{IN} = 2.7V to 5V (Note 7)			0.0106	0.080	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	Measured in Servo Loop; V_{ITH} = 0.3V to 0.9V			0.036	0.065	%
V_{OVL}	Output Overvoltage Lockout	Reference to Nominal V_{FB}		2.5	4.8	9	%
$V_{RUN/SS}$	Shutdown Threshold	$V_{RUN/SS}$ Ramping Up	●	0.7	1.09	1.2	V
$I_{RUN/SS}$	Soft-Start Current Source	$V_{RUN/SS}$ = 0V		2	3.79	6	μA
f_{OSC}	Oscillator Frequency Start-Up Oscillator Frequency	V_{OUT} = 4.2V V_{OUT} = 1.8V, $V_{RUN/SS}$ = 1.8V, V_{SW} = 1.1V	●	460 150	530 225	680	kHz kHz
$V_{SYNC/MODE}$	SYNC/MODE Threshold	$V_{SYNC/MODE}$ Ramping Down from 1.2V		1.03	1.13	1.25	V
DC MAX	Maximum Duty Cycle	f_{OSC} = 550kHz		84	88	92	%
$\Delta V_{SENSE(MAX)}$	Maximum Current Sense Voltage		●	55 63	78	100	mV mV
I_{LIMIT}	Current Limit At Start-Up	V_{OUT} = 1.8V		40	60		mA
g_m	Transconductance of Error Amplifier	V_{FB} = V_{REF} ± 10mV		0.65	0.9	1.30	m℧

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = 3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	TG Transition Time					
TG t_r	TG Gate Drive Rise Time	C_{LOAD} = 3000pF, 10% to 90%		60	100	ns
TG t_f	TG Gate Drive Fall Time	C_{LOAD} = 3000pF, 90% to 10%		60	100	ns
	BG Transition Time					
BG t_r	BG Gate Drive Rise Time	C_{LOAD} = 3000pF, 10% to 90%		80	100	ns
BG t_f	BG Gate Drive Fall Time	C_{LOAD} = 3000pF, 90% to 10%		50	70	ns
	Dead Time					
t_{dll}	BG and TG Gates Go Low	C_{LOAD} = 3000pF on BG and TG		88	110	ns
t_{dhh}	BG and TG Gates Go High	C_{LOAD} = 3000pF on TG and BG		66	90	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1700E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet 150°C/W)$$

Note 4: At an input supply less than 2.3V, only the start-up circuitry of the LTC1700 is active. This test ensures the start-up circuitry is working.

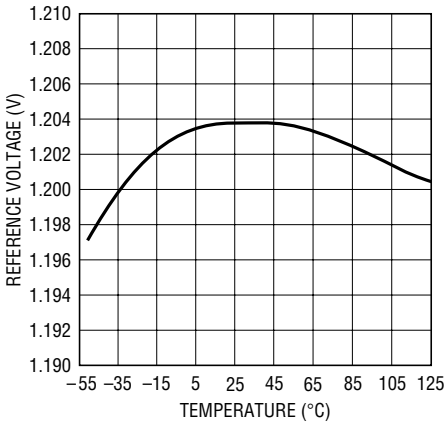
Note 5: An input supply at or above this minimum operating voltage activates the main control loop. Start-up circuitry of the LTC1700 is shut off.

Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

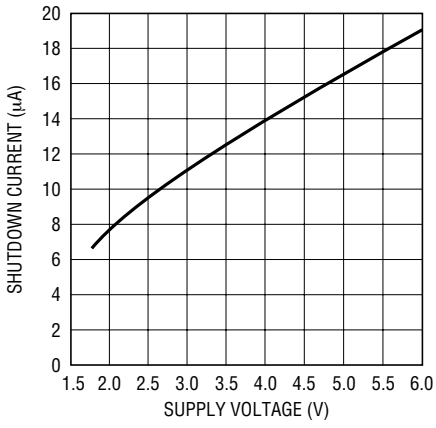
Note 7: The LTC1700 is tested in a feedback loop that servos V_{FB} to the feedback point for the error amplifier (V_{ITH} = 0.6V)

TYPICAL PERFORMANCE CHARACTERISTICS

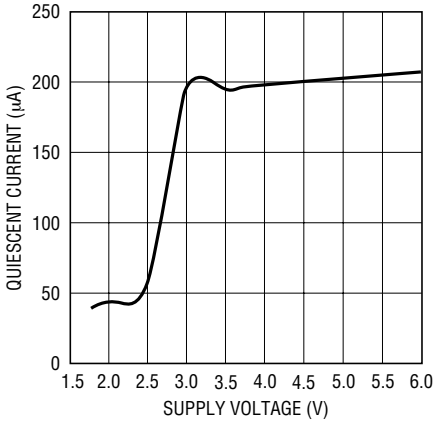
Reference Voltage vs Temperature



Shutdown Current vs Supply Voltage

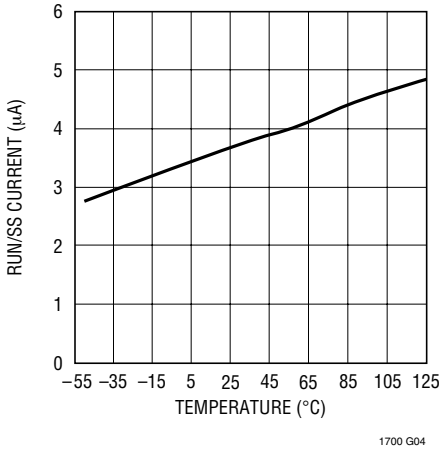


Quiescent Current vs Supply Voltage

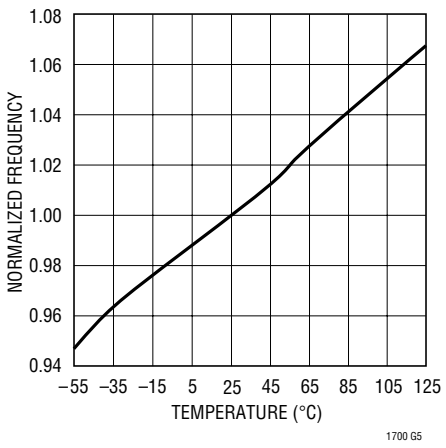


TYPICAL PERFORMANCE CHARACTERISTICS

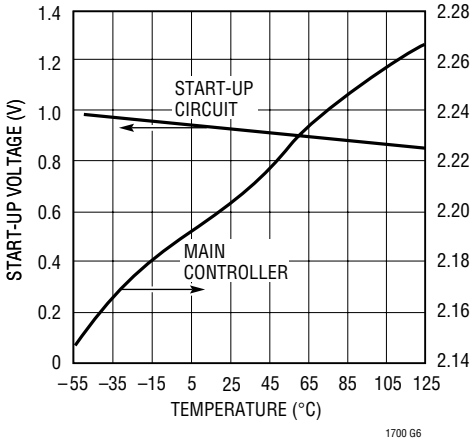
RUN/SS Current vs Temperature



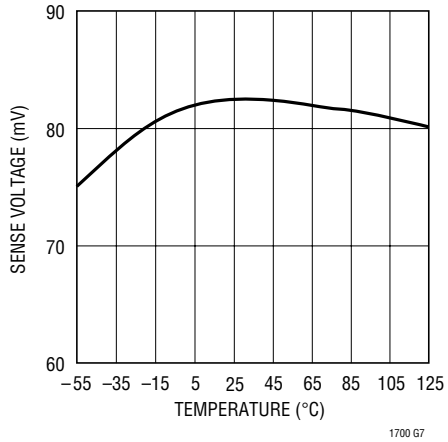
Normalized Oscillator Frequency vs Temperature



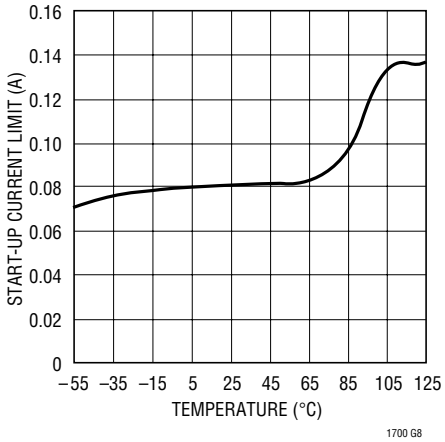
Minimum Operating Voltage vs Temperature



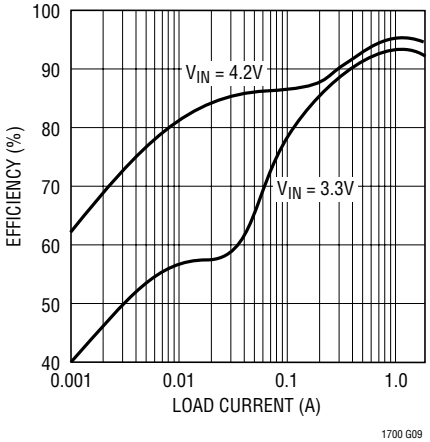
Maximum Current Sense Voltage vs Temperature



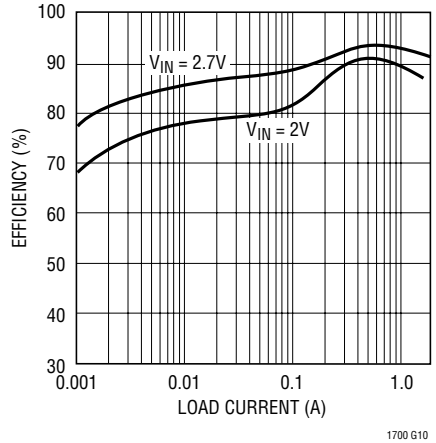
Start-Up Current Limit vs Temperature



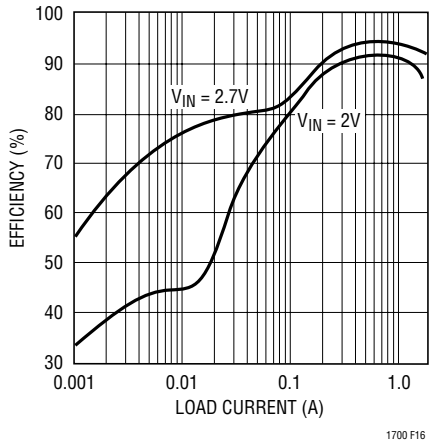
Efficiency vs Load Current (Burst Mode Operation Disabled)



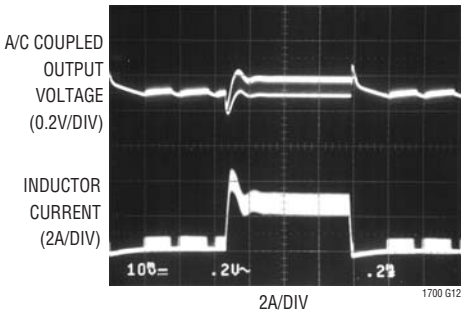
3.3V Output Efficiency, Circuit of Figure 1 with Burst Mode Operation



3.3V Output Efficiency, Circuit of Figure 1 with Burst Mode Operation Inhibited



Load Step Transient Response Burst Mode Operation Enabled



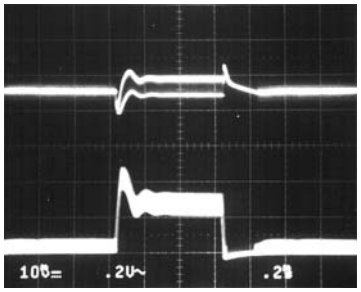
2A/DIV

V_{IN} = 3.3V V_{SYNC} = V_{IN}

V_{OUT} = 5V LOAD STEP = 100mA TO 1.7A

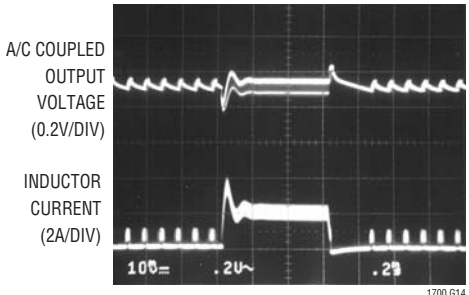
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step Transient Response
Burst Mode Operation Inhibited



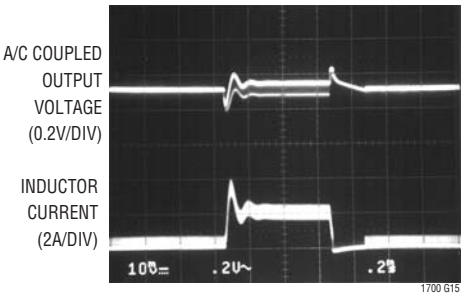
V_{IN} = 3.3V V_{SYNC} = 0V
V_{OUT} = 5V LOAD STEP = 100mA TO 1.7A

Load Step Transient Response
Burst Mode Operation Enabled



V_{IN} = 4.2V V_{SYNC} = V_{IN}
V_{OUT} = 5V LOAD STEP = 100mA TO 1.7A

Load Step Transient Response
Burst Mode Operation Inhibited



V_{IN} = 4.2V V_{SYNC} = 0V
V_{OUT} = 5V LOAD STEP = 100mA TO 1.7A

PIN FUNCTIONS

SGND (Pin 1): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

I_{TH} (Pin 2): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.18V.

V_{FB} (Pin 3): Receives the feedback voltage from an external resistive divider across the output capacitor.

RUN/SS (Pin 4): Combination of Soft-Start and Run Control Inputs. A capacitor to ground at this pin sets the ramp time to full output current. The time is approximately 0.45s/μF. Forcing this pin below 1.08V causes all circuitry to be shut down.

SYNC/MODE (Pin 5): This pin performs three functions. A voltage greater than 1.2V on this pin allows Burst Mode operation at low load currents, while grounding or applying a clock signal on this pin defeats Burst Mode operation. An external clock between 400kHz and 750kHz applied to this pin forces the LTC1700 to operate at the external clock frequency. *Do not attempt to synchronize below 400kHz or above 750kHz.*

TG (Pin 6): Top Gate Drive. Drives the external synchronous P-channel MOSFET with a voltage swing between 0V to V_{OUT}.

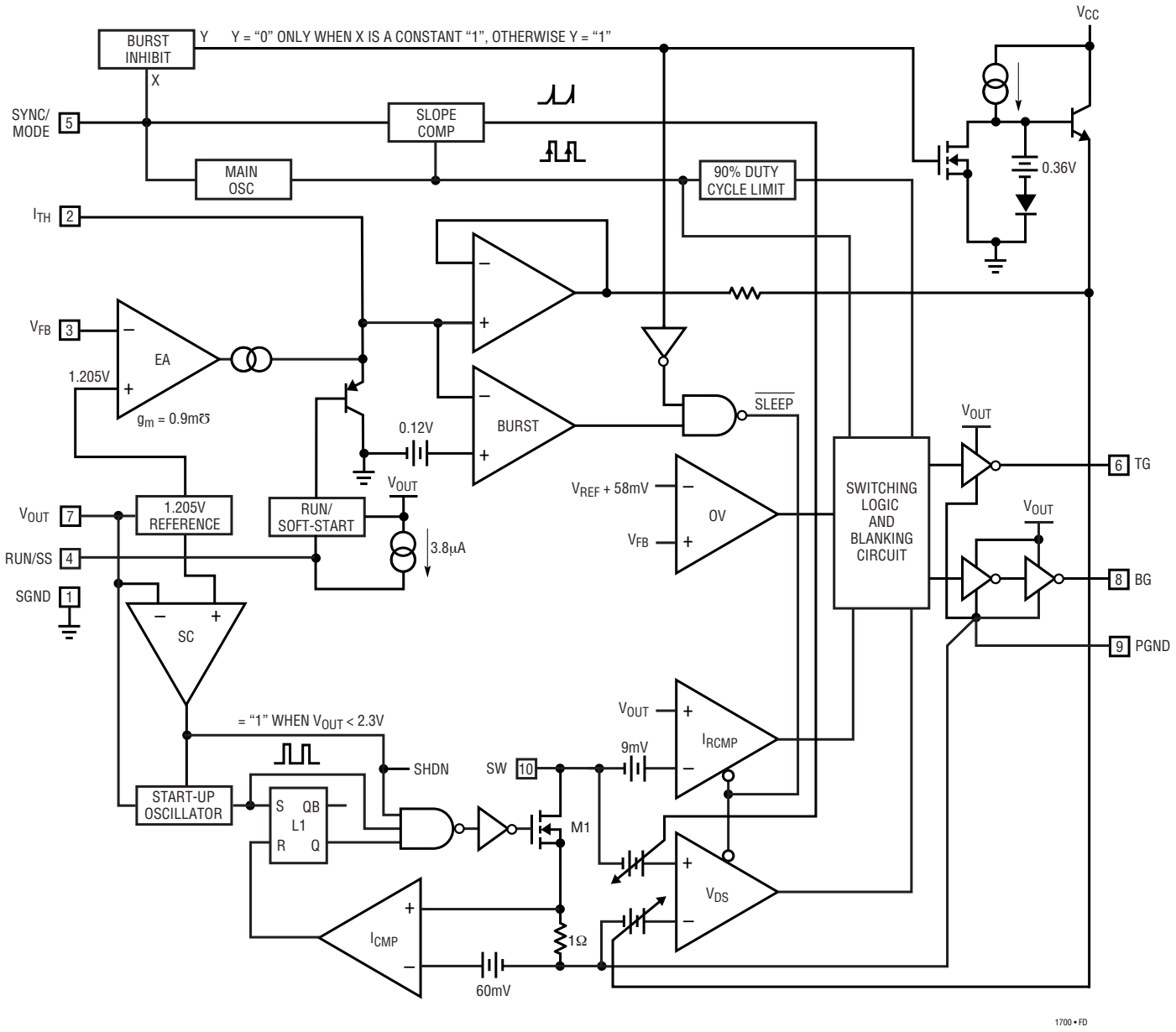
V_{OUT} (Pin 7): This pin performs two functions. It serves as the supply pin and also as one of the inputs to the current reversal comparator.

BG (Pin 8): Bottom Gate Drive. Drives the external main N-channel MOSFET with a voltage swing between 0V to V_{OUT}.

PGND (Pin 9): Top and Bottom Gate Drivers Ground. Connects to the (–) terminal of C_{OUT}. Source of the main N-channel MOSFET must be connected close to this pin since this pin is also one of the inputs to the V_{DS} sense amplifier.

SW (Pin 10): This pin connects to the inputs of two comparators: The V_{DS} sense amplifier and the current reversal comparator. The drain of an internal N-channel start-up MOSFET (M1) is also connected to this pin.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC1700 is a constant frequency, current mode controller for DC/DC step-up converters. In normal operation, the main external N-channel power MOSFET is turned on when the oscillator sets a latch and turned off either when the V_{DS} sense amplifier (V_{DS}) resets the latch or the duty cycle has reached 90%. When the main MOSFET is turned off, the synchronous rectifier P-channel MOSFET is turned on until either the inductor current is about to reverse, as determined by the current reversal comparator (I_{RCMP}), or the next cycle begins. Inductor current is measured by sensing the V_{DS} potential across the conducting MOSFET. The peak inductor current is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier (EA). An external resistive divider connected between V_{OUT} and GND allows EA to receive an

OPERATION

output feedback voltage V_{FB}. When the load current increases, it causes a slight decreases in V_{FB} relative to the 1.205V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current.

The internal oscillator can be synchronized to an external clock applied to the SYNC/MODE pin and can lock to a frequency between 400kHz to 750kHz. When not synchronized, the oscillator runs at 530kHz.

The main control loop is shut down by pulling the RUN/SS pin low. Releasing the RUN/SS pin allows an internal 3.8μA current source to charge up an external soft-start capacitor (C_{SS}). When this voltage reaches 0.8V, the main control loop is enabled with the I_{TH} voltage clamped at approximately 5% of its maximum value. As C_{SS} continues to charge, I_{TH} is gradually released allowing normal operation to resume.

An overvoltage comparator OV guards against transient overshoots greater than 5% above regulated voltage by turning off both the external MOSFETs and keeping them off until the fault is removed.

To prevent excessive inductor current buildup, the main N-channel MOSFET is only allowed to turn on for a maximum duty cycle of 90%.

Burst Mode Operation

The LTC1700 can be enabled to go into Burst Mode operation at low load currents simply by connecting the SYNC/MODE pin to a voltage of at least 1.2V. In this mode, the peak current of the inductor is set as if V_{ITH} = 0.36V (at low duty cycles) even though the voltage at the I_{TH} pin is actually at a lower value. If the inductor's average current is greater than the load requirement, the voltage at the I_{TH} pin will drop. When the I_{TH} voltage goes below 0.12V, the internal sleep signal goes low, turning off both external MOSFETs. Now the load current will solely be supplied by the output capacitor and the output voltage begins to droop. This drooping of the output voltage results in the rise of I_{TH} voltage and once it has risen above 0.22V, switching will then be resumed on the next oscillator cycle.

Frequency Synchronization

The LTC1700 can be externally driven by a CMOS (0V to 1.2V) compatible clock signal between 400kHz and 750kHz. *Do not* synchronize the LTC1700 below 400kHz or above 750kHz as this may cause abnormal operation. During synchronization, Burst Mode operation is inhibited.

Low Input Operation

When the voltage at V_{OUT} is less than 2.3V, the LTC1700 operates in the "start-up" mode. In this mode, most internal circuitry is turned off except the start-up oscillator, current comparator (I_{CMP}) and the start-up comparator (SC). The voltage at pins TG and BG are forced to ensure both the external MOSFETs are off. The start-up oscillator runs at about 210kHz at 50% duty cycle and is used to set the latch (L1) which turns on the internal MOSFET M1 (see Functional Diagram). When the inductor's current reaches 60mA, the current comparator (I_{CMP}) is tripped and resets the latch. This turns M1 off and the parasitic diode of the external P-channel MOSFET is used to transfer the energy from the inductor to the output capacitor. The above cycle repeats again on the next oscillator pulse.

When the output voltage rises above 2.3V, the start-up comparator will trip, powering up the rest of the LTC1700. All start-up circuitry will then be turned off. Now the LTC1700 has successfully transitioned out of its start-up mode and commences normal operation as described under the section "Main Control Loop."

Protection Circuitry

Two protection circuits are incorporated into the LTC1700.

To prevent the inductor from saturating the maximum duty cycle of the regulator is limited to 90%. This is done to ensure that at least 10% of the time energy is being transferred from the inductor to the output capacitor.

Output overvoltage protection is also provided. Should the output rises about 5% above the regulated value, both the external MOSFETs will be forced off.

APPLICATIONS INFORMATION

Power MOSFET Selection

The LTC1700 requires two external power MOSFETs, one for the main switch (N-channel) and one for the synchronous rectifier (P-channel). Since the voltage operating range of the LTC1700 is limited to less than 6V, the breakdown voltage of the MOSFETs is not a concern. Therefore the MOSFETs parameters that should be used for selecting the power MOSFETs are threshold voltage $V_{GS(TH)}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{D(MAX)}$.

The gate drive voltage is set by the output voltage, V_{OUT}. Since the LTC1700 exits the start-up mode at 2.3V, sub-logic level threshold MOSFETs should be used in LTC1700 applications. Newer MOSFETs with guaranteed R_{DSON} at gate voltage of 1.8V are now available and will work very well with the LTC1700.

The MOSFETs on-resistance is chosen based on the required load current. The maximum average output current $I_{O(MAX)}$ is :

$$I_{O(MAX)} = (I_{PK} - 0.5\Delta I)(1 - DC)$$

where:

I_{PK} = Peak Inductor Current

ΔI = Inductor Ripple Current

DC = Duty Cycle

The peak inductor current is inherently limited in a current mode controller. The maximum V_{DS} sense voltage of the main MOSFET is limited to 78mV. The LTC1700 will not allow peak inductor current to exceed 78mV/$R_{DS(ON)(N\text{-}CHANNEL)}$. The following equation is a good guide for determining the required $R_{DS(ON)(MAX)}$, allowing some margin for ripple current, current limit and variations in the LTC1700 and external component values:

$$R_{DS(ON)(MAX)} \cong \frac{\Delta V_{SENSE}}{\left(\frac{I_{O(MAX)}}{1-DC} + \frac{1}{2}\Delta I_L\right)(\rho_T)}$$

For 25°C operating condition, set ΔV_{SENSE} = 65mV. For conditions that vary over the full temperature range, set ΔV_{SENSE} = 55mV.

The ρ_T is a normalized term accounting for the significant variation in $R_{DS(ON)}$ with temperature, typically about 0.375%/°C as shown in Figure 2. Junction to case temperature T_{JC} is around 10°C in most applications. For a maximum ambient temperature of 70°C, using $\rho_{80°C} \cong 1.2$ in the above equation is a reasonable choice. This equation is plotted in Figure 3 to illustrate the dependence of maximum output current on $R_{DS(ON)}$, assuming $\Delta I = 0.4I_{O(MAX)}$.

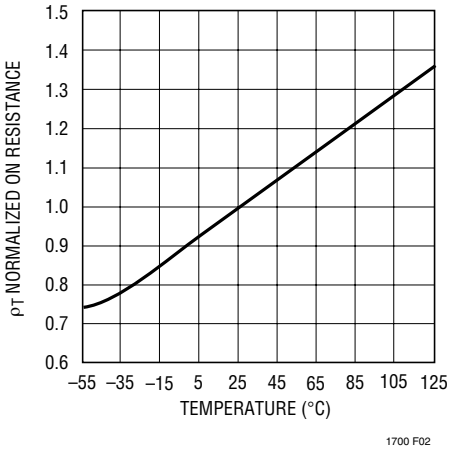


Figure 2. $R_{DS(ON)}$ vs Temperature

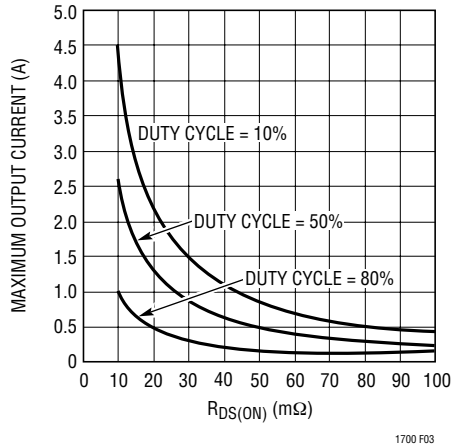


Figure 3. Maximum Current vs $R_{DS(ON)}$

Power dissipated by the main and synchronous MOSFETs depends upon their respective duty cycles and

APPLICATIONS INFORMATION

load current. When the LTC1700 is operating in continuous mode, the duty cycles for the MOSFETs are:

Main MOSFET Duty Cycle = $1 – V_{IN}/V_{OUT}$

Synchronous MOSFET Duty Cycle = V_{IN}/V_{OUT}

The MOSFET power dissipations at maximum output current are:

$$P_{MAIN} = (1 – V_{IN}/V_{OUT})(I_{O(MAX)}^2)(\rho T_{(MAIN)})(R_{DS(ON)}) + (k)(V_{OUT}^2)(I_{O(MAX)})C_{RSS}(f)$$

$$P_{SYNC} = (V_{IN}/V_{OUT})(I_{O(MAX)}^2)(\rho T_{(BOT)})(R_{DS(ON)})$$

Both MOSFETs have I^2R losses and the P_{MAIN} equation includes an additional term for transition losses, which are largest at high output voltages. The constant k = 2.5 can be used to estimate the amount of transition loss. The synchronous MOSFET losses are greatest at high input voltage and low output voltage.

Start-Up Load Current

In start-up mode, the current limit is set at 60mA and the oscillator runs at 210kHz with 50% duty cycle at V_{IN} = 1.8V. Since the current limit is low, the amount of energy that is stored in the inductor during the on time is small. Therefore the LTC1700 is incapable of supplying the full load current. Figure 4 shows the amount of load current the LTC1700 can provide while successfully exiting out of the start-up mode. If the load current exceeds the amount shown in Figure 4 during start-up, the output voltage will not increase but will "hang" at a value below the regulated voltage. However, if the load current is lower, then there is a net positive amount of energy stored in the output capacitor for every cycle. The output voltage then rises and once it exceeds 2.3V, the LTC1700 will successfully exit out of its start-up mode.

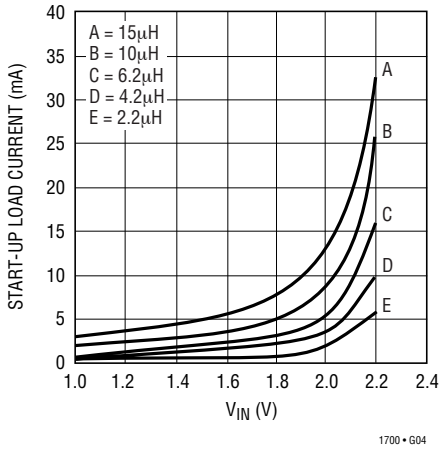


Figure 4. Start-Up Load Current

Operating Frequency and Synchronization

The choice of operating frequency and inductor value is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator runs at a nominal 530kHz frequency when the SYNC/MODE pin is either connected to GND or V_{IN}. When a CMOS compatible clock is applied to the SYNC/MODE pin, the internal oscillator will lock on to the external clock. The LTC1700 uses a novel technique to phase lock to the external clock without the requirement of an external PLL filter, hence minimizing components. The capture range is between 400kHz to 750kHz. Do not synchronize below or above the capture range as this will cause abnormal operation. During synchronization, Burst Mode operation is inhibited.

The LTC1700 will lock on at the leading edge of the external clock and the minimum pulse width required is 200ns.

Remember just because you can operate at a high switching frequency doesn't always mean you should. At higher frequencies the switching loss increases, so the C_{RSS} of the N-channel MOSFET becomes very critical to keep efficiencies high.

Slope Compensation and Peak Inductor Current

Current mode switching regulators that operate with a duty cycle greater than 50% with continuous inductor current can exhibit duty cycle instability. While the regulator will not be damaged and may even continue to function acceptably, a look at its frequency spectrum will indicate harmonics. These harmonics may interfere with other sensitive devices and will cause non-optimal performance.

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To eliminate this subharmonic oscillation, a compensating ramp is added internally to the LTC1700 on the inductor current waveform when the duty cycle exceeds 5%. This scheme, known as slope compensation, makes the loop perceive that there is more inductor current than it actually has. As a result, the maximum current capability of the regulator is reduced. This reduction is proportional to the duty cycle and is shown in Figure 5. Hence for applications that operate at high duty cycles, the N-channel MOSFET chosen should have a lower $R_{DS(ON)}$ to make up for this reduction (See Design Example).

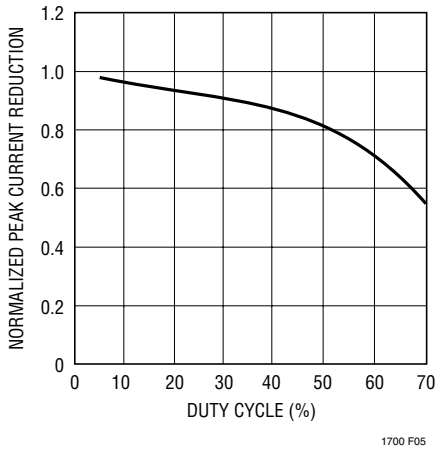

Figure 5. Maximum Output Current vs Duty Cycle

Inductor Value Selection

Given the input voltage, inductor value and operating frequency, the ripple current can be calculated:

$$\Delta I_L = V_{IN}\left(\frac{DC}{fL}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with small ripple current. To achieve this, however, requires a larger inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{O(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L_{MIN} \geq V_{IN(MAX)}\left(\frac{DC}{f\Delta I_L}\right)$$

With Burst Mode operation enabled on the LTC1700, the ripple current is normally set such that the inductor current is continuous during burst periods. Remember that during bursting, the peak current is clamped at approximately:

$$I_{BURST(PEAK)} \cong 36mV/R_{DS(ON)}$$

Hence the peak-to-peak ripple selected for optimal burst mode operation should not exceed $I_{BURST(PEAK)}$. This implies a minimum inductance of:

$$L_{MINBURST} = \frac{V_{IN(MAX)}(DC)}{(f)(0.66)\left(\frac{I_{OMAX}}{1-DC}\right)}$$

In applications that invoke Burst Mode operation, the inductor should be chosen so it has low ripple ($0.4I_{OMAX}$) current during heavy load and continuous operation during bursting. The criteria for selecting which equation to use is:

Use L_{MIN} for Duty Cycle > 36%

Use $L_{MINBURST}$ for Duty Cycle ≤ 36%

A smaller value than L_{MIN} could be used in the circuit; however, the inductor current will not be continuous during burst periods. The advantage of using a smaller inductance than L_{MIN} is primarily size. The disadvantage is higher output ripple.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy, or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core losses and are

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preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and output voltage ripple. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available which do not increase the height significantly.

C_{OUT} Selection

During continuous operation, the output capacitor has a trapezoidal current profile. The RMS current into the capacitor is then given by:

$$I_{COUT(RMS)} \cong \left(I_{OUT} \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \right)$$

The RMS current is greatest at $I_{OUT(MAX)}$ and minimum input working voltage. Therefore the output capacitor should be chosen with a rating at least $I_{COUT(RMS)}$. Several capacitors can also be paralleled to meet this requirement. Besides RMS current rating, the selection of C_{OUT} is also driven by the required effective series resistance (ESR). The ESR of the capacitor together with its capacitance determines the output ripple voltage and can be expressed as:

$$\Delta V_{OUT} \approx I_{PK}(ESR) + \frac{2I_{OUT}}{C_{OUT}} t_{ON}$$

where C_{OUT} = output capacitance, t_{ON} = on time of main MOSFET and I_{PK} = peak inductor current. A common technique to lower the total ESR at the output is to parallel the output capacitor with a 10μF ceramic capacitor.

The choice of using a smaller output capacitance increases the output ripple voltage due to the frequency dependent term but can be compensated for by using capacitors of very low ESR to maintain low ripple voltage. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR (size) product of any aluminum electrolytic at a somewhat higher price.

Multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum, available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo OS-CON, Nichicon PL series and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Setting Output Voltage

The LTC1700 develops a 1.205V reference voltage between the feedback (Pin 3) terminal and ground (see Figure 6). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 1.205(1 + R2/R1)$$

For most applications, a 30k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to LTC1700.

Efficiency Considerations

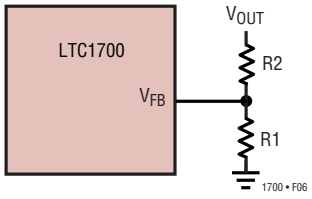

Figure 6. Setting Output Voltage

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The efficiency of a switching regulator is equal to the output power divided by the input power (× 100%). Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1700 circuits:

1. LTC1700 supply current. This DC supply current, given in the electrical characteristics, excludes MOSFET drivers and control current. This supply current results in a small loss which increases with V_{OUT}.

2. MOSFETs gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched on and then off, a packet of gate charge Q_g moves from V_{OUT} to ground. The resulting current out from V_{OUT} is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_{g(TOP)} + Q_{g(BOT)})$. At high switching frequencies, this loss becomes increasingly important.

3. DC I^2R Losses. Since there is no sense resistor needed, DC I^2R losses arise only from the resistances of the MOSFETs and inductor. In continuous mode, the average current flows through the inductor but is "chopped" between the synchronous P-channel MOSFET and the main N-channel MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistance of the inductor to obtain the DC I^2R loss. For example, if each $R_{DS(ON)} = 0.05\Omega$ and $R_L = 0.15\Omega$, then the total resistance is 0.2Ω. This results in losses ranging from 2% to 8% as the output current increases from 0.5A to 2A for a 5V output. I^2R losses cause the efficiency to drop at high output currents.

4. Transition losses apply to the main external MOSFET and increase at higher operating frequencies and output voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = 2.5(V_{OUT})^2 I_{O(MAX)} C_{RSS}(f)$$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, and inductor core losses, generally account for less than 2% total loss.

Run/Soft-Start Function

The RUN/SS pin is a dual purpose pin that provides the soft-start function and a means to shut down the LTC1700. Soft-start reduces input surge current from V_{IN} by gradually increasing the internal current limit. Power supply sequencing can also be accomplished using this pin.

An internal 3.8μA current source charges up an external capacitor C_{SS}. When the voltage on the RUN/SS pin reaches 0.7V, the LTC1700 begins operating. As the voltage on RUN/SS continues to ramp from 0.7V to 1V, the internal current limit is also ramped at a proportional linear rate. The current limit begins near 0A (at $V_{RUN/SS} = 0.7V$) and ends at $0.078/R_{DS(ON)}$ ($V_{RUN/SS} \approx 2.2V$). The output current thus ramps up slowly, reducing the starting surge current required from the input power supply. If the RUN/SS has been pulled all the way to ground, there will be a delay before the current limit starts increasing and is given by:

$$t_{DELAY} = 1.13 C_{SS}/I_{CHG}$$

For input voltages less than 2.3V during the start-up duration, the soft-start function has no effect on the internal 60mA current limit. Therefore to fully take advantage of this feature, the soft-start capacitor has to be sized accordingly to account for the time it takes V_{OUT} to reach 2.3V. An approximate mathematical representation for the time it takes V_{OUT} to reach 2.3V upon powering up is given by:

$$t_{POWER-UP} = \frac{C_{OUT}(2.3 - V_{IN} - V_D)}{\frac{260(L)}{2.3 - V_{IN}} - I_{OUT}}$$

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where:

V_D = Voltage drop of P-channel parasitic diode

I_{OUT} = Initial load current during start-up

C_{OUT} = Output capacitance

Hence you would select the start-up capacitor, C_{SS}, to ensure $t_{DELAY} > t_{POWERUP}$. Remember that the above equation is only valid for $V_{IN} < 2.3V$. If V_{IN} is greater than 2.3V, then $t_{POWERUP} = 0ns$.

Design Example

Assume the LTC1700 is used to convert a 3.3V input to 5V output. Load current requirement is a maximum 3A and a minimum of 100mA. Efficiency at both low and high load currents is important. Ambient temperature = 25°C.

Since low load current efficiency is important, Burst Mode operation is enabled by connecting pin 5 to V_{OUT}.

Duty Cycle = $1 - V_{IN}/V_{OUT} = 0.34$

Since the duty cycle is less than 36%, the value of the inductor is chosen based on the $L_{MINBURST}$ equation.

$L_{MINBURST} = 0.8\mu H$.

In the application, (Figure 7) a 4.6μH inductor is used to further reduce ripple current. The actual ripple current is now:

$$\Delta I_L = 3.3V\left(\frac{0.34}{530kHz(4.6\mu H)}\right) = 0.46A$$

For the main N-channel MOSFET, the $R_{DS(ON)}$ should be:

$$R_{DS(ON)(N-CHANNEL)} = \frac{63mV}{\frac{I_{O(MAX)}}{1-D} + 0.5(\Delta I_L)} = 13.2m\Omega$$

Accounting for the peak current reduction due to slope compensation (see Figure 5), the $R_{DS(ON)}$ of the N-channel should be:

$R_{DS(ON)} = (13.2)(0.9)$

$= 11.9m\Omega$

The factor, 0.9, is obtained from Figure 5 using a duty cycle of 34%. The peak current of the inductor is 5A. Select an inductor that does not saturate at this current level. The average current through the N-channel MOSFET is 1.62A while the average current through the synchronous P-channel MOSFET is 3A.

The FDS6670A and FDS6375 are chosen for the N-channel and P-channel MOSFET respectively. We can now calculate the temperature rise in the FDS6670A. RMS current flowing through the FDS6670A is 2.78A. Hence power dissipated is:

$P_{DISS} = (2.78)^2 (8 \times 10^{-3})$

$= 61.82mW$

The θ_{JA} of the FDS6670A is 50°C/W. Therefore temperature rise is:

$T_{RISE} = 61.82mW \times 50$

$= 3.1°C$

This is an insignificant temperature rise and therefore the omission of the ρT in calculating the required $R_{DS(ON)}$ does not generate a large error.

At 3A load, the RMS current into the output capacitor is given by:

$I_{COUT(RMS)} = 3(5/3.3 - 1)^{0.5} = 2.15A$

To meet the RMS current requirement, two SANYO POSCAP 100μF capacitors are paralleled. These capacitors have low ESR (55mΩ) and to futher reduce the overall ESR, a 10μF ceramic capacitor is placed in parallel with the POSCAP capacitor. Figure 7 shows the complete circuit.

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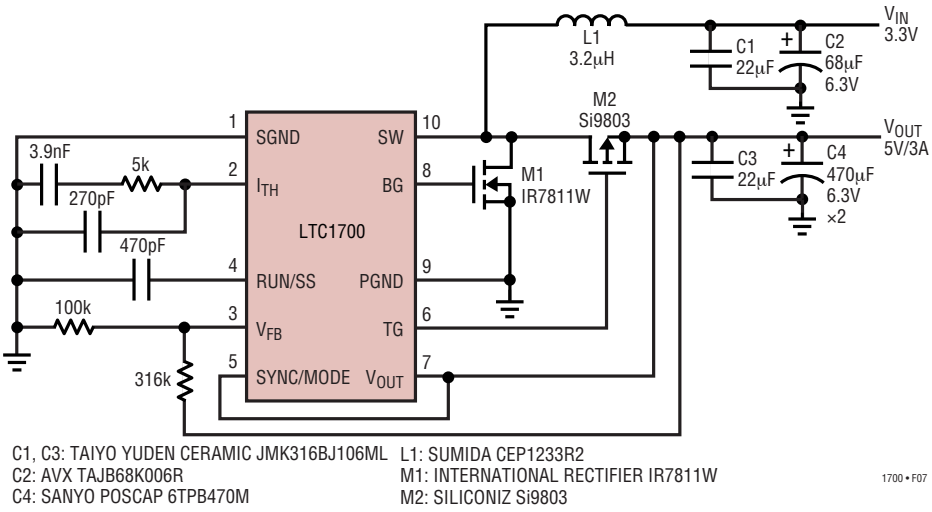


Figure 7. Design Example Schematic

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1700. These items are illustrated graphically in the layout diagram in Figure 8. Check the following in your layout:

1. Are all the components connected close to the SW node (Pin 10)? The SW pin is the input to the V_{DS} sense amplifier and the current reverse comparator.

2. Connect the V_{OUT} lead directly to the source of the P-channel MOSFET. Besides supplying current to the LTC1700, it also serves as the other input to the current reverse comparator.

3. Connect the (+) plate of C2 to the source of the P-channel MOSFET. This capacitor supports the load current when the inductor is being "recharged".

4. Connect the (–) plate of C2 to the source of the N-channel MOSFET. Connect the power and signal ground to this node.

5. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1 and R2 must be connected between the (+) plate of C2 and signal ground.

6. Keep the switching node SW away from sensitive small signal nodes.

7. Switched currents flow in M1, M2 and C2, keep the loop formed by these components as small as possible.

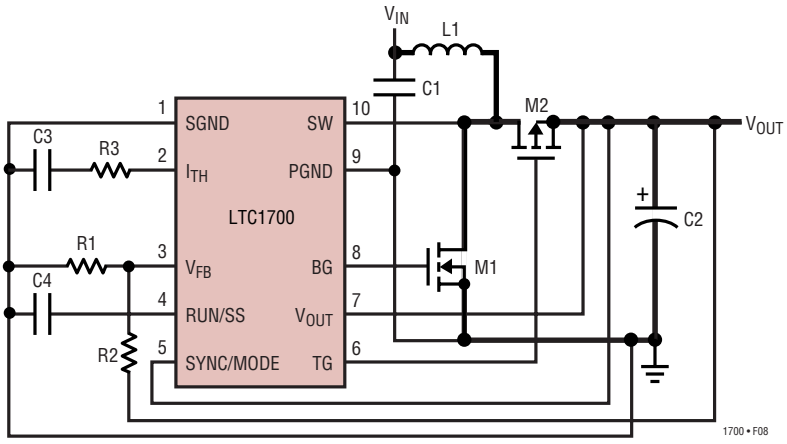
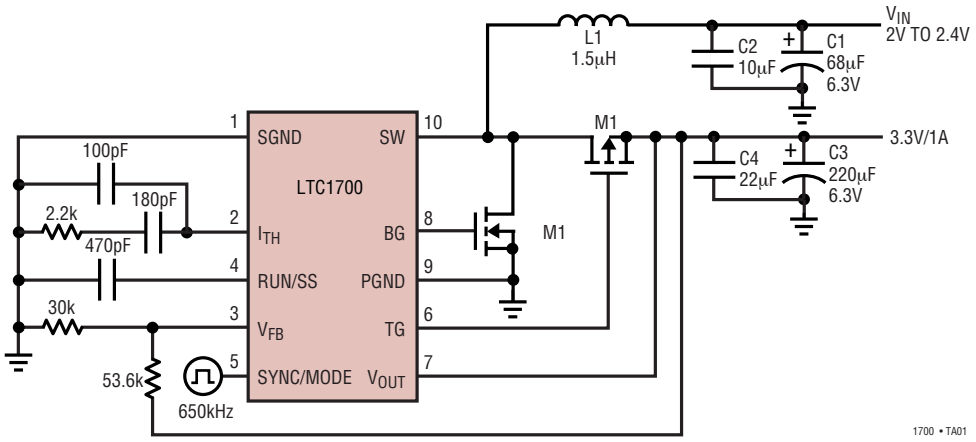


Figure 8. LTC1700 Layout Diagram (See PC Board Layout Checklist)

TYPICAL APPLICATION

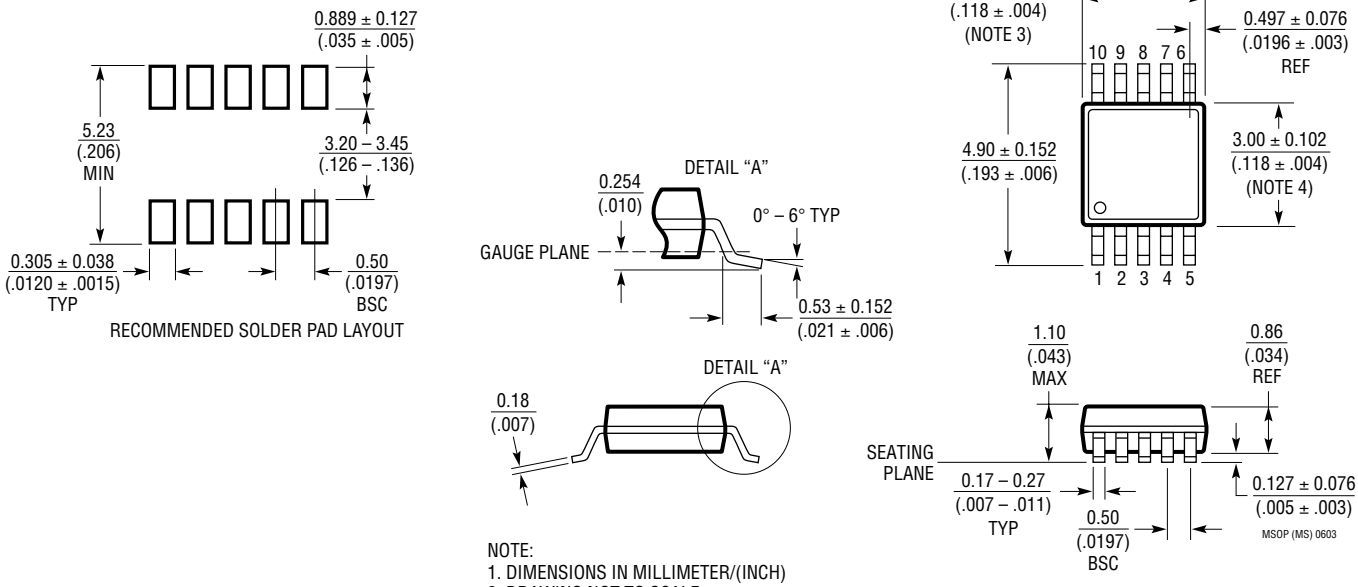
LTC1700 3.3V/1A Regulator with External Frequency Synchronization



C1: AVX TAJB686K006R
C2: TAIYO YUDEN CERAMIC JMK316BJ106ML
C3: AVX TPSD227M006R0100
C4: TAIYO YUDEN CERAMIC JMK325BJ226MM
L1: MURATA LQN6C
M1: SILICONIX Si6562DQ

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

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