Dual Smart Card Interface with Serial Control

FEATURES

- **Compatible with ISO7816-3 and EMV Electrical Specifications**
- **Power Management and Control for Two Smart Cards**
- **Control/Status Serial Port May Be Daisychained for Multicard Applications**
- **Automatic Shutdown on Electrical Faults**
- **Buck/Boost Charge Pump Generates 5V, 3V or 1.8V Outputs (Smart Card Classes A, B and C)**
- Independent 5V/3V/1.8V Level Control for Both Cards
- Automatic Level Translation
- Supervisory Functions Prevent Smart Card Faults
- Low Operating Current: 250µA Typical
- Ultralow Shutdown Current
- >10kV ESD on Smart Card Pins
- Small 32-Lead 5mm × 5mm QFN Package

APPLICATIONS

- Handheld Payment Terminals
- Pay Telephones
- ATM Machines
- POS Terminals
- Computer Keyboards
- Multiple S.A.M. Sockets

DESCRIPTION

The LTC®1955 provides all necessary supervisory and power control functions for two smart cards, two S.A.M. cards or a combination of S.A.M. and smart cards. It provides a charge pump for battery-powered applications as well as all necessary level shifting circuitry.

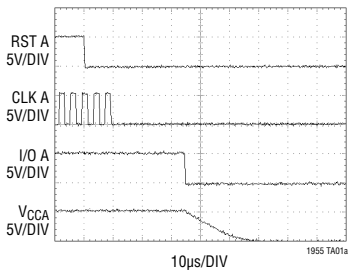
The card voltages can be independently set to 1.8V, 3V or 5V. Both card interfaces include a card detection channel with automatic debounce circuitry. To reduce wiring costs, the LTC1955 interfaces to a microcontroller via a simple 4-wire serial interface. Multiple devices may be connected in daisychain fashion so that the number of wires to the card socket board is independent of the number of sockets. Status data is returned over the same interface.

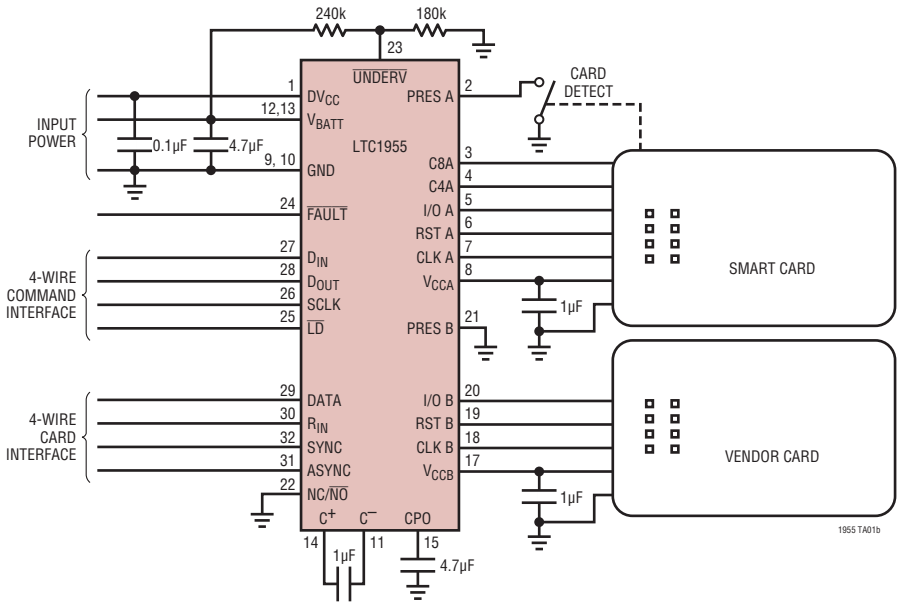
Extensive security features ensure proper deactivation sequencing in the event of a supply fault or a smart card electrical fault. The smart card pins can withstand greater than 10kV ESD in-situ with no additional components.

The LTC1955 is available in a low profile (0.75mm) 5mm × 5mm QFN package.

TYPICAL APPLICATION

Deactivation Sequence



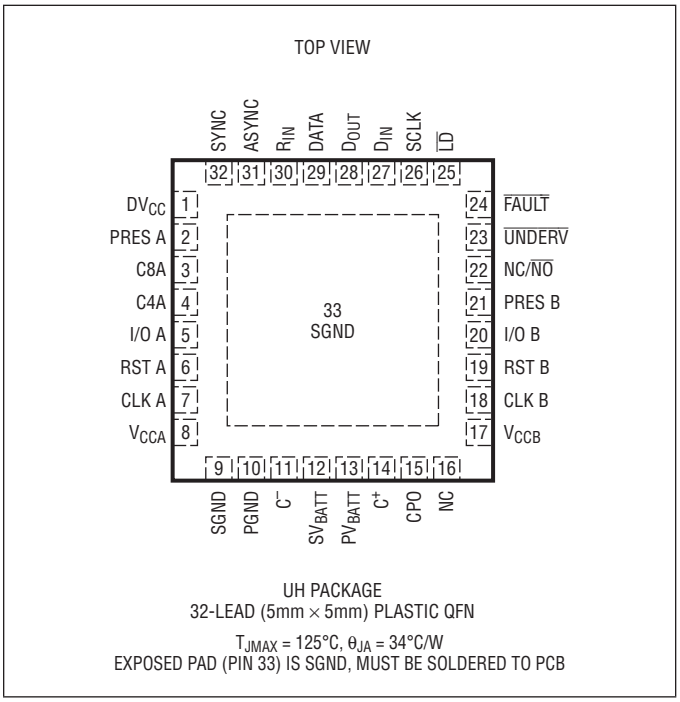


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BATT}, DV_{CC}, CPO, $\overline{FAULT}$, $\overline{UNDERV}$ to GND ..... –0.3V to 6.0V
PRES A/PRES B, DATA, R_{IN}, SYNC, ASYNC, $\overline{LD}$, D_{IN}, SCLK to GND.....–0.3V to (DV_{CC} + 0.3V)
I/O A..... –0.3V to (V_{CCA} + 0.3V)
I/O B..... –0.3V to (V_{CCB} + 0.3V)
I_{VCCA}/IV_{CCB}.....80mA
V_{CCA}/V_{CCB} Short-Circuit Duration..... Indefinite
Operating Temperature Range (Note 4).... –40°C to 85°C
Junction Temperature ..... 125°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1955EUH#PBF	LTC1955EUH#TRPBF	1955	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC1955IUH#PBF	LTC1955IUH#TRPBF	1955	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC1955EUH	LTC1955EUH#TR	1955	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC1955IUH	LTC1955IUH#TR	1955	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{PVBATT} = V_{SVBATT} = 3.3V, DV_{CC} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply						
V_{BATT} Operating Voltage		●	2.7		5.5	V
I_{PVBATT} + I_{SVBATT} Operating Current	V_{CCA} = 5V, V_{CCB} = 0V, I_{CCA} = 0µA V_{CCA} = V_{CCB} = 5V, I_{CCA} = I_{CCB} = 0µA	● ●		250 350	400 500	µA µA
I_{PVBATT} + I_{SVBATT} Shutdown Current	No Cards Present. V_{CPO} = 0V	●		0.75	1.75	µA
DV_{CC} Operating Voltage		●	1.7		5.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{PVBATT} = V_{SVBATT} = 3.3V, DV_{CC} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{DVCC} Operating Current		●		10	25	µA
I_{DVCC} Shutdown Current		●		0.5	1.5	µA
Charge Pump						
R_{OLCP} 5V Mode Open-Loop Output Resistance	V_{BATT} = 3.075V, I_{CPO} = I_{CCA} + I_{CCB} = 120mA (Note 3)	●		5.7	8.5	Ω
CPO Turn-On Time	$I_{CCA/B}$ = 0mA, 10% to 90%	●		0.6	1.5	ms
Smart Card Supplies V_{CCA}, V_{CCB}						
$V_{CCA/B}$ Output Voltage	5V Mode, 0 < $I_{CCA/B}$ < 60mA 3V Mode, 0 < $I_{CCA/B}$ < 50mA 1.8V Mode, 0 < $I_{CCA/B}$ < 30mA	● ● ●	4.65 2.75 1.65	5 3 1.8	5.35 3.25 1.95	V V V
$V_{CCA/B}$ Turn-On Time	$I_{CCA/B}$ = 0mA, 10% to 90%	●		0.8	1.5	ms
Undervoltage Detection	Relative to Nominal Output	●	–9	–5	–2.5	%
Overcurrent Detection	5V Mode	●	65	100	135	mA
Smart Card Detection						
Debounce Time (↓ PRES A/B to ↑ D15/D7)	$V_{NC/\overline{NO}}$ = 0V	●	20	35	60	ms
PRES A, PRES B Pull-Up Current	$V_{PRESA/B}$ = 0	●		1.25	2.5	µA
Deactivation Time (↓ RST to V_{CC} = 0.4V)	$I_{CCA/B}$ = 0mA, $C_{VCCA/B}$ = 1µF	●		20	250	µs
CLK A, CLK B						
Low Level Output Voltage (V_{OL}), (Note 2)	Sink Current = –200µA	●			0.2	V
High Level Output Voltage (V_{OH}), (Note 2)	Source Current = 200µA	●	$V_{CCA/B}$ – 0.2			V
Rise/Fall Time (Note 2)	Loaded with 50pF, 10% to 90%	●			16	ns
CLK A, CLK B Frequency (Note 2)		●	10			MHz
RST A, RST B, C4A, C8A						
Low Level Output Voltage (V_{OL}), (Note 2)	Sink Current = –200µA	●			0.2	V
High Level Output Voltage (V_{OH}), (Note 2)	Source Current = 200µA	●	$V_{CCA/B}$ – 0.2			V
Rise/Fall Time (Note 2)	Loaded with 50pF, 10% to 90%	●			100	ns
I/O A, I/O B						
Low Level Output Voltage (V_{OL}), (Note 2)	Sink Current = –1mA (V_{DATA} = 0V)	●			0.3	V
High Level Output Voltage (V_{OH}), (Note 2)	Source Current = 20µA (V_{DATA} = V_{DVCC})	●	0.85 • $V_{CCA/B}$			V
Rise/Fall Time (Note 2)	Loaded with 50pF, 10% to 90%	●			500	ns
Short-Circuit Current (Note 2)	V_{DATA} = 0V	●		5	10	mA
DATA						
Low Level Output Voltage (V_{OL})	Sink Current = –500µA ($V_{I/OA/B}$ = 0V)	●			0.3	V
High Level Output Voltage (V_{OH})	Source Current = 20µA ($V_{I/OA/B}$ = $V_{CCA/B}$)	●	0.8 • DV_{CC}			V
Rise/Fall Time	Loaded with 50pF, 10% to 90%	●			500	ns
R_{IN}, D_{IN}, SCLK, $\overline{LD}$, SYNC, ASYNC, NC/$\overline{NO}$						
Low Input Threshold (V_{IL})		●			0.15 • DV_{CC}	V
High Input Threshold (V_{IH})		●	0.85 • DV_{CC}			V
Input Current (I_{IH}/I_{IL})		●	–1		1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{PVBATT} = V_{SVBATT} = 3.3V, DV_{CC} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D_{OUT}						
Low Level Output Voltage (V_{OL})	Sink Current = –200µA	●			0.3	V
High Level Output Voltage (V_{OH})	Source Current = 200µA	●	DV_{CC} – 0.3			V
$\overline{UNDERV}$						
Threshold		●	1.17	1.23	1.29	V
Leakage Current	$V_{\overline{UNDERV}}$ = 3.3V	●			50	nA
$\overline{FAULT}$						
Low Level Output Voltage (V_{OL})	Sink Current = –200µA	●		0.005	0.3	V
Leakage Current	$V_{\overline{FAULT}}$ = 5.5V	●			1	µA

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Port Timing							
t_{DS}	D_{IN} Valid to SCLK Setup		●	8			ns
t_{DH}	D_{IN} Valid to SCLK Hold		●	8			ns
t_{DD}	D_{OUT} Output Delay	C_{LOAD} = 15pF	●	15		60	ns
t_L	SCLK Low Time		●	50			ns
t_H	SCLK High Time		●	50			ns
t_{CL}	SCLK to $\overline{LD}$		●	50			ns
t_{LC}	$\overline{LD}$ to SCLK		●	0			ns
t_{LFC}	$\overline{LD}$ Falling to SCLK		●	50			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

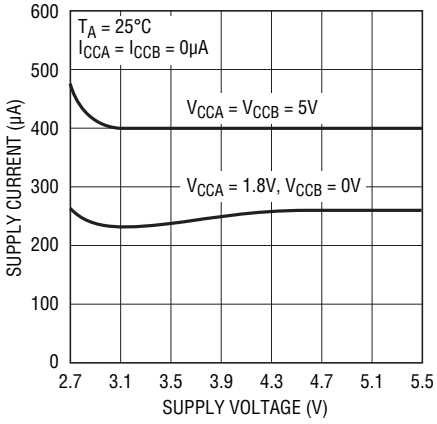
Note 2: This specification applies to all three smart card voltage classes: 1.8V, 3V and 5V.

Note 3: $R_{OLCP} \cong (2V_{BATT} – V_{CPO})/I_{CPO}$; V_{CPO} will depend upon total load (I_{CCA} + I_{CCB}) and minimum supply voltage V_{BATT}. See Figure 5.

Note 4: The LTC1955E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1955I is guaranteed to meet performance specifications over the full –40°C to 85°C temperature range.

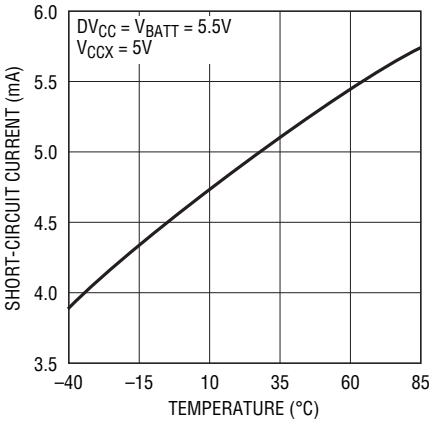
TYPICAL PERFORMANCE CHARACTERISTICS

No Load Supply Current vs V_{BATT}



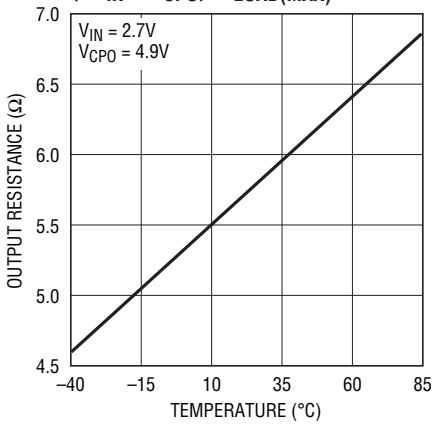
1955 G01

I/O X Short-Circuit Current vs Temperature



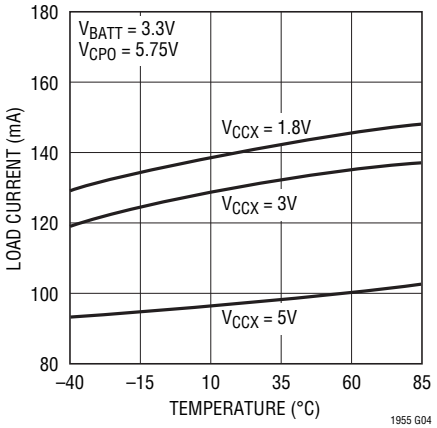
1955 G02

Charge Pump Open-Loop Output Resistance vs Temperature ($2V_{IN} – V_{CPO}$) / $I_{LOAD(MAX)}$



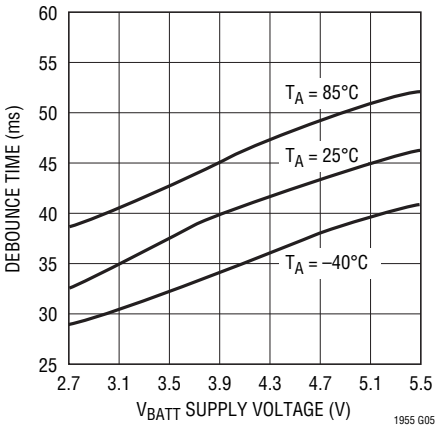
1955 G03

V_{CCX} Overcurrent Shutdown Threshold vs Temperature



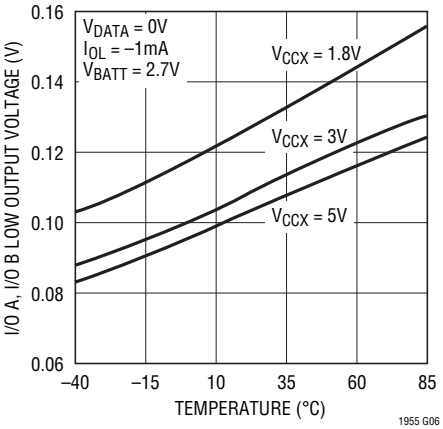
1955 G04

Card Detection Debounce Time vs V_{BATT} Supply Voltage



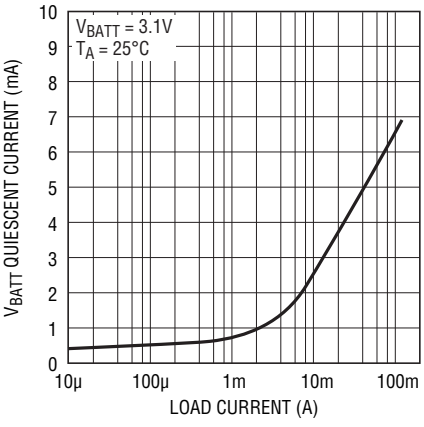
1955 G05

Bidirectional Channel (I/O A, I/O B) Low Output Level vs Temperature



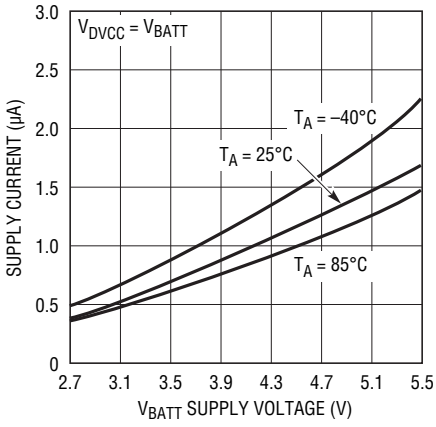
1955 G06

V_{BATT} Quiescent Current [I_{BATT} – 2 (I_{CCA} + I_{CCB})] vs Load Current



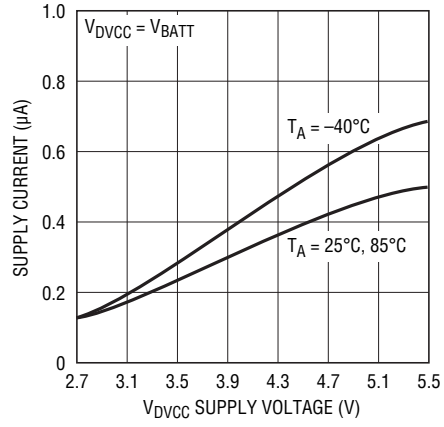
1955 G07

V_{BATT} Shutdown Current vs Supply Voltage



1955 G08

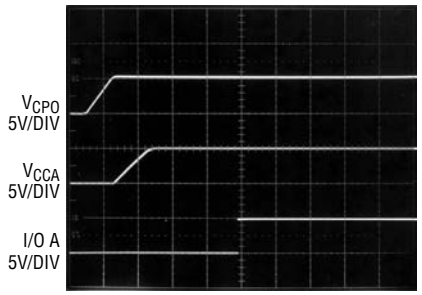
DV_{CC} Shutdown Current vs Supply Voltage



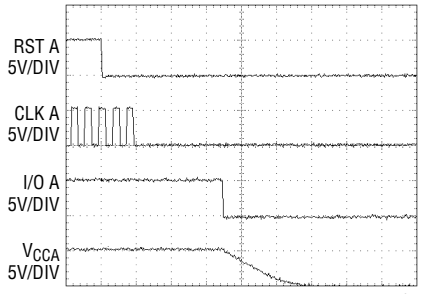
1955 G09

TYPICAL PERFORMANCE CHARACTERISTICS

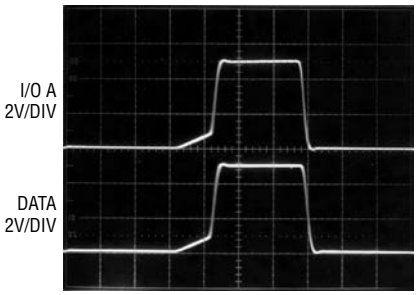
Charge Pump and LDO Activation



Deactivation Sequence



Data – I/O Channel, C_L = 50pF



PIN FUNCTIONS

SV_{BATT}: Power. Supply voltage for analog sections of the LTC1955.

PV_{BATT}: Power. Supply voltage for the charge pump.

DV_{CC}: Power. Reference voltage for the control logic.

SGND: Ground. Signal ground for analog sections of the LTC1955. The Exposed Pad must be soldered to PCB ground.

PGND: Ground. Power ground for the charge pump. This pin should be connected directly to a low impedance ground plane.

CPO: Charge Pump. CPO is the output of the charge pump. When one or both of the smart cards requires power, the charge pump will charge CPO to either 3.7V or 5.35V depending on what smart card voltages are required. A low impedance 4.7µF X5R or X7R ceramic capacitor is required on CPO.

C^+, C^-: Charge Pump. Charge pump flying capacitor pins. A 1µF X5R or X7R ceramic capacitor should be connected from C^+ to C^-.

DATA: Input/Output. Microcontroller side data I/O pin. The DATA pin provides the bidirectional communication path to both smart cards. One, both or neither of the cards may be selected to communicate via the DATA pin. If several LTC1955s are connected in parallel, the DATA pin can be made high impedance by selecting neither card. The C4A and C8A synchronous card pins can be selected to connect to the DATA pin via the serial port (see Table 4).

R_{IN}: Input. The R_{IN} pin supplies the RST signal to both smart cards. It is level shifted and transmitted directly to the RST pin of a selected card socket. When a card is deselected, the RST A/RST B pin for that channel is latched at its current state.

SYNC: Input. The SYNC pin provides the clock input for synchronous smart cards. When a synchronous card is selected, its CLK pin follows SYNC directly. When a synchronous card is deselected, the CLK A/CLK B pin for that channel is latched at its current state.

ASYNC: Input. The ASYNC pin provides the clock input for asynchronous cards and should be connected to a free running clock. The clock signal to the smart card can be a ÷1, ÷2, ÷4 or ÷8 version of the signal on ASYNC. Asynchronous cards can also be placed in clock stop mode with the clock stopped either high or low.

D_{IN}: Input. Input for the serial port. Command data is shifted into D_{IN} synchronously with SCLK. D_{IN} can be connected directly to a microcontroller or the D_{OUT} pin of another LTC1955 for daisychained operation.

D_{OUT}: Output. Output for the serial port. Smart card status data is shifted out of D_{OUT} synchronously with SCLK. D_{OUT} can be connected directly to a microcontroller or the D_{IN} pin of another LTC1955 for daisychained operation.

PIN FUNCTIONS

SCLK: Input. The SCLK pin clocks the serial port. Each new data bit is received on the rising edge of SCLK. SCLK should be left high during idle times and should not be clocked when $\overline{LD}$ is low.

$\overline{LD}$: Input. The falling edge of this pin loads the current state of the shift register into the command register. Command changes to both smart card channels will be updated on the falling edge of $\overline{LD}$. The rising edge of $\overline{LD}$ latches status information from the smart card channels into the shift register for the next read/write cycle.

NC/$\overline{NO}$: Input. This pin controls the activation level of the PRES A/PRES B pins. When it is high (DV_{CC}), the PRES pins are active high. When it is low (GND), the PRES pins are active low. When a ground side N.O. switch is used, the NC/$\overline{NO}$ pin should be grounded. When a ground side N.C. switch is used, the NC/$\overline{NO}$ pin should be connected to DV_{CC}.

Note: If an N.C. switch is used, a small current (several microamperes) will flow through the switch whenever a smart card is not present. For ultralow power consumption in shutdown, an N.O. switch is optimum.

PRES A/PRES B: Card Socket. The PRES A/PRES B pins are used to detect the presence of the smart cards. They can be connected to either normally open or normally closed detection switches on the smart card acceptor's sockets. The NC/$\overline{NO}$ pin should be set appropriately. These pins have a pull-up current source on-chip so no external components are required.

C4A/C8A: Card Socket. These pins connect to the C4 and C8 pins of synchronous memory cards on smart card socket A. The signal for these pins is unidirectional and can only be sent to the card. Data for C4A and C8A is transmitted via the DATA pin and may be selected in place of I/OA via the serial port (see Table 4). When either C4A or C8A is selected, it will follow the DATA pin. When it is deselected, it will remain latched at its current state.

I/O A/I/O B: Card Socket. The I/O A/I/O B pins connect to the I/O pins of the respective smart card sockets. When a smart card is selected, its I/O pin connects to the DATA pin. When a smart card is deselected, its I/O A/I/O B pin returns to the idle state (H).

RST A/RST B: Card Socket. These pins should be connected to the RST pins of the respective smart card sockets. The RST A/RST B signals are derived from the R_{IN} pin. When a card is selected, its RST pin follows R_{IN}. When a card is deselected, the RST A/RST B pin for that channel holds the current value on R_{IN}.

CLK A/CLK B: Card Socket. The CLK A/CLK B pins should be connected to the CLK pins of the respective smart card sockets. The CLK A/CLK B signals can be derived from either the SYNC input or the ASYNC input depending on which type of card is being accessed. The card type is selected via the serial port (see Tables 1 and 3).

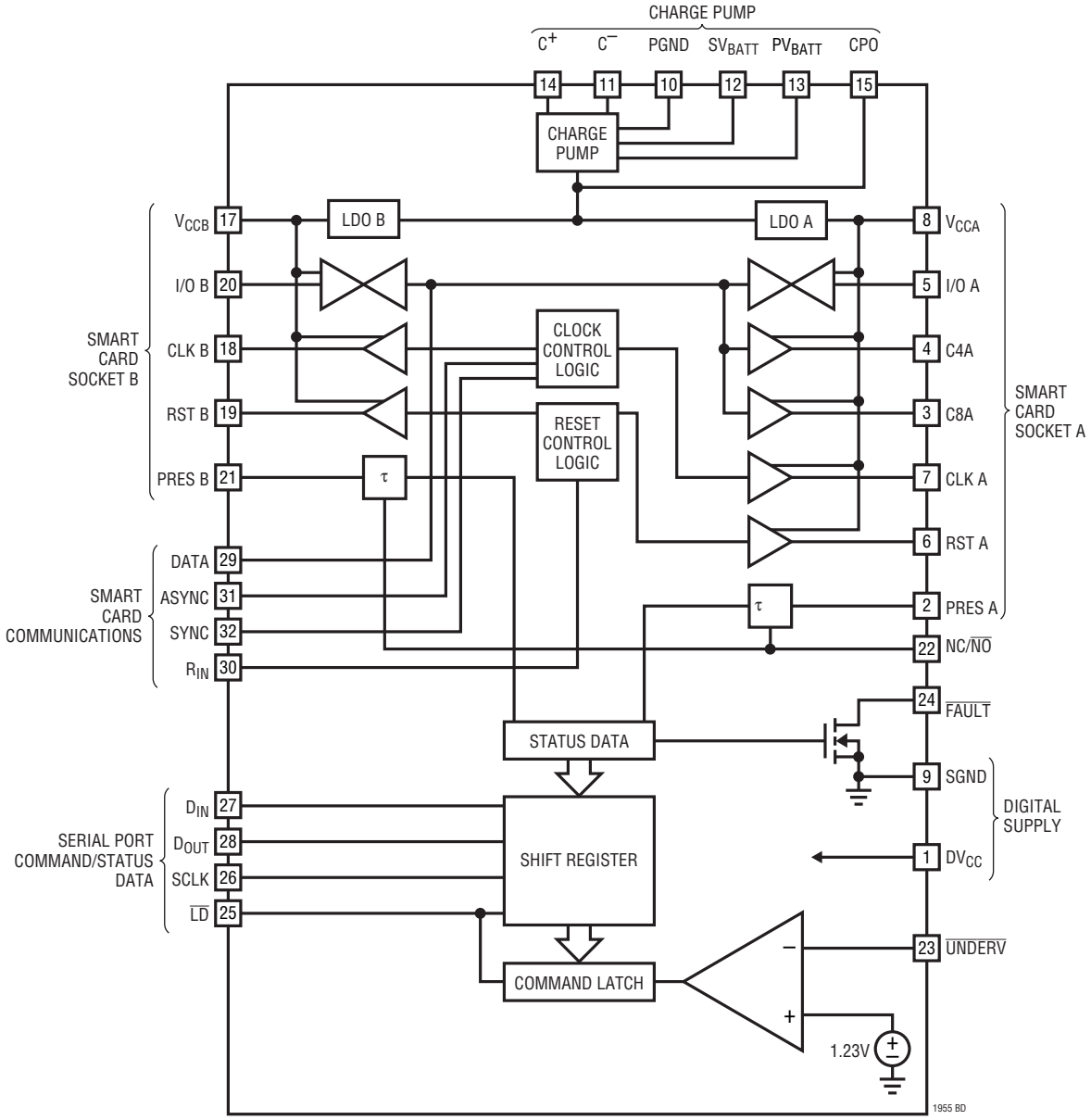
V_{CCA}, V_{CCB}: Card Socket. The V_{CCA}/V_{CCB} pins should be connected to the V_{CC} pins of the respective smart card sockets. The activation of a V_{CCA}/V_{CCB} pin is controlled by the serial port (see Tables 1 and 2) and can be set to 0V, 1.8V, 3V or 5V. The voltage levels of the two card sockets are controlled independently for maximum flexibility.

$\overline{FAULT}$: Output. The $\overline{FAULT}$ pin can be used as an interrupt to a microcontroller to indicate when a fault has occurred. It is an open-drain output, which is logically equivalent to $\overline{D4 + D5 + D12 + D13}$. (See Table 1)

$\overline{UNDERV}$: Input. The $\overline{UNDERV}$ pin provides security by supplying a precision undervoltage threshold for external supply monitoring. An external resistive voltage divider programs the desired undervoltage threshold. Once $\overline{UNDERV}$ falls below 1.23V, the LTC1955 automatically begins the deactivation sequence on any channel that is active.

If external supply monitoring is not required, the $\overline{UNDERV}$ pin should be connected to either SV_{BATT} or DV_{CC}.

BLOCK DIAGRAM



OPERATION

Serial Port

The microcontroller compatible serial port provides all of the command and control inputs for the LTC1955, as well as the status of the two smart cards. Data on the D_{IN} input is loaded on the rising edge of SCLK. D15 is loaded first and D0 last. At the same time, the command bits are being shifted into the D_{IN} input, the status bits are being shifted out of the D_{OUT} output. The status bits are presented to D_{OUT} on the rising edge of SCLK. Once all bits have been clocked into the shift register, the command data is loaded into the command latch by bringing $\overline{LD}$ low. At this time, the command latch is updated and the LTC1955 will begin to act on the new command set. The status data is latched into the shift register on the rising edge of $\overline{LD}$. SCLK should be low when $\overline{LD}$ is brought low and should be high when $\overline{LD}$ is brought high. This requires a 9th clock cycle per transaction. Figure 1 shows the recommended operation of the serial port.

Multiple LTC1955s may be daisychained together by connecting the D_{OUT} pin of one LTC1955 to the D_{IN} pin of another. Figure 6 shows an example of multiple LTC1955s daisychained together.

The maximum clock rate for the serial port is 10MHz.

The serial port controls the following parameters of each smart card socket:

- Selection/deselection of a smart card
- V_{CC} voltage level of each card (5V/3V/1.8V/0V)
- Clock mode of each card (synchronous or asynchronous)
- Operating mode of asynchronous cards (clock stop high, low, ÷1, ÷2, ÷4 or ÷8)
- Selection of the I/O, C4 or C8 pins for card socket A

The serial port provides the following status data:

- It indicates the presence or absence of the smart cards.
- It indicates the readiness of the smart card V_{CC} supplies. Communication with a smart card is disabled until its power supply voltage has reached the final value.
- It indicates fault status. In the event of an electrical or ATR fault, the fault is reported. For electrical faults, the LTC1955 will automatically deactivate the smart card.

Table 1 illustrates the command inputs and status outputs associated with each bit of the serial data word.

Three voltage options are available from the LTC1955: 5V, 3V and 1.8V. Bits D0, D1 (card B) and D8, D9 (card A) determine which voltage is selected. Setting both control bits of a channel to 0 deactivates that channel and sets the smart card supply voltage to 0V. If both channels are deactivated, the LTC1955 is in shutdown. Table 2 shows the operation of the supply control bits.

The CLK A/CLK B pins to the smart cards can be programmed for various modes. Both synchronous and asynchronous cards are supported. There are several options available with asynchronous cards. Table 3 shows how all clock options are obtained using bits D5–D7 (card B) and D13–D15 (card A). The default state of the LTC1955 on power up is synchronous mode.

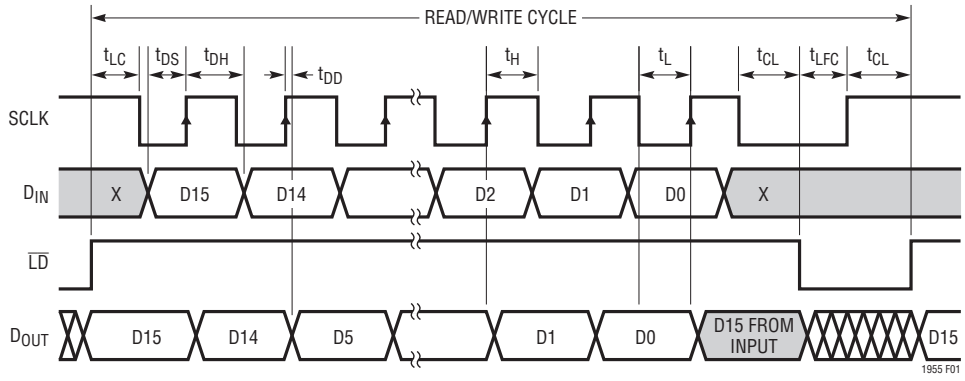


Figure 1. Serial Port Timing Diagram

OPERATION

Table 1. Serial Port Comand

	STATUS OUTPUT	BIT	COMMAND INPUT
CARD B	0	D0	V_{CCB} Options (See Table 2)
	0	D1	
	0	D2	Card B Select/Deselect
	0	D3	Data Pull-Up Defeat
	Card B Electrical Fault	D4	Reserved (Always Set to "0")
	Card B ATR Fault	D5	Card B Clock Options (See Table 3)
	Card B V_{CC} Ready	D6	
	Card B Present	D7	
CARD A	0	D8	V_{CCA} Options (See Table 2)
	0	D9	
	0	D10	Card A Select/Deselect
	0	D11	Card A Communications Options (See Table 4)
	Card A Electrical Fault	D12	
	Card A ATR Fault	D13	Card A Clock Options (See Table 3)
	Card A V_{CC} Ready	D14	
	Card A Present	D15	

Table 2. V_{CC} and Shutdown Options

D9 D1	D8 D0	STATUS (CARD A) STATUS (CARD B)
0	0	V_{CC} = 0V (Shutdown)
0	1	V_{CC} = 1.8V
1	0	V_{CC} = 3V
1	1	V_{CC} = 5V

Table 3. Clock Options

D7 D15	D6 D14	D5 D13	CLOCK MODE (CARD B) CLOCK MODE (CARD A)
0	0	0	Synchronous Mode
0	0	1	Unused
0	1	0	Asynchronous Stop Low
0	1	1	Asynchronous Stop High
1	0	0	Asynchronous ÷1
1	0	1	Asynchronous ÷2
1	1	0	Asynchronous ÷4
1	1	1	Asynchronous ÷8

To receive status data from the serial port, a read/write operation must be performed. When polling for the presence of a smart card on both channels, the input word should be set to $0000 since this is the shutdown command for the LTC1955. However, consider the example where some operation is already being performed on channel A. If, for example, the previous command was $BE00 ($V_{CCA}$ set to 3V, card selected, I/O A connected to DATA and CLK A set to ASYNC÷2), then the commands for this channel must be rewritten to the serial port each time. To poll for the presence of a card on channel B, or even the V_{CCA} ready status, then $BE00 should be rewritten on each new read/write cycle. Once a card is detected on channel B, the commands for channel B can be changed but the $BExx should continue to be rewritten for channel A.

Bidirectional Channels

The bidirectional channels are level shifted to the appropriate $V_{CCA/B}$ voltages at the I/O A/I/O B pins.

An NMOS pass transistor performs the level shifting. The gate of the NMOS transistor is biased such that the transistor is completely off when both sides have relinquished the channel. If one side of the channel asserts an L, then the transistor will convey the L to the other side. Note that current passes from the receiving side of the channel to the transmitting side. The low output voltage of the receiving side will be dependent upon the voltage at the transmitting side plus the I • R drop of the pass transistor.

When a card socket is selected, it becomes a candidate to drive data on the DATA pin, and likewise, receive data from the DATA pin. When a card socket is deselected, the voltage on its I/O A/I/O B pin will return to the idle state (H), and the DATA side of that channel will become high impedance. If both cards are deselected, the DATA pin will be high impedance.

Both cards may be deselected at the same time to allow communication with a second LTC1955.

Card channel A includes provision for unidirectional communication with the C4 and C8 pins of the smart card. The C4, C8 and I/O pins of card A are individually multiplexed to the DATA pin using bits D11 and D12, as shown in Table 4.

OPERATION

Table 4. Card A Communications Options

D12	D11	CARD A COMMUNICATION MODE
0	0	Nothing Selected
0	1	C4A Connected to DATA Pin
1	0	C8A Connected to DATA Pin
1	1	I/O A Connected to DATA Pin

Note that if a reset is initiated with both cards selected, then both may give an answer to reset and collide on the DATA line. No damage will occur but data could be lost or corrupted.

Dynamic Pull-Up Current Sources

The current sources on the bidirectional pins (DATA, I/O A/I/O B) are dynamically activated to achieve a fast rise time with a relatively small static current.* Once a bidirectional pin is relinquished, a small start-up current begins to charge the node. An edge rate detector determines if the pin is released by comparing its slew rate with an internal reference value. If a valid transition is detected, a large pull-up current enhances the edge rate on the node. The higher slew rate corroborates the decision to charge the node thereby affecting a dynamic form of hysteresis.

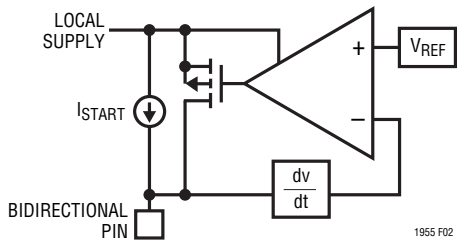


Figure 2. Dynamic Pull-Up Current Sources

Clock Channels

As described in the section Serial Port, the LTC1955 supports both synchronous and asynchronous smart cards. On start-up, or when bits D13-D15 for card A and bits D5-D7 for card B are set to 0s, the clock channel is in synchronous mode. The remaining modes are used for asynchronous cards.

In synchronous mode, the CLK A/CLK B pins follow the SYNC pin for a channel that is selected. If a channel is deselected (via the serial port), the CLK A/CLK B line for that channel is latched at its current value.

In asynchronous mode, the CLK A/CLK B pins follow either the ASYNC pin (÷1 mode) or a divided version of this pin. The CLK A/CLK B pins can also be stopped high or low. The available divider ratios include ÷2, ÷4 and ÷8. When switching between divider ratios, the internal selection circuitry ensures that no spikes or glitches appear on the CLK A/CLK B pins. Consequently, it may take up to 8 clock pulses for the clock frequency change command to take affect. Synchronization circuitry ensures that no glitches occur when entering or exiting one of the stop modes. For example, when entering stop low mode, the selection circuitry waits for the next falling edge of the respective CLK A/CLK B signal to make the change. Likewise, if stop high is selected, it will occur on the next rising edge.

Deselection of an asynchronous card does not affect its CLK A/CLK B pin. Its clock can be started, stopped or its divider ratio changed at any time.

To clean up the duty cycle of the incoming clock in asynchronous applications, any of the clock divider modes ÷2, ÷4 or ÷8 will yield a very nearly 50% duty cycle.

Additional synchronization circuitry prevents glitches from occurring when switching between synchronous mode and asynchronous mode. Because of this circuitry, two edges (a falling edge followed by a rising edge) are necessary at the CLK pin to switch modes from asynchronous to synchronous. For example, if clock stop mode is engaged, the clock channel will not change modes until clock stop mode is disengaged.

Any combination of cards, synchronous or asynchronous, can be used as both channels can be set to any of the clock modes or divider ratios independently.

Both SYNC and ASYNC inputs are independently level shifted to the appropriate voltage for the CLK A/CLK B pins (5V, 3V, 1.8V).

Reset Channels

When a card is selected, the reset channels provide a level shifted path from the R_{IN} pin to the RST A/RST B pins. When a card is deselected, its RST A/RST B pin is latched at the current value of R_{IN}.

* U.S. Patent No. 6,356,140

OPERATION

Smart Card Detection Circuits

The PRES A/PRES B pins are used to detect the presence of a smart card. An automatic debounce circuit waits until a smart card has been present for a continuous period of typically 35ms. Once a valid card indication exists, the status bit for that channel is updated and may be polled by cycling data through the serial port. The D_{OUT} pin (equivalent to D15) of the serial port can be used to indicate the presence of a card on channel A in real time if $\overline{LD}$ is held low.

The PRES A/PRES B pins have built-in pull-up current sources, so no external components are required for switch detection. The pull-up current sources are designed to have a small current when the pin voltage is below approximately 1V, but somewhat higher current when the pin voltage reaches 1V. This helps maintain low power dissipation when a card is present and yet fast response time to a card removal.

The PRES A/PRES B pins can be configured to respond to either normally open or normally closed switches via the NC/$\overline{NO}$ pin.

Activation/Deactivation

For maximum flexibility, the activation sequencing of the smart card is left to the application programmer. Upon activation, to comply with relevant smart card standards, none of the smart card signal pins will be allowed to go high before the smart card supply voltage (V_{CCA}/V_{CCB}) has reached its final value. Deactivation can be achieved either manually or automatically. An electrical fault condition will trigger the automatic deactivation.

Manual deactivation may be performed under software control by setting the smart card pins to 0V in the desired sequence via the control pins (SYNC, ASYNC, R_{IN}, DATA and the serial port). For most applications, this will be cumbersome and the built-in deactivation will be used instead.

Automatic Deactivation

The built-in deactivation sequence can be executed via the serial port simply by setting the appropriate control bits (D0 and D1 or D8 and D9) to 0. The deactivation sequence is outlined below.

1. The RST A/RST B pin for that channel is immediately brought low.
2. The deactivation of the CLK A/CLK B pins depends upon which type of card is used:

   If the smart card was set to asynchronous mode, then the CLK A/CLK B pin will be latched low on its next falling edge. If no falling edges occur within 5µs (min), then the CLK A/CLK B line is forced low.

   If the smart card was set to synchronous mode, then the CLK A/CLK B pin is immediately latched at its current value (either high or low) and then forced low after a duration of 5µs (min). During the 5µs timeout period, changes on SYNC will be ignored.
3. The I/O A/I/O B, C4A and C8A pins for that channel are brought low.
4. The V_{CCA}/V_{CCB} pin is brought low.

If an error occurs on one smart card, operation of the other card is unaffected.

Electrical Fault Detection

Several types of faults are detected by the LTC1955. They include V_{CCA}/V_{CCB} undervoltage, V_{CCA}/V_{CCB} overcurrent, CLK A/CLK B, RST A/RST B, C8A, C4A short-circuit, card removal during a transaction, failed answer to reset (ATR), supply undervoltage or $\overline{UNDERV}$ and chip overtemperature. To prevent false errors from plaguing the microcontroller, the electrical faults are acted upon only after a 5µs (min) timeout period. Card removal during transaction faults initiate the deactivation sequence immediately.

OPERATION

V_{CCA}/V_{CCB} undervoltage faults are determined by comparing the actual output voltage with the internal reference voltage. If the output is more than ~5% below its set point for the entire timeout period, the fault is reported and the deactivation sequence is initiated.

V_{CCA}/V_{CCB} overcurrent faults are detected by comparing the output current of the LDOs with an internal reference level. If the current of an LDO is more than 100mA (typ) for the entire timeout period, the fault is reported and the deactivation sequence is initiated.

CLK A/CLK B and RST A/RST B faults are detected by comparing the outputs of these pins with their expected signals. If the signal on a pin is incorrect for the entire timeout period, the fault is reported and the deactivation sequence is initiated.

The clock channels are a special case. Since they can have a free running clock, the error indication is accumulated over a longer period of time without being cleared. Even though the clock may be running, an error will still be detected.

An overtemperature fault is detected by sensing the junction temperature of the IC. If the junction temperature exceeds approximately 150°C for the entire timeout period, the fault is reported by setting both fault bits (D4 and D12) and the deactivation sequence is initiated.

A card removal fault is determined as soon as the PRES A/PRES B pin is high (for NC/$\overline{NO}$ = 0). Once this occurs, the fault is reported and the deactivation sequence is initiated.

If no card is present, and the application software attempts to power-up a card socket, an automatic fault will result on that channel.

Short-circuits on the I/O A/I/O B lines will not be detected by the fault detection hardware; however, a short-circuit from these lines to their respective V_{CCA}/V_{CCB} pins will be compliant with the maximum current limits set by applicable standards (<15mA).

An electrical fault can be cleared on either channel by setting the voltage of that channel to 0V. Set D0 and D1 to 00 to clear channel B and set D8 and D9 to 00 to clear channel A. It is not necessary to set all four bits to zeros.

Answer to Reset (ATR) Fault Detection

Answer to reset faults are detected by an internal counter that is started once the RST A/B line goes high. If the DATA pin remains high for 40,000 clock cycles, the ATR fault bit for a given channel is set in the serial port's status register (see Table 1) and the $\overline{FAULT}$ pin is brought low.

An ATR fault cannot occur if the clock mode of a channel is set to synchronous. ATR faults will only occur for asynchronous smart cards.

ATR faults are cleared by bringing the RST A/B pin low for the faulted channel. This will also clear the $\overline{FAULT}$ pin to the Hi-Z state (assuming no other errors are causing $\overline{FAULT}$ to be low).

An ATR fault will not automatically deactivate a card channel. It is the application programmer's responsibility to check the status register for ATR faults and deactivate the smart card channel in accordance with smart card standards. Generally, the application has 50ms (EMV 2.1.3.1, 2.1.3.2) from the 40,000th clock pulse to deactivate the card. Once the LTC1955 receives the deactivation command, it will shut down a card channel in less than 250µs.

Using the $\overline{FAULT}$ Pin

The $\overline{FAULT}$ pin can be used as an interrupt to a microcontroller. It is an open-drain output and generally requires a pull-up resistor. The $\overline{FAULT}$ pin will go low when either an electrical fault, or an answer to reset fault, occurs on either channel. Thus, there are four possible faults that can cause it to indicate a problem. The serial port's status register must be polled to find out what type of fault occurred and on which channel. The $\overline{FAULT}$ pin is logically equivalent to D4 + D5 + D12 + D13 (see Table 1).

APPLICATIONS INFORMATION

10kV ESD Protection

All smart card pins (CLKA/CLKB, RSTA/RSTB, I/OA/I/OB, C4A, C8A and V_{CCA}/V_{CCB}) can withstand over 10kV of human body model ESD in-situ. In order to ensure proper ESD protection, careful board layout is required. The PGND and SGND pins should be tied directly to a ground plane. The V_{CCA}/V_{CCB} capacitors should be located very close to the V_{CCA}/V_{CCB} pins and tied immediately to the ground plane.

Capacitor Selection

Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitor since its voltage can reverse upon start-up of the LTC1955. Low ESR ceramic capacitors should always be used for the flying capacitor.

A total of six capacitors are required to operate the LTC1955. An input bypass capacitor is required at PV_{BATT}, SV_{BATT} and DV_{CC}. Output bypass capacitors are required on each of the smart card V_{CCA}/V_{CCB} pins. A charge pump flying capacitor is required from C^+ to C^- and a charge storage capacitor is required on the charge pump out pin CPO.

To prevent excessive noise spikes due to charge pump operation, low ESR (equivalent series resistance) multilayer ceramic capacitors are strongly recommended.

There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R/X5R ceramic capacitors have excellent voltage and temperature stability but relatively low packing density. Y5V ceramic capacitors have apparently higher packing density but poor performance over their rated voltage or temperature ranges. Under certain voltage and temperature conditions, Y5V and X7R/X5R ceramic capacitors can be compared directly by case size rather than specified value for a desired minimum capacitance.

Placement of the capacitors is critical for correct operation of the LTC1955. Because the charge pump generates large current steps, all of the capacitors should be placed as close to the LTC1955 as possible. The low impedance nature of multilayer ceramic chip capacitors will minimize voltage spikes but only if the power path is kept very short (i.e., minimum inductance). The PV_{BATT}/SV_{BATT} nodes should be especially well bypassed. The capacitor for this node should be directly adjacent to the QFN package. The CPO and flying capacitors should be very close as well. The LTC1955 can tolerate more distance between the LDO capacitors and the $V_{CCA/B}$ pins.

Figure 3 shows an example of a tight printed circuit board using single-layer copper. For best performance, a multilayer board can be used and should employ a solid ground plane on at least one layer.

The following capacitors are recommended for use with the LTC1955.

	TYPE	VALUE	CASE SIZE	MURATA P/N
C_{IN} CPO	X5R	4.7µF	0805	GRM40-034 X5R 475K 6.3
C_{FLY} $V_{CCA/B}$	X5R	1µF	0603	GRM39 X5R 105K 6.3
CDV_{CC}	X5R	0.1µF	0402	GRM36 X5R 104K 10

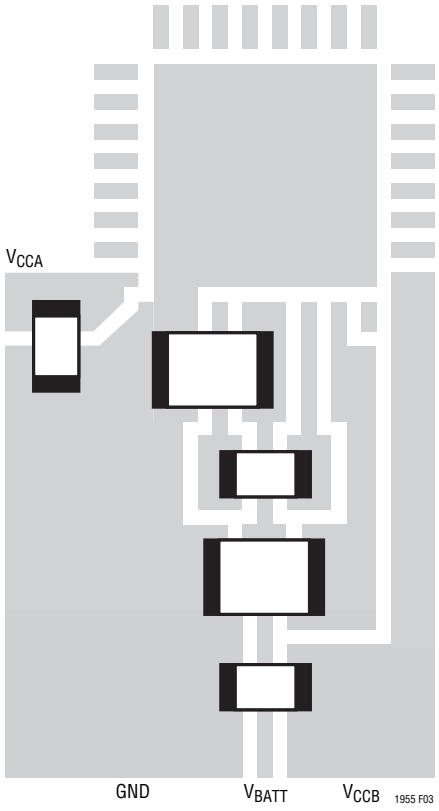


Figure 3. Optimum Single-Layer PCB Layout

APPLICATIONS INFORMATION

Interfacing to a Microcontroller

The serial port of the LTC1955 can be connected directly to a 68HC11 style microcontroller's serial port. The microcontroller should be configured as the master device and its clock's idle state should be set to high (MSTR = 1, CPOL = 1 and CPHA = 0 for the MC68HC11 family). Figure 4 shows the recommended configuration and direction of data flow. Note that an additional I/O line is necessary for $\overline{LD}$ to load the data once it has shifted around the loop. Command data is latched into the command register on the falling edge of the $\overline{LD}$ signal. The LTC1955 will begin to act on new command data as soon as $\overline{LD}$ goes low. Any general purpose microcontroller I/O line can be configured to control the $\overline{LD}$ pin.

The status of the LTC1955 is returned over the serial port. Status data is latched into the shift register on the rising edge of the $\overline{LD}$ pin. Whenever the system is waiting for status data from the LTC1955, its $\overline{LD}$ pin should be held low.

Daisychained Operation

For applications requiring more than two card sockets, the serial port of the LTC1955 is designed to be easily daisychained. The D_{OUT} pin of one LTC1955 can be connected directly to the D_{IN} pin of another LTC1955. Rather than sending two 8-bit bytes before asserting $\overline{LD}$, the microcontroller should send two 8-bit bytes per device. $\overline{LD}$ should only be asserted after all devices have been updated. Figure 6 shows three LTC1955s cascaded in daisychain fashion. In this case, the microcontroller would write six 8-bit bytes before asserting the $\overline{LD}$ pin. Alternatively, if two serial ports are available on the microcontroller, then two LTC1955s can be controlled independently.

If the DATA lines of two or more LTC1955s are connected together, the static pull-up current will be the sum of the devices. The static current can be brought back to the level of a single LTC1955 by setting bit D3 on all but one of the LTC1955s to 1 (see Table 1). Bit D3 disables the pull-up current source on the DATA pin. This will help prevent V_{OL} problems in multiple LTC1955 applications when driving the DATA or I/O pins low.

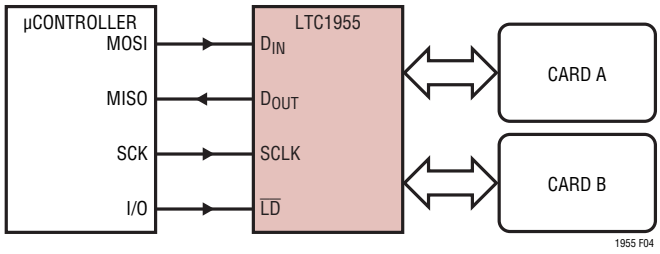


Figure 4. Microcontroller Interface

APPLICATIONS INFORMATION

Using S.A.M. Cards

For applications using one or more installed S.A.M. cards, the PRES A/PRES B pins for those sockets must be grounded before operation of the card can occur (assuming NC/$\overline{NO}$ is grounded). The PRES A/PRES B pull-up current is designed for very low consumption, but ultralow current can be achieved in shutdown by using a microcontroller output to pull down on the PRES A/PRES B pins only when communication is necessary. The fault detection circuitry will not allow a card socket to be operated unless a card is detected.

Asynchronous Channel A Card Detection

Since the shift register is transparent when $\overline{LD}$ is held low, D_{OUT} is the same as D15. Recall from Table 1 that D15 indicates the status of the card detection channel for channel A. Thus, it is not necessary to perform an entire read/write operation to determine the card detection status of channel A. With $\overline{LD}$ low, D_{OUT} can be used to generate a real time card detection interrupt. This could be useful for one S.A.M. card, one smart card application.

Inter Card Communication

Communication is possible directly from one card socket to the other when both cards are selected at the same time. This can be achieved by the following sequence of actions.

1. Start with both cards off and deselected
2. Activate the supply of the slave card
3. Select the slave card only
4. Initiate a reset on the slave card
5. Deselect the slave card
6. Activate the supply of the master card
7. Select the master card only
8. Initiate a reset on the master card
9. Select both cards

Using the $\overline{UNDERV}$ Pin

The $\overline{UNDERV}$ pin can be used to add protection against a supply undervoltage fault. By using two external programming resistors, the undervoltage detection can be set to an arbitrary level (Figure 7). To ensure that the smart cards are properly shut down, there must be sufficient energy available in the input bypass capacitor to run one or both smart cards until the deactivation cycle begins. It can take approximately 30µs from the detection of a fault until the deactivation sequence begins. It is desirable to maintain the V_{BATT} supply at 2.7V or greater during this period.

Consider the following (worst-case) example:

1. The $\overline{UNDERV}$ pin is programmed to trip below 3.1V.
2. It is possible to have both cards activated at 5V and drawing 60mA.

Since the output voltage is programmed to 5V, the charge pump will be acting as a voltage doubler. With two cards drawing 60mA each, the input current will be 2 • (60mA + 60mA), or about 240mA. Allowing the V_{BATT} supply to droop from 3.1V to 2.7V during the 30µs timeout period, the input capacitance would need to be at least:

240mA / [(3.1V – 2.7V) / 30µs] or 18µF.

Thermal Management

To minimize power dissipation, the LTC1955 will actively decide whether to step up or down depending on the required output voltages and available input voltage. However, for optimum efficiency, the LTC1955 should be powered from a 3.3V supply.

If the input voltage is above 3.6V, and both cards are drawing maximum current, there can be substantial power dissipation in the LTC1955. If the junction temperature increases above approximately 150°C, the thermal shutdown circuitry will automatically deactivate both channels. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended.

Zero Shutdown Current

Although the LTC1955 is designed to have very low shutdown current, it can still draw over a microampere on both

APPLICATIONS INFORMATION

DV_{CC} and V_{BATT} when in shutdown. For applications that require virtually zero shutdown current, the DV_{CC} pin can be grounded. This will reduce the V_{BATT} current to well under a single microampere. Internal logic ensures that the LTC1955 is in shutdown when DV_{CC} is grounded. Note, however, that all of the logic signals that are referenced to DV_{CC} (D_{IN}, SCLK, $\overline{LD}$, DATA, R_{IN}, SYNC, ASYNC and NC/$\overline{NO}$) will have to be at 0V as well, to prevent ESD diodes to DV_{CC} from being forward-biased.

Operation at Higher Supplies

If a 5.5V to 6V supply voltage is available, it is possible to achieve some power savings by bypassing the charge pump. The higher supply can be connected directly to the CPO pin. As long as the voltage on CPO is higher than that at which it ordinarily regulates (5.35V or 3.7V depending on voltage selections), the charge pump's oscillator will not run. This configuration can give considerable power savings since the charge pump is not being used.

A voltage source is still needed on both DV_{CC} and SV_{BATT}/PV_{BATT} in this configuration. Recall that DV_{CC} sets the logic reference level for all the control and smart card communication pins. The voltage on SV_{BATT}/PV_{BATT} can be any convenient level that meets the parameters in the Electrical Characteristics table.

The 5.5V to 6V supply can be left permanently connected to CPO, but there will be approximately 5µA of current flow into CPO when the LTC1955 is in shutdown.

Charge Pump Strength

Under low V_{BATT} conditions, the amount of current available to the smart cards is limited by the charge pump.

Figure 5 shows how the LTC1955 can be modeled as a Thevenin equivalent circuit to determine the amount of current available given the effective input voltage, $2V_{BATT}$ and the effective open-loop output resistance, R_{OLCP}.

From Figure 5, the available current is given by:

$$I_{CCA} + I_{CCB} \leq \frac{2V_{BATT} - V_{CPO}}{R_{OLCP}}$$

R_{OLCP} is dependent on a number of factors including the switching term, $1/(f_{OSC} \bullet C_{FLY})$, internal switch resistances and the nonoverlap period of the switching circuit. However, for a given R_{OLCP}, the minimum CPO voltage can be determined from the following expression:

$$V_{CPO} \geq 2V_{BATT} - (I_{CCA} + I_{CCB})R_{OLCP}$$

The LDOs have been designed to meet all applicable smart card standards for V_{CC} with V_{CPO} as low as 5.13V. Given this information, trade-offs can be made by the user with regard to total consumption (I_{CCA} + I_{CCB}) and minimum supply voltage.

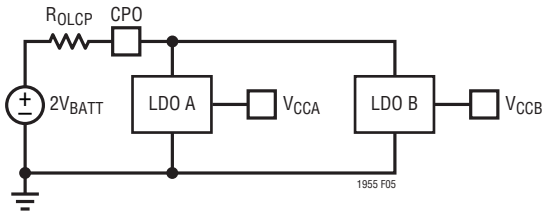


Figure 5. Equivalent Open-Loop Circuit

Changing the Smart Card Supply Voltage

Although the LTC1955 control system will allow the smart card voltage to be changed from one value to the next without an interim power-down, this is not recommended. When changing from a higher voltage to a lower voltage there will generally not be a problem; however, changing from a lower voltage to a higher voltage will result in both an undervoltage condition and an overcurrent condition on that channel. The likely result is that the channel will automatically deactivate. Applicable smart card standards specify that the smart card supply be powered to zero before applying a new voltage.

Compliance Testing

Inductance due to long leads on type approval equipment can cause ringing and overshoot that leads to testing problems. Small amounts of capacitance and damping resistors can be included in the application without compromising the normal electrical performance of the LTC1955 or smart card system. Generally, a 100Ω resistor and a 20pF capacitor will accomplish this, as shown in Figure 8.

APPLICATIONS INFORMATION

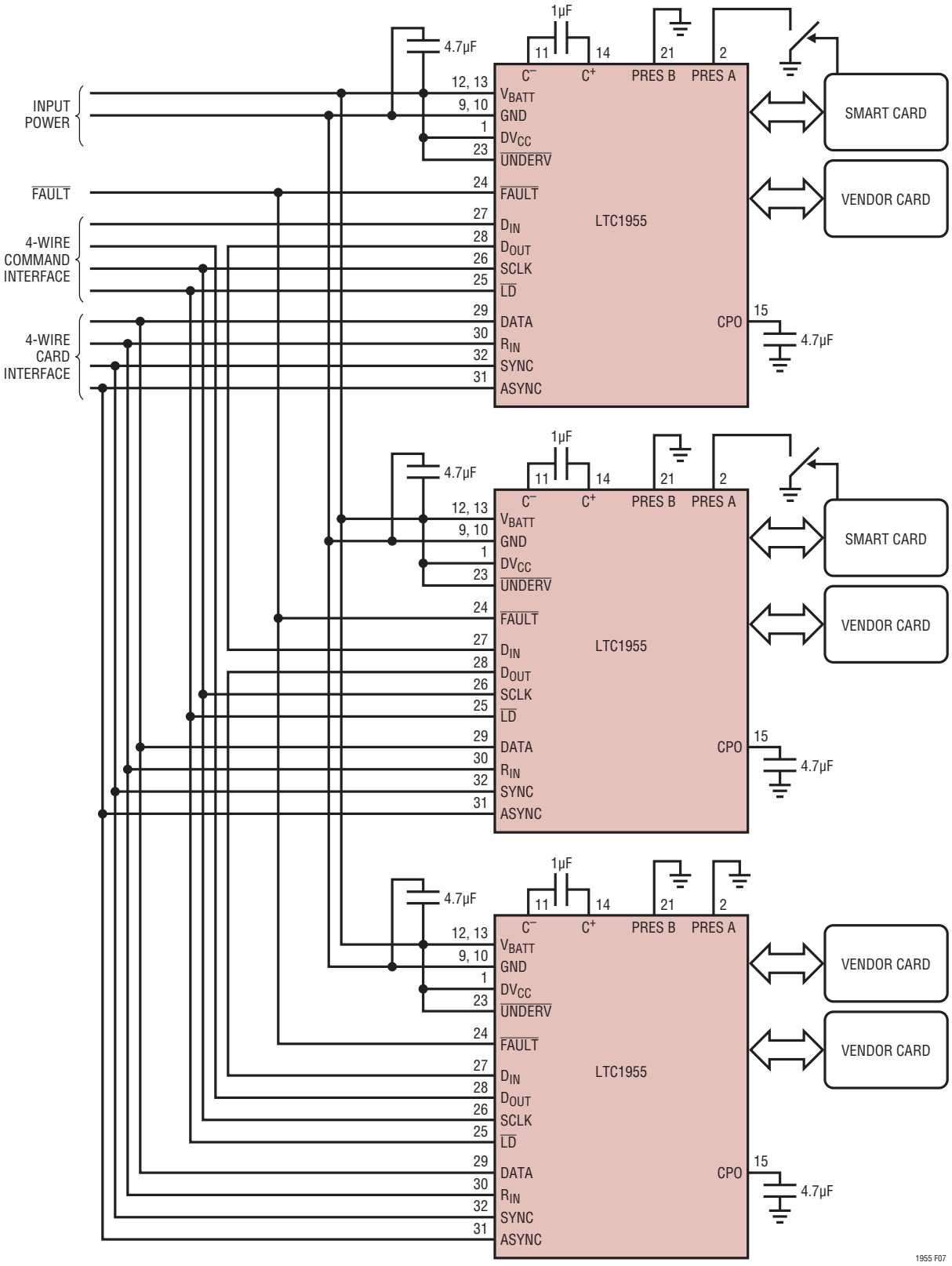


Figure 6. Multiple LTC1955s Daisychained Together

APPLICATIONS INFORMATION

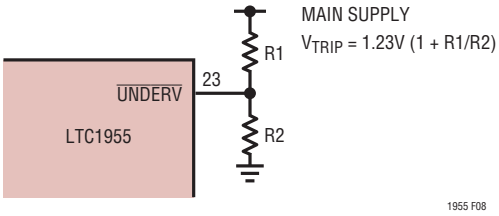


Figure 7. Setting the Undervoltage Trip Point

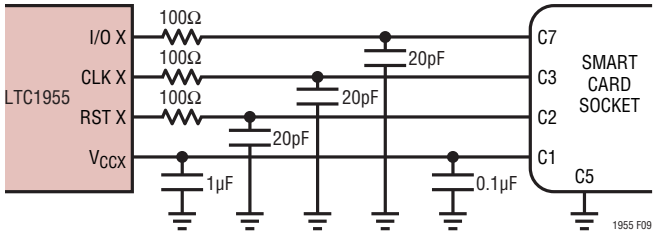
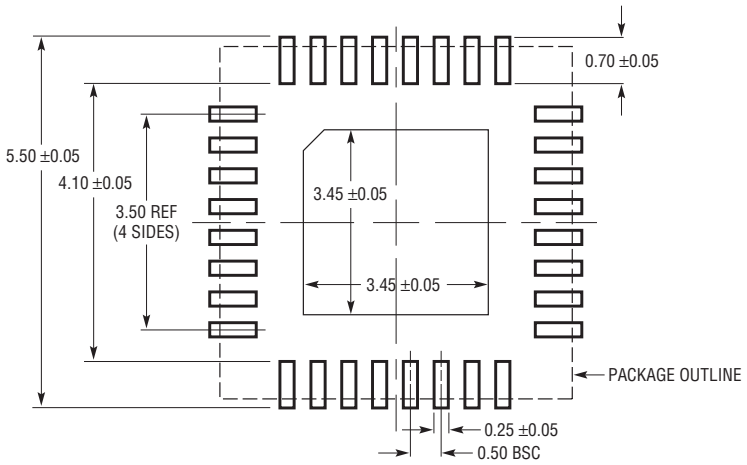


Figure 8. Additional Components for Improved Compliance Testing

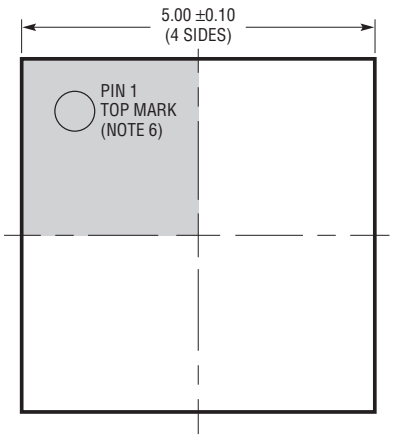
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

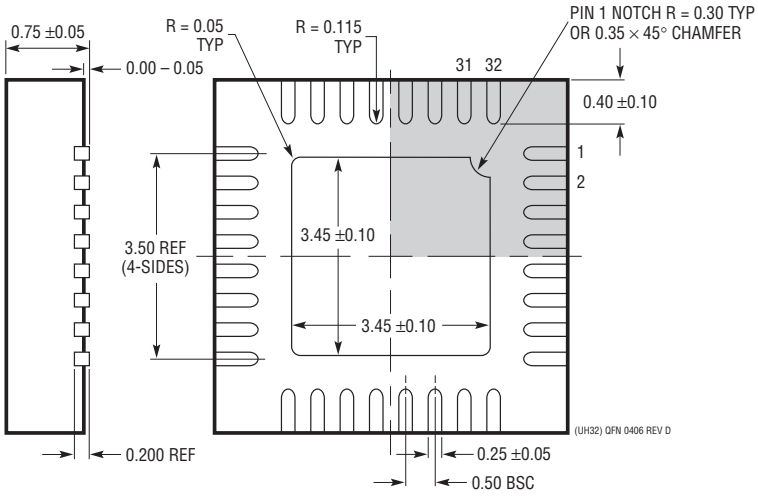
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/13	Remove t_{LW} spec from Serial Port Timing	4
		Revised Serial Port Timing section and diagram	9
D	2/14	Added t_{LFC} parameter to Serial Port Timing electrical parameters.	4
		Modified Figure 1.	9