1Msps/3Msps, 12-Bit Serial Sampling ADCs in TSOT

FEATURES

- **12-Bit Resolution**
- **1Msps/3Msps Sampling Rates**
- **Low Noise: 73dB SNR**
- **Low Power Dissipation: 6mW**
- Single Supply 2.35V to 3.6V Operation
- No Data Latency
- Sleep Mode with 0.1µA Typical Supply Current
- Dedicated External Reference (TSOT23-8)
- 1V to 3.6V Digital Output Supply (TSOT23-8)
- SPI/MICROWIRE Compatible Serial I/O
- Guaranteed Operation from –40°C to 125°C
- 6- and 8-Lead TSOT-23 Packages

APPLICATIONS

- Communication Systems
- Data Acquisition Systems
- Handheld Terminal Interface
- Medical Imaging
- Uninterrupted Power Supplies
- Battery-Operated Systems
- Automotive

DESCRIPTION

The LTC®2365/LTC2366 are 1Msps/3Msps, 12-bit, sampling A/D converters that draw only 2mA and 2.6mA, respectively, from a single 3V supply. These high performance devices include a high dynamic range sample-and-hold and a high speed serial interface. The full-scale input is 0V to V_{DD} or V_{REF}. Outstanding AC performance includes 72dB SINAD and –80dB THD at sample rates of 3Msps. The serial interface provides flexible power management and allows maximum power efficiency at low throughput rates. These devices are available in tiny 6- and 8-lead TSOT-23 packages.

The serial interface, tiny TSOT-23 package and extremely high sample rate-to-power ratio make the LTC2365/LTC2366 ideal for compact, low power, high speed systems.

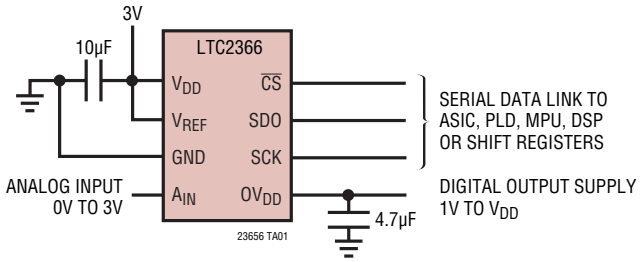
The high impedance single-ended analog input and the ability to operate with reduced spans (down to 1.4V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

TYPICAL APPLICATION

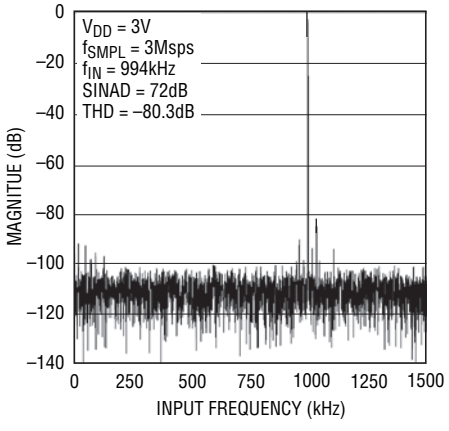
12-Bit TSOT23-6/-8 ADC Family

DATA OUTPUT RATE	3Msps	1Msps	500ksps	250ksps	100ksps
Part Number	LTC2366	LTC2365	LTC2362	LTC2361	LTC2360

Single 3V Supply, 3Msps, 12-Bit Sampling ADC



1MHz Sine Wave 8192 FFT Plot

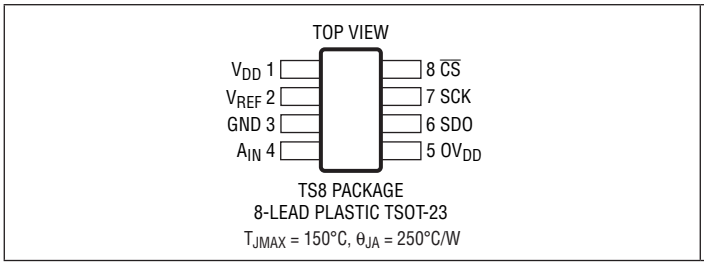


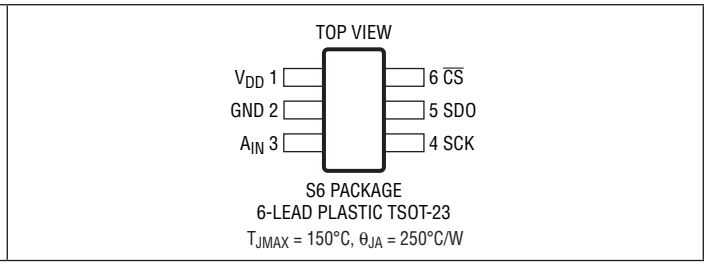
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 4.0V
Supply Voltage (OV_{DD}) ..... Min (V_{DD} + 0.3V, 4.0V)
V_{REF} and Analog Input Voltage
(Note 3) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage ..... –0.3V to (V_{DD} + 0.3V)
Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 100mW
Operating Temperature Range
LTC2365C/LTC2366C ..... 0°C to 70°C
LTC2365I/LTC2366I ..... –40°C to 85°C
LTC2365H/LTC2366H (Note 13) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION





ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2366CTS8#TRMPBF	LTC2366CTS8#TRPBF	LTCYZ	8-lead Plastic TSOT-23	0°C to 70°C
LTC2366ITS8#TRMPBF	LTC2366ITS8#TRPBF	LTCYZ	8-lead Plastic TSOT-23	–40°C to 85°C
LTC2366HTS8#TRMPBF	LTC2366HTS8#TRPBF	LTCYZ	8-lead Plastic TSOT-23	–40°C to 125°C
LTC2366CS6#TRMPBF	LTC2366CS6#TRPBF	LTCXK	6-lead Plastic TSOT-23	0°C to 70°C
LTC2366IS6#TRMPBF	LTC2366IS6#TRPBF	LTCXK	6-lead Plastic TSOT-23	–40°C to 85°C
LTC2366HS6#TRMPBF	LTC2366HS6#TRPBF	LTCXK	6-lead Plastic TSOT-23	–40°C to 125°C
LTC2365CTS8#TRMPBF	LTC2365CTS8#TRPBF	LTDCB	8-lead Plastic TSOT-23	0°C to 70°C
LTC2365ITS8#TRMPBF	LTC2365ITS8#TRPBF	LTDCB	8-lead Plastic TSOT-23	–40°C to 85°C
LTC2365HTS8#TRMPBF	LTC2365HTS8#TRPBF	LTDCB	8-lead Plastic TSOT-23	–40°C to 125°C
LTC2365CS6#TRMPBF	LTC2365CS6#TRPBF	LTDCC	6-lead Plastic TSOT-23	0°C to 70°C
LTC2365IS6#TRMPBF	LTC2365IS6#TRPBF	LTDCC	6-lead Plastic TSOT-23	–40°C to 85°C
LTC2365HS6#TRMPBF	LTC2365HS6#TRPBF	LTDCC	6-lead Plastic TSOT-23	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		LTC2365 MIN	LTC2365 TYP	LTC2365 MAX	LTC2366 MIN	LTC2366 TYP	LTC2366 MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 5, 6)	●		±0.25	±1		±0.25	±1	LSB
Differential Linearity Error	(Note 6)	●		±0.25	±1		±0.25	±1	LSB
Transition Noise	(Note 7)			0.34			0.34		LSB_{RMS}
Offset Error	(Note 6)	●		2	±3.5		2	±3.5	LSB
Gain Error	(Note 6)	●		1	±2		1	±2	LSB
Total Unadjusted Error	S6 Package (Note 6) TS8 Package (Note 6)	● ●		2 3	±3.5 ±4.5		2 3	±3.5 ±4.5	LSB LSB

ANALOG INPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Voltage	S6 Package TS8 Package	● ●	–0.05 –0.05		V_{DD} + 0.05 V_{REF} + 0.05	V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			20 4		pF pF
V_{REF}	Reference Input Voltage	TS8 Package	●	1.4		V_{DD} + 0.05	V
I_{REF}	Reference Input Leakage Current	TS8 Package	●			±1	µA
C_{REF}	Reference Input Capacitance	TS8 Package			4		pF
t_{AP}	Sample-and-Hold Aperture Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				0.3		ns

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC2365 MIN	LTC2365 TYP	LTC2365 MAX	LTC2366 MIN	LTC2366 TYP	LTC2366 MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 1MHz	●	68	72		68	71		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 1MHz	●	70	73		69	72		dB
THD	Total Harmonic Distortion	f_{IN} = 1MHz	●		–86	–72		–80	–72	dB
SFDR	Spurious Free Dynamic Range	f_{IN} = 1MHz			87			82		
IMD	Intermodulation Distortion	f_{IN1} = 0.97MHz, f_{IN2} = 1MHz for LTC2366 f_{IN1} = 97kHz, f_{IN2} = 100kHz for LTC2365			 –76			–71.5		dB
	Full-Power Bandwidth	At 3dB At 0.1dB			30 5			50 8		MHz MHz
	Full-Linear Bandwidth	SINAD ≥ 68dB			2			2.5		MHz

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	2.7V < V_{DD} ≤ 3.6V 2.35V ≤ V_{DD} ≤ 2.7V	● ●	2 1.7			V V
V_{IL}	Low Level Input Voltage	2.7V < V_{DD} ≤ 3.6V 2.35V ≤ V_{DD} ≤ 2.7V	● ●			0.8 0.7	V V
I_{IH}	High Level Input Current	V_{IN} = V_{DD}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
C_{IN}	Digital Input Capacitance				2		pF
V_{OH}	High Level Output Voltage	V_{DD} = 2.35V to 3.6V, I_{SOURCE} = 200µA	●	V_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	V_{DD} = 2.35V to 3.6V, I_{SINK} = 200µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = V_{DD}	●			±3	µA
C_{OZ}	Hi-Z Output Capacitance	$\overline{CS}$ = V_{DD}			4		pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	2.35	3.0	3.6	V
O_{VDD}	Digital Output Supply Voltage		●	1		3.6	V
I_{DD}	Supply Current, Static Mode Operational Mode, LTC2366 Operational Mode, LTC2365 Sleep Mode Sleep Mode	$\overline{CS}$ = 0V, SCK = 0V or V_{DD} f_{SMPL} = 3Msps f_{SMPL} = 1Msps –40°C to 85°C 85°C to 125°C	 ● ● ● ●		1 2.6 2 0.1	 4 3.5 2 5	mA mA mA µA µA
P_D	Power Dissipation, Static Mode Operational Mode, LTC2366 Operational Mode, LTC2365 Sleep Mode Sleep Mode	$\overline{CS}$ = 0V, SCK = 0V or V_{DD} f_{SMPL} = 3Msps f_{SMPL} = 1Msps –40°C to 85°C 85°C to 125°C	 ● ● ● ●		 7.8 6 0.3	3.6 14.4 12.6 7.2 18	mW mW mW µW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LTC2365 MIN	LTC2365 TYP	LTC2365 MAX	LTC2366 MIN	LTC2366 TYP	LTC2366 MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	(Notes 8, 9)	●	1			3			MHz
f_{SCK}	Shift Clock Frequency	(Notes 8, 9, 10)	●	0.5		16	0.5		48	MHz
t_{SCK}	Shift Clock Period		●	62.5		2000	20.8		2000	ns
$t_{THROUGHPUT}$	Minimum Throughput Time, $t_{ACQ} + t_{CONV}$		●			1000			333	ns
t_{ACQ}	Acquisition Time		●	181.5			56			ns
t_{CONV}	Conversion Time		●	818.5			277			ns
t_{QUIET}	SDO Hi-Z State to $\overline{CS}\downarrow$	(Notes 8, 9)	●	4			4			ns
t_1	Minimum Positive or Negative $\overline{CS}$ Pulse Width	(Notes 8)	●	4			4			ns
t_2	SCK↓ Setup Time After $\overline{CS}\downarrow$	(Notes 8)	●	6		2000	6		2000	ns
t_3	SDO Enabled Time After $\overline{CS}\downarrow$	(Notes 9, 11, 12)	●			4			4	ns
t_4	SDO Data Valid Access Time After SCK↓	(Notes 8, 9, 11)	●			15			15	ns
t_5	SCK LOW Time		●	40%			40%			t_{SCK}
t_6	SCK HIGH Time		●	40%			40%			t_{SCK}
t_7	SDO Data Valid Hold Time After SCK↓	(Notes 8, 9, 11)	●	5			5			ns
t_8	SDO into Hi-Z State Time After SCK↓	(Notes 9, 12)	●	5		30	5		14	ns
t_9	SDO into Hi-Z State Time After $\overline{CS}\uparrow$	(Notes 9, 12)	●			4.2			4.2	ns
$t_{POWER-UP}$	Power-Up Time from Sleep Mode	See Sleep Mode section	●			1000			333	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: When this pin, A_{IN}, is taken below GND or above V_{DD}, it will be clamped by internal diodes. These products can handle input currents greater than 100mA below GND or above V_{DD} without latchup.

Note 4: $V_{DD} = OV_{DD} = V_{REF}$ = 2.35V to 3.6V, $f_{SMPL} = f_{SMPL(MAX)}$ and $f_{SCK} = f_{SCK(MAX)}$ unless otherwise specified.

Note 5: Integral linearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Linearity, offset and gain specifications apply for a single-ended A_{IN} input with respect to GND.

Note 7: Typical RMS noise at code transitions.

Note 8: Guaranteed by characterization. All input signals are specified with $t_r = t_f$ = 2ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6V.

Note 9: All timing specifications given are with a 10pF capacitance load. With a capacitance load greater than this value, a digital buffer or latch must be used.

Note 10: Minimum f_{SCK} at which specifications are guaranteed.

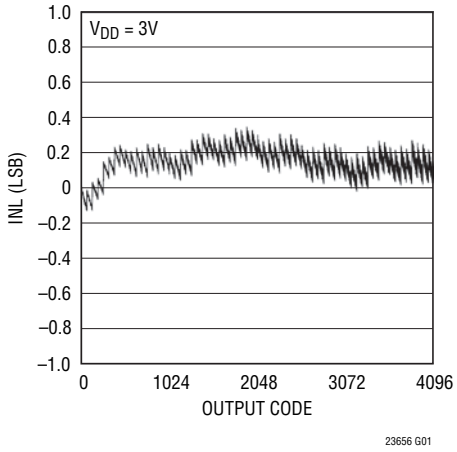
Note 11: The time required for the output to cross the V_{IH} or V_{IL} voltage.

Note 12: Guaranteed by design, not subject to test.

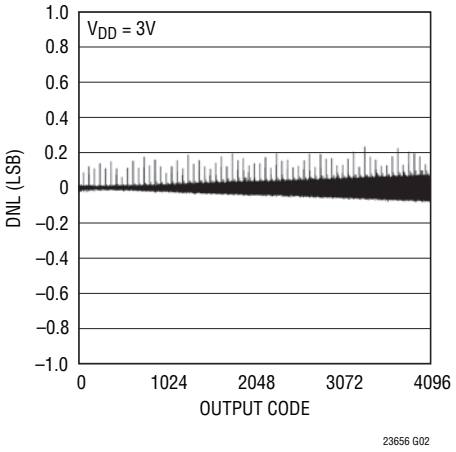
Note 13: High temperatures degrade operating lifetimes. Operating lifetime is derated at temperatures greater than 105°C.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = OV_{DD} = V_{REF}$ (LTC2365, Note 4)

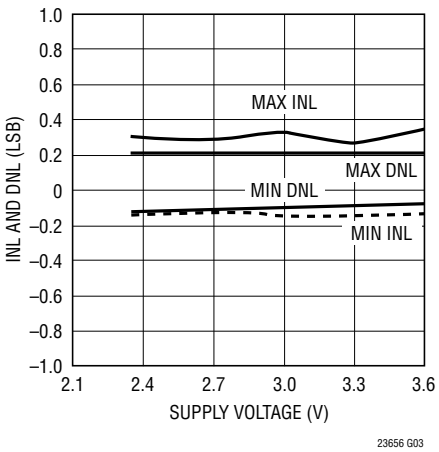
Integral Nonlinearity vs Output Code



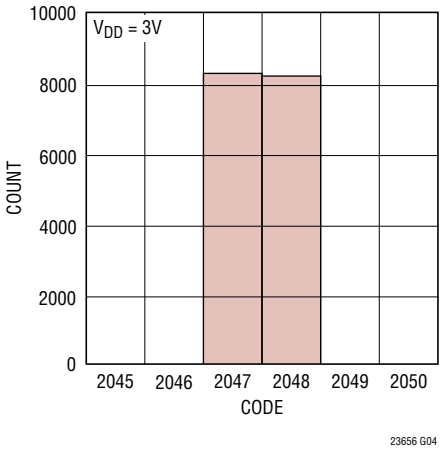
Differential Nonlinearity vs Output Code



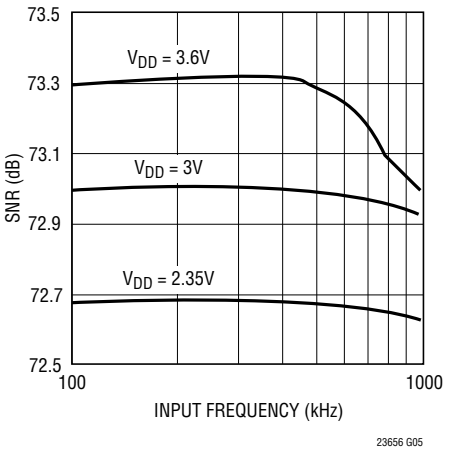
Integral and Differential Nonlinearity vs Supply Voltage



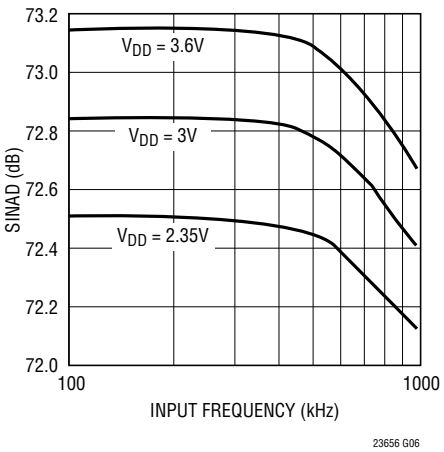
Histogram for 16384 Conversions



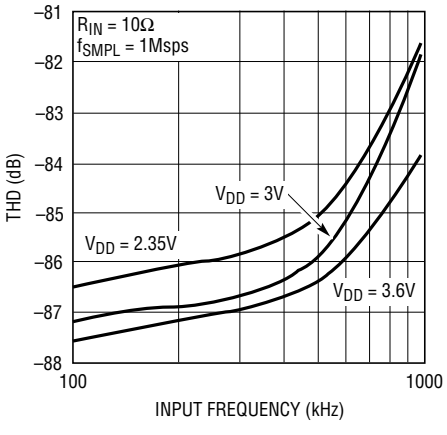
SNR vs Input Frequency



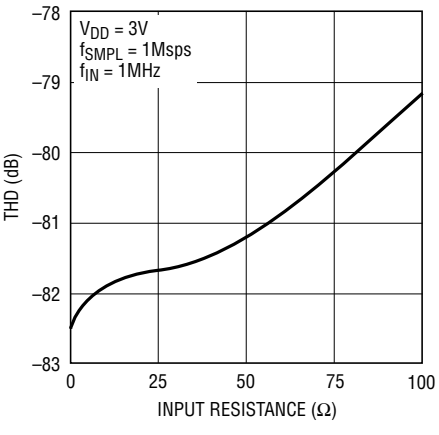
SINAD vs Input Frequency



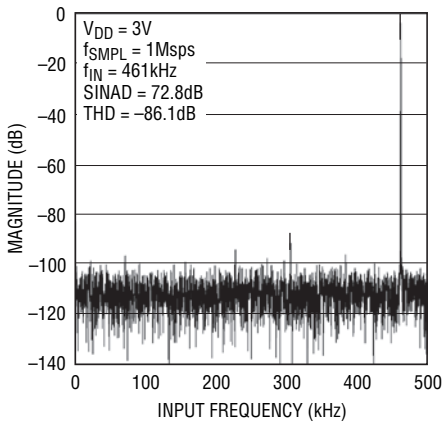
THD vs Input Frequency



THD vs Input Resistance

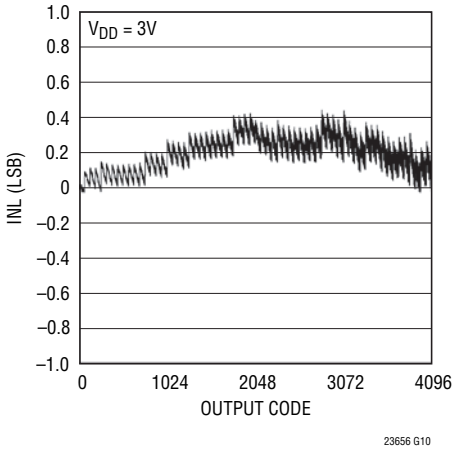


461kHz Sine Wave 8192 FFT Plot



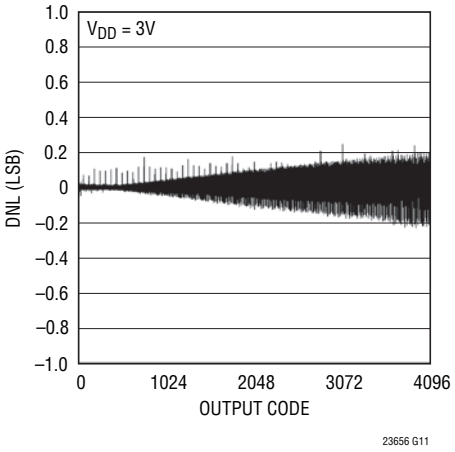
TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = OV_{DD} = V_{REF}$ (LTC2366, Note 4)

Integral Nonlinearity vs Output Code



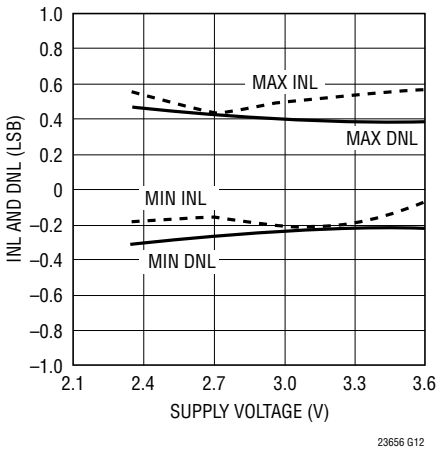
23656 G10

Differential Nonlinearity vs Output Code



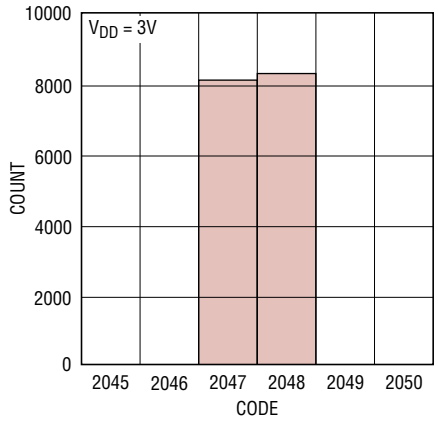
23656 G11

Integral and Differential Nonlinearity vs Supply Voltage



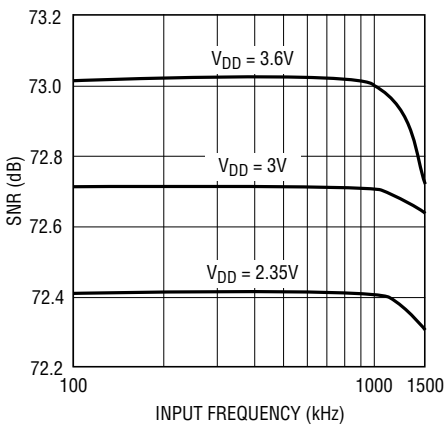
23656 G12

Histogram for 16384 Conversions



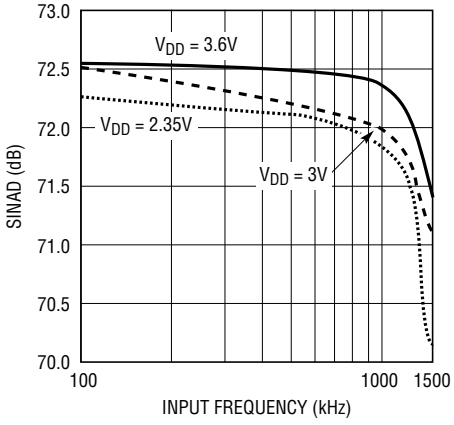
23656 G13

SNR vs Input Frequency



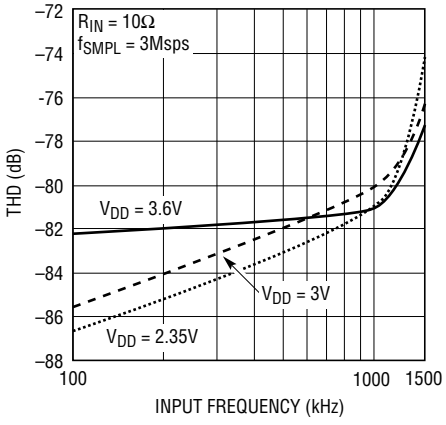
23656 G14

SINAD vs Input Frequency



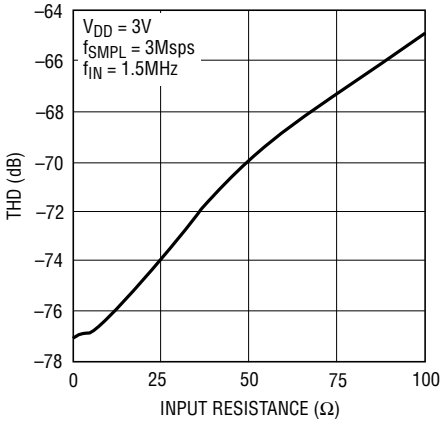
23656 G15

THD vs Input Frequency



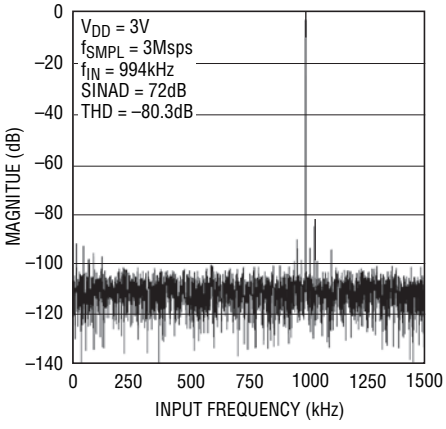
23656 G16

THD vs Input Resistance



23656 G17

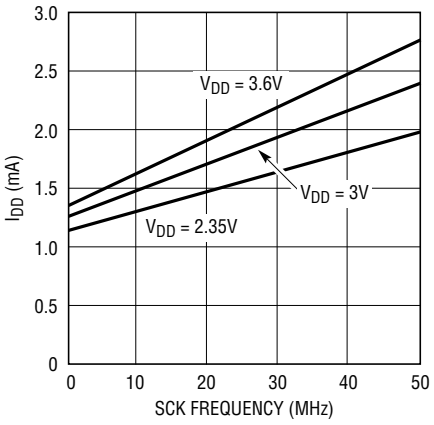
1MHz Sine Wave 8192 FFT Plot



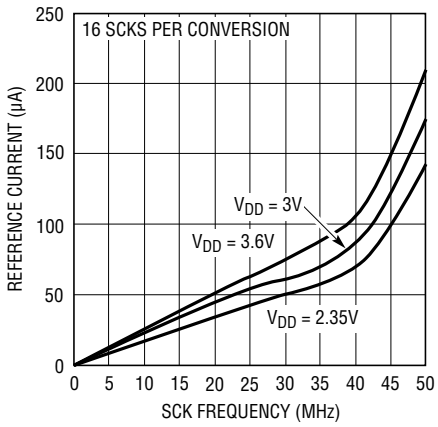
23656 G18

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{DD} = OV_{DD} = V_{REF}$ (LTC2365/LTC2366, Note 4)

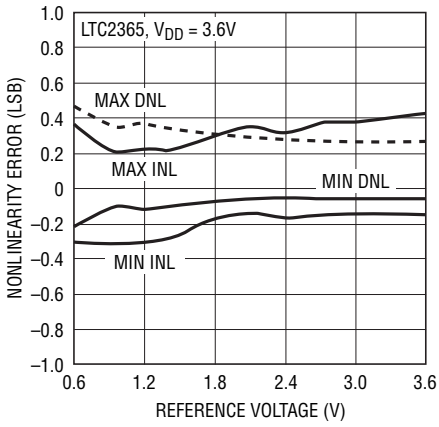
Supply Current vs SCK Frequency



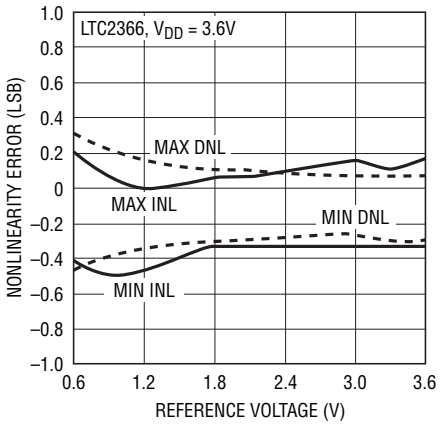
Reference Current vs SCK Frequency (TS8 Package)



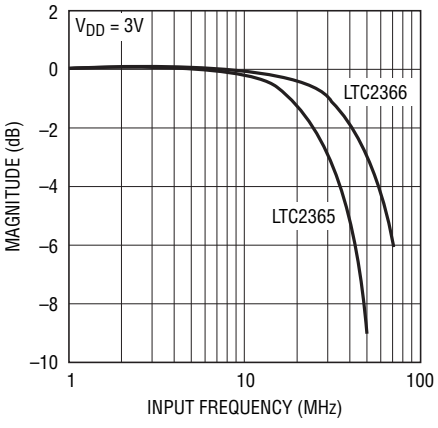
Integral and Differential Nonlinearity vs Reference Voltage (TS8 Package)



Integral and Differential Nonlinearity vs Reference Voltage (TS8 Package)



Input Power Bandwidth



PIN FUNCTIONS

LTC2365/LTC2366 (S6 Package)

V_{DD} (Pin 1): Positive Supply. The V_{DD} range is 2.35V to 3.6V. V_{DD} also defines the input span of the ADC, 0V to V_{DD}. Bypass to GND and to a solid ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 2): Ground. The GND pin must be tied directly to a solid ground plane.

A_{IN} (Pin 3): Analog Input. A_{IN} is a single-ended input with respect to GND with a range from 0V to V_{DD}.

SCK (Pin 4): Shift Clock Input. The SCK serial clock advances the conversion process. SDO data transitions on the falling edge of SCK.

SDO (Pin 5): Three-State Serial Data Output. The A/D conversion result is shifted out on SDO as a serial data stream with MSB first. The data stream consists of two leading zeros followed by 12 bits of conversion data and two trailing zeros.

$\overline{CS}$ (Pin 6): Chip Select Input. This active low signal starts a conversion on the falling edge and frames the serial data transfer.

LTC2365/LTC2366 (TS8 Package)

V_{DD} (Pin 1): Positive Supply. The V_{DD} range is 2.35V to 3.6V. Bypass to GND and to a solid ground plane with a 10µF ceramic capacitor (or 10µF tantalum in parallel with 0.1µF ceramic).

V_{REF} (Pin 2): Reference Input. V_{REF} defines the input span of the ADC, 0V to V_{REF} and the V_{REF} range is 1.4V to V_{DD}. Bypass to GND and to a solid ground plane with a 4.7µF ceramic capacitor (or 4.7µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 3): Ground. The GND pin must be tied directly to a solid ground plane.

A_{IN} (Pin 4): Analog Input. A_{IN} is a single-ended input with respect to GND with a range from 0V to V_{REF}.

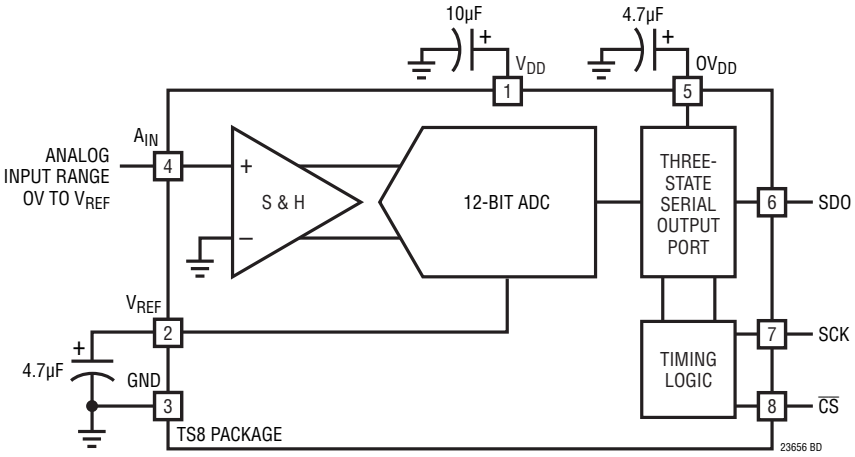
OV_{DD} (Pin 5): Output Driver Supply for SDO. The OV_{DD} range is 1V to V_{DD}. Bypass to GND and to a solid ground plane with a 4.7µF ceramic capacitor (or 4.7µF tantalum in parallel with 0.1µF ceramic).

SDO (Pin 6): Three-State Serial Data Output. The A/D conversion result is shifted out on SDO as a serial data stream with MSB first. The data stream consists of two leading zeros followed by 12 bits of conversion data and two trailing zeros.

SCK (Pin 7): Shift Clock Input. The SCK serial clock advances the conversion process. SDO data transitions on the falling edge of SCK.

$\overline{CS}$ (Pin 8): Chip Select Input. This active low signal starts a conversion on the falling edge and frames the serial data transfer.

BLOCK DIAGRAM



TIMING DIAGRAMS

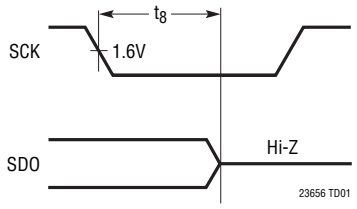


Figure 1. SDO Into Hi-Z State After SCK Falling Edge

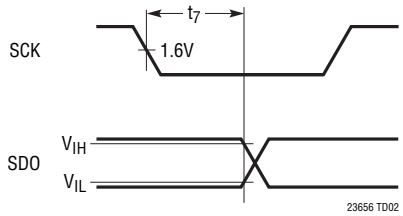


Figure 2. SDO Data Valid Hold Time After SCK Falling Edge

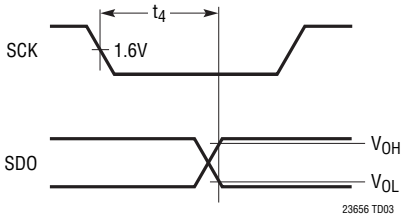


Figure 3. SDO Data Valid Access Time After SCK Falling Edge

APPLICATIONS INFORMATION

DC PERFORMANCE

The noise of an ADC can be evaluated in two ways: signal-to-noise ratio (SNR) in the frequency domain and histogram in the time domain. The LTC2365/LTC2366 excel in both. Figures 5 and 6 demonstrate that the LTC2365/LTC2366 have an SNR of over 72dB. The noise in the time domain histogram is the transition noise associated with a 12-bit resolution ADC which can be measured with a fixed DC signal applied to the input of the ADC. The resulting output codes are collected over a large number of conversions. The shape of the distribution of codes will give an indication of the magnitude of the transition noise. In Figure 4, the distribution of output codes is shown for a DC input that has been digitized 16384 times. The distribution is Gaussian and the RMS code transition is about 0.34LSB. This corresponds to a noise level of 72.7dB relative to a full scale of 3V.

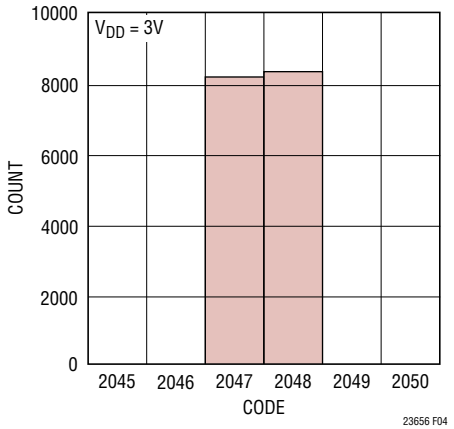


Figure 4. Histogram for 16384 Conversions

DYNAMIC PERFORMANCE

The LTC2365/LTC2366 have excellent high speed sampling capability. Fast fourier transform (FFT) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figures 5 and 6 show typical LTC2365 and LTC2366 FFT plots, respectively.

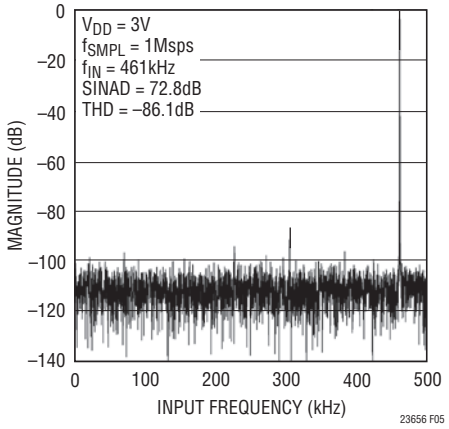


Figure 5. LTC2365 FFT Plot

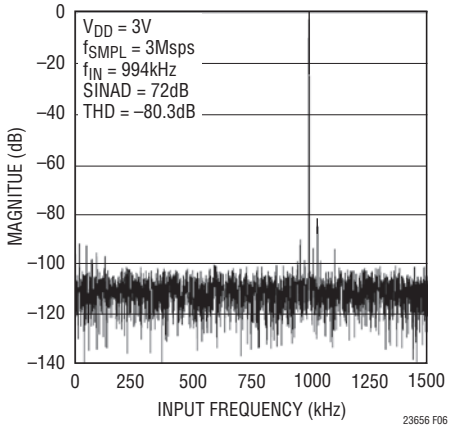


Figure 6. LTC2366 FFT Plot

APPLICATIONS INFORMATION

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 6 shows a typical FFT with a 3MHz sampling rate and a 1MHz input. The dynamic performance is excellent for input frequencies up to and beyond the Nyquist frequency of 1.5MHz.

Effective Number of Bits

The effective number of bits (ENOB) is a measurement of the resolution of an ADC and is directly related to SINAD by the equation:

$$ENOB = (SINAD - 1.76)/6.02$$

where ENOB is the effective number of bits of resolution and SINAD is expressed in dB. At the maximum sampling rate of 3MHz, the LTC2366 maintains ENOB above 11 bits up to the Nyquist input frequency of 1.5MHz (refer to Figure 7).

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_n^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_n are the amplitudes of the second through nth harmonics. THD versus Input Frequency is shown in Figure 8. The LTC2366 has excellent distortion performance up to the Nyquist frequency and beyond.

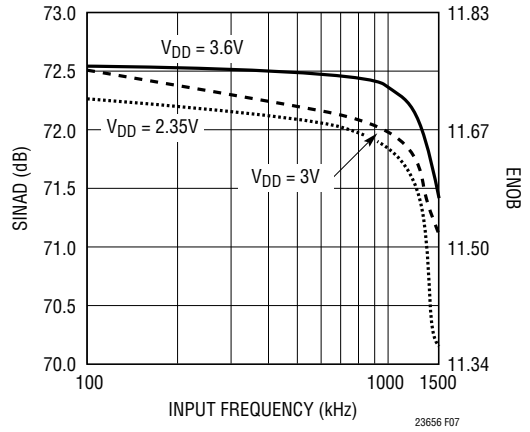


Figure 7. LTC2366 ENOB and SINAD vs Input Frequency

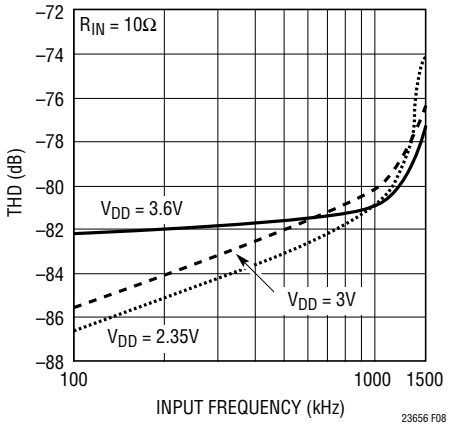


Figure 8. LTC2366 Distortion vs Input Frequency

APPLICATIONS INFORMATION

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a \pm f_b)$. If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(f_a \pm f_b) = 20\log \frac{\text{Amplitude at } (f_a \pm f_b)}{\text{Amplitude at } f_a}$$

The LTC2365/LTC2366 have good IMD as shown in Figure 9a and Figure 9b, respectively.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of reconstructed fundamental is reduced by 3dB for full-scale input signal.

The full-linear bandwidth is the input frequency at which the SINAD has dropped to 68dB (11 effective bits). The LTC2365/LTC2366 have been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; SINAD becomes dominated by distortion at frequencies far beyond Nyquist.

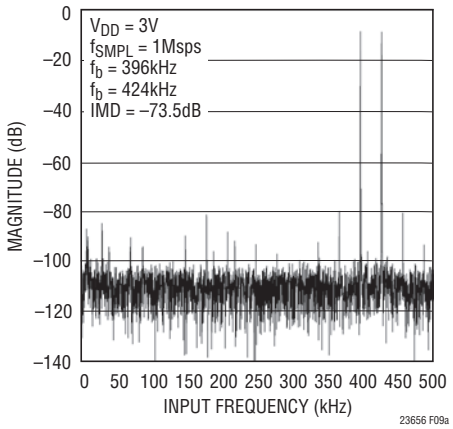


Figure 9a. LTC2365 Intermodulation Distortion Plot

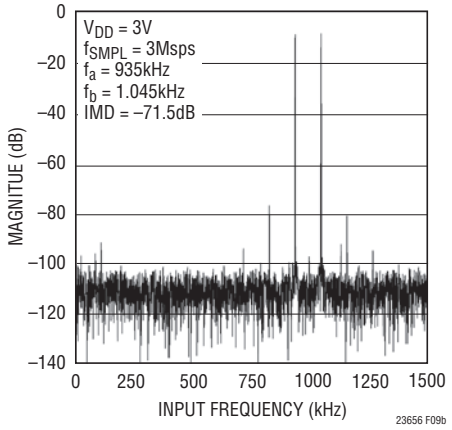


Figure 9b. LTC2366 Intermodulation Distortion Plot

APPLICATIONS INFORMATION

OVERVIEW

The LTC2365/LTC2366 use a successive approximation algorithm and internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output. Both devices operate from a single 2.35V to 3.6V supply. The LTC2366 samples at a rate of 3Msps with a 48MHz clock while the LTC2365 samples at a rate of 1Msps with a 16MHz clock.

The LTC2365/LTC2366 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, and a serial interface (see Block Diagram) and are available in tiny 6- and 8-lead TSOT-23 packages. The devices provide sleep mode control through the serial interface to save power during inactive periods (see the SLEEP MODE section).

The S6 package of the LTC2365/LTC2366 uses V_{DD} as the reference and has an analog input range of 0V to V_{DD}. The ADC samples the analog input with respect to GND and outputs the result through the serial interface.

The TS8 package provides two additional pins: a reference input pin, V_{REF}, and an output supply pin, OV_{DD}. The ADC can operate with reduced spans down to 1.4V and achieve 342µV resolution. OV_{DD} controls the output swing of the digital output pin, SDO, and allows the device to communicate with 1.8V, 2.5V or 3V digital systems.

SERIAL INTERFACE

The LTC2365/LTC2366 communicate with microcontrollers, DSPs and other external circuitry via a 3-wire interface. Figure 10 shows the serial interface timing diagram, while Figures 11 and 12 detail the timing diagrams of conversion cycles in 14 and 16 SCK cycles, respectively.

Data Transfer

A falling $\overline{CS}$ edge starts a conversion and frames the serial data transfer. SCK provides the conversion clock and controls the data transfer during the conversion.

$\overline{CS}$ going LOW clocks out the first leading zero and subsequent SCK falling edges clock out the remaining data, beginning with the second leading zero. (Therefore, the first SCK falling edge captures the first leading zero and clocks out the second leading zero). The timing diagram in Figure 12 shows that the final bit in the data transfer is valid on the 16th falling edge, since it is clocked out on the previous 15th falling edge.

In applications with a slower SCK, it is possible to capture data on each SCK rising edge. In such cases, the first falling edge of SCK clocks out the second leading zero and can be captured on the first rising edge. However, the first leading zero clocked out when $\overline{CS}$ goes LOW is missed, as shown in Figures 11 and 12. In Figure 12, the 15th falling edge of SCK clocks out the last bit and can be captured on the 15th rising SCK edge.

If $\overline{CS}$ goes LOW while SCK is LOW, then $\overline{CS}$ clocks out the first leading zero and can be captured on the SCK rising edge. The next SCK falling edge clocks out the second leading zero and can be captured on the following rising edge, as shown in Figure 10.

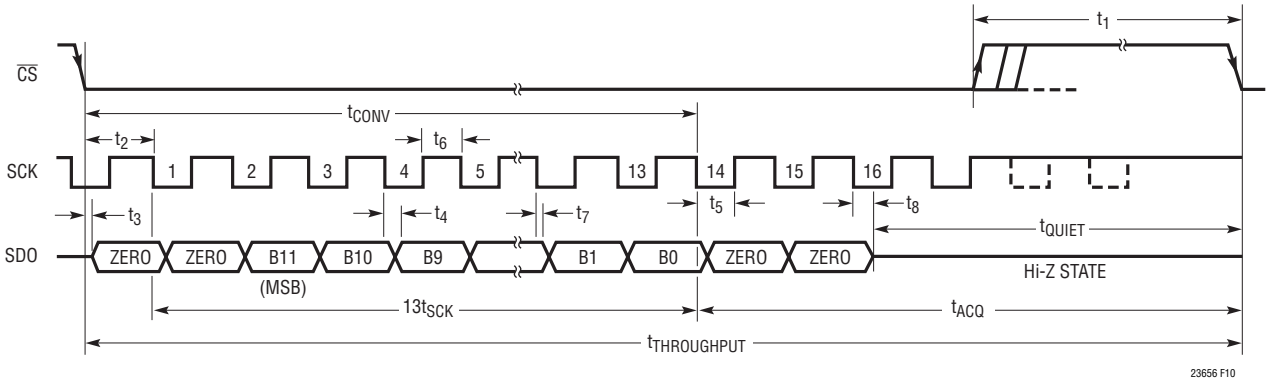


Figure 10. LTC2365/LTC2366 Serial Interface Timing Diagram

APPLICATIONS INFORMATION

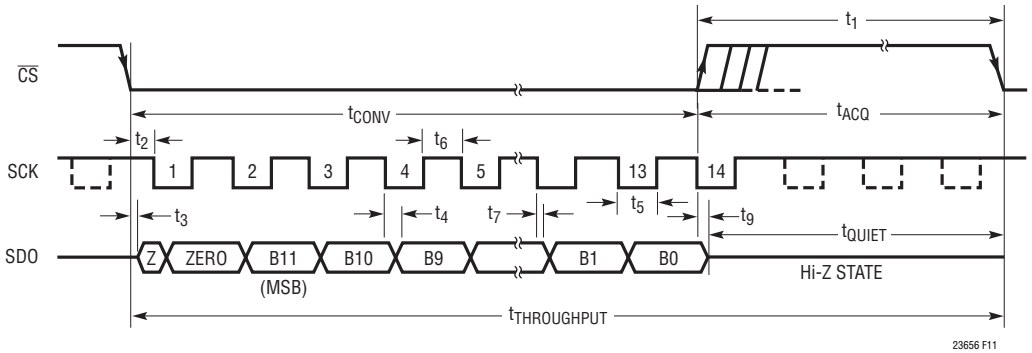


Figure 11. LTC2365/LTC2366 Serial Interface Timing Diagram for 14 SCK Cycles

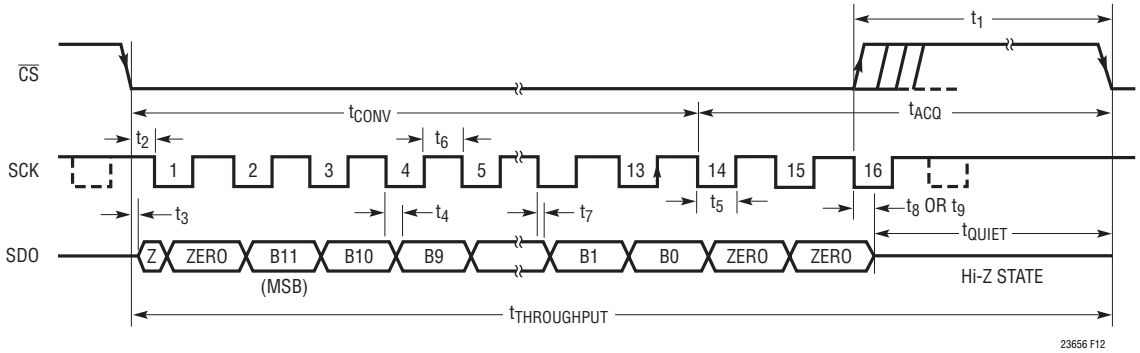


Figure 12. LTC2365/LTC2366 Serial Interface Timing Diagram for 16 SCK Cycles

Achieving 3Msps Sample Rate with LTC2366

$\overline{CS}$ going LOW places the sample-and-hold into hold mode and starts a conversion. The LTC2365/LTC2366 require at least 14 SCK cycles to finish the conversion. The conversion terminates after the 13th falling SCK edge, which clocks out B0. The 14th falling SCK edge places the sample-and-hold back into sample mode.

Ignoring the last two trailing zeros, the user can bring $\overline{CS}$ HIGH after the 14th falling SCK edge. The user can also keep the last two trailing zeros by bringing $\overline{CS}$ HIGH right after the 16th falling SCK. In both cases, a sample rate of 3Msps can be achieved by using a 48MHz SCK clock on the LTC2366, where $t_{THROUGHPUT}$ is 333ns.

Serial Data Output (SDO)

The SDO output remains in the high impedance state while $\overline{CS}$ is HIGH. The falling edge of $\overline{CS}$ starts the conversion and enables SDO. The A/D conversion result is shifted out on the SDO pin as a serial data stream with the MSB first. The data stream consists of two leading zeros followed by 12 bits of conversion data and two trailing zeros. The SDO output returns to the high impedance state at the 16th falling edge of SCK or sooner by bringing $\overline{CS}$ HIGH before the 16th falling edge of SCK.

The output swing on the SDO pin is controlled by the V_{DD} pin voltage in the S6 package and by the OV_{DD} pin voltage in the TS8 package.

APPLICATIONS INFORMATION

SLEEP MODE

The LTC2365/LTC2366 provide a sleep mode to conserve power during inactive periods. Upon power-up, holding $\overline{CS}$ HIGH initializes the ADC to sleep mode. In sleep mode, all bias circuitry is shut down and only leakage currents remain (0.1µA typ).

Entering Sleep Mode

The ADC achieves the fastest sampling rate in operational mode (full power-up). The device can also be put into sleep mode for power savings during inactive periods. To force the LTC2365/LTC2366 into sleep mode, the user can interrupt the conversion process by bringing $\overline{CS}$ HIGH between the 2nd and 10th falling edges of SCK (see Figures 13 and 14). If $\overline{CS}$ is brought HIGH after the 10th falling edge and before the 16th falling edge, the device remains powered up, but the conversion is terminated and SDO returns to the high impedance state.

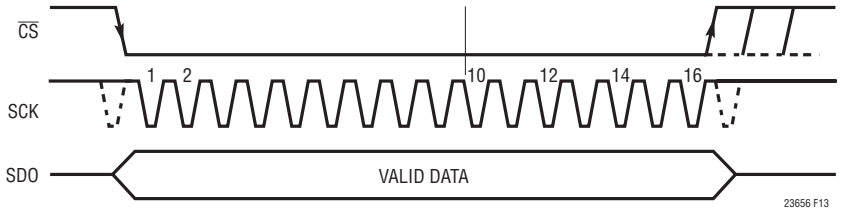


Figure 13. LTC2365/LTC2366 Operational Mode

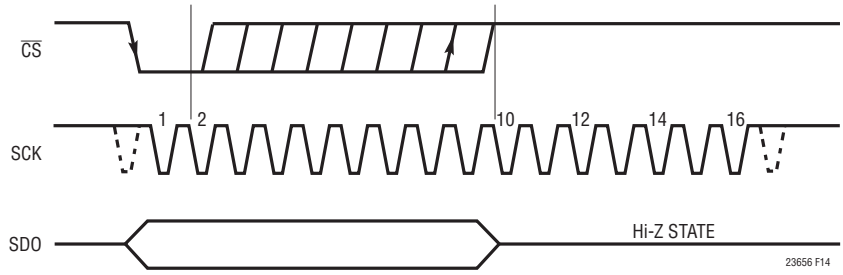


Figure 14. LTC2365/LTC2366 Entering Sleep Mode

APPLICATIONS INFORMATION

Exiting Sleep Mode and Power-Up Time

To exit sleep mode, pull $\overline{CS}$ LOW and perform a dummy conversion. The LTC2365/LTC2366 device power up completely after the 16th falling edge of SCK. After powering up, the ADC can continuously acquire an input signal and perform conversions as described in the SERIAL INTERFACE section (see Figure 15). The wake-up time is 333ns for the LTC2366 with a 48MHz SCK and 1µs for the LTC2365 with a 16MHz SCK.

The sample-and-hold is in hold mode while the device is in sleep mode. The ADC returns to sample mode after the 1st falling edge of SCK during power-up (see Figure 15).

POWER VERSUS SAMPLING RATE

Figure 16 shows the power consumption of the LTC2365/LTC2366 in operational mode. By taking the ADC into sleep mode when not performing a conversion, the average power consumption of the ADC decreases as the sampling rate decreases. Figure 17 shows the power consumption versus sampling rate with the device in sleep mode when not performing a conversion.

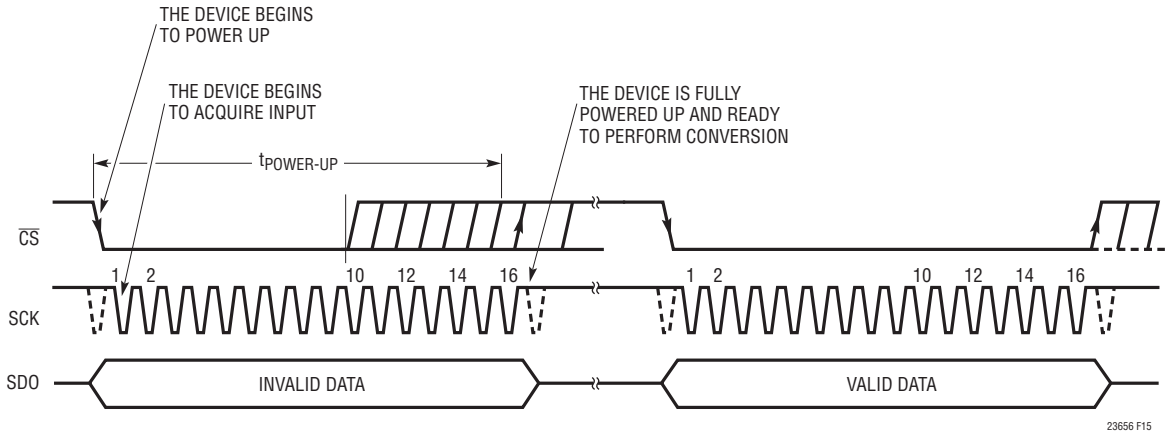


Figure 15. LTC2365/LTC2366 Exiting Sleep Mode

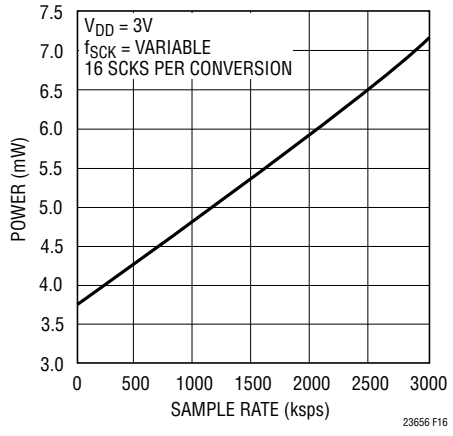


Figure 16. Power Consumption vs Sample Rate while the Device Remains Powered Up Continuously

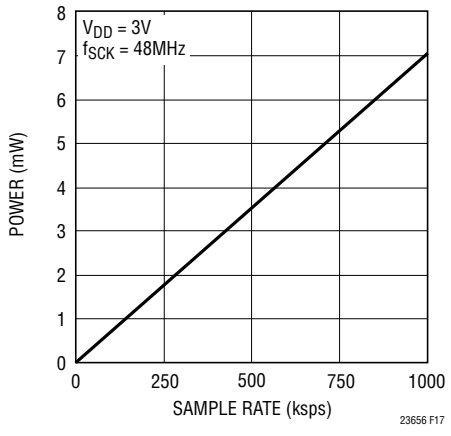


Figure 17. Power Consumption vs Sample Rate while the Device Enters Sleep Mode when not Performing Conversions

APPLICATIONS INFORMATION

SINGLE-ENDED ANALOG INPUT

Driving the Analog Input

The analog input of the LTC2365/LTC2366 is easy to drive. The input draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During the conversion, the analog input draws only a small leakage current. If the source impedance of the driving circuit is low, then the input of the LTC2365/LT2366 can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier should be used. The main requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts (settling time must be less than 56ns for full throughput rate). While choosing an input amplifier, also keep in mind the amount of noise and harmonic distortion the amplifier contributes.

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 40MHz to ensure adequate small signal settling for full throughput rate. If slower op amps are used, more time for settling can be provided by increasing the time between conversions. The best choice for an op amp to drive the LTC2365/LTC2366 will depend on the application. Generally, applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical. The following list is a summary of the op amps that are suitable for driving the LTC2365/LTC2366. (More detailed information is available on the Linear Technology website at www.linear.com.)

LTC1566-1: Low Noise 2.3MHz Continuous Time Lowpass Filter.

LT®1630: Dual 30MHz Rail-to-Rail Voltage Feedback Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 500µV offset and 520ns settling to 0.5LSB for a 4V swing. THD and noise are –93dB to 40kHz and below 1LSB to 320kHz (A_V = 1, $2V_{P-P}$ into 1k, V_S = 5V), making the part excellent for AC applications (to 1/3 Nyquist) where rail-to-rail performance is desired. Quad version is available as LT1631.

LT1632: Dual 45MHz Rail-to-Rail Voltage Feedback Amplifier. 2.7V to ±15V supplies. Very high A_{VOL}, 1.5mV offset and 400ns settling to 0.5LSB for a 4V swing. It is suitable for applications with a single 5V supply. THD and noise are –93dB to 40kHz and below 1LSB to 800kHz (A_V = 1, $2V_{P-P}$ into 1k, V_S = 5V), making the part excellent for AC applications where rail-to-rail performance is desired. Quad version is available as LT1633.

LT1813: Dual 100MHz 750V/µs 3mA Voltage Feedback Amplifier. 5V to ±5V supplies. Distortion is –86dB to 100kHz and –77dB to 1MHz with ±5V supplies ($2V_{P-P}$ into 500). Excellent part for fast AC applications with ±5V supplies.

LT1801: 180MHz GBWP, –75dBc at 500kHz, 2mA/Amplifier, 8.5nV/$\sqrt{Hz}$.

LT1806/LT1807: 325MHz GBWP, –80dBc Distortion at 5MHz, Unity-Gain Stable, R-R In and Out, 10mA/Amplifier, 3.5nV/$\sqrt{Hz}$.

LT1810: 180MHz GBWP, –90dBc Distortion at 5MHz, Unity-Gain Stable, R-R In and Out, 15mA/Amplifier, 16nV/$\sqrt{Hz}$.

LT1818/LT1819: 400MHz, 2500V/µs, 9mA, Single/Dual Voltage Mode Operational Amplifier.

LT6200: 165MHz GBWP, –85dBc Distortion at 1MHz, Unity-Gain Stable, R-R In and Out, 15mA/Amplifier, 0.95nV/$\sqrt{Hz}$.

LT6203: 100MHz GBWP, –80dBc Distortion at 1MHz, Unity-Gain Stable, R-R In and Out, 3mA/Amplifier, 1.9nV$\sqrt{Hz}$.

APPLICATIONS INFORMATION

Input Filtering and Source Impedance

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC2365/LTC2366 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 50MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 18 shows a 47pF capacitor from A_{IN} to ground and a 51Ω source resistor to limit the input bandwidth to 47MHz. The 47pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling-glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems. When high amplitude unwanted signals are close in frequency to the desired signal frequency, a multiple pole filter is required. High external source resistance, combined with the 20pF of input capacitance, will reduce the rated 50MHz bandwidth and increase acquisition time beyond 56ns.

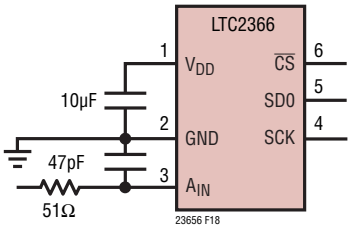


Figure 18. RC Input Filter

Reference Input

On the TS8 package of the LTC2365/LTC2366, the voltage on the V_{REF} pin defines the full-scale range of the ADC. The reference voltage can range from V_{DD} down to 1.4V.

Input Range

The analog input of the LTC2365/LTC2366 is driven single-ended with respect to GND from a single supply. The input may swing up to V_{DD} for the S6 package and to V_{REF} for the TS8 package. The 0V to 2.5V range is also ideally suited for single-ended input use with V_{DD} or V_{REF} = 2.5V for single supply applications. If the difference between the A_{IN} input and GND exceeds V_{DD} for the S6 package or V_{REF} for the TS8 package, the output code will stay fixed at all ones, and if this difference goes below 0V, the output code will stay fixed at all zeros.

Figure 19 shows the ideal input/output characteristics for the LTC2365/LTC2366. The code transitions occur midway between successive integer LSB values (i.e. 0.5LSB, 1.5LSB, 2.5LSB, …, FS –1.5LSB). The output code is straight binary with 1LSB = V_{DD}/4096 for the S6 package and 1LSB = V_{REF}/4096 for the TS8 package.

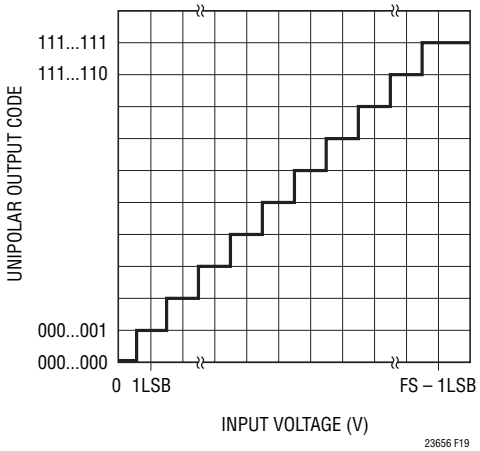


Figure 19. LTC2365/LTC2366 Transfer Characteristics

APPLICATIONS INFORMATION

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution and/or high speed A/D converters. To obtain the best performance from the LTC2365/LTC2366, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by the ground plane.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in the Typical Application circuit on the first page of this data sheet. For optimum performance, a 10µF surface mount AVX capacitor with a 0.1µF ceramic is recommended for the V_{DD} pin and a 4.7µF surface mount AVX capacitor with a 0.1µF ceramic is recommended for the V_{REF} and OV_{DD} pins. Alternatively, 4.7µF and 10µF ceramic chip capacitors such as Murata GRM235Y5V106Z016 may be used. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Figure 20 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC2365/LTC2366. The ground return from the LTC2365/LTC2366 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

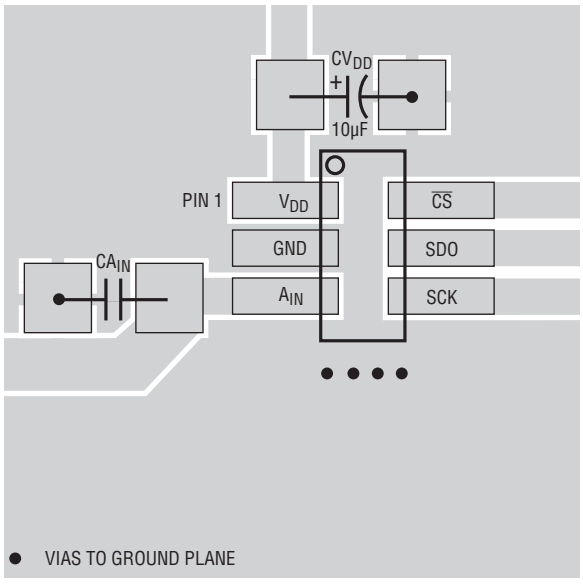
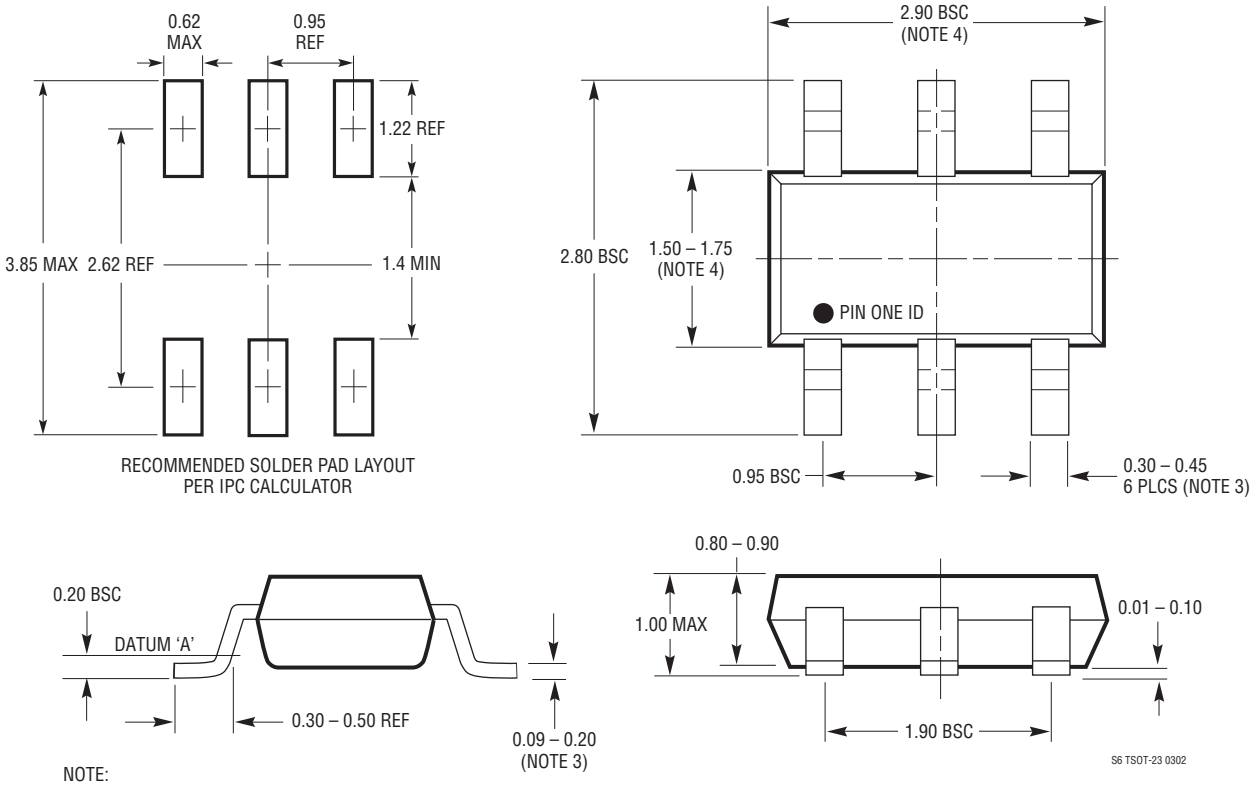


Figure 20. Power Supply Ground Practice

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

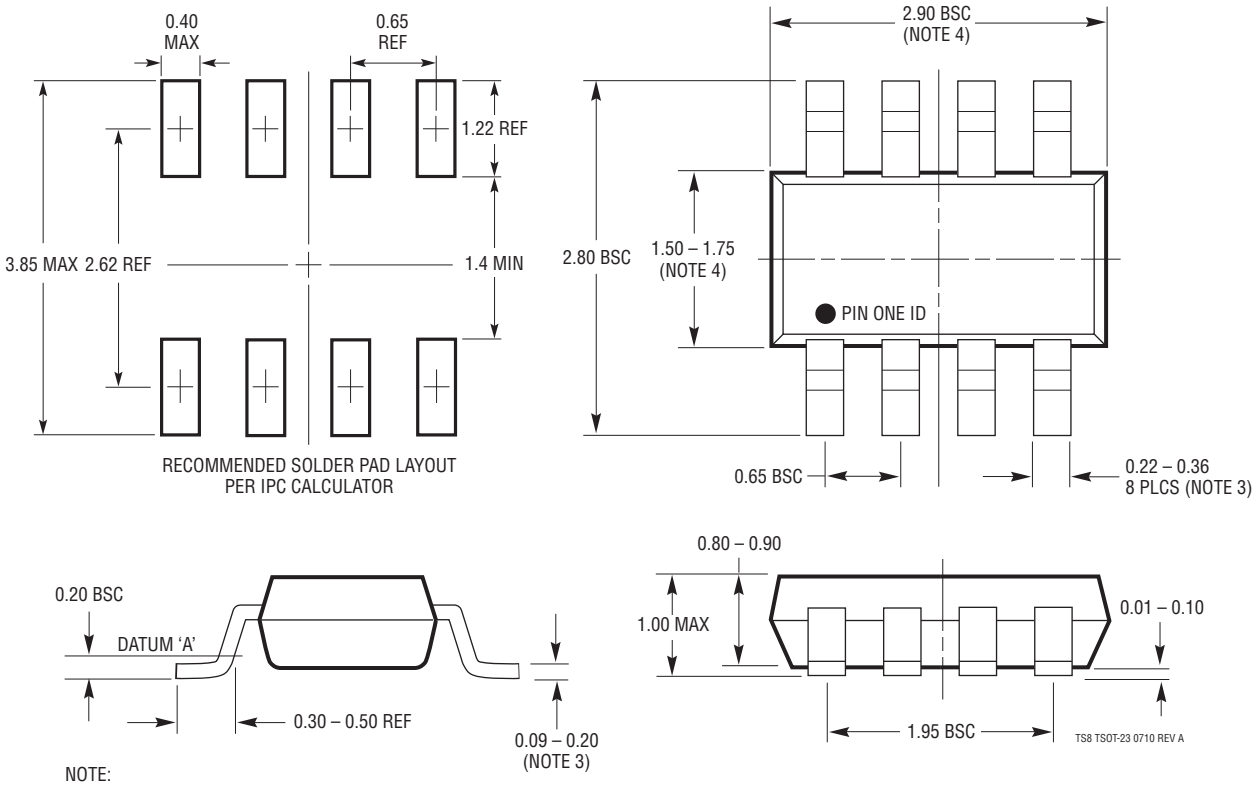


NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	12/13	Updated TS8 package drawing	22