16-Bit, 250ksps SAR ADC with 94dB SNR

FEATURES

- **250ksps Throughput Rate**
- **±2LSB INL (Max)**
- **Guaranteed 16-Bit No Missing Codes**
- **94dB SNR (Typ) at f_{IN} = 20kHz**
- Guaranteed Operation to 125°C
- Single 5V Supply
- 1.8V to 5V I/O Voltages
- 95mW Power Dissipation
- ±4.096V Differential Input Range
- Internal Reference (20ppm/°C Max)
- No Pipeline Delay, No Cycle Latency
- Parallel and Serial Interface
- Internal Conversion Clock
- 48-Lead 7mm × 7mm LQFP and QFN Packages

APPLICATIONS

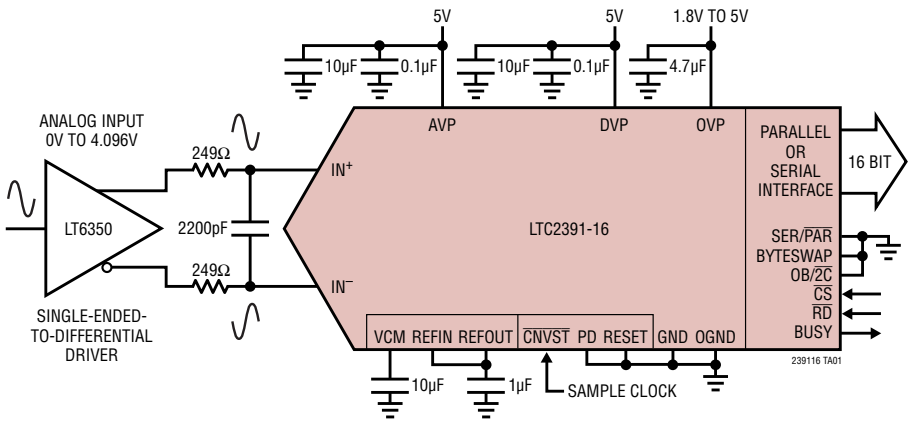
- Medical Imaging
- High Speed Data Acquisition
- Digital Signal Processing
- Industrial Process Control
- Instrumentation
- ATE

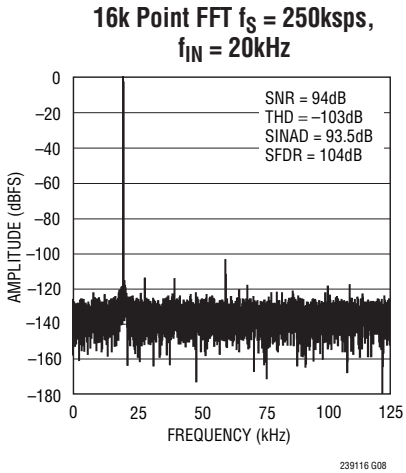
DESCRIPTION

The LTC®2391-16 is a low noise, high speed 16-bit successive approximation register (SAR) ADC. Operating from a single 5V supply, the LTC2391-16 supports a large ±4.096V fully differential input range, making it ideal for high performance applications which require maximum dynamic range. The LTC2391-16 achieves ±2LSB INL max, no missing codes at 16-bits and 94dB SNR (typ).

The LTC2391-16 includes a precision internal reference with a guaranteed 0.5% initial accuracy and a ±20ppm/°C (max) temperature coefficient. Fast 250ksps throughput with no cycle latency in both parallel and serial interface modes makes the LTC2391-16 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2391-16 dissipates only 95mW at 250ksps, while both nap and sleep power-down modes are provided to further reduce power during inactive periods.

TYPICAL APPLICATION



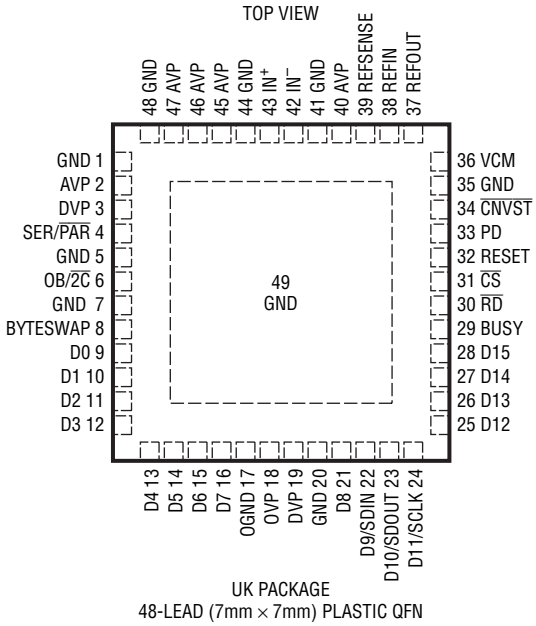


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{AVP}, V_{DVP}, V_{OVP}) 6.0V
Analog Input Voltage (Note 3)
IN^+, IN^-, REFIN, $\overline{CNVST}$ .. (GND – 0.3V) to (V_{AVP} + 0.3V)
Digital Input Voltage..... (GND – 0.3V) to (V_{OVP} + 0.3V)
Digital Output Voltage ..... (GND – 0.3V) to (V_{OVP} + 0.3V)
Power Dissipation 500mW

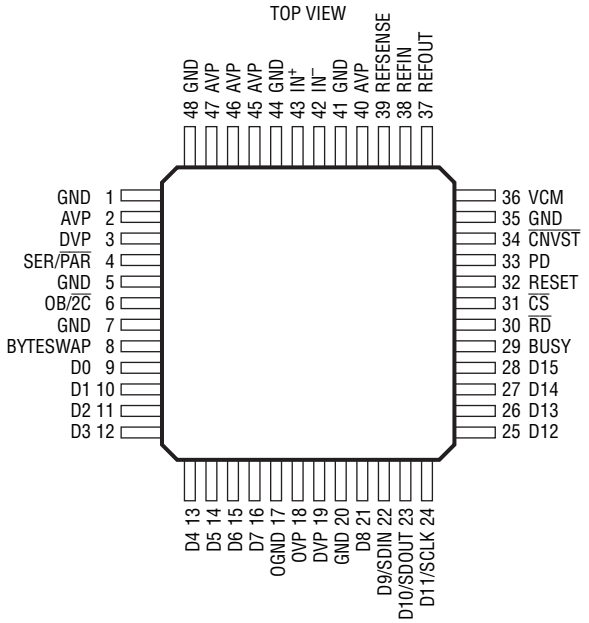
Operating Temperature Range
LTC2391C ..... 0°C to 70°C
LTC2391I..... –40°C to 85°C
LTC2391H ..... –40°C to 125°C
Storage Temperature Range..... –65°C to 150°C

PIN CONFIGURATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB



LX PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP

T_{JMAX} = 150°C, θ_{JA} = 55°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2391CUK-16#PBF	LTC2391CUK-16#TRPBF	LTC2391UK-16	48-Lead 7mm × 7mm Plastic QFN	0°C to 70°C
LTC2391IUK-16#PBF	LTC2391IUK-16#TRPBF	LTC2391UK-16	48-Lead 7mm × 7mm Plastic QFN	–40°C to 85°C
LEAD FREE FINISH	**TRAY**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2391CLX-16#PBF	LTC2391CLX-16#PBF	LTC2391LX-16	48-Lead 7mm × 7mm Plastic LQFP	0°C to 70°C
LTC2391ILX-16#PBF	LTC2391ILX-16#PBF	LTC2391LX-16	48-Lead 7mm × 7mm Plastic LQFP	–40°C to 85°C
LTC2391HLX-16#PBF	LTC2391HLX-16#PBF	LTC2391LX-16	48-Lead 7mm × 7mm Plastic LQFP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (IN^+)	(Note 5)	●	–0.05		AVP	V
V_{IN}^-	Absolute Input Range (IN^-)	(Note 5)	●	–0.05		AVP	V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	$V_{IN} = V_{IN}^+ – V_{IN}^-$	●	$–V_{REF}$		V_{REF}	V
V_{CM}	Common Mode Input Range		●	$V_{REF}/2 – 0.05$	$V_{REF}/2$	$V_{REF}/2 + 0.05$	V
I_{IN}	Analog Input Leakage Current		●			±1	µA
C_{IN}	Analog Input Capacitance	Sample Mode Hold Mode			45 5		pF pF
CMRR	Input Common Mode Rejection Ratio				70		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	16			Bits
	No Missing Codes		●	16			Bits
	Transition Noise				0.3		LSB_{RMS}
INL	Integral Linearity Error	(Note 6)	●	–2	±1	2	LSB
DNL	Differential Linearity Error		●	–1		1	LSB
BZE	Bipolar Zero Error	(Note 7)	●	–7		7	LSB
	Bipolar Zero Error Drift				1		ppm/°C
FSE	Bipolar Full-Scale Error	External Reference Internal Reference (Note 7)	●			0.14 0.1	% %
	Bipolar Full-Scale Error Drift				±10		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS (Notes 4, 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	f_{IN} = 20kHz	●	90.5	93.5		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 20kHz	●	91	94		dB
THD	Total Harmonic Distortion	f_{IN} = 20kHz, First 5 Harmonics	●		–103	–94	dB
SFDR	Spurious-Free Dynamic Range	f_{IN} = 20kHz			104		dB
	–3dB Input Bandwidth				50		MHz
	Aperture Delay				0.5		ns
	Aperture Jitter				7		ps_{RMS}
	Transient Response	Full-Scale Step			60		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		4.076	4.096	4.116	V
V_{REF} Output Tempco	I_{OUT} = 0 (I-, H-Grades) (Note 11)	●		±10	±20	ppm/°C
V_{REF} Output Impedance	–0.1mA ≤ I_{OUT} ≤ 0.1mA			2.6		kΩ
External Reference Voltage			2.5	4.096	AVP – 0.5	V
REFIN Input Impedance				85		kΩ
V_{REF} Line Regulation	AVP = 4.75V to 5.25V			0.3		mV/V
VCM Output Voltage	I_{OUT} = 0			2.08		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OVP			V
V_{IL}	Low Level Input Voltage		●			0.5	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OVP	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OVP – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OVP	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OVP			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{AVP}, V_{DVP}	Supply Voltage		●	4.75	5	5.25	V
V_{OVP}	Supply Voltage			1.71		5.25	V
I_{DD}	Supply Current Power Down Mode	250ksps Sample Rate with Nap Mode Conversion Done and All Digital Inputs Tied to OVP	● ●		19 35	25 250	mA µA
P_D	Power Dissipation Power Down Mode	250ksps Sample Rate with Nap Mode Conversion Done and All Digital Inputs Tied to OVP			95 175	125 1250	mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Sampling Frequency		●			250	ksps
t_{CONV}	Conversion Time		●			2500	ns
t_{ACQ}	Acquisition Time		●			1485	ns
t_4	$\overline{CNVST}$ Low Time		●	20			ns
t_5	$\overline{CNVST}$ High Time		●	250			ns
t_6	$\overline{CNVST}\downarrow$ to BUSY Delay	C_L = 15pF	●			15	ns
t_7	RESET Pulse Width		●	5			ns
t_8	SCLK Period	(Note 9)	●	12.5			ns
t_9	SCLK High Time		●	4			ns
t_{10}	SCLK Low Time		●	4			ns
t_r, t_f	SCLK Rise and Fall Times	(Note 10)				1	µs
t_{11}	SDIN Setup Time		●	2			ns
t_{12}	SDIN Hold Time		●	1			ns
t_{13}	SDOUT Delay After SCLK↑	C_L = 15pF	●	2		8	ns
t_{14}	SDOUT Delay After $\overline{CS}\downarrow$		●			8	ns
t_{15}	$\overline{CS}\downarrow$ to SCLK Setup Time		●	20			ns
t_{16}	Data Valid to BUSY↓		●	1			ns
t_{17}	Data Access Time after $\overline{RD}\downarrow$ or BYTESWAP↑		●	10			ns
t_{18}	Bus Relinquish Time		●			10	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above AVP, DVP or OVP, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above AVP, DVP or OVP without latchup.

Note 4: AVP = DVP = OVP = 5V, f_{SMPL} = 250ksps, external reference equal to 4.096V unless otherwise noted.

Note 5: Recommended operating conditions.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Bipolar zero error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Bipolar full-scale error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

Note 8: All specifications in dB are referred to a full-scale ±4.096V input with a 4.096V reference voltage.

Note 9: t_{13} of 8ns maximum allows a shift clock frequency up to $2 \bullet (t_{13} + t_{SETUP})$ for falling edge capture with 50% duty cycle and up to 80MHz for rising capture. t_{SETUP} is the set-up time of the receiving logic.

Note 10: Guaranteed by design.

Note 11: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

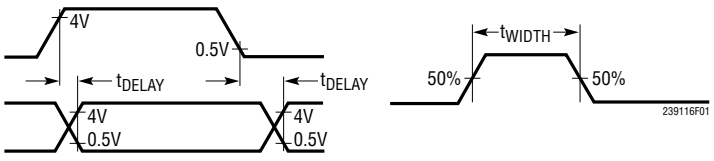
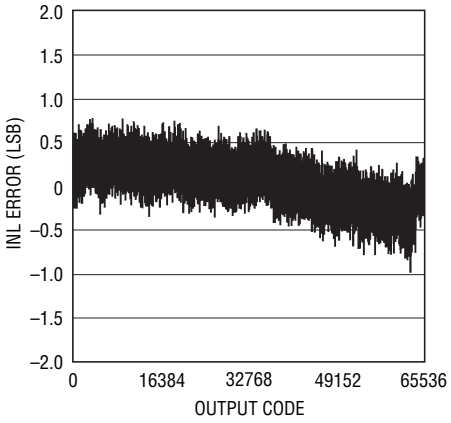


Figure 1. Voltage Levels for Timing Specifications

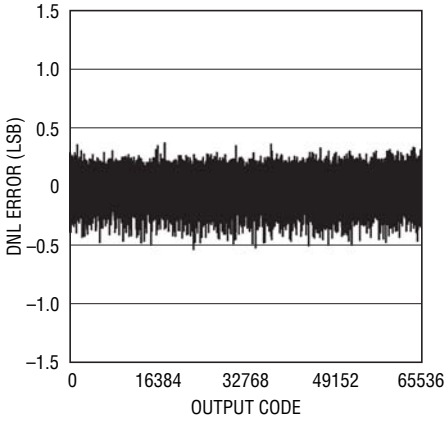
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, f_{SMPL} = 250ksps, unless otherwise noted.

Integral Nonlinearity vs Output Code



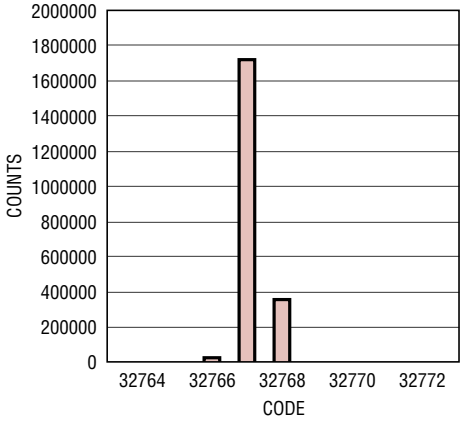
239116 G01

Differential Nonlinearity vs Output Code



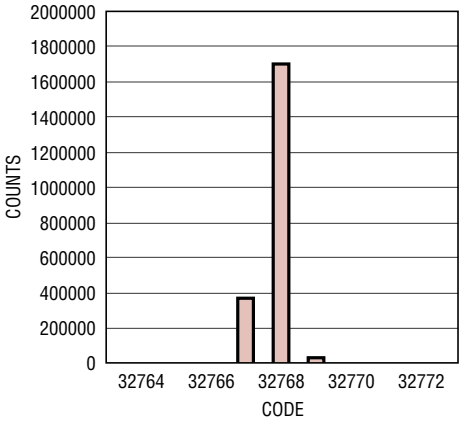
239116 G02

DC Histogram (External Reference)



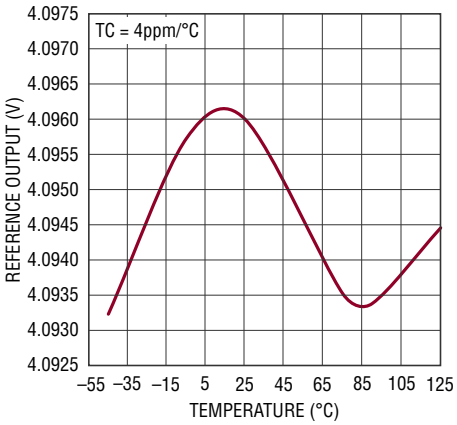
239116 G03

DC Histogram (Internal Reference)



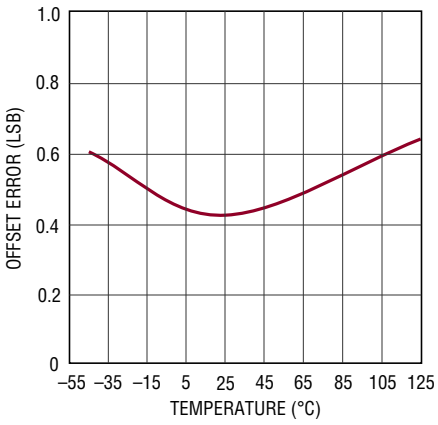
239116 G04

Internal Reference Output vs Temperature



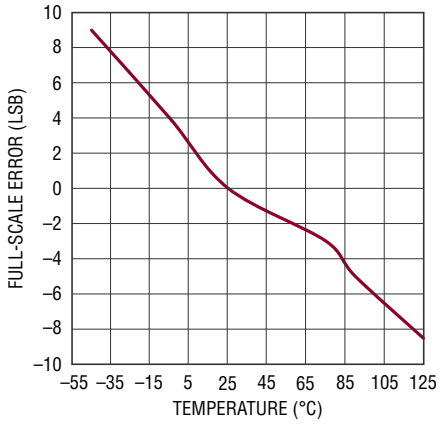
239116 G05

Offset Error vs Temperature



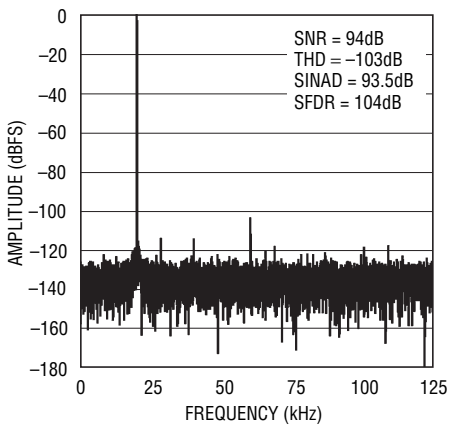
239116 G06

Full-Scale Error vs Temperature



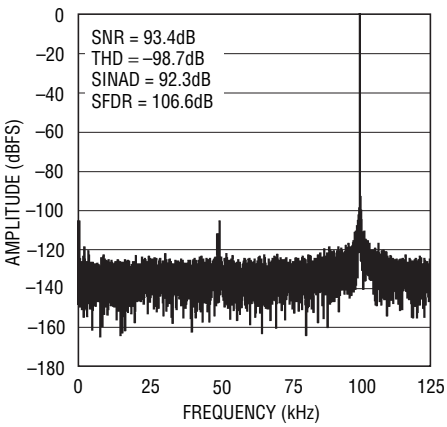
239116 G07

16k Point FFT f_S = 250ksps, f_{IN} = 20kHz



239116 G08

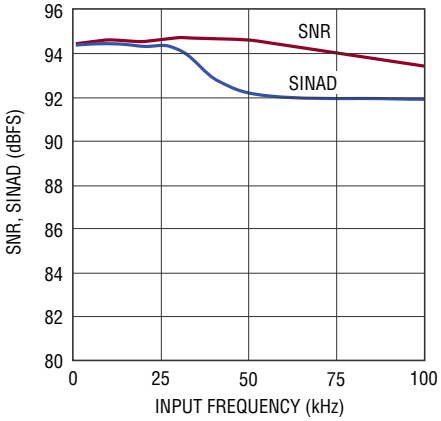
16k Point FFT f_S = 250ksps, f_{IN} = 100kHz



239116 G09

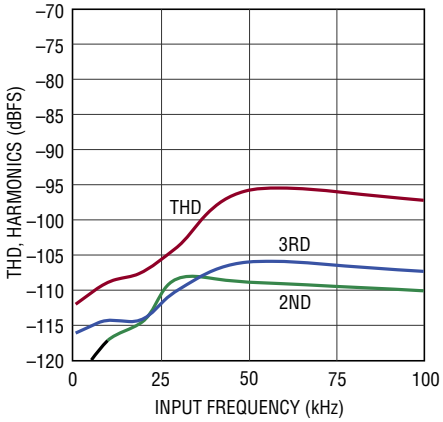
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, f_{SMPL} = 250ksps, unless otherwise noted.

SNR, SINAD vs Input Frequency



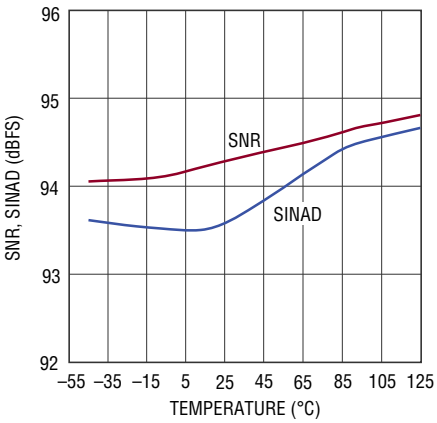
239116 G10

THD, Harmonics vs Input Frequency



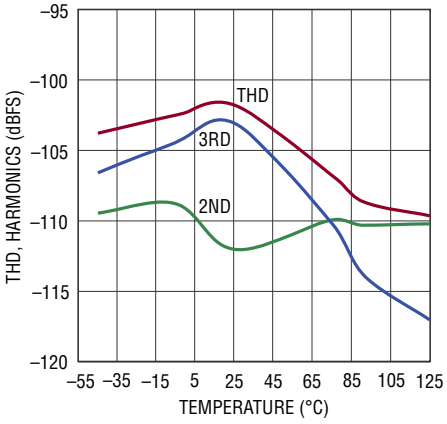
239116 G11

SNR, SINAD at f_{IN} = 20kHz vs Temperature



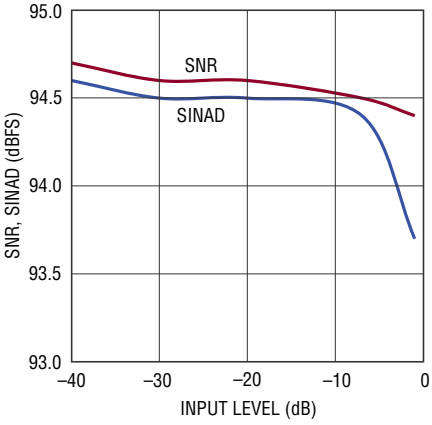
239116 G12

THD, Harmonics at f_{IN} = 20kHz vs Temperature



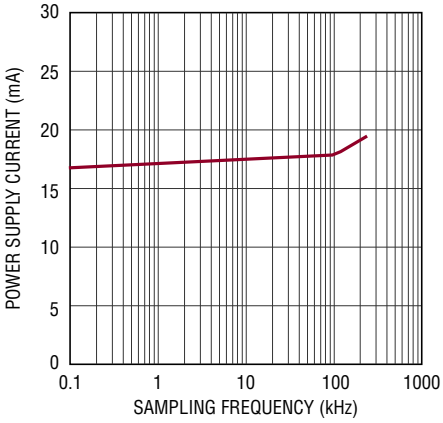
239116 G13

SNR, SINAD vs Input Level



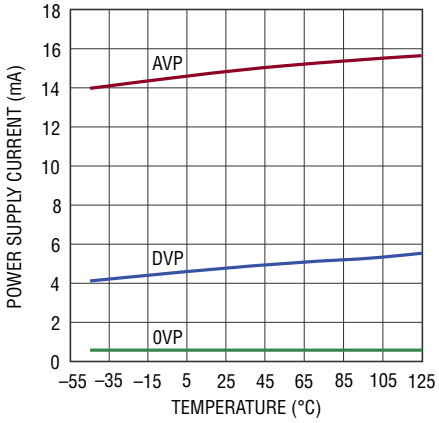
239116 G14

Supply Current vs Sampling Frequency



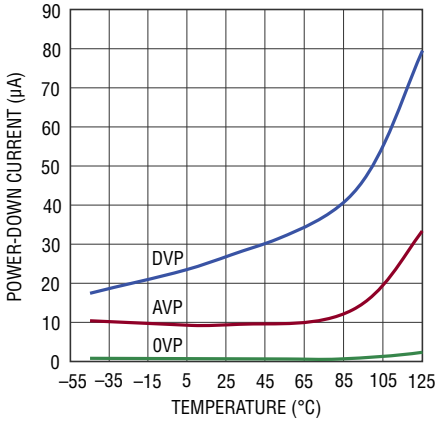
239116 G15

Supply Current vs Temperature



239116 G16

Power-Down Current vs Temperature



239116 G17

PIN FUNCTIONS

GND (Pins 1, 5, 7, 20, 35, 41, 44, 48, Exposed Pad Pin 49): Ground. All GND pins must be connected to a solid ground plane.

AVP (Pins 2, 40, 45, 46, 47): 5V Analog Power Supply. The range of AVP is 4.75V to 5.25V. Bypass AVP to GND with a good quality 0.1µF and a 10µF ceramic capacitor in parallel.

DVP (Pins 3, 19): 5V Digital Power Supply. The range of DVP is 4.75V to 5.25V. Bypass DVP to GND with a good quality 0.1µF and a 10µF ceramic capacitor in parallel.

SER/$\overline{\text{PAR}}$ (Pin 4): Serial/Parallel Selection Input. This pin controls the digital interface. A logic high on this pin selects the serial interface and a logic low selects the parallel interface. In the serial mode the non-active digital outputs are high impedance.

OB/$\overline{\text{2C}}$ (Pin 6): Offset Binary/Two's Complement Input. When OB/$\overline{\text{2C}}$ is high, the digital output is offset binary. When low, the MSB is inverted resulting in two's complement output.

BYTESWAP (Pin 8): BYTESWAP Input. With BYTESWAP low, data will be output with Pin 28 (D15) being the MSB and Pin 9 (D0) being the LSB. With BYTESWAP high, the upper eight bits and the lower eight bits will be switched. The MSB is output on Pin 16 and Bit 8 is output on Pin 9. Bit 7 is output on Pin 28 and the LSB is output on Pin 21.

D0 (Pin 9): Data Bit 0. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 0 of the parallel port data output bus.

D1 (Pin 10): Data Bit 1. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 1 of the parallel port data output bus.

D2 (Pin 11): Data Bit 2. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 2 of the parallel port data output bus.

D3 (Pin 12): Data Bit 3. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 3 of the parallel port data output bus.

D4 (Pin 13): Data Bit 4. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 4 of the parallel port data output bus.

D5 (Pin 14): Data Bit 5. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 5 of the parallel port data output bus.

D6 (Pin 15): Data Bit 6. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 6 of the parallel port data output bus.

D7 (Pin 16): Data Bit 7. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 7 of the parallel port data output bus.

OGND (Pin 17): Digital Ground for the Input/Output Interface.

OVP (Pin 18): Digital Power Supply for the Input/Output Interface. The range for OVP is 1.8V to 5V. Bypass OVP to OGND with a good quality 4.7µF ceramic capacitor close to the pin.

D8 (Pin 21): Data Bit 8. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 8 of the parallel port data output bus.

D9/SDIN (Pin 22): Data Bit 9/Serial Data Input. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 9 of the parallel port data output bus. When SER/$\overline{\text{PAR}}$ = 1, (serial mode) this is the serial data input. SDIN can be used as a data input to daisy chain two or more conversion results into a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 16 SCLK periods after the start of the read sequence.

D10/SDOUT (Pin 23): Data Bit 10/Serial Data Output. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 10 of the parallel port data output bus. When SER/$\overline{\text{PAR}}$ = 1, (serial mode) this is the serial data output. The conversion result can be clocked out serially on this pin synchronized to SCLK. The data is clocked out MSB first on the rising edge of SCLK and is valid on the falling edge of SCLK. The data format is determined by the logic level of OB/$\overline{\text{2C}}$.

D11/SCLK (Pin 24): Data Bit 11/Serial Clock Input. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 11 of the parallel port data output bus. When SER/$\overline{\text{PAR}}$ = 1, (serial mode) this is the serial clock input.

D12 (Pin 25): Data Bit 12. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 12 of the parallel port data output bus.

D13 (Pin 26): Data Bit 13. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 13 of the parallel port data output bus.

D14 (Pin 27): Data Bit 14. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 14 of the parallel port data output bus.

D15 (Pin 28): Data Bit 15. When SER/$\overline{\text{PAR}}$ = 0 this pin is Bit 15 of the parallel port data output bus. The data format is determined by the logic level of OB/$\overline{\text{2C}}$.

PIN FUNCTIONS

BUSY (Pin 29): Busy Output. A low-to-high transition occurs when a conversion is started. It stays high until the conversion is complete. The falling edge of BUSY can be used as the data-ready clock signal.

$\overline{RD}$ (Pin 30): Read Data Input. When $\overline{CS}$ and $\overline{RD}$ are both low, the parallel and serial output bus is enabled.

$\overline{CS}$ (Pin 31): Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both low, the parallel and serial output bus is enabled. $\overline{CS}$ is also used to gate the external shift clock.

RESET (Pin 32): Reset Input. When high the LTC2391-16 is reset, and if this occurs during a conversion, the conversion is halted and the data bus is put into Hi-Z mode.

PD (Pin 33): Power-Down Input. When high, the LTC2391-16 is powered down and subsequent conversion requests are ignored. Before entering power shutdown, the digital output data should be read.

$\overline{CNVST}$ (Pin 34): Conversion Start Input. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold mode and starts a conversion. $\overline{CNVST}$ is independent of $\overline{CS}$.

VCM (Pin 36): Common Mode Analog Output. Typically the output voltage is 2.048V. Bypass to GND with a 10µF capacitor.

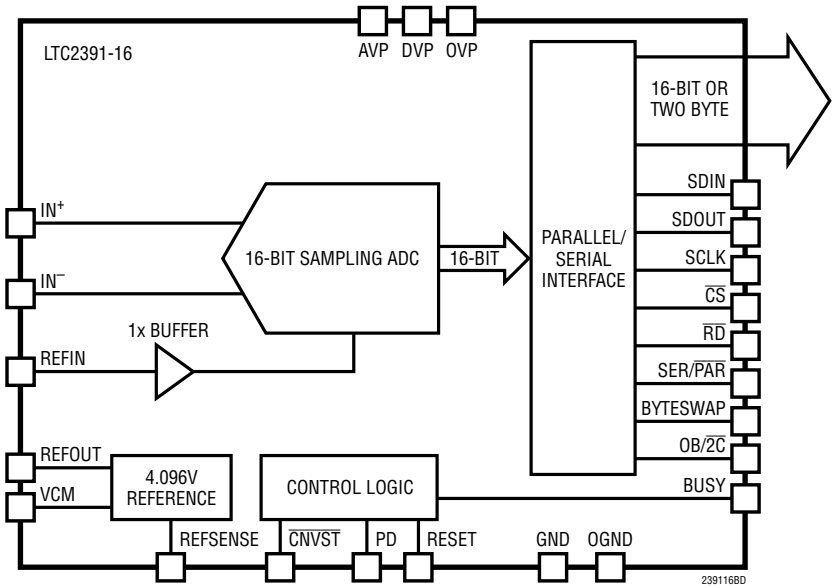
REFOUT (Pin 37): Internal Reference Output. Nominal output voltage is 4.096V. Connect this pin to REFIN if using the internal reference. If an external reference is used connect REFOUT to ground.

REFIN (Pin 38): Reference Input. An external reference can be applied to REFIN if a more accurate reference is required. If an external reference is used tie REFOUT to ground.

REFSENSE (Pin 39): Reference Input Sense. Leave REFSENSE open when using the internal reference. If an external reference is used connect REFSENSE to the ground pin of the external reference.

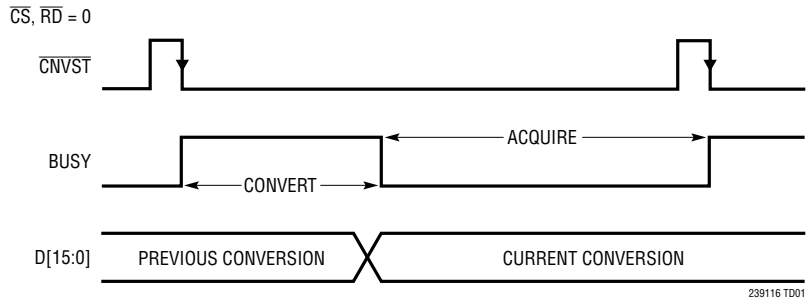
IN^-, IN^+ (Pin 42, Pin 43): Differential Analog Inputs. $IN^+ – (IN^-)$ can range up to $\pm V_{REF}$.

FUNCTIONAL BLOCK DIAGRAM

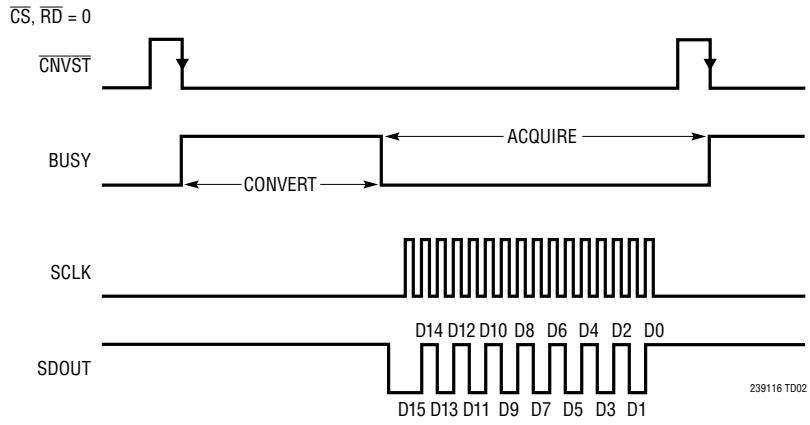


TIMING DIAGRAMS

Conversion Timing Using the Parallel Interface



Conversion Timing Using the Serial Interface



APPLICATIONS INFORMATION

OVERVIEW

The LTC2391-16 is a low noise, high speed 16-bit successive approximation register (SAR) ADC. Operating from a single 5V supply, the LTC2391-16 supports a large ±4.096V fully differential input range, making it ideal for high performance applications which require a wide dynamic range. The LTC2391-16 achieves ±2LSB INL max, no missing codes at 16 bits and 94dB SNR (typ).

The LTC2391-16 includes a precision internal reference with a guaranteed 0.5% initial accuracy and a ±20ppm/°C (max) temperature coefficient. Fast 250ksps throughput with no cycle latency in both parallel and serial interface modes makes the LTC2391-16 ideally suited for a wide variety of high speed applications. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2391-16 dissipates only 95mW at 250ksps, while both nap and sleep power-down modes are provided to further reduce power during inactive periods.

CONVERTER OPERATION

The LTC2391-16 operates in two phases. During the acquisition phase, the charge redistribution capacitor D/A converter (CDAC) is connected to the IN^+ and IN^- pins to sample the differential analog input voltage. A falling edge on the $\overline{CNVST}$ pin initiates a conversion. During the conversion phase, the 16-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REF}/2$, $V_{REF}/4$ … $V_{REF}/65536$) using the differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 16-bit digital output code for parallel or serial transfer.

TRANSFER FUNCTION

The LTC2391-16 digitizes the full-scale voltage of $2 \cdot V_{REF}$ into 2^{16} levels, resulting in an LSB size of 125µV when V_{REF} = 4.096V. The ideal transfer function for two's complement is shown in Figure 2. The OB/$\overline{2C}$ pin selects either offset binary or two's complement format.

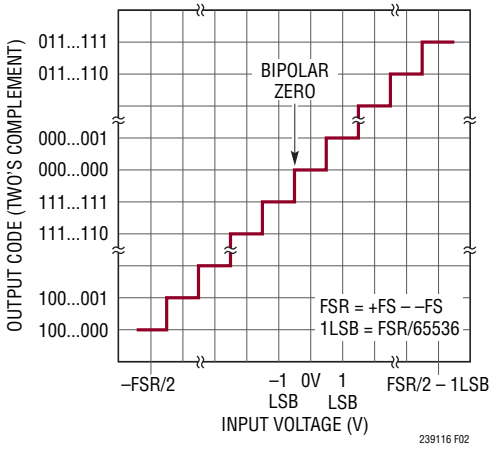


Figure 2. LTC2391-16 Two's Complement Transfer Function

ANALOG INPUT

The analog inputs of the LTC2391-16 are fully differential in order to maximize the signal swing that can be digitized. The analog inputs can be modeled by the equivalent circuit shown in Figure 3. The diodes at the input provide ESD protection. The analog inputs should not exceed the supply or go below ground. In the acquisition phase, each input sees approximately 40pF (C_{IN}) from the sampling CDAC in series with 50Ω (R_{IN}) from the on-resistance of the sampling switch. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC. The inputs draw only one small current spike while charging the C_{IN} capacitors during acquisition. During conversion, the analog inputs draw only a small leakage current.

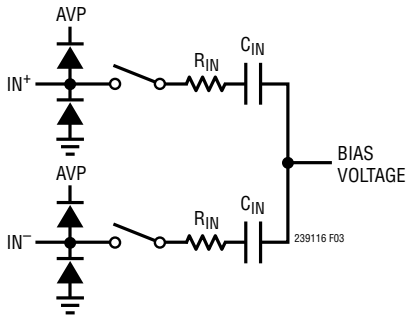


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2391-16

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2391-16 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2391-16. The amplifier provides low output impedance to allow for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs which draw a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and other circuitry must be considered since they add to the ADC noise and distortion. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

Large filter RC time constants slow down the settling at the analog inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle to 16-bit resolution within the acquisition time (t_{ACQ}).

High quality capacitors and resistors should be used in the RC filter since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Single-to-Differential Conversion

For single-ended input signals, a single-ended-to-differential conversion circuit must be used to produce a differential signal at the ADC inputs. The LT6350 ADC driver is recommended for performing a single-ended-to-differential conversion, as shown in Figure 4a. Its low noise and good DC linearity allows the LTC2391-16 to meet full data sheet specifications. An alternative solution using two op amps is shown in Figure 4b. Using two LT®1806 op amps, the circuit achieves 94dB signal-to-noise ratio (SNR). For a 20kHz input signal, the input of the LTC2391-16 has been bandwidth limited to about 25kHz.

ADC REFERENCE

A low noise, low temperature drift reference is critical to achieving the full data sheet performance of the ADC. The LTC2391-16 provides an excellent internal reference with a ±20ppm/°C (max) temperature coefficient. For better accuracy, an external reference can be used.

The high speed, low noise internal reference buffer is used for both internal and external reference applications. It cannot be bypassed.

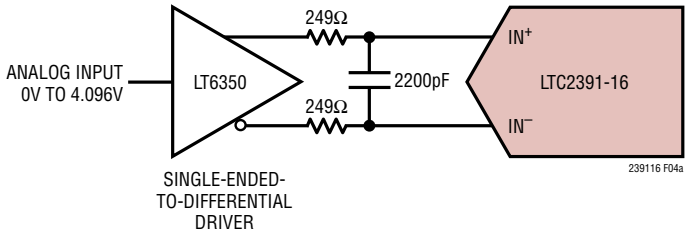


Figure 4a. Recommended Single-Ended-to-Differential Conversion Circuit Using the LT6350 ADC Driver

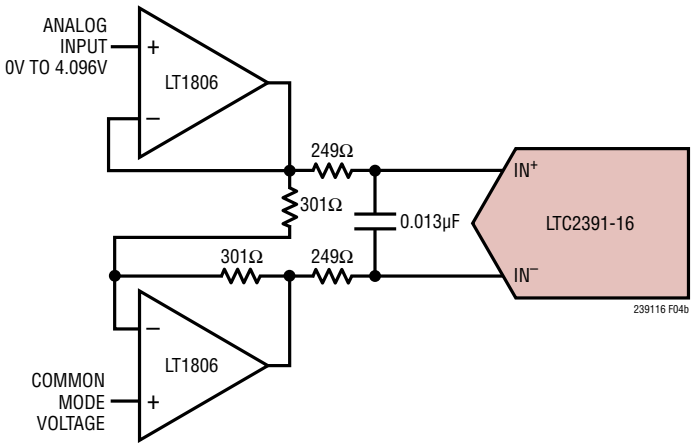


Figure 4b. Alternative Single-Ended-to-Differential Conversion Circuit Using Two LT1806 Op Amps

APPLICATIONS INFORMATION

Internal Reference

To use the internal reference, simply tie the REFOUT and REFIN pins together. This connects the 4.096V output of the internal reference to the input of the internal reference buffer. The output impedance of the internal reference is approximately 2.6kΩ and the input impedance of the internal reference buffer is about 85kΩ. It is recommended that this node be bypassed to ground with a 1µF or larger capacitor to filter the output noise of the internal reference. The REFSENSE pin should be left floating when using the internal reference.

External Reference

An external reference can be used with the LTC2391-16 when even higher performance is required. The LT1790-4.096 offers 0.05% (max) initial accuracy and 10ppm/°C (max) temperature coefficient. When using an external reference, connect the reference output to the REFIN pin and connect the REFOUT pin to ground. The REFSENSE pin should be connected to the ground of the external reference.

DYNAMIC PERFORMANCE

Fast fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2391-16 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies from above DC and below half the sampling frequency. Figure 5 shows that the LTC2391-16 achieves a typical SINAD of 93.5dB at a 250ksps sampling rate with a 20kHz input.

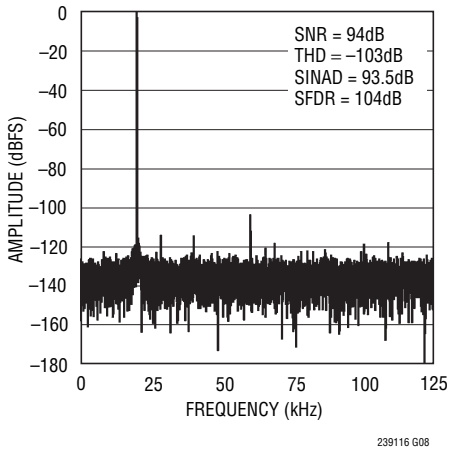


Figure 5. 16k Point FFT of the LTC2391-16, f_S = 250ksps, f_{IN} = 20kHz

APPLICATIONS INFORMATION

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 5 shows that the LTC2391-16 achieves a typical SNR of 94dB at a 250kHz sampling rate with a 20kHz input.

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2391-16 provides three sets of power supply pins: the analog 5V power supply (AVP), the digital 5V power supply (DVP) and the digital input/output interface power supply (OVP). The flexible OVP supply allows the LTC2391-16 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

Power Supply Sequencing

The LTC2391-16 does not have any specific power supply sequencing requirements. Care should be taken to observe the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2391-16 has a power-on reset (POR) circuit. With the POR, the result of the first conversion is valid after power has been applied to the ADC. The LTC2391-16 will reset itself if the power supply voltage drops below 2.5V. Once the supply voltage is brought back to its nominal value, the POR will reinitialize the ADC and it will be ready to start a new conversion.

Nap Mode

The LTC2391-16 can be put into the nap mode after a conversion has been completed to reduce the power consumption between conversions. In this mode some of the circuitry on the device is turned off. Nap mode is enabled by keeping $\overline{CNVST}$ low between conversions. When the next conversion is requested, bring $\overline{CNVST}$ high and hold for at least 250ns, then start the next conversion by bringing $\overline{CNVST}$ low. See Figure 6.

Power Shutdown Mode

When PD is tied high, the LTC2391-16 enters power shutdown and subsequent requests for conversion are ignored. Before entering power shutdown, the digital output data needs to be read. However, if a request for power shutdown (PD = high) occurs during a conversion, the conversion will finish and then the device will power down. The data from that conversion can be read after PD

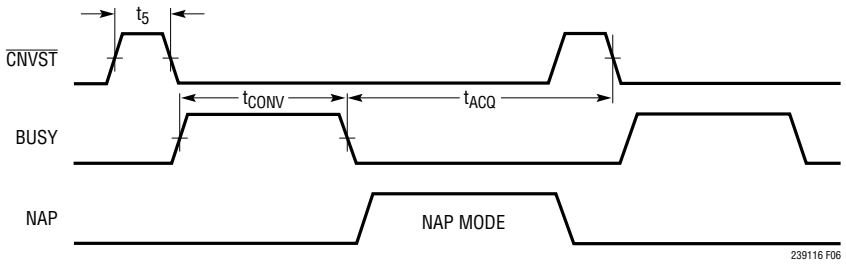


Figure 6. Nap Mode Timing for the LTC2391-16

APPLICATIONS INFORMATION

= low is applied. In this mode, power consumption drops to a typical value of 175µW from 95mW. This mode can be used if the LTC2391-16 is inactive for a long period of time and the user wants to minimize the power dissipation.

Recovery from Power Shutdown Mode

Once the PD pin is returned to a low level, ending the power shutdown request, the internal circuitry will begin to power up. If the internal reference is used, the 2.6kΩ output impedance with the 1µF bypass capacitor on the REFIN/REFOUT pins will be the main time constant for the power-on recovery time. If an external reference is used, typically allow 5ms for recovery before initiating a new conversion.

Power Dissipation vs Sampling Frequency

The power dissipation of the LTC2391-16 will decrease as the sampling frequency is reduced when nap mode is activated. See Figure 7. In nap mode, a portion of the circuitry on the LTC2391-16 is turned off after a conversion has been completed. Increasing the time allowed between conversions lowers the average power.

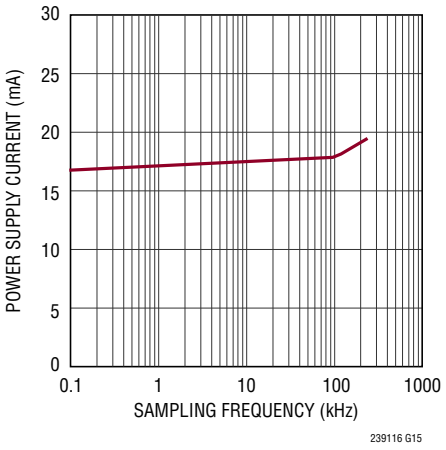


Figure 7. Power Dissipation of the LTC2391-16 Decreases with Decreasing Sampling Frequency

TIMING AND CONTROL

The LTC2391-16 conversion is controlled by $\overline{CNVST}$. A falling edge on $\overline{CNVST}$ will start a conversion. $\overline{CS}$ and $\overline{RD}$ control the digital interface on the LTC2391-16. When either $\overline{CS}$ or $\overline{RD}$ is high, the digital outputs are high impedance.

$\overline{CNVST}$ Timing

The LTC2391-16 conversion is controlled by $\overline{CNVST}$. A falling edge on $\overline{CNVST}$ will start a conversion. Once a conversion has been initiated, it cannot be restarted until the conversion is complete. For optimum performance $\overline{CNVST}$ should be a clean low jitter signal. Converter status is indicated by the BUSY output which remains high while the conversion is in progress. To ensure no errors occur in the digitized results return the rising edge either within 40ns from the start of the conversion or wait until after the conversion has been completed. The $\overline{CNVST}$ timing needed to take advantage of the reduced power mode of operation is described in the Nap Mode section.

Internal Conversion Clock

The LTC2391-16 has an internal clock that is trimmed to achieve a maximum conversion time of 2500ns. No external adjustments are required and with a maximum acquisition time of 1485ns, a throughput performance of 250ksps is guaranteed.

DIGITAL INTERFACE

The LTC2391-16 allows both parallel and serial digital interfaces. The flexible OVP supply allows the LTC2391-16 to communicate with any digital logic operating between 1.8V and 5V, including 2.5V and 3.3V systems.

APPLICATIONS INFORMATION

Parallel Modes

The parallel output data interface is active when the SER/$\overline{PAR}$ pin is tied low and when both $\overline{CS}$ and $\overline{RD}$ are low. The output data can be read as a 16-bit word as shown in Figures 8, 9 and 10 or it can be read as two 8-bit bytes by using the BYTESWAP pin. As shown in Figure 11, with the BYTESWAP pin low, the first eight MSBs are output on the D15 to D8 pins and the eight LSBs are output on the D7 to DO pins. When BYTESWAP is taken high, the eight LSBs now are output on the D15 to D8 pins and the eight MSBs are output on the D7 to D0 pins.

Serial Modes

The serial output data interface is active when the SER/$\overline{PAR}$ pin is tied high and when both $\overline{CS}$ and $\overline{RD}$ are low. The serial output data will be clocked out on the SDOUT pin when an external clock is applied to the SCLK pin. Clocking out the data after the conversion will yield the best performance. With a shift clock frequency of at least 15MHz, a 250ksps throughput is achieved. The serial output data changes state on the rising edge of SCLK and can be captured on the falling edge of SCLK. D15 remains valid till the first rising edge of shift clock after the first falling edge of shift clock. The non-active digital outputs are high impedance when operating in the serial mode.

If $\overline{CS}$ and $\overline{RD}$ are used to gate the serial output data, the full conversion result should be read before $\overline{CS}$ and $\overline{RD}$ are returned to a high level.

The SDIN input pin is used to daisy chain multiple converters. This is useful for applications where hardware constraints may limit the number of lines needed to interface to a large number of converters. For example, if two devices are cascaded, the MSB of the first device will appear at the output after 17 SCLK cycles. The first MSB is clocked in on the falling edge of the first SCLK. See Figure 12.

Data Format

When OB/$\overline{2C}$ is high, the digital output is offset binary. When low, the MSB is inverted resulting in two's complement output. This pin is active in both the parallel and serial modes of operation.

Reset

When the RESET pin is high, the LTC2391-16 is reset, and if this occurs during a conversion, the conversion is halted and the data bus is put into Hi-Z mode. In reset, requests for new conversions are ignored. Once RESET returns low, the LTC2391-16 is ready to start a new conversion after the acquisition time plus 2µs has been met. See Figure 13.

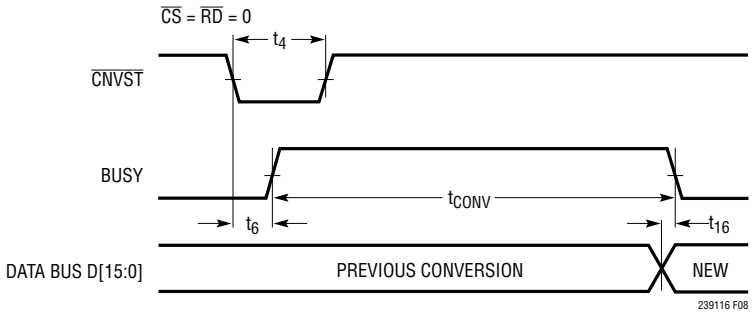


Figure 8. Read the Parallel Data Continuously. The Data Bus is Always Driven and Can't Be Shared

APPLICATIONS INFORMATION

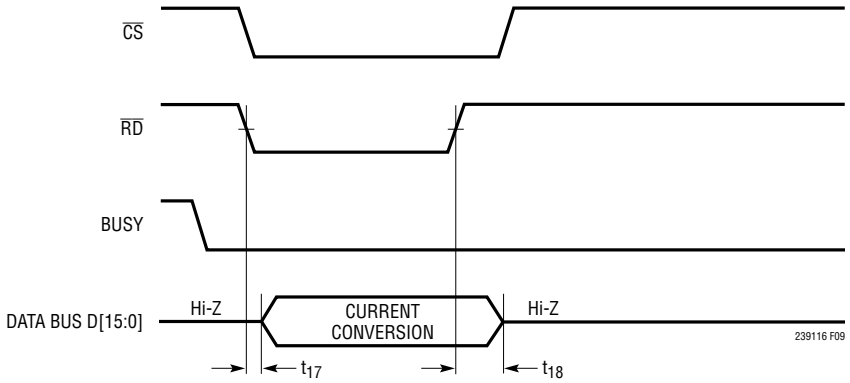


Figure 9. Read the Parallel Data After the Conversion

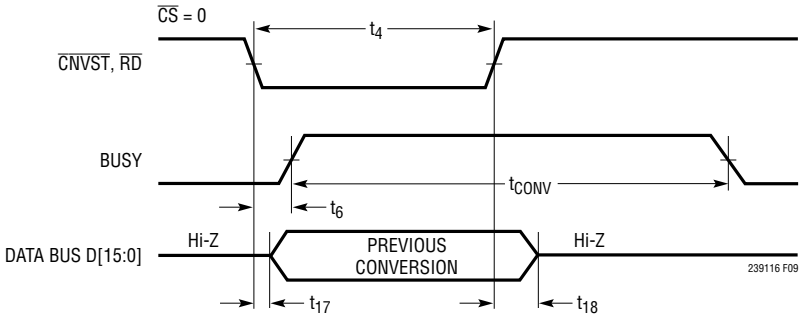


Figure 10. Read the Parallel Data During the Conversion

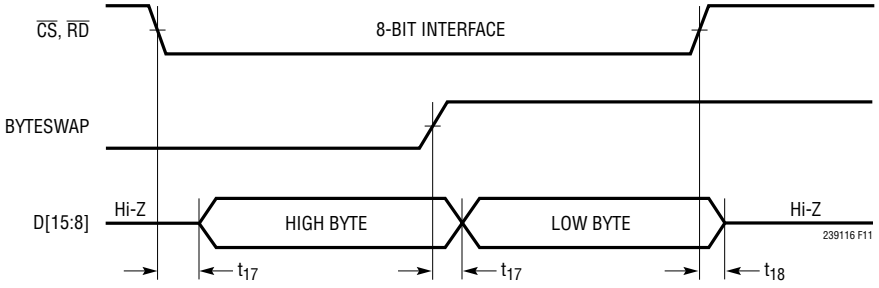


Figure 11. 8-Bit Parallel Interface Using the BYTESWAP Pin

APPLICATIONS INFORMATION

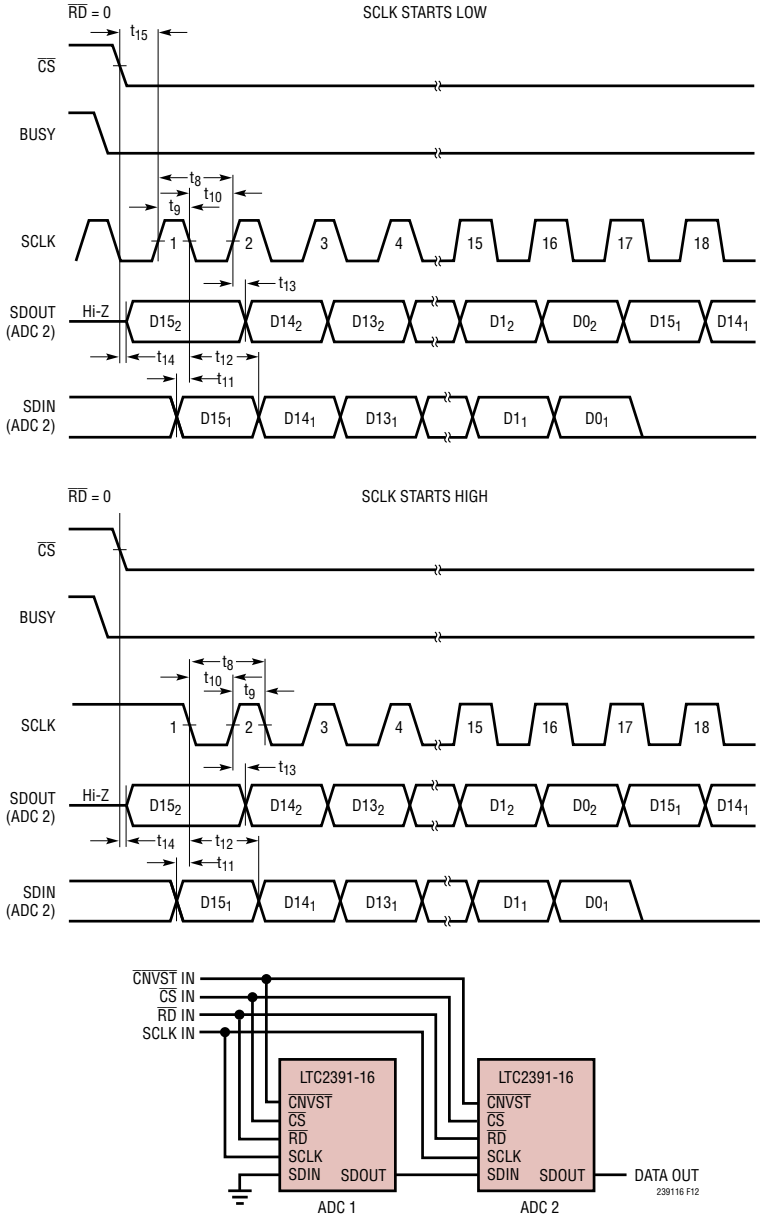


Figure 12. Serial Interface with External Clock. Read After the Conversion. Daisy Chain Multiple Converters

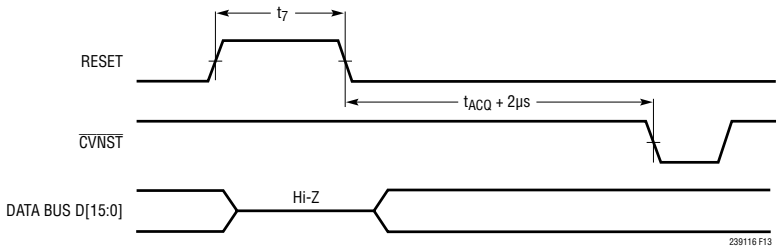


Figure 13. RESET Pin Timing

APPLICATIONS INFORMATION

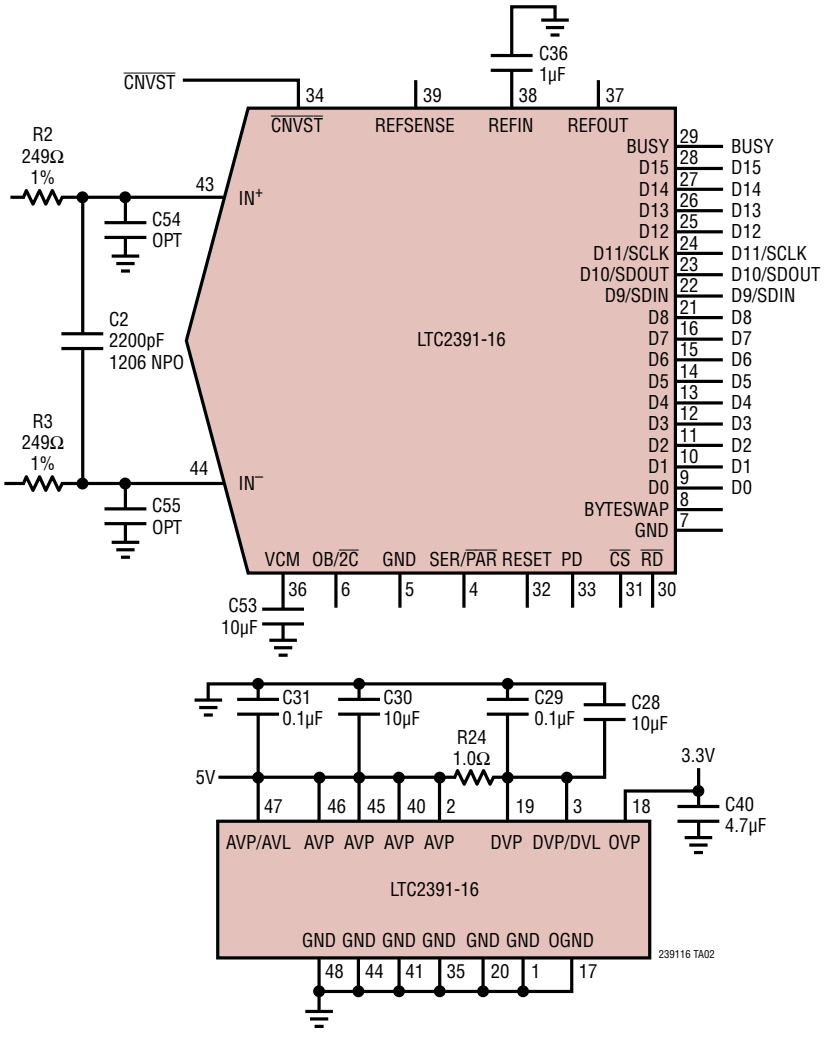
BOARD LAYOUT

To obtain the best performance from the LTC2391-16, a printed circuit board (PCB) is recommended. Layout for the printed circuit board should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC.

Recommended Layout

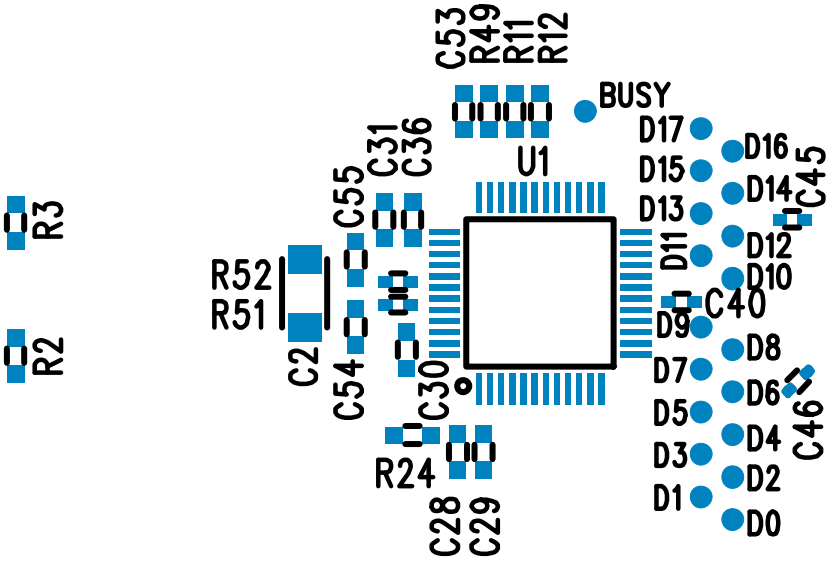
The following is an example of a recommended PCB layout. A single solid ground plane is used. Bypass capacitors to the supplies are placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. The analog input traces are screened by ground. For more details and information refer to DC1500A, the evaluation kit for the LTC2391-16

Partial Schematic of Demoboard

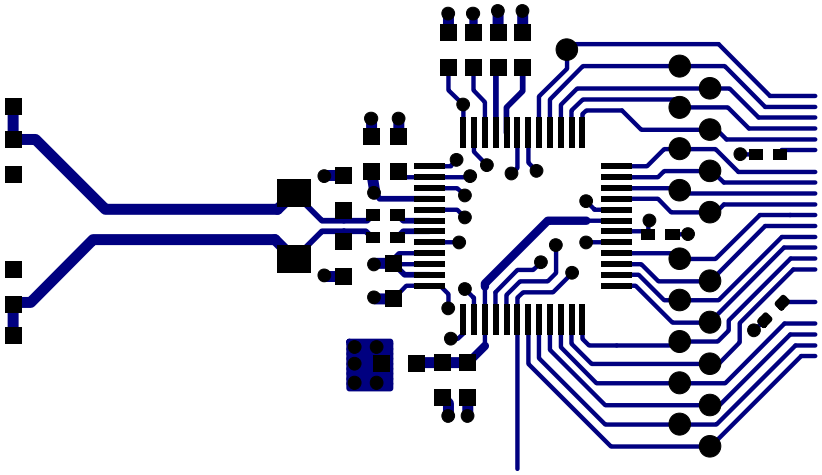


APPLICATIONS INFORMATION

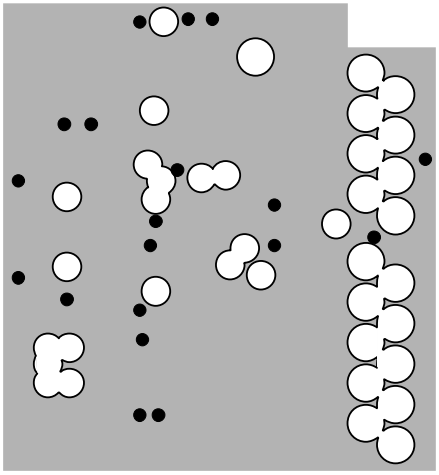
Partial Top Silkscreen



Partial Layer 1 Component Side



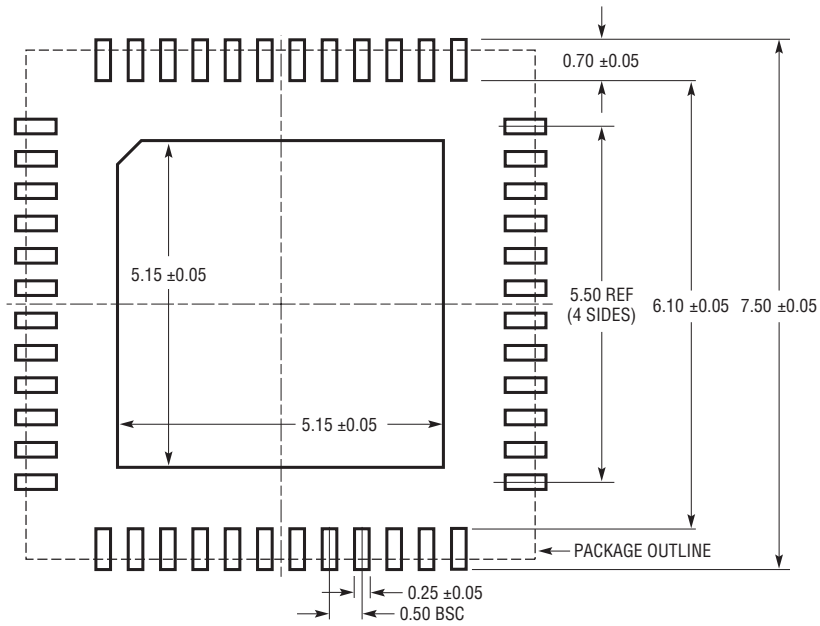
Partial Layer 2 Ground Plane



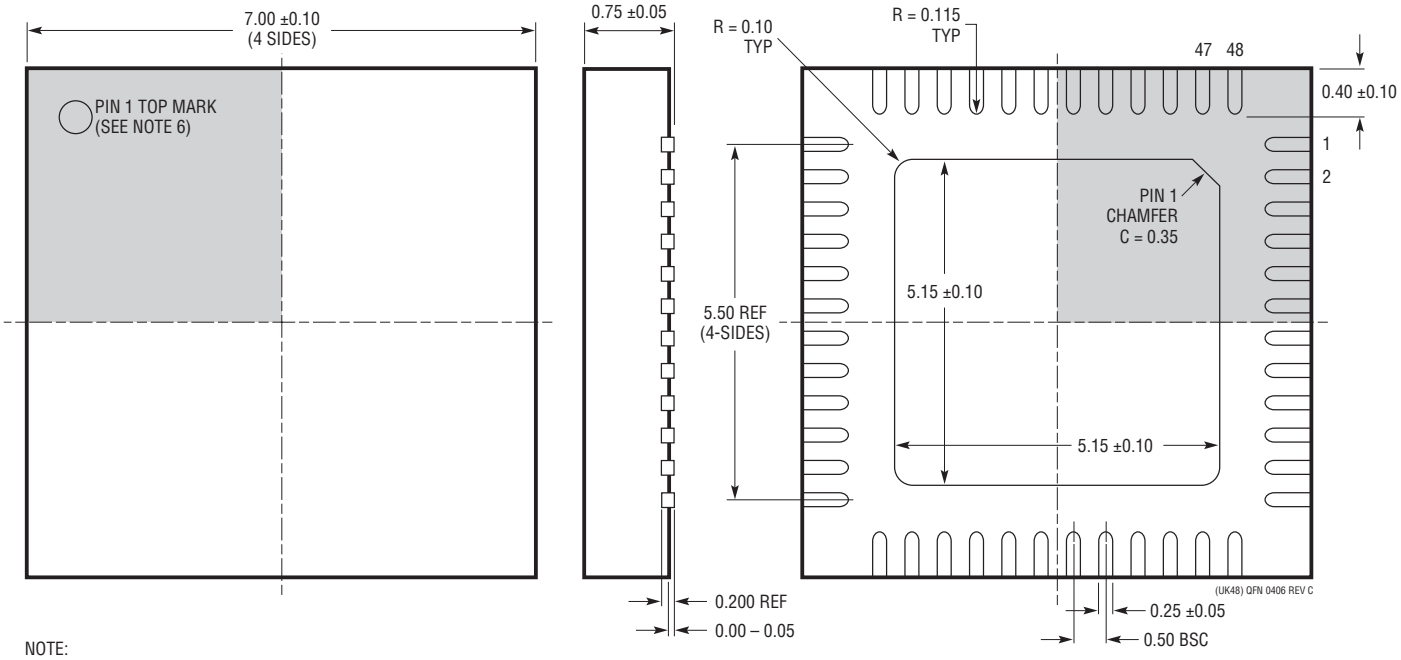
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



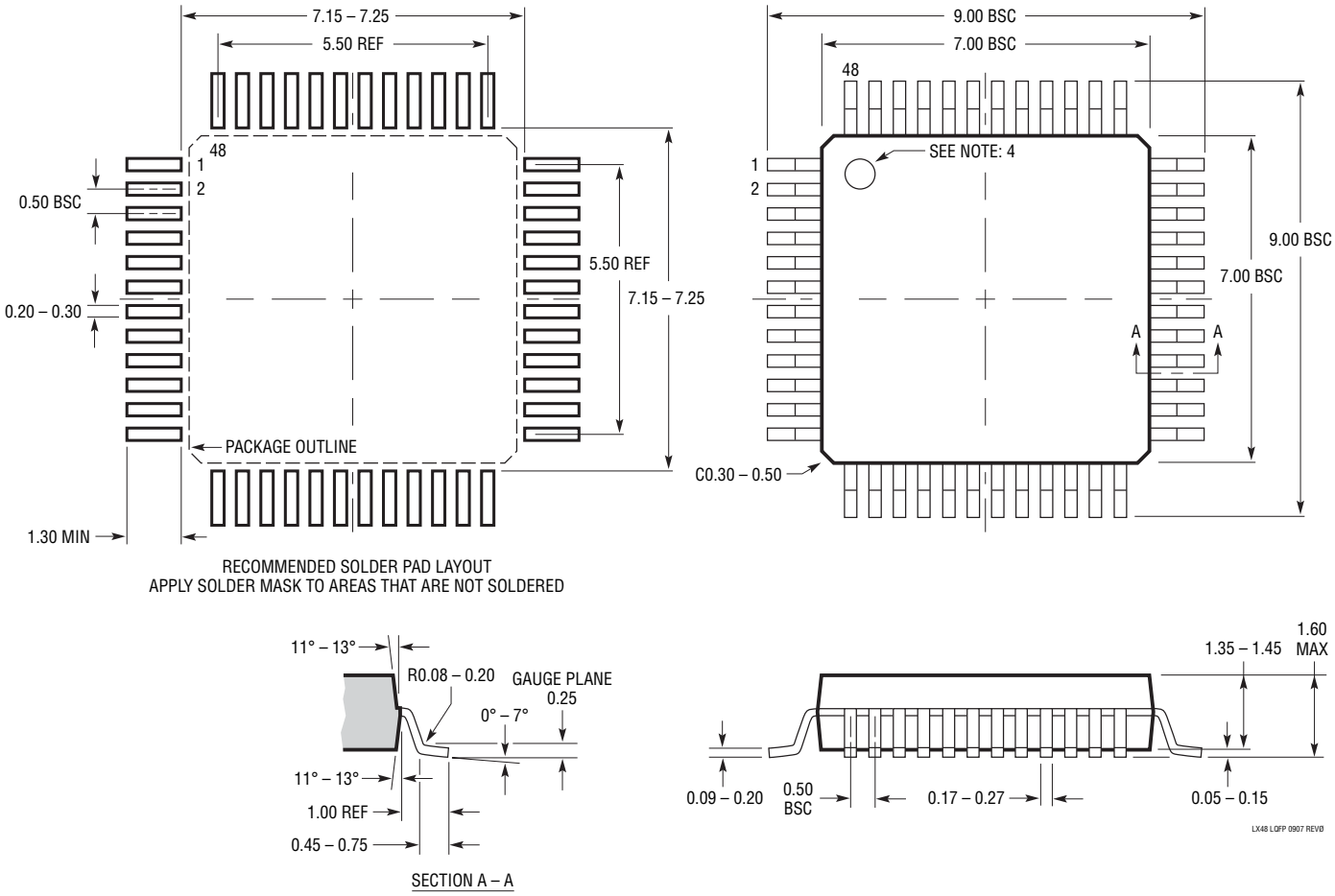
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LX Package
48-Lead Plastic LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1760 Rev Ø)



NOTE:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC #MS-026 PACKAGE OUTLINE
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
4. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
5. DRAWING IS NOT TO SCALE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	7/12	Increased T_{JMAX} to 150°C on LQFP package	2
		Added condition for reading conversion result under Serial Modes	16
		Added plus 2µs to acquisition time in Reset section and Fig 13	16, 18
		Updated data bit numbering on Figure 12	18