3.3V Software-Selectable Multiprotocol Transceiver

FEATURES

- **Software-Selectable Transceiver Supports: RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21**
- **Operates from Single 3.3V Supply with LTC2846 or a Single 5V Supply with 3.3V Logic with LTC2847**
- TUV Rheinland of North America Inc. Certified NET1, NET2 and TBR2 Compliant, Report No.: TBR2/050101/02
- Complete DTE or DCE Port with LTC2846 or LTC2847
- Available in a 36-Lead Narrow (0.209") SSOP and 38-Lead (7mm x 5mm) QFN package

APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

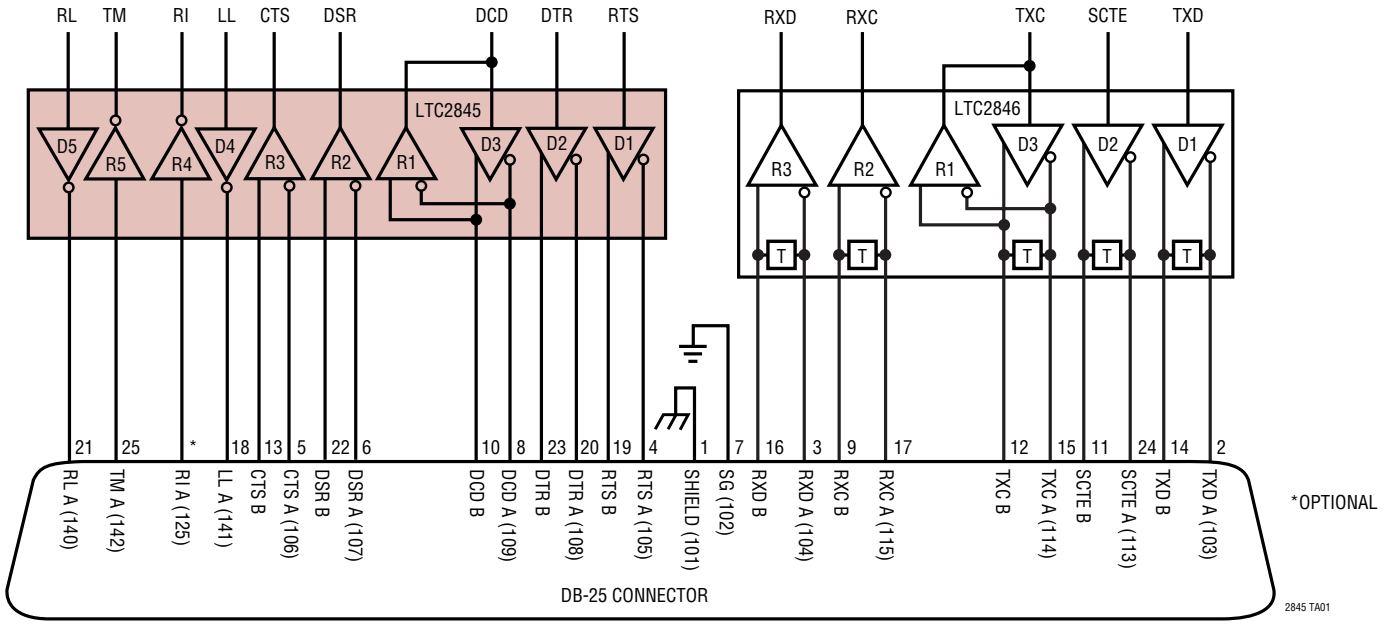
DESCRIPTION

The LTC®2845 is a 5-driver/5-receiver multiprotocol transceiver. The LTC2845 and LTC2846 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols.

The LTC2845 operates from a 3.3V supply and supplies provided by the LTC2846. This part is available in a 36-lead SSOP and 38-lead (7mm x 5mm) QFN package. The LTC2845 and LTC2847 in QFN packages offer the smallest multiprotocol serial port available.

TYPICAL APPLICATION

DTE or DCE Multiprotocol Serial Interface with DB-25 Connector



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- V_{CC} ..... –0.3V to 6.5V
- V_{IN} ..... –0.3V to 6.5V
- V_{EE} ..... –10V to 0.3V
- V_{DD} ..... –0.3V to 10V

Input Voltage
- Transmitters ..... –0.3V to (V_{CC} + 0.3V)
- Receivers ..... –18V to 18V
- Logic Pins ..... –0.3V to (V_{CC} + 0.3V)

Output Voltage
- Transmitters ..... (V_{EE} – 0.3V) to (V_{DD} + 0.3V)
- Receivers ..... –0.3V to (V_{IN} + 0.3V)

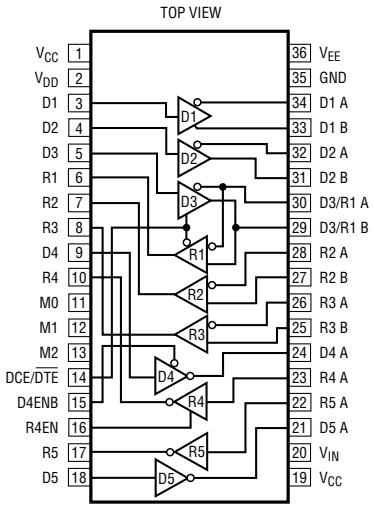
Short-Circuit Duration
- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite
- V_{EE} ..... 30 sec

Operating Temperature Range
- LTC2845C ..... 0°C to 70°C
- LTC2845I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

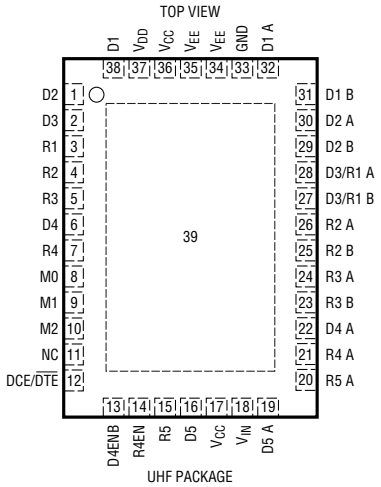


G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 90°C/W, θ_{JC} = 35°C/W

ORDER PART NUMBER

LTC2845CG
LTC2845IG



UHF PACKAGE
38-LEAD (7mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD IS V_{EE} (PIN 39)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LTC2845CUHF
LTC2845IUHF

UHF PART MARKING

2845
2845I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{IN} = 3.3V, V_{DD} = 8V, V_{EE} = – 7V for V.28, –5.5V for V.10, V.11 (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	V_{CC} Supply Current (DCE Mode, All Digital Pins = GND or V_{IN})	RS530, RS530-A, X.21 Modes, No Load			2.7		mA
		RS530, RS530-A, X.21 Modes, Full Load	●		110	150	mA
		V.28 Mode, No Load	●		1	3	mA
		V.28 Mode, Full Load	●		1	3	mA
		No-Cable Mode	●		700	1400	µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{IN} = 3.3V, V_{DD} = 8V, V_{EE} = – 7V for V.28, – 5.5V for V.10, V.11 (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{EE}	V_{EE} Supply Current (DCE Mode, All Digital Pins = GND or V_{IN})	RS530, RS530-A, X.21 Modes, No Load RS530, X.21 Modes, Full Load RS530-A, Full Load V.28 Mode, No Load V.28 Mode, Full Load No-Cable Mode			2 23 34 1 12 10		mA mA mA mA mA µA
I_{DD}	V_{DD} Supply Current (DCE Mode, All Digital Pins = GND or V_{IN})	RS530, RS530-A, X.21 Modes, No Load RS530, RS530-A, X.21 Modes, Full Load V.28 Mode, No Load V.28 Mode, Full Load No-Cable Mode			0.3 0.3 1 13.5 10		mA mA mA mA µA
I_{VIN}	V_{IN} Supply Current (DCE Mode, All Digital Pins = GND or V_{IN})	All Modes Except No-Cable Mode			650		µA
P_D	Internal Power Dissipation (DCE Mode, All Digital Pins = GND or V_{IN})	RS530, RS530-A, X.21 Modes, Full Load V.28 Mode, Full Load			240 64		mW mW
Logic Inputs and Outputs							
V_{IH}	Logic Input High Voltage		●	2			V
V_{IL}	Logic Input Low Voltage	V_{CC} = 5V R4EN when V_{CC} = 3.3V	● 			0.8 0.5	V V
I_{IN}	Logic Input Current	D1, D2, D3, D4, D5 M0, M1, M2, DCE, D4ENB, R4EN = GND M0, M1, M2, DCE, D4ENB, R4EN = V_{IN}	● ● ●	 –30 	 –75 	±10 –120 ±10	µA µA µA
V_{OH}	Output High Voltage	I_O = –3mA	●	2.7	3		V
V_{OL}	Output Low Voltage	I_O = 1.6mA	●		0.2	0.4	V
I_{OSR}	Output Short-Circuit Current	0V ≤ V_O ≤ V_{IN}	●			±50	mA
I_{OZR}	Three-State Output Current	M0 = M1 = M2 = V_{IN}, V_O = GND M0 = M1 = M2 = V_{IN}, V_O = V_{IN}	● ●	–30 	–85 	–160 ±10	µA µA
V.11 Driver							
V_{ODO}	Open Circuit Differential Output Voltage	R_L = 1.95k (Figure 1)	●			±5	V
V_{ODL}	Loaded Differential Output Voltage	R_L = 50Ω (Figure 1)	 ●	0.5V_{ODO} ±2		0.67V_{ODO}	V V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			3	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	R_L = 50Ω (Figure 1)	●			0.2	V
I_{SS}	Short-Circuit Current	V_{OUT} = GND				±150	mA
I_{OZ}	Output Leakage Current	–0.25V ≤ V_O ≤ 0.25V, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
t_r, t_f	Rise or Fall Time	LTC2845C (Figures 2, 5) LTC2845I (Figures 2, 5)	● ●	2 2	15 15	25 35	ns ns
t_{PLH}	Input to Output	LTC2845C (Figures 2, 5) LTC28451 (Figures 2, 5)	● ●	20 20	40 40	65 75	ns ns
t_{PHL}	Input to Output	LTC2845C (Figures 2, 5) LTC2845I (Figures 2, 5)	● ●	20 20	40 40	65 75	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	LTC2845C (Figures 2, 5) LTC2845I (Figures 2, 5)	● ●	0 0	3 3	12 17	ns ns
t_{SKEW}	Output to Output Skew	(Figures 2, 5)			3		ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{IN} = 3.3V, V_{DD} = 8V, V_{EE} = – 7V for V.28, – 5.5V for V.10, V.11 (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V.11 Receiver							
V_{TH}	Input Threshold Voltage	$-7V \le V_{CM} \le 7V$	●	–0.2		0.2	V
ΔV_{TH}	Input Hysteresis	$-7V \le V_{CM} \le 7V$	●		15	40	mV
I_{IN}	Input Current (A, B)	$-10V \le V_{A,B} \le 10V$	●			±0.66	mA
R_{IN}	Input Impedance	$-10V \le V_{A,B} \le 10V$	●	15	30		kΩ
t_r, t_f	Rise or Fall Time	(Figures 2, 6)			15		ns
t_{PLH}	Input to Output	LTC2845C C_L = 50pF (Figures 2, 6) LTC2845I C_L = 50pF (Figures 2, 6)	● ●		50 50	80 90	ns ns
t_{PHL}	Input to Output	LTC2845C C_L = 50pF (Figures 2, 6) LTC2845I C_L = 50pF (Figures 2, 6)	● ●		50 50	80 90	ns ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	LTC2845C C_L = 50pF (Figures 2, 6) LTC2845I C_L = 50pF (Figures 2, 6)	● ●	0 0	4 4	16 21	ns ns
V.10 Driver							
V_O	Output Voltage	Open Circuit, R_L = 3.9k	●	±4		±6	V
V_T	Output Voltage	R_L = 450Ω (Figure 3) R_L = 450Ω (Figure 3)	●	±3.6 $0.9V_O$			V
I_{SS}	Short-Circuit Current	V_O = GND				±150	mA
I_{OZ}	Output Leakage Current	$-0.25V \le V_O \le 0.25V$, Power Off or No-Cable Mode or Driver Disabled	●		±0.1	±100	µA
t_r, t_f	Rise or Fall Time	R_L = 450Ω, C_L = 100pF (Figures 3, 7)			2		µs
t_{PLH}	Input to Output	R_L = 450Ω, C_L = 100pF (Figures 3, 7)			1		µs
t_{PHL}	Input to Output	R_L = 450Ω, C_L = 100pF (Figures 3, 7)			1		µs
V.10 Receiver							
V_{TH}	Receiver Input Threshold Voltage		●	–0.25		0.25	V
ΔV_{TH}	Receiver Input Hysteresis		●		25	50	mV
I_{IN}	Receiver Input Current	$-10V \le V_A \le 10V$	●			±0.66	mA
R_{IN}	Receiver Input Impedance	$-10V \le V_A \le 10V$	●	15	30		kΩ
t_r, t_f	Rise or Fall Time	C_L = 50pF (Figures 4, 8)			15		ns
t_{PLH}	Input to Output	C_L = 50pF (Figures 4, 8)			55		ns
t_{PHL}	Input to Output	C_L = 50pF (Figures 4, 8)			109		ns
Δt	Input to Output Difference, $\lvert t_{PLH} - t_{PHL} \rvert$	C_L = 50pF (Figures 4, 8)			60		ns
V.28 Driver							
V_O	Output Voltage	Open Circuit R_L = 3k (Figure 3)	● ●	 ±5	 ±8.5	±10	V V
I_{SS}	Short-Circuit Current	V_O = GND	●			±150	mA
I_{OZ}	Output Leakage Current	$-0.25V \le V_O \le 0.25V$, Power Off or No-Cable Mode or Driver Disabled	●		±1	±100	µA
SR	Slew Rate	R_L = 3k, C_L = 2500pF (Figures 3, 7)	●	4		30	V/µs
t_{PLH}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 3, 7)	●		1.3	2.5	µs
t_{PHL}	Input to Output	R_L = 3k, C_L = 2500pF (Figures 3, 7)	●		1.3	2.5	µs

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{IN} = 3.3V, V_{DD} = 8V, V_{EE} = –7V for V.28, –5.5V for V.10, V.11 (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V.28 Receiver							
V_{THL}	Input Low Threshold Voltage		●			0.8	V
V_{TLH}	Input High Threshold Voltage		●	2			V
ΔV_{TH}	Receiver Input Hysterisis		●		0.1	0.3	V
R_{IN}	Receiver Input Impedance	$-15V \le V_A \le 15V$	●	3	5	7	kΩ
t_r, t_f	Rise or Fall Time	C_L = 50pF (Figures 4, 8)			15		ns
t_{PLH}	Input to Output	C_L = 50pF (Figures 4, 8)	●		60	100	ns
t_{PHL}	Input to Output	C_L = 50pF (Figures 4, 8)	●		150	500	ns

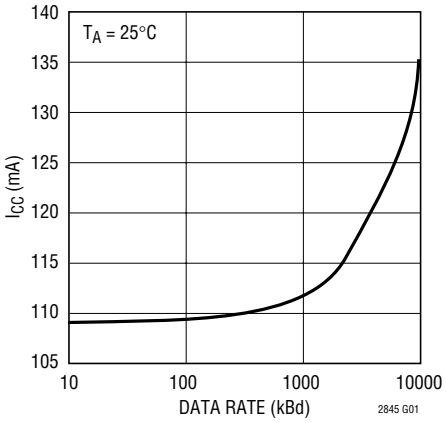
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

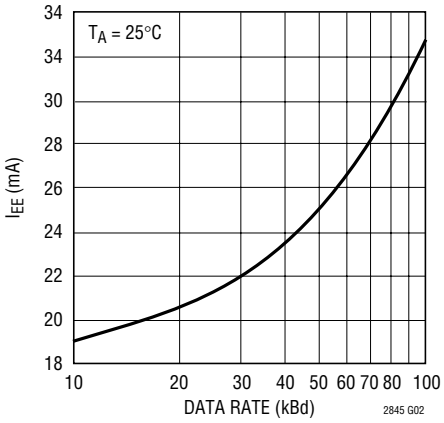
Note 3: All typicals are given for V_{CC} = 5V, V_{IN} = 3.3V, V_{DD} = 8V, V_{EE} = –7V for V.28, –5.5V for V.10, V.11 and T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

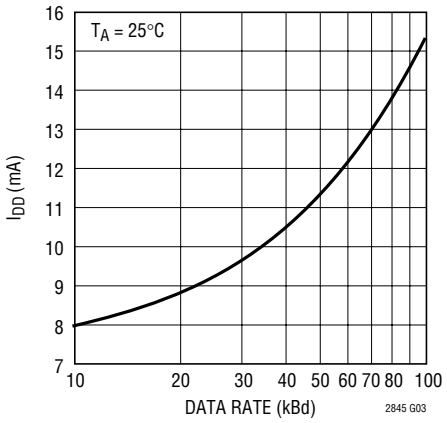
RS530, X.21 in DCE Mode (Three V.11, Two V.10 Drivers with Full Load) I_{CC} vs Data Rate



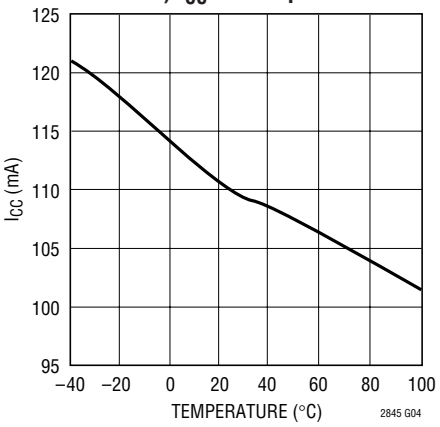
RS530-A in DCE Mode (Three V.10 Drivers with Full Load) I_{EE} vs Data Rate



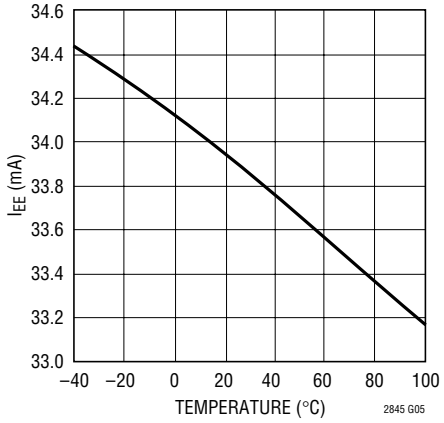
V.28 in DCE Mode (Five V.28 Drivers with Full Load) I_{DD} vs Data Rate



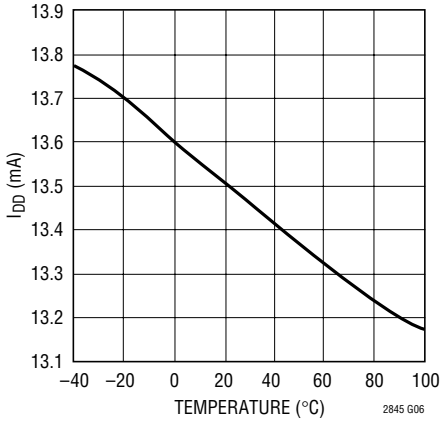
RS530, X.21 in DCE Mode (Three V.11, Two V.10 Drivers with Full Load) I_{CC} vs Temperature



RS530-A in DCE Mode (Three V.10 Drivers with Full Load) I_{EE} vs Temperature



V.28 in DCE Mode (Five V.28 Drivers with Full Load) I_{DD} vs Temperature



PIN FUNCTIONS (G-36/QFN-38 Packages)

V_{CC} (Pins 1, 19/Pins 17, 36): Positive Supply for the Transceivers. Connect to V_{CC} Pin 8 on LTC2846 or to 5V supply. Connect a 1µF capacitor to ground.

V_{DD} (Pin 2/Pin 37): Positive Supply Voltage for V.28. Connect to V_{DD} Pin 7 on LTC2846 or 8V supply. Connect a 1µF capacitor to ground.

D1 (Pin 3/Pin 38): TTL Level Driver 1 Input.

D2 (Pin 4/Pin 1): TTL Level Driver 2 Input.

D3 (Pin 5/Pin 2): TTL Level Driver 3 Input.

R1 (Pin 6/Pin 3): CMOS Level Receiver 1 Output. Receiver outputs have a weak pull up to V_{IN} when high impedance.

R2 (Pin 7/Pin 4): CMOS Level Receiver 2 Output.

R3 (Pin 8/Pin 5): CMOS Level Receiver 3 Output.

D4 (Pin 9/Pin 6): TTL Level Driver 4 Input.

R4 (Pin 10/Pin 7): CMOS Level Receiver 4 Output.

M0 (Pin 11/Pin 8): TTL Level Mode Select Input 0. Mode select inputs pull up to V_{IN}.

M1 (Pin 12/Pin 9): TTL Level Mode Select Input 1.

M2 (Pin 13/Pin 10): TTL Level Mode Select Input 2.

DCE/$\overline{\text{DTE}}$ (Pin 14/Pin 12): TTL Level Mode Select Input. Logic high enables Driver 3. Logic low enables Receiver 1.

D4ENB (Pin 15/Pin 13): TTL Level Enable Input. Logic low enables Driver 4. Pulls up to V_{IN}.

R4EN (Pin 16/Pin 14): TTL Level Enable Input. Logic high enables Receiver 4. Pulls up to V_{IN}.

R5 (Pin 17/Pin 15): CMOS Level Receiver 5 Output.

D5 (Pin 18/Pin 16): TTL Level Driver 5 Input.

V_{IN} (Pin 20/Pin 18): Positive Supply for the Receiver Outputs. $3V \leq V_{IN} \leq 3.6V$. Connect a 1µF capacitor to ground.

D5 A (Pin 21/Pin 19): Driver 5 Inverting Output.

R5 A (Pin 22/Pin 20): Receiver 5 Inverting Input.

R4 A (Pin 23/Pin 21): Receiver 4 Inverting Input.

D4 A (Pin 24/Pin 22): Driver 4 Inverting Input.

R3 B (Pin 25/Pin 23): Receiver 3 Noninverting Input.

R3 A (Pin 26/Pin 24): Receiver 3 Inverting Input.

R2 B (Pin 27/Pin 25): Receiver 2 Noninverting Input.

R2 A (Pin 28/Pin 26): Receiver 2 Inverting Input.

D3/R1 B (Pin 29/Pin 27): Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

D3/R1 A (Pin 30/Pin 28): Receiver 1 Inverting Input and Driver 3 Inverting Output.

D2 B (Pin 31/Pin 29): Driver 2 Noninverting Output.

D2 A (Pin 32/Pin 30): Driver 2 Inverting Output.

D1 B (Pin 33/Pin 31): Driver 1 Noninverting Output.

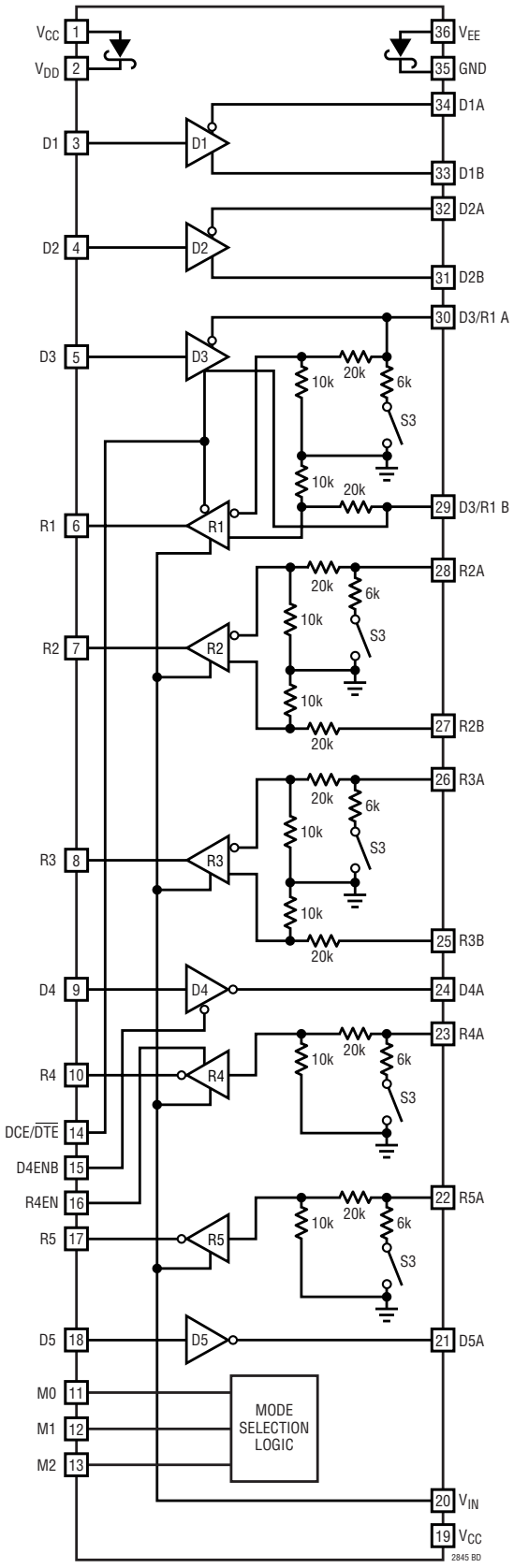
D1 A (Pin 34/Pin 32): Driver 1 Inverting Output.

GND (Pin 35/Pin 33): Ground.

V_{EE} (Pin 36/Pins 34, 35): Negative Supply Voltage. Connect to V_{EE} Pin 31 on LTC2846 or to –7V supply. Connect a 1µF capacitor to ground.

EXPOSED Pad V_{EE} (Pin 39): Must be Soldered to PCB.

BLOCK DIAGRAM



TEST CIRCUITS

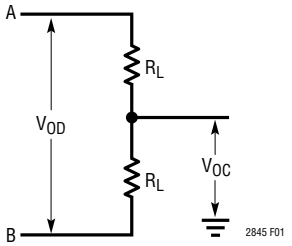


Figure 1. V.11 Driver Test Circuit

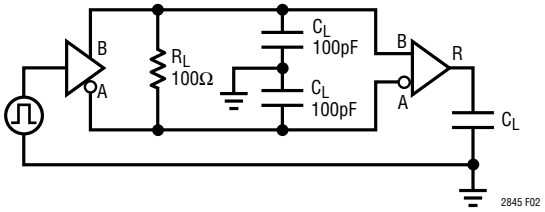


Figure 2. V.11 Driver/Receiver AC Test Circuit

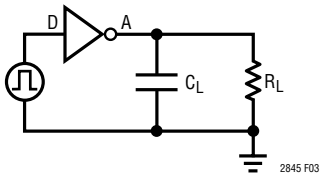


Figure 3. V.10/V.28 Driver Test Circuit

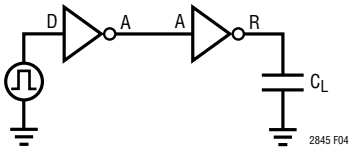


Figure 4. V.10/V.28 Receiver Test Circuit

MODE SELECTION

MODE NAME	M2	M1	M0	DCE /$\overline{\text{DTE}}$	(Note 1) (Note 4) D1, D2, D4, D5	(Note 1) D3	D1		D2		D3		(Note 4) D4A D5A
							A	B	A	B	A	B	
Not Used (Default V.11)	0	0	0	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.10
RS530A	0	0	1	0	TTL	X	V.11	V.11	V.10	Z	Z	Z	V.10
RS530	0	1	0	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.10
X.21	0	1	1	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.10
V.35	1	0	0	0	TTL	X	V.28	Z	V.28	Z	Z	Z	V.28
RS449/V.36	1	0	1	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.10
V.28/RS232	1	1	0	0	TTL	X	V.28	Z	V.28	Z	Z	Z	V.28
No Cable	1	1	1	0	X	X	Z	Z	Z	Z	Z	Z	Z
Not Used (Default V.11)	0	0	0	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	V.10
RS530A	0	0	1	1	TTL	TTL	V.11	V.11	V.10	Z	V.11	V.11	V.10
RS530	0	1	0	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	V.10
X.21	0	1	1	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.35	1	0	0	1	TTL	TTL	V.28	Z	V.28	Z	V.28	Z	V.28
RS449/V.36	1	0	1	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.28/RS232	1	1	0	1	TTL	TTL	V.28	Z	V.28	Z	V.28	Z	V.28
No Cable	1	1	1	1	X	X	Z	Z	Z	Z	Z	Z	Z

MODE NAME	M2	M1	M0	DCE /$\overline{\text{DTE}}$	(Note 2) R1		(Note 2) R2		(Note 2) R3		(Note 2) (Note 5) R4A R5A	(Note 3) R1	(Note 3) (Note 5) R2, R3 R4, R5
					A	B	A	B	A	B			
Not Used (Default V.11)	0	0	0	0	V.11	V.11	V.11	V.11	V.11	V.11	V.10	CMOS	CMOS
RS530A	0	0	1	0	V.11	V.11	V.10	30k	V.11	V.11	V.10	CMOS	CMOS
RS530	0	1	0	0	V.11	V.11	V.11	V.11	V.11	V.11	V.10	CMOS	CMOS
X.21	0	1	1	0	V.11	V.11	V.11	V.11	V.11	V.11	V.10	CMOS	CMOS
V.35	1	0	0	0	V.28	30k	V.28	30k	V.28	30k	V.28	CMOS	CMOS
RS449/V.36	1	0	1	0	V.11	V.11	V.11	V.11	V.11	V.11	V.10	CMOS	CMOS
V.28/RS232	1	1	0	0	V.28	30k	V.28	30k	V.28	30k	V.28	CMOS	CMOS
No Cable	1	1	1	0	30k	30k	30k	30k	30k	30k	30k	Z	Z
Not Used (Default V.11)	0	0	0	1	30k	30k	V.11	V.11	V.11	V.11	V.10	Z	CMOS
RS530A	0	0	1	1	30k	30k	V.10	30k	V.11	V.11	V.10	Z	CMOS
RS530	0	1	0	1	30k	30k	V.11	V.11	V.11	V.11	V.10	Z	CMOS
X.21	0	1	1	1	30k	30k	V.11	V.11	V.11	V.11	V.10	Z	CMOS
V.35	1	0	0	1	30k	30k	V.28	30k	V.28	30k	V.28	Z	CMOS
RS449/V.36	1	0	1	1	30k	30k	V.11	V.11	V.11	V.11	V.10	Z	CMOS
V.28/RS232	1	1	0	1	30k	30k	V.28	30k	V.28	30k	V.28	Z	CMOS
No Cable	1	1	1	1	30k	30k	30k	30k	30k	30k	30k	Z	Z

Note 1: Driver inputs are TTL level compatible.
Note 2: Unused receiver inputs are terminated with 30k to ground.
Note 3: Receiver outputs are CMOS level compatible and have a weak pull-up to V_{IN} when Z.
Note 4: Driver 4 is enabled by D4ENB=0 (Pin 15).
Note 5: Receiver 4 is enabled by R4EN=1 (Pin 16).

SWITCHING TIME WAVEFORMS

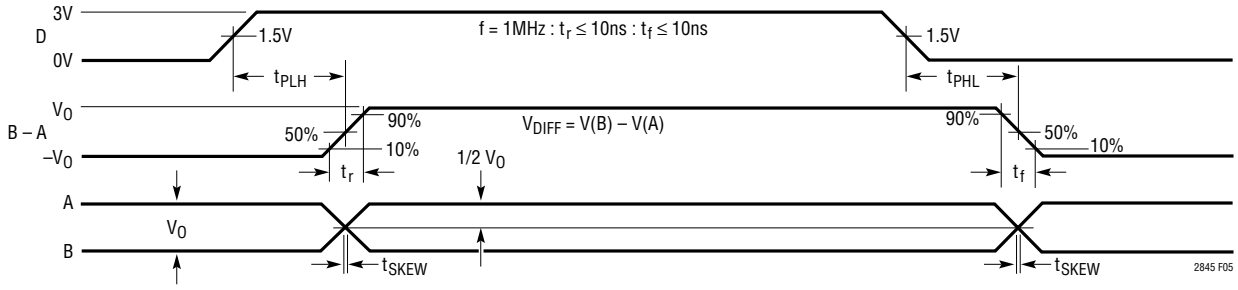


Figure 5. V.11 Driver Propagation Delays

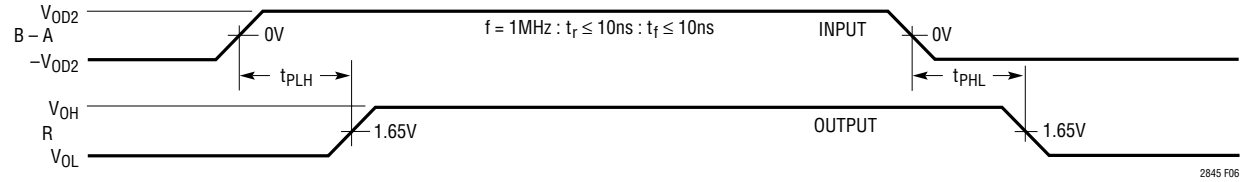


Figure 6. V.11 Receiver Propagation Delays

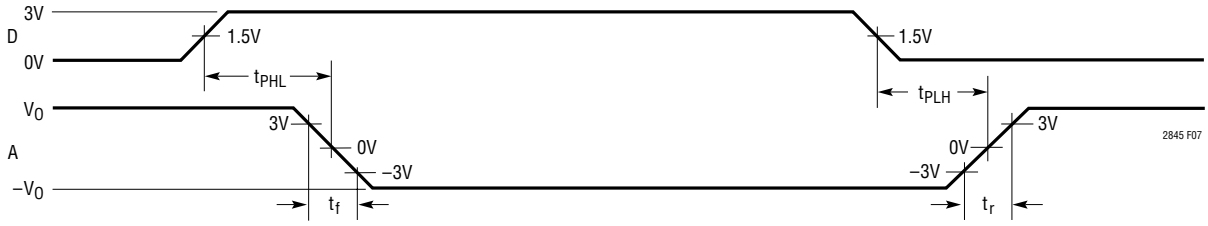


Figure 7. V.10, V.28 Driver Propagation Delays

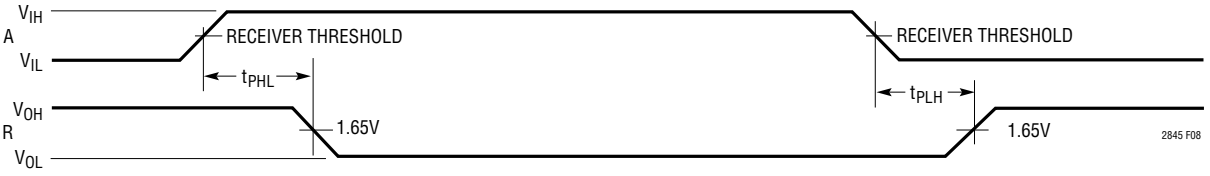


Figure 8. V.10, V.28 Receiver Propagation Delays

APPLICATIONS INFORMATION

Overview

The LTC2846/LTC2845 or LTC2847/LTC2845 form the core of a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 or X.21 protocols. Cable termination is provided on-chip, eliminating the need for discrete designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 9. The LTC2846 of each port is used to generate the clock and data signals. The LTC2845 is used to generate the control signals along with LL (Local Loop-Back), RL (Remote Loop-Back), TM (Test Mode) and RI (Ring Indicate). Cable termination is used only for the clock and data signals because they must support V.11 cable termination. The control signals do not need any external resistors.

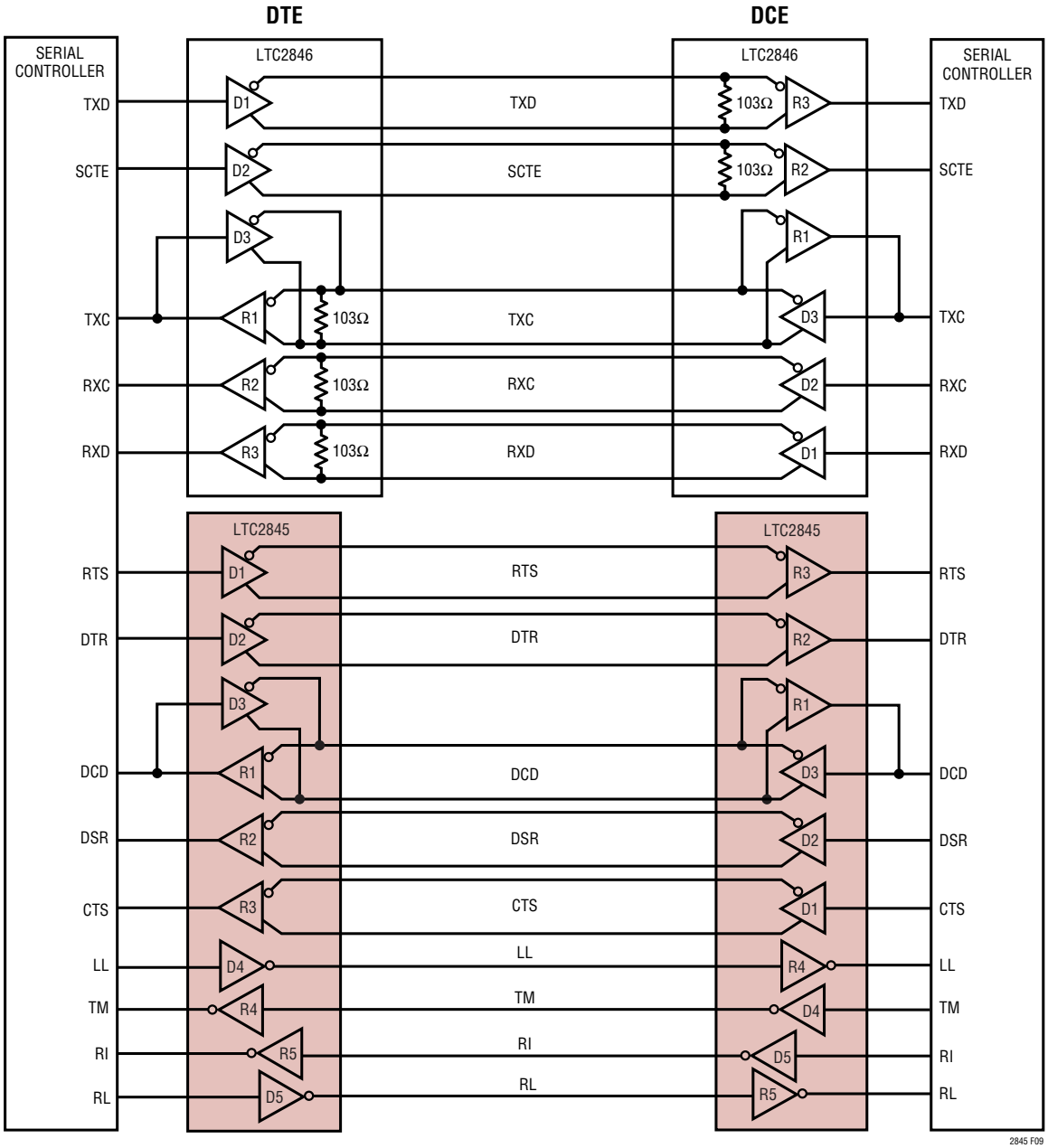


Figure 9. Complete Multiprotocol Interface in EIA530 Mode

APPLICATIONS INFORMATION

Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see the Mode Selection table).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 10.

The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected and that the LTC2846/LTC2845 enters the no-cable mode when the cable is removed. In the no-cable mode the LTC2846/LTC2845 supply current drops to less than 1000µA and all driver outputs are forced into a high impedance state.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{IN}.

Cable Termination

Traditional implementations have included switching resistors with expensive relays, or required the user to change termination modules every time the interface standard has changed. Custom cables have been used with the termination in the cable head or separate terminations are built on the board and a custom cable routes the signals to the appropriate termination. Switching the termination with FETs is difficult because the FETs must remain off even though the signal voltage is beyond the supply voltage for the FET drivers or the power is off.

Using the LTC2846/LTC2845 solves the cable termination switching problem. Via software control, appropriate termination for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols is chosen.

V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 11. A V.10 single-ended generator output A with ground C is connected to a differential receiver with inputs A' connected to A, and input C' connected to the signal return ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 12.

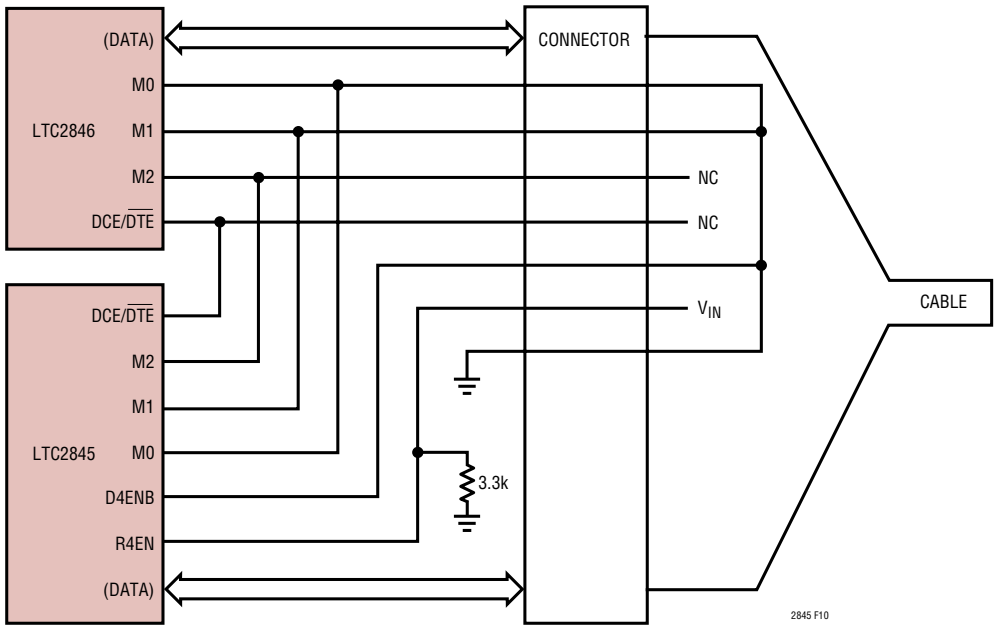


Figure 10. Single Port DCE V.35 Mode Selection in the Cable

APPLICATIONS INFORMATION

The V.10 receiver configuration in the LTC2845 is shown in Figure 13. In V.10 mode switch S3 inside the LTC2845 is turned off. The noninverting input is disconnected inside the LTC2845 receiver and connected to ground.The cable termination is then the 30k input impedance to ground of the LTC2845 V.10 receiver.

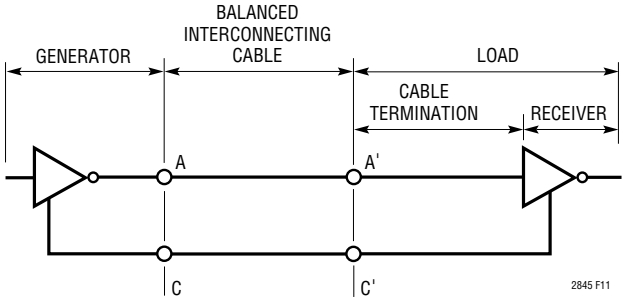


Figure 11. Typical V.10 Interface

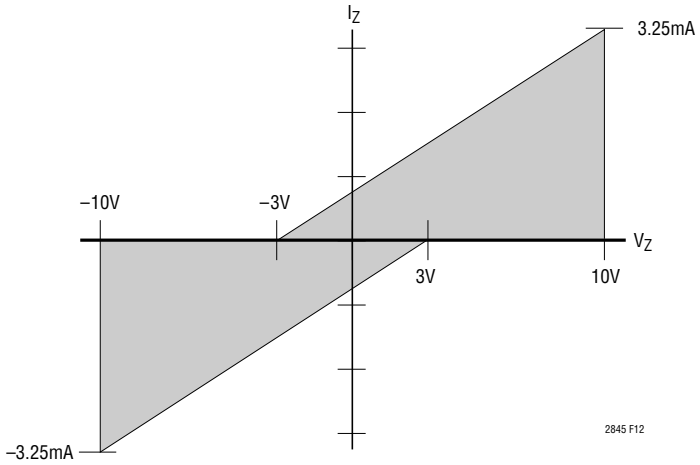


Figure 12. V.10 Receiver Input Impedance

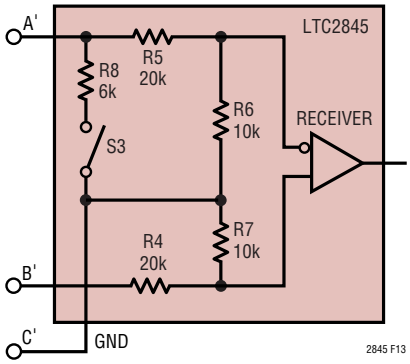


Figure 13. V.10 Receiver Configuration

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 14. A V.11 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 12.

In V.11 mode, all switches are off except S1 of the LTC2846's receivers which connects a 103Ω differential termination impedance to the cable as shown in Figure 15[1]. The LTC2845 only handles control signals, so no termination other than its V.11 receivers' 30k input impedance is necessary.

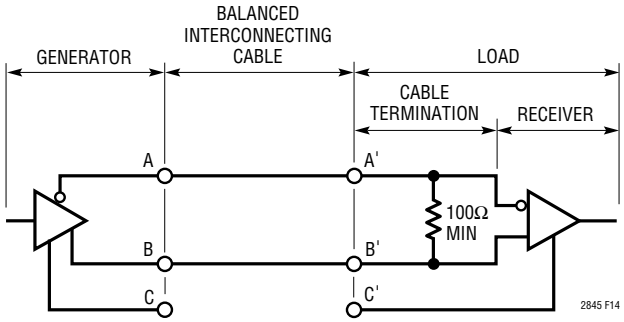


Figure 14. Typical V.11 Interface

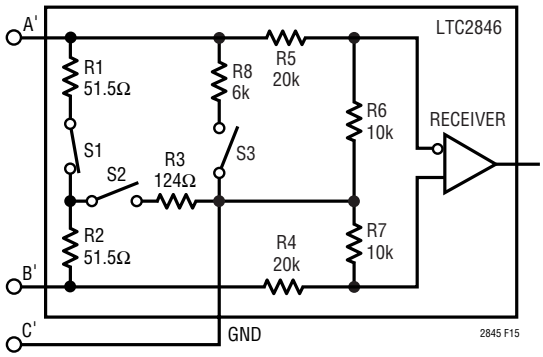


Figure 15. V.11 Receiver Configuration

[1]Actually, there is no switch S1 in receivers R2 and R3. However, for simplicity, all termination networks on the LTC2846 can be treated identically if it is assumed that an S1 switch exists and is always closed on the R2 and R3 receivers.

APPLICATIONS INFORMATION

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 16. A V.28 single-ended generator output A with ground C is connected to a single-ended receiver with input A' connected to A, ground C' connected via the signal return ground C.

In V.28 mode, all switches are off except S3 inside the LTC2846/LTC2845 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 17. The noninverting input is disconnected inside the LTC2846/LTC2845 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.

V.35 Interface

A typical V.35 balanced interface is shown in Figure 18. A V.35 differential generator with outputs A and B with ground C is connected to a differential receiver with ground C', inputs A' connected to A, B' connected to B. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100Ω ±10Ω, and the impedance between shorted terminals (A' and B') and ground C' must be 150Ω ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC2846 are on, connecting the T network impedance as shown in Figure 19. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground C must be 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on as shown in Figure 20.

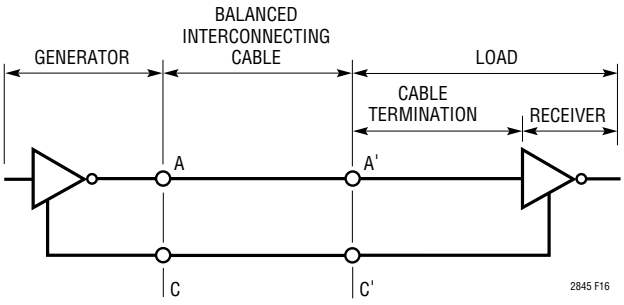


Figure 16. Typical V.28 Interface

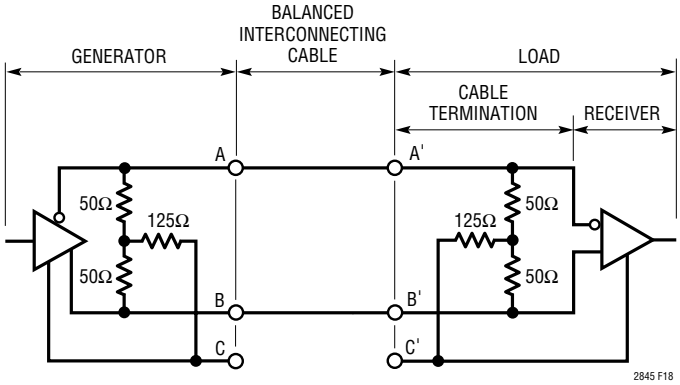


Figure 18. Typical V.35 Interface

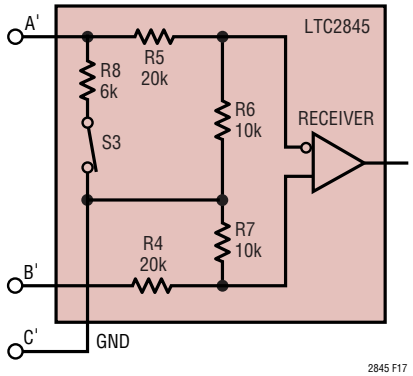


Figure 17. V.28 Receiver Configuration

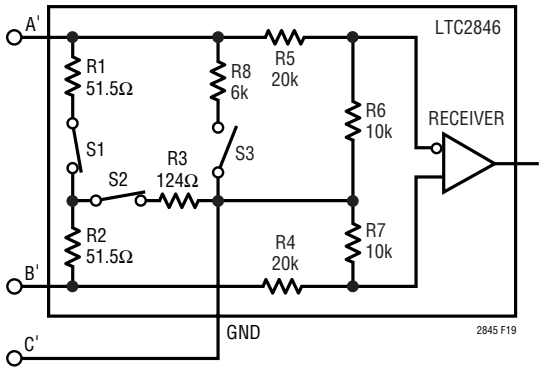


Figure 19. V.35 Receiver Configuration

APPLICATIONS INFORMATION

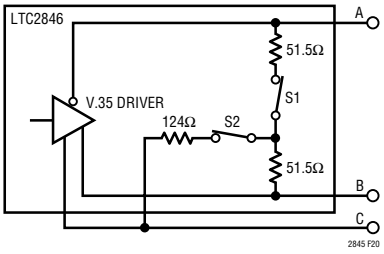


Figure 20. V.35 Driver

No-Cable Mode

The no-cable mode (M0 = M1 = M2 = D4ENB = 1, R4EN = 0) is intended for the case when the cable is disconnected from the connector. The bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the supply current drops to less than 700µA.

LTC2846 and LTC2847 Supplies

The LTC2846 and LTC2847 use an internal capacitive charge pump to generate V_{DD} and V_{EE} as shown in Figure 21. A voltage doubler generates about 8V on V_{DD} and a voltage inverter generates about –7.5V for V_{EE}. Three 1µF surface mounted tantalum or ceramic capacitors are required for C1, C2 and C3. The V_{EE} capacitor C4 should be a minimum of 3.3µF. All capacitors are 16V and should be placed as close as possible to the LTC2846 to reduce EMI.

The LTC2846 has an internal boost switching regulator which generates a 5V output from the 3.3V supply as shown in Figure 22. The 5V V_{CC} supplies its internal charge pump and transceivers as well as its companion chip. The LTC2847 requires an external 5V supply.

Receiver Fail-Safe

All LTC2846/LTC2845 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or shorted together by a termination resistor, the receiver output will always be forced to a logic high.

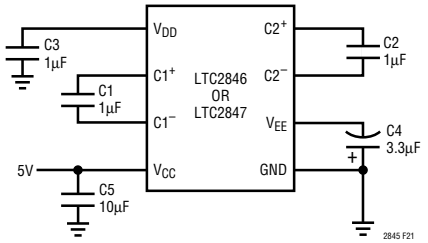


Figure 21. Charge Pump

DTE vs DCE Operation

The DCE/$\overline{\text{DTE}}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC2846, and Driver 3/Receiver 1 in the LTC2845.

The LTC2846/LTC2845 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender, or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC2846/LTC2845 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 23. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{IN} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 24.

A port with one DB-25 connector, can be configured for either DTE or DCE operation is shown in Figure 25. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via Driver 1 in the LTC2846. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

Compliance Testing

The LTC2846/LTC2845 chipset has been tested by TUV Rheinland of North America Inc. and passed the NET1, NET2 and TBR2 requirements. Copies of the test report are available from LTC or TUV Rheinland of North America Inc.

The title of the report is Test Report No.TBR2/050101/02

The address of TUV Rheinland of North America Inc. is:

TUV Rheinland of North America Inc.
1775, Old Highway 8 NW, Suite 107
St. Paul, MN 55112
Tel. (651) 639-0775
Fax (651) 639-0873

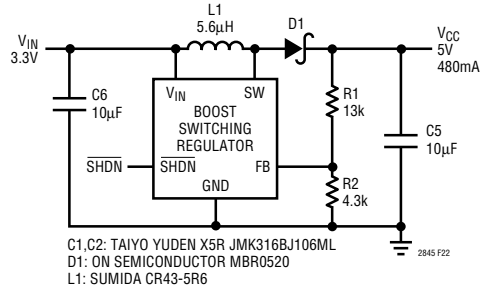


Figure 22. LTC2846 Boost Switching Regulator

TYPICAL APPLICATIONS

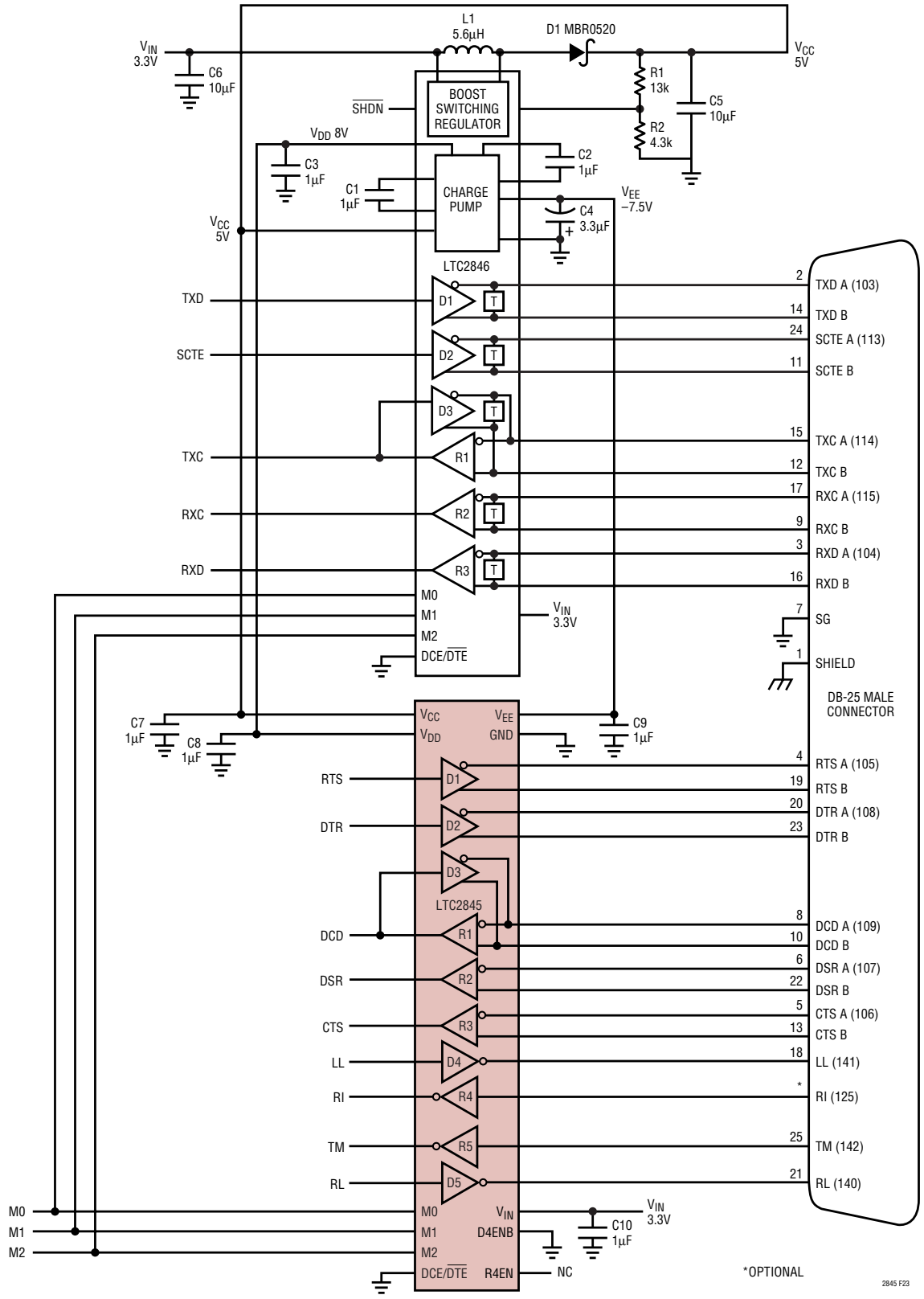


Figure 23. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

TYPICAL APPLICATIONS

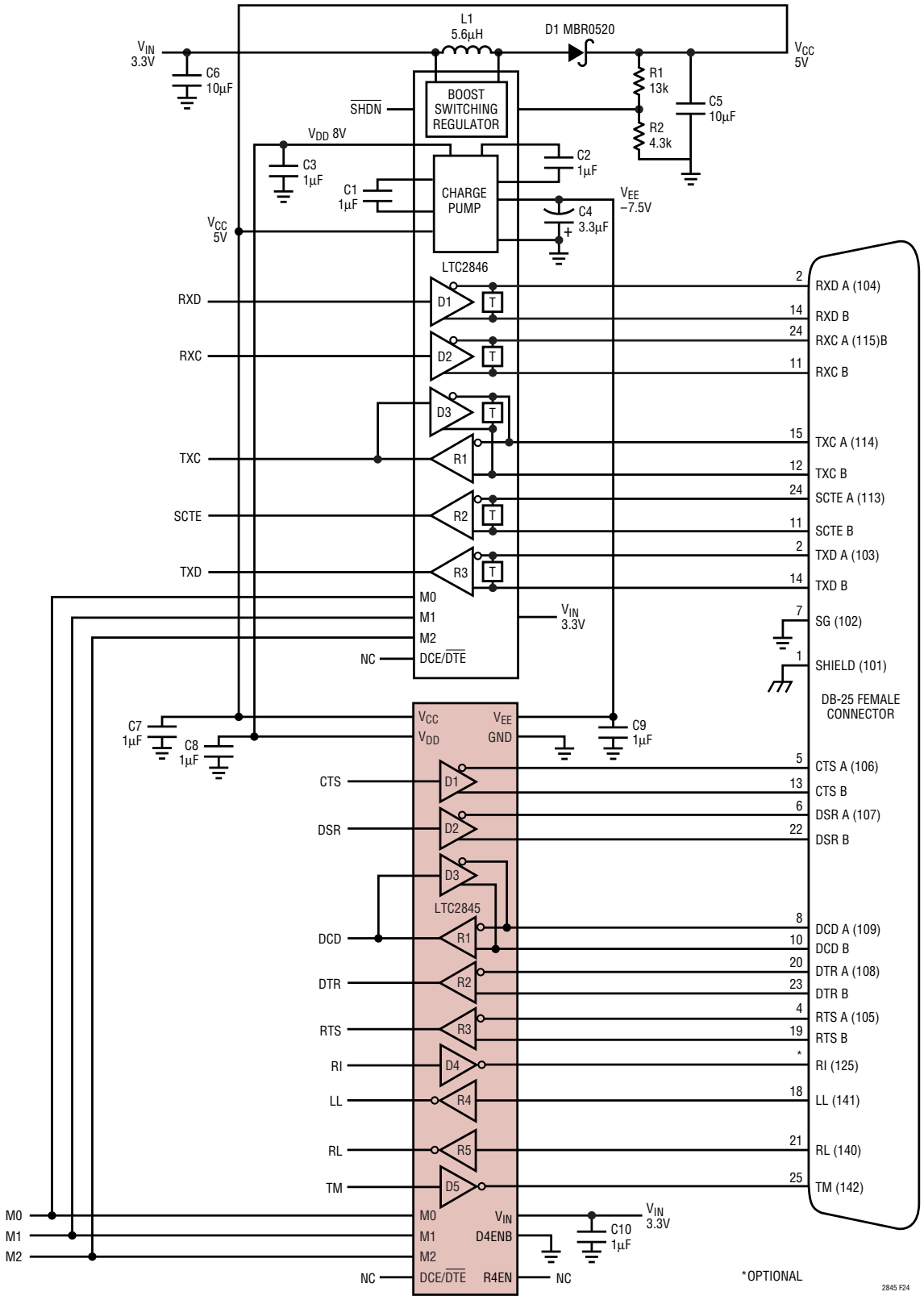


Figure 24. Controller-Selectable DCE Port with DB-25 Connector

TYPICAL APPLICATIONS

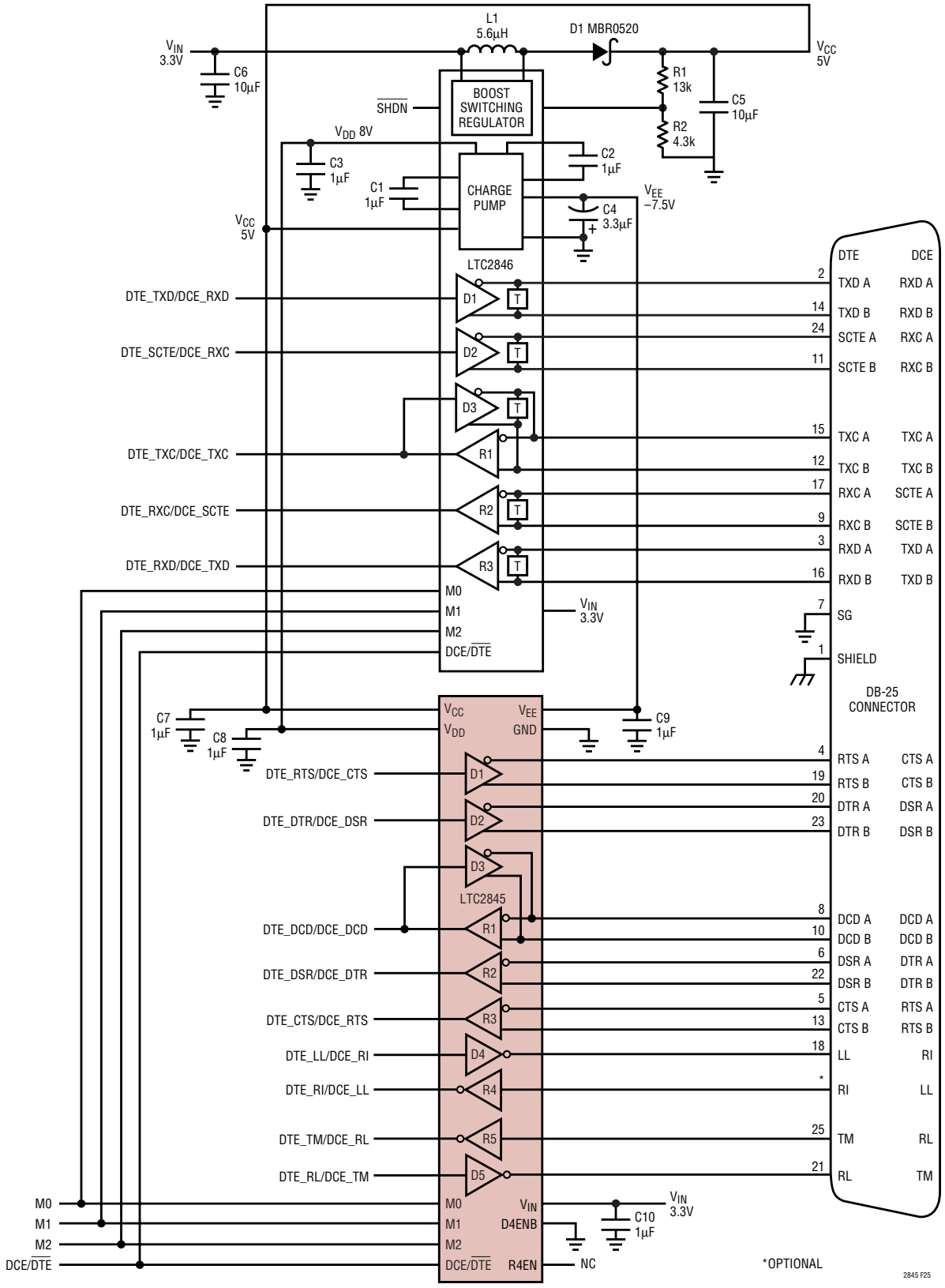
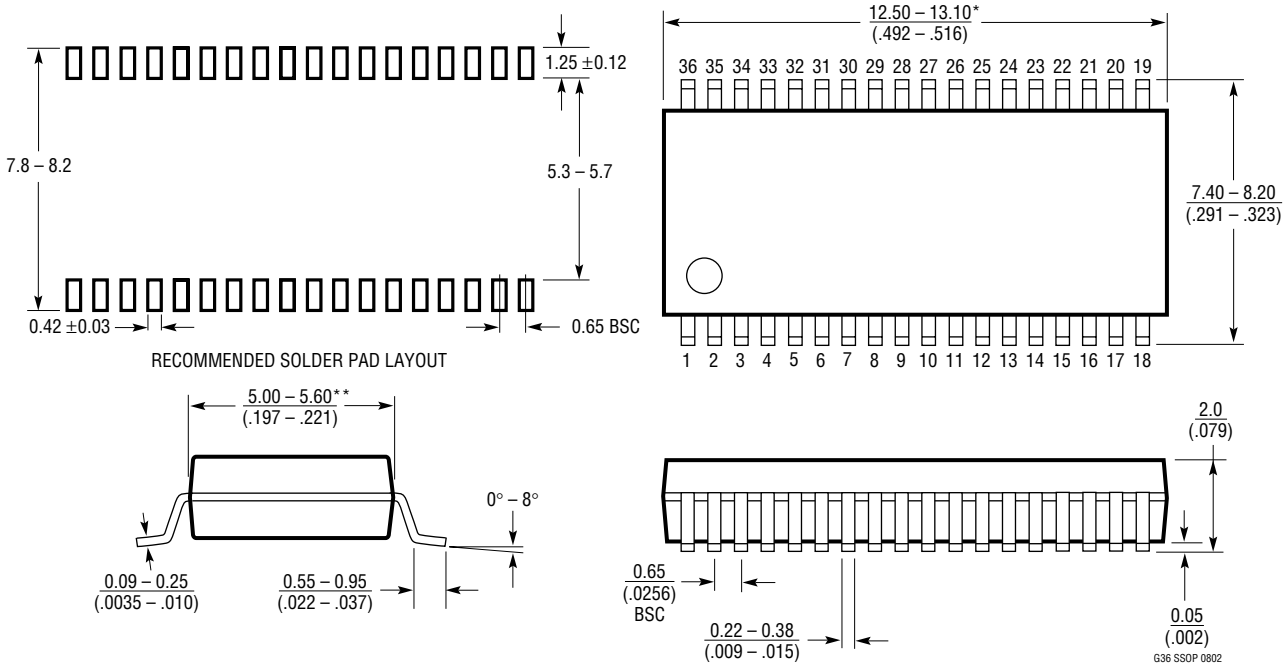


Figure 25. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

PACKAGE DESCRIPTION

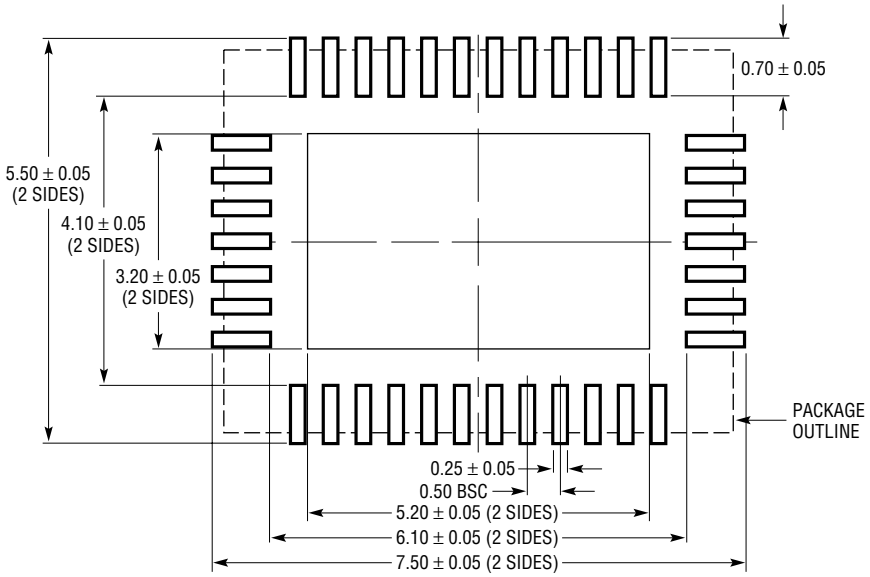
G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



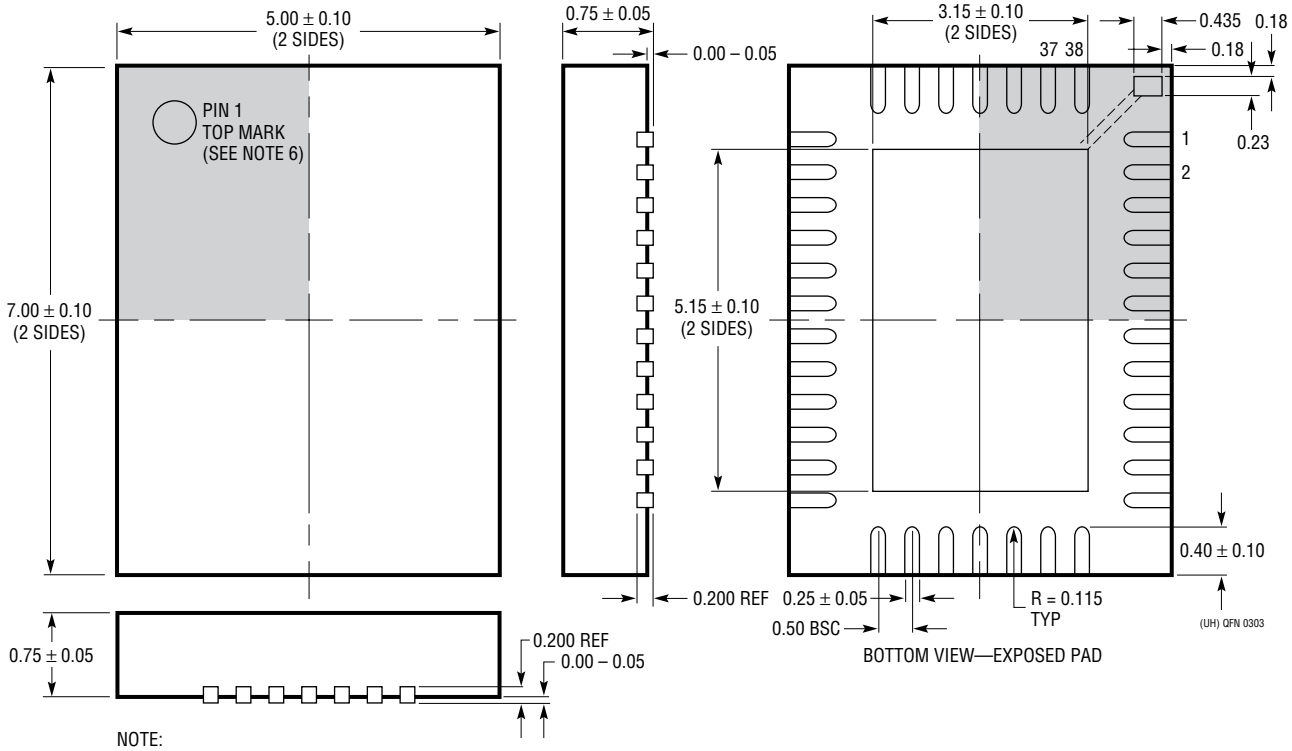
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE