

Software-Selectable Multiprotocol Transceiver with Termination and 3.3V Digital Interface

FEATURES

- **Software-Selectable Transceiver Supports:** RS232, RS449, EIA530, EIA530-A, V.35, V.36, X.21
- **Operates from Single 5V Supply**
- **Separate Supply Pin for Digital Interface Works down to 3V**
- On-Chip Cable Termination
- Complete DTE or DCE Port with LTC2845
- Available in 38-Pin 5mm × 7mm QFN Package

APPLICATIONS

- Data Networking
- CSU and DSU
- Data Routers

DESCRIPTION

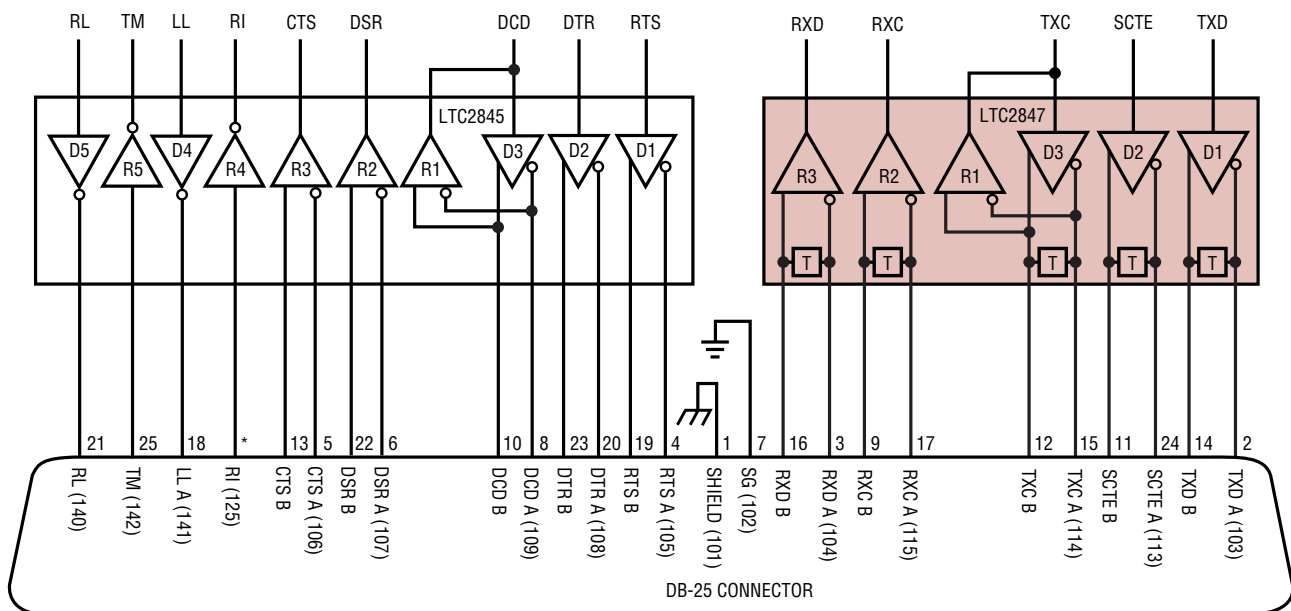
The LTC[®]2847 is a 3-driver/3-receiver multiprotocol transceiver with on-chip cable termination. When combined with the LTC2845, this chip set forms a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 and X.21 protocols. All necessary cable termination is provided inside the LTC2847.

The V_{CC} supplies the drivers, the receivers and an internal charge pump that requires only five space-saving surface mounted capacitors. The V_{IN} supply drives the digital interface circuitry including the receiver output drivers. It can be tied to V_{CC} or be powered off a lower supply (down to 3V) to interface with low voltage ASICs. The LTC2847 is available in a 0.8mm tall, 5mm × 7mm QFN package.

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TYPICAL APPLICATION

Complete DTE or DCE Multiprotocol Serial Interface with DB-25 Connector



*OPTIONAL

2847 TA01

sn2847 2847fs

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Voltage	-0.3V to 6.5V
V_{IN} Voltage	-0.3V to 6.5V
Input Voltage	
Transmitters	-0.3V to ($V_{CC} + 0.3V$)
Receivers	-18V to 18V
Logic Pins	-0.3V to ($V_{CC} + 0.3V$)
Output Voltage	
Transmitters	($V_{EE} - 0.3V$) to ($V_{DD} + 0.3V$)
Receivers	-0.3V to ($V_{IN} + 0.3V$)
V_{EE}	-10V to 0.3V
V_{DD}	-0.3V to 10V
Short-Circuit Duration	
Transmitter Output	Indefinite
Receiver Output	Indefinite
V_{EE}	30 sec
Operating Temperature Range	
LTC2847C	0°C to 70°C
LTC2847I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

UHF PACKAGE
38-LEAD (7mm × 5mm) PLASTIC QFN
UNDERSIDE METAL INTERNALLY CONNECTED TO V_{EE}
(PCB CONNECTION OPTIONAL)
 $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 34^{\circ}C/W$

ORDER PART NUMBER

LTC2847CUHF
LTC2847IUHF

UHF PART MARKING

2847
2847I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_{CC} = 5V$, $V_{IN} = 3.3V$, unless otherwise noted (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supplies						
I_{CC}	V_{CC} Supply Current (DCE Mode, All Digital Pins = GND or V_{IN})	RS530, RS530-A, X.21 Modes, No Load	●	14		mA
		RS530, RS530-A, X.21 Modes, Full Load	●	100	130	mA
		V.35 Mode	●	126	170	mA
		V.28 Mode, No Load	●	20		mA
		V.28 Mode, Full Load	●	35	75	mA
	No-Cable Mode	●	300	900	μA	
I_{VIN}	V_{IN} Supply Current (DCE Mode, All Digital Pins = GND or V_{IN})	All Modes Except No-Cable Mode		405		μA
P_D	Internal Power Dissipation (DCE Mode)	RS530, RS530-A, X.21 Modes, Full Load		410		mW
		V.35 Mode, Full Load		625		mW
		V.28 Mode, Full Load		150		mW
V^+	Positive Charge Pump Output Voltage	V.11 or V.28 Mode, No Load	●	8	9.3	V
		V.35 Mode	●	7	8.0	V
		V.28 Mode, with Load	●	8	8.7	V
		V.28 Mode, with Load, $I_{DD} = 10mA$			6.5	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V^-	Negative Charge Pump Output Voltage	V.28 Mode, No Load		-9.6		V
		V.28 Mode, Full Load	●	-7.5	-8.5	V
		V.35 Mode	●	-5.5	-6.5	V
		RS530, RS530-A, X.21 Modes, Full Load	●	-4.5	-6.0	V
f_{OSC}	Charge Pump Oscillator Frequency			500		kHz
t_r	Charge Pump Rise Time	No-Cable Mode/Power-Off to Normal Operation		2		ms

Logic Inputs and Outputs

V_{IH}	Logic Input High Voltage	D1, D2, D3, M0, M1, M2, DCE/ $\overline{\text{DTE}}$	●	2.0		V	
V_{IL}	Logic Input Low Voltage	D1, D2, D3, M0, M1, M2, DCE/ $\overline{\text{DTE}}$	●		0.8	V	
I_{IN}	Logic Input Current	D1, D2, D3	●		± 10	μA	
		M0, M1, M2, DCE/ $\overline{\text{DTE}} = \text{GND}$	●	-30	-75	-120	μA
		M0, M1, M2, DCE/ $\overline{\text{DTE}} = V_{IN}$	●			± 10	μA
V_{OH}	Output High Voltage	$I_O = -3\text{mA}$	●	2.7	3	V	
V_{OL}	Output Low Voltage	$I_O = 1.6\text{mA}$	●		0.2	0.4	V
I_{OSR}	Output Short-Circuit Current	$0\text{V} \leq V_O \leq V_{IN}$	●			± 50	mA
I_{OZR}	Three-State Output Current	$M0 = M1 = M2 = V_{IN}, V_O = \text{GND}$	●	-30	-85	-160	μA
		$M0 = M1 = M2 = V_{IN}, V_O = V_{IN}$	●			± 10	μA

V.11 Driver

V_{ODO}	Open Circuit Differential Output Voltage	$R_L = 1.95\text{k}$ (Figure 1)	●			± 5	V
V_{ODL}	Loaded Differential Output Voltage	$R_L = 50\Omega$ (Figure 1)	●	$0.5V_{ODO}$		$0.67V_{ODO}$	V
		$R_L = 50\Omega$ (Figure 1)	●	± 2			V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	$R_L = 50\Omega$ (Figure 1)	●			0.2	V
V_{OC}	Common Mode Output Voltage	$R_L = 50\Omega$ (Figure 1)	●			3	V
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	$R_L = 50\Omega$ (Figure 1)	●			0.2	V
I_{SS}	Short-Circuit Current	$V_{OUT} = \text{GND}$				± 150	mA
I_{OZ}	Output Leakage Current	$ V_A $ and $ V_B \leq 0.25\text{V}$, Power Off or No-Cable Mode or Driver Disabled	●		± 1	± 100	μA
t_r, t_f	Rise or Fall Time	(Figures 2, 13)	●	2	15	25	ns
t_{PLH}	Input to Output Rising	(Figures 2, 13)	●	15	40	65	ns
t_{PHL}	Input to Output Falling	(Figures 2, 13)	●	15	40	65	ns
Δt	Input to Output Difference, $ t_{PLH} - t_{PHL} $	(Figures 2, 13)	●	0	3	12	ns
t_{SKEW}	Output to Output Skew	(Figures 2, 13)			3		ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{IN} = 3.3\text{V}$, unless otherwise noted (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V.11 Receiver							
V_{TH}	Input Threshold Voltage	$-7\text{V} \leq V_{CM} \leq 7\text{V}$	●	-0.2	0.2	V	
ΔV_{TH}	Input Hysteresis	$-7\text{V} \leq V_{CM} \leq 7\text{V}$	●	15	40	mV	
R_{IN}	Input Impedance	$-7\text{V} \leq V_{CM} \leq 7\text{V}$ (Figure 3)	●	100	103	Ω	
t_r, t_f	Rise or Fall Time	$C_L = 50\text{pF}$ (Figures 4, 14)		15		ns	
t_{PLH}	Input to Output Rising	$C_L = 50\text{pF}$ (Figures 4, 14)	●	50	90	ns	
t_{PHL}	Input to Output Falling	$C_L = 50\text{pF}$ (Figures 4, 14)	●	50	90	ns	
Δt	Input to Output Difference, $ t_{PLH} - t_{PHL} $	$C_L = 50\text{pF}$ (Figures 4, 14)	●	0	4	25	ns
V.35 Driver							
V_{OD}	Differential Output Voltage	Open Circuit, $R_L = 1.95\text{k}$ (Figure 5) With Load, $-4\text{V} \leq V_{CM} \leq 4\text{V}$ (Figure 6)	●	± 0.44	± 0.55	± 1.2 ± 0.66	V V
V_{OA}, V_{OB}	Single-Ended Output Voltage	Open Circuit, $R_L = 1.95\text{k}$ (Figure 5)	●			± 1.2	V
V_{OC}	Transmitter Output Offset	$R_L = 50\Omega$ (Figure 5)	●			± 0.6	V
I_{OH}	Transmitter Output High Current	$V_A, V_B = 0\text{V}$	●	-9	-11	-13	mA
I_{OL}	Transmitter Output Low Current	$V_A, V_B = 0\text{V}$	●	9	11	13	mA
I_{OZ}	Transmitter Output Leakage Current	$ V_A $ and $ V_B \leq 0.25\text{V}$	●		± 1	± 100	μA
R_{OD}	Transmitter Differential Mode Impedance		●	50	100	150	Ω
R_{OC}	Transmitter Common Mode Impedance	$-2\text{V} \leq V_{CM} \leq 2\text{V}$ (Figure 7)		135	150	165	Ω
t_r, t_f	Rise or Fall Time	(Figures 8, 13)		5			ns
t_{PLH}	Input to Output	(Figures 8, 13)	●	15	35	65	ns
t_{PHL}	Input to Output	(Figures 8, 13)	●	15	35	65	ns
Δt	Input to Output Difference, $ t_{PLH} - t_{PHL} $	(Figures 8, 13)	●		0	16	ns
t_{SKEW}	Output to Output Skew	(Figures 8, 13)		4			ns
V.35 Receiver							
V_{TH}	Differential Receiver Input Threshold Voltage	$-2\text{V} \leq V_{CM} \leq 2\text{V}$ (Figure 9)	●	-0.2	0.2	V	
ΔV_{TH}	Receiver Input Hysteresis	$-2\text{V} \leq V_{CM} \leq 2\text{V}$ (Figure 9)	●		15	40	mV
R_{ID}	Receiver Differential Mode Impedance	$-2\text{V} \leq V_{CM} \leq 2\text{V}$	●	90	103	110	Ω
R_{IC}	Receiver Common Mode Impedance	$-2\text{V} \leq V_{CM} \leq 2\text{V}$ (Figure 10)		135	150	165	Ω
t_r, t_f	Rise or Fall Time	$C_L = 50\text{pF}$ (Figures 4, 14)			15		ns
t_{PLH}	Input to Output	$C_L = 50\text{pF}$ (Figures 4, 14)	●		50	90	ns
t_{PHL}	Input to Output	$C_L = 50\text{pF}$ (Figures 4, 14)	●		50	90	ns
Δt	Input to Output Difference, $ t_{PLH} - t_{PHL} $	$C_L = 50\text{pF}$ (Figures 4, 14)	●	0	4	25	ns
V.28 Driver							
V_O	Output Voltage	Open Circuit $R_L = 3\text{k}$ (Figure 11)	● ●	± 5	± 8.5	± 10	V V
I_{SS}	Short-Circuit Current	$V_{OUT} = \text{GND}$	●			± 150	mA
R_{OZ}	Power-Off Resistance	$-2\text{V} < V_O < 2\text{V}$, Power Off or No-Cable Mode	●	300			Ω
SR	Slew Rate	$R_L = 7\text{k}$, $C_L = 0$ (Figures 11, 15)	●	4		30	V/ μs
t_{PLH}	Input to Output	$R_L = 3\text{k}$, $C_L = 2500\text{pF}$ (Figures 11, 15)	●		1.5	2.5	μs
t_{PHL}	Input to Output	$R_L = 3\text{k}$, $C_L = 2500\text{pF}$ (Figures 11, 15)	●		1.5	2.5	μs

ELECTRICAL CHARACTERISTICS The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CC} = 5\text{V}$, $V_{IN} = 3.3\text{V}$, unless otherwise noted (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
V.28 Receiver							
V_{THL}	Input Low Threshold Voltage	(Figure 12)	●		0.8	V	
V_{TLH}	Input High Threshold Voltage	(Figure 12)	●	2		V	
ΔV_{TH}	Receiver Input Hysteresis	(Figure 12)	●	0	0.05	0.3	V
R_{IN}	Receiver Input Impedance	$-15\text{V} \leq V_A \leq 15\text{V}$	●	3	5	7	$\text{k}\Omega$
t_r, t_f	Rise or Fall Time	$C_L = 50\text{pF}$ (Figures 12, 16)		15		ns	
t_{PLH}	Input to Output	$C_L = 50\text{pF}$ (Figures 12, 16)	●	60	300	ns	
t_{PHL}	Input to Output	$C_L = 50\text{pF}$ (Figures 12, 16)	●	160	300	ns	

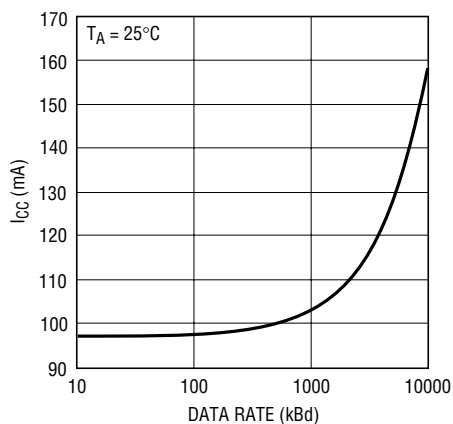
Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5\text{V}$, $V_{IN} = 3.3\text{V}$, $C_{VCC} = C_{VIN} = 10\mu\text{F}$, $C_{VDD} = 1\mu\text{F}$, $C_{VEE} = 3.3\mu\text{F}$ and $T_A = 25^\circ\text{C}$.

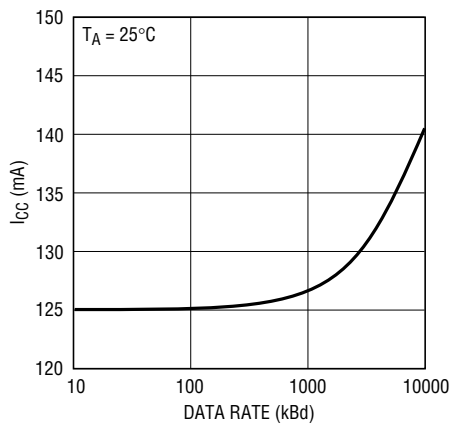
TYPICAL PERFORMANCE CHARACTERISTICS

V.11 Mode I_{CC} vs Data Rate



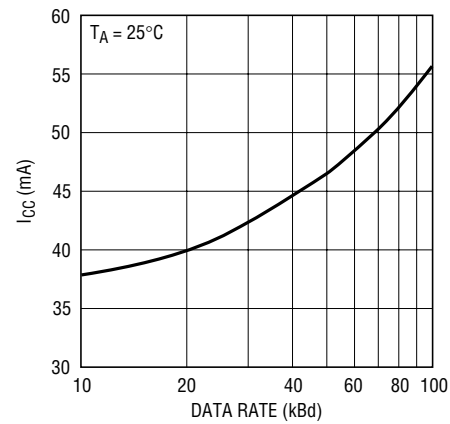
2846 G04

V.35 Mode I_{CC} vs Data Rate



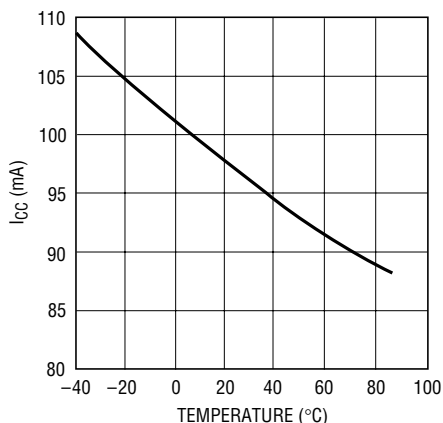
2846 G05

V.28 Mode I_{CC} vs Data Rate



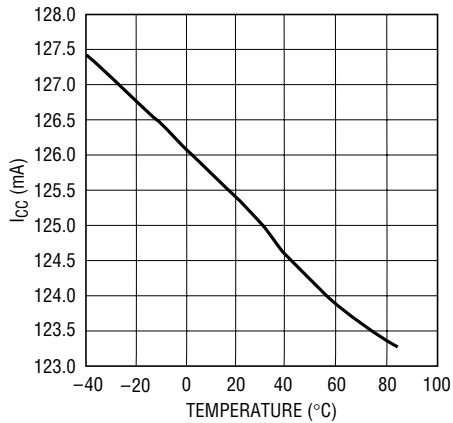
2846 G06

V.11 Mode I_{CC} vs Temperature



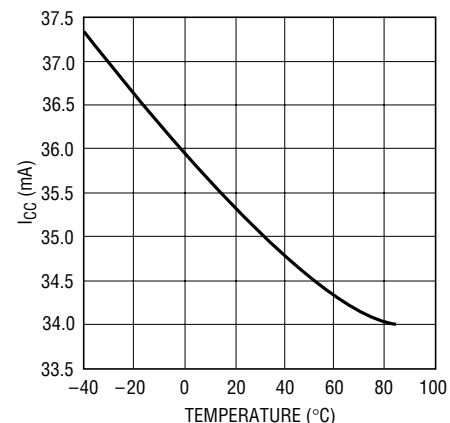
2846 G07

V.35 Mode I_{CC} vs Temperature



2846 G08

V.28 Mode I_{CC} vs Temperature



3846 G09

sn2847 2847fs

PIN FUNCTIONS

NC (Pins 1,3,18,19,22,23): No Connect.

V_{DD} (Pin 2): Generated Positive Supply Voltage for V.28. Connect a 1 μ F capacitor to ground.

V_{CC} (Pin 4): Input Supply Pin. Input supply to charge pump and transceiver. $4.75V \leq V_{CC} \leq 5.25V$. Connect a 1 μ F capacitor to GND.

D1 (Pin 5): TTL Level Driver 1 Input.

D2 (Pin 6): TTL Level Driver 2 Input.

D3 (Pin 7): TTL Level Driver 3 Input.

R1 (Pin 8): CMOS Level Receiver 1 Output with Pull-Up to V_{IN} when Three-Stated.

R2 (Pin 9): CMOS Level Receiver 2 Output with Pull-Up to V_{IN} when Three-Stated.

R3 (Pin 10): CMOS Level Receiver 3 Output with Pull-Up to V_{IN} when Three-Stated.

M0 (Pin 11): TTL Level Mode Select Input 0 with Pull-Up to V_{IN}. See Table 1.

M1 (Pin 12): TTL Level Mode Select Input 1 with Pull-Up to V_{IN}. See Table 1.

V_{IN} (Pin 13): Input Supply Pin. Input supply to digital interface including receiver output drivers. $3V \leq V_{IN} \leq 5.25V$. Connect to V_{CC} (Pin 4) or to separate supply for lower receiver output swing. Connect a 1 μ F capacitor to GND.

M2 (Pin 14): TTL Level Mode Select Input 2 with Pull-Up to V_{IN}. See Table 1.

DCE/ \overline{DTE} (Pin 15): TTL Level Mode Select Input with Pull-Up to V_{IN}. See Table 1.

R3 B (Pin 16): Receiver 3 Noninverting Input.

R3 A (Pin 17): Receiver 3 Inverting Input.

R2 B (Pin 20): Receiver 2 Noninverting Input.

R2 A (Pin 21): Receiver 2 Inverting Input.

D3/R1 B (Pin 24): Receiver 1 Noninverting Input and Driver 3 Noninverting Output.

D3/R1 A (Pin 25): Receiver 1 Inverting Input and Driver 3 Inverting Output.

D2 B (Pin 26): Driver 2 Noninverting Output.

D2 A (Pin 27): Driver 2 Inverting Output.

D1 B (Pin 28): Driver 1 Noninverting Output.

D1 A (Pin 29): Driver 1 Inverting Output.

GND (Pins 30,31): Transceiver Ground.

V_{EE} (Pins 32,33,36): Generated Negative Supply Voltage. Connect a 3.3 μ F capacitor to GND. Exposed pad can also be connected to V_{EE}.

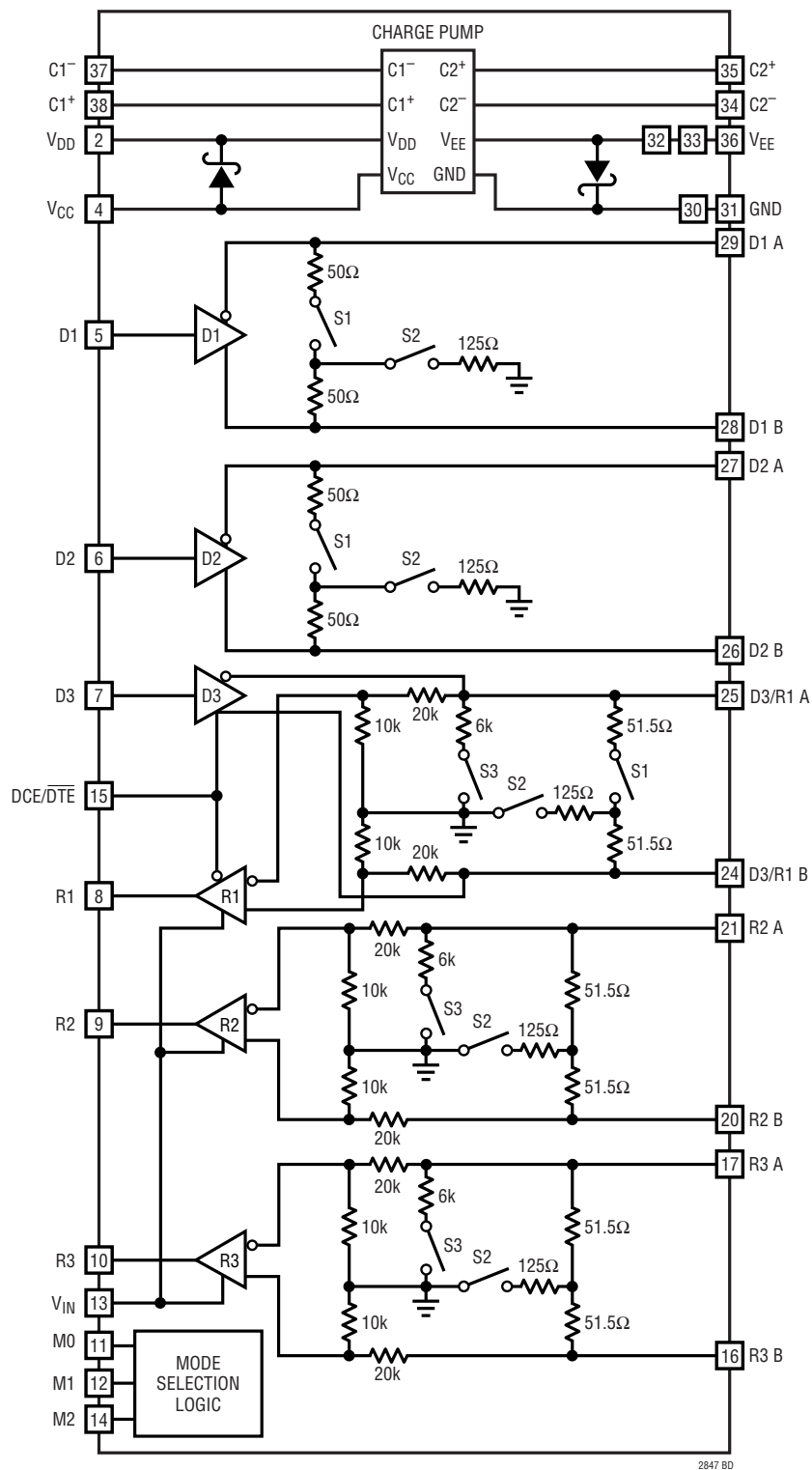
C2⁻ (Pin 34): Capacitor C2 Negative Terminal. Connect a 1 μ F capacitor between C2⁺ and C2⁻.

C2⁺ (Pin 35): Capacitor C2 Positive Terminal. Connect a 1 μ F capacitor between C2⁺ and C2⁻.

C1⁻ (Pin 37): Capacitor C1 Negative Terminal. Connect a 1 μ F capacitor between C1⁺ and C1⁻.

C1⁺ (Pin 38): Capacitor C1 Positive Terminal. Connect a 1 μ F capacitor between C1⁺ and C1⁻.

BLOCK DIAGRAM



TEST CIRCUITS

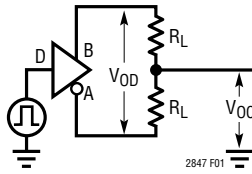


Figure 1. V.11 Driver DC Test Circuit

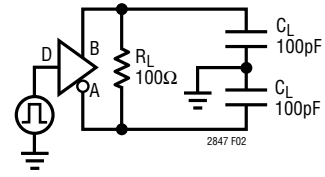


Figure 2. V.11 Driver AC Test Circuit

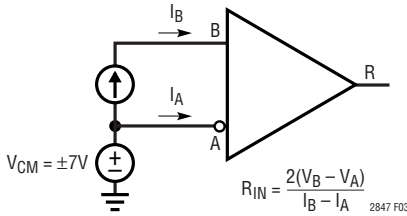


Figure 3. Input Impedance Test Circuit

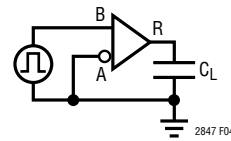


Figure 4. V.11, V.35 Receiver AC Test Circuit

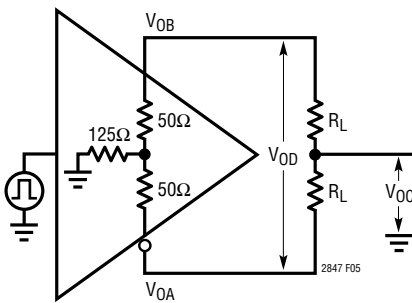


Figure 5. V.35 Driver Open-Circuit Test

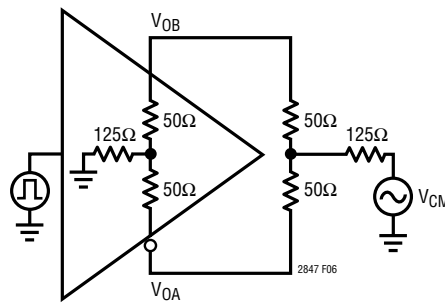


Figure 6. V.35 Driver Test Circuit

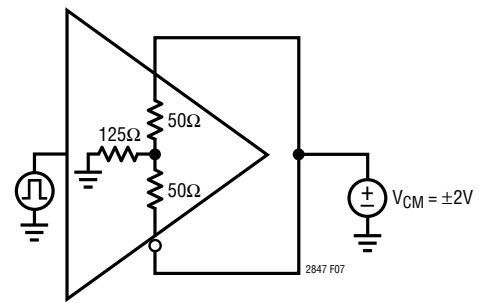


Figure 7. V.35 Driver Common Mode Impedance Test Circuit

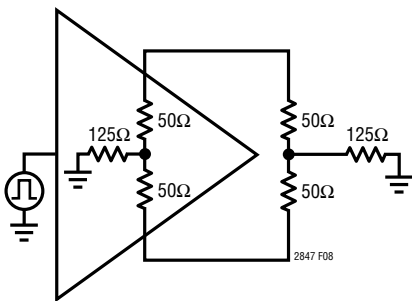


Figure 8. V.35 Driver AC Test Circuit

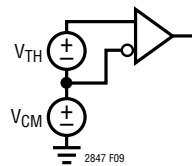


Figure 9. V.35 Receiver DC Test Circuit

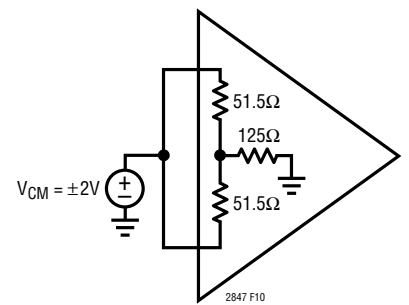


Figure 10. Receiver Common Mode Impedance Test Circuit

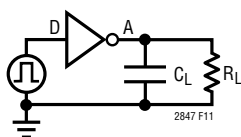


Figure 11. V.28 Driver Test Circuit

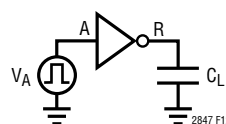


Figure 12. V.28 Receiver Test Circuit

MODE SELECTION

Table 1

Mode Name	M2	M1	M0	DCE/ DTE	D1,2 (Note 1)	D3 (Note 1)	D1		D2		D3		R1 (Note 2)		R2 (Note 2)		R3 (Note 2)		R1 (Note 3)	R2,R3 (Note 3)	V _{DD} (Note 4)	V _{EE} (Note 5)
							A	B	A	B	A	B	A	B	A	B						
Not Used (Default V.11)	0	0	0	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.11	V.11	V.11	V.11	V.11	V.11	CMOS	CMOS	9.3V	-6V
RS530A	0	0	1	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.11	V.11	V.11	V.11	V.11	V.11	CMOS	CMOS	9.3V	-6V
RS530	0	1	0	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.11	V.11	V.11	V.11	V.11	V.11	CMOS	CMOS	9.3V	-6V
X.21	0	1	1	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.11	V.11	V.11	V.11	V.11	V.11	CMOS	CMOS	9.3V	-6V
V.35	1	0	0	0	TTL	X	V.35	V.35	V.35	V.35	Z	Z	V.35	V.35	V.35	V.35	V.35	V.35	CMOS	CMOS	8V	-6.5V
RS449/V.36	1	0	1	0	TTL	X	V.11	V.11	V.11	V.11	Z	Z	V.11	V.11	V.11	V.11	V.11	V.11	CMOS	CMOS	9.3V	-6V
V.28/RS232	1	1	0	0	TTL	X	V.28	Z	V.28	Z	Z	Z	V.28	30k	V.28	30k	V.28	30k	CMOS	CMOS	8.7V	-8.5V
No Cable	1	1	1	0	X	X	Z	Z	Z	Z	Z	Z	30k	30k	30k	30k	30k	30k	Z	Z	4.7V	0.3V
Not Used (Default V.11)	0	0	0	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	30k	30k	V.11	V.11	V.11	V.11	Z	CMOS	9.3V	-6V
RS530A	0	0	1	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	30k	30k	V.11	V.11	V.11	V.11	Z	CMOS	9.3V	-6V
RS530	0	1	0	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	30k	30k	V.11	V.11	V.11	V.11	Z	CMOS	9.3V	-6V
X.21	0	1	1	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	30k	30k	V.11	V.11	V.11	V.11	Z	CMOS	9.3V	-6V
V.35	1	0	0	1	TTL	TTL	V.35	V.35	V.35	V.35	V.35	V.35	30k	30k	V.35	V.35	V.35	V.35	Z	CMOS	8V	-6.5V
RS449/V.36	1	0	1	1	TTL	TTL	V.11	V.11	V.11	V.11	V.11	V.11	30k	30k	V.11	V.11	V.11	V.11	Z	CMOS	9.3V	-6V
V.28/RS232	1	1	0	1	TTL	TTL	V.28	Z	V.28	Z	V.28	Z	30k	30k	V.28	30k	V.28	30k	Z	CMOS	8.7V	-8.5V
No Cable	1	1	1	1	X	X	Z	Z	Z	Z	Z	Z	30k	30k	30k	30k	30k	30k	Z	Z	4.7V	0.3V

Note 1: Driver inputs are TTL level compatible.

Note 2: Unused receiver inputs are terminated with 30k to ground. In addition, R2 and R3 are always terminated by a 103Ω differential impedance (see Block Diagram on page 7).

Note 3: Receiver Outputs are CMOS level compatible and have a weak pull up to V_{IN} when Z.

Note 4: V_{DD} values shown are typical values for V_{CC} = 5V, V_{IN} = 3.3V and T_A = 25°C with LTC2847 under full load for each mode.

Note 5: V_{EE} values shown are typical values for V_{CC} = 5V, V_{IN} = 3.3V and T_A = 25°C with LTC2847 under full load for each mode.

SWITCHING TIME WAVEFORMS

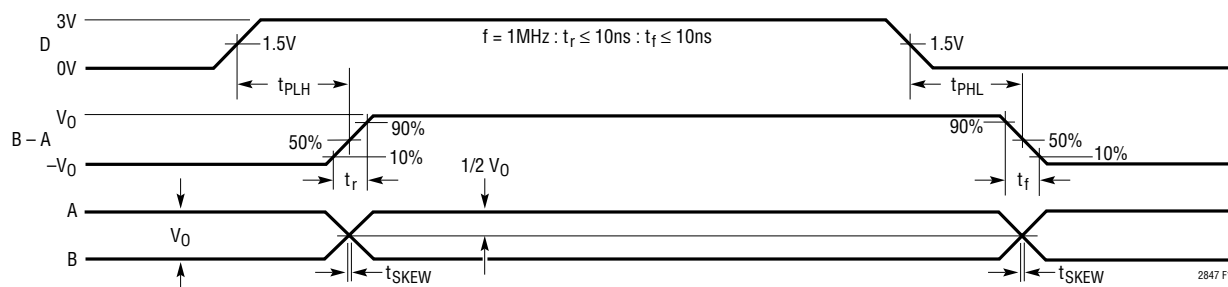


Figure 13. V.11, V.35 Driver Propagation Delays

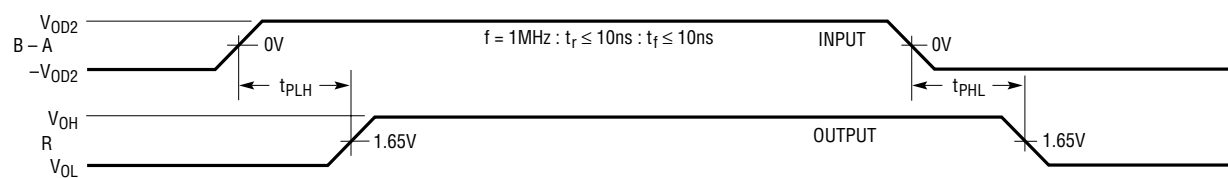


Figure 14. V.11, V.35 Receiver Propagation Delays

SWITCHING TIME WAVEFORMS

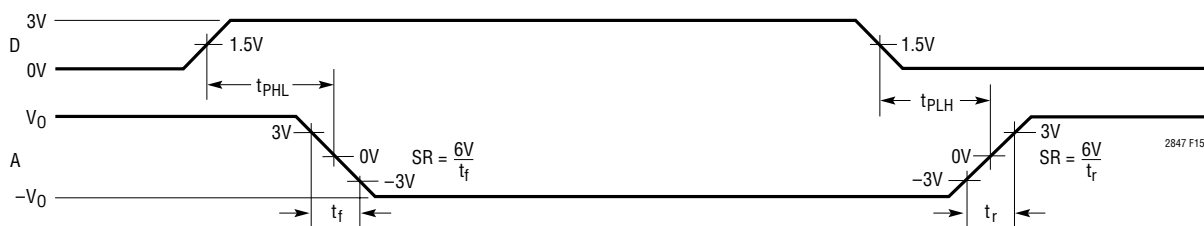


Figure 15. V.28 Driver Propagation Delays

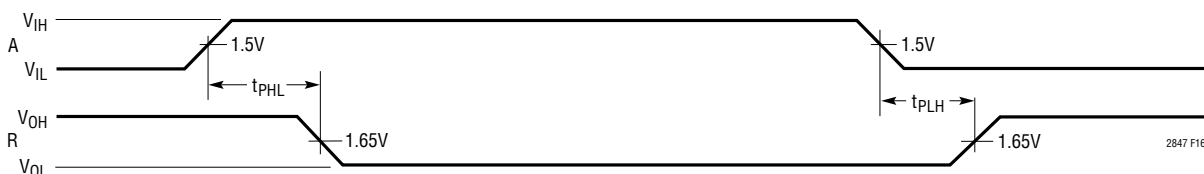


Figure 16. V.28 Receiver Propagation Delays

APPLICATIONS INFORMATION

Overview

The LTC2847 consists of a charge pump and a 3-driver/3-receiver transceiver. The 5V V_{CC} input powers the charge pump and transceiver. The charge pump generates the V_{DD} and V_{EE} supplies. The LTC2847's V_{DD} and V_{EE} supplies can be used to power a companion chip like the LTC2845. The V_{IN} input powers the digital interface including the receiver output drivers. Having a separate pin to power the digital interface allows the flexibility of controlling the receiver output swing to interface with 5V or 3.3V logic.

The LTC2847 and LTC2845 form a complete software-selectable DTE or DCE interface port that supports the RS232, RS449, EIA530, EIA530-A, V.35, V.36 and X.21 protocols. Cable termination is provided on-chip, eliminating the need for discrete termination designs.

A complete DCE-to-DTE interface operating in EIA530 mode is shown in Figure 17. The LTC2847 half of each port is used to generate and appropriately terminate the clock and data signals. The LTC2845 is used to generate the control signals along with LL (local loopback),

RL (Remote Loop-Back), TM (Test Mode) and RI (Ring Indicate).

Mode Selection

The interface protocol is selected using the mode select pins M0, M1 and M2 (see Table 1).

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, the drivers and receivers will operate in V.28 (RS232) electrical mode. For the clock and data signals, the drivers and receivers will operate in V.35 electrical mode. The DCE/DTE pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected simply by plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable as shown in Figure 18. The internal pull-up current sources will ensure a binary 1 when a pin is left unconnected.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{IN} .

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APPLICATIONS INFORMATION

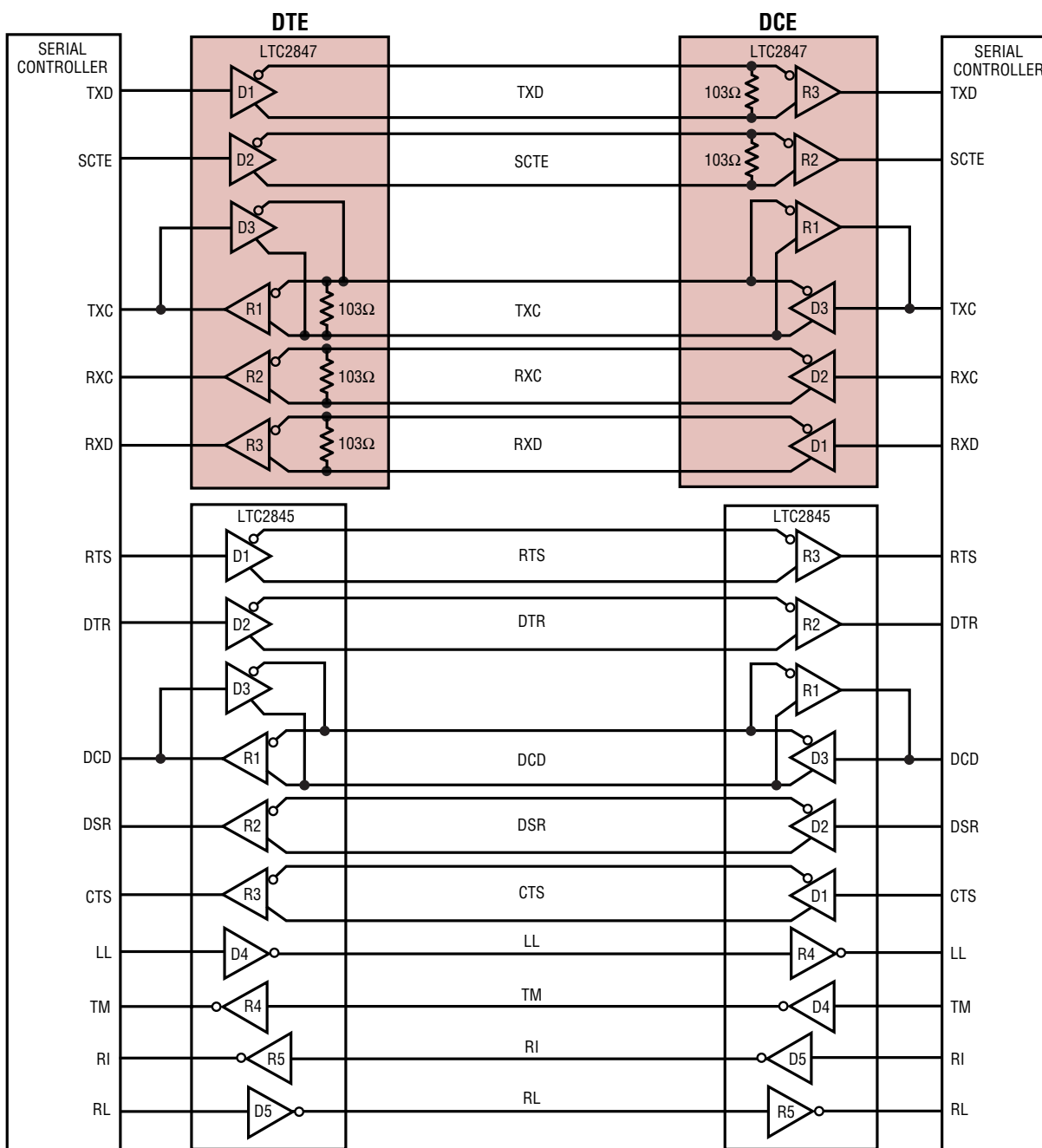


Figure 17. Complete Multiprotocol Interface in EIA530 Mode

When the cable is removed, leaving all mode pins unconnected, the LTC2847/LTC2845 will enter no-cable mode. In this mode the LTC2847/LTC2845 supply current drops to less than 1000 μ A and the LTC2847/LTC2845 driver outputs are forced into a high impedance state. At the same time, the R2 and R3 receivers of the LTC2847 are differentially terminated with 103 Ω and the other receiv-

ers on the LTC2847 and LTC2845 are terminated with 30k Ω to ground.

Cable Termination

Traditional implementations used expensive relays to switch resistors or required the user to change termination modules every time a new interface standard was

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APPLICATIONS INFORMATION

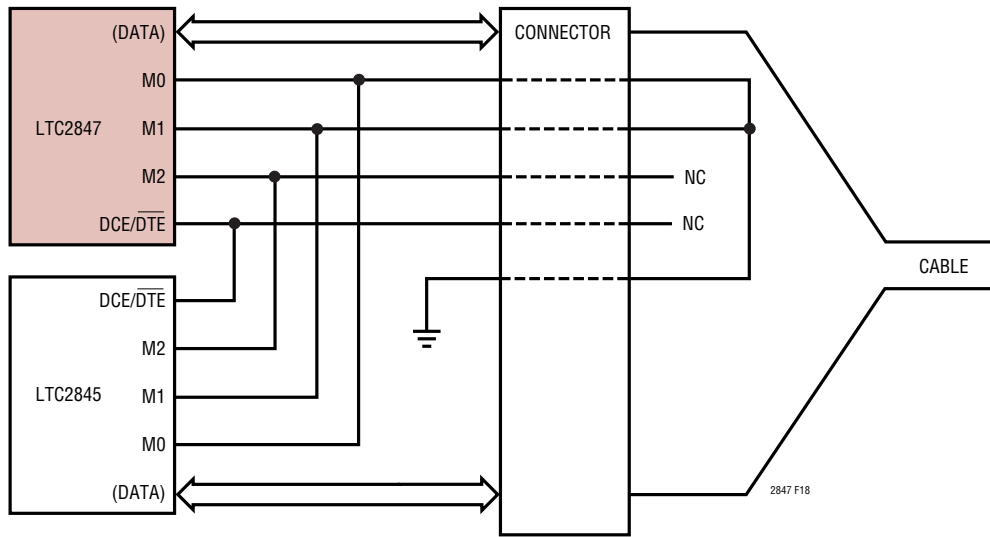


Figure 18. Single Port DCE V.35 Mode Selection in the Cable

selected. Switching the terminations with FETs is difficult because the FETs must remain off when the signal voltage is beyond the supply voltage. Alternatively, custom cables may contain termination in the cable head or route signals to various terminations on the board.

The LTC2847/LTC2845 chip set solves the cable termination switching problem by automatically providing the appropriate termination and switching on-chip for the V.10 (RS423), V.11 (RS422), V.28 (RS232) and V.35 electrical protocols.

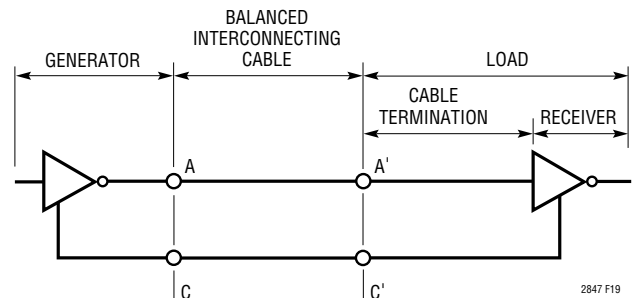


Figure 19. Typical V.10 Interface

V.10 (RS423) Interface

All V.10 drivers and receivers necessary for the RS449, EIA530, EIA530-A, V.36 and X.21 protocols are implemented on the LTC2845.

A typical V.10 unbalanced interface is shown in Figure 19. A V.10 single-ended generator with output A and ground C is connected to a differential receiver with input A' connected to A, and ground C' connected via the signal return to ground C. Usually, no cable termination is required for V.10 interfaces, but the receiver inputs must be compliant with the impedance curve shown in Figure 20.

The V.10 receiver configuration in the LTC2845 is shown in Figure 21. In V.10 mode, switch S3 inside the LTC2845 is turned off. The noninverting input is disconnected inside the LTC2845 receivers and connected to ground.

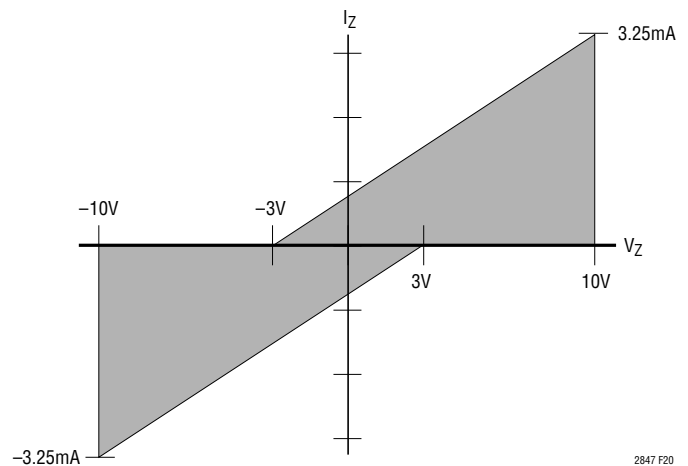


Figure 20. V.10 Receiver Input Impedance

APPLICATIONS INFORMATION

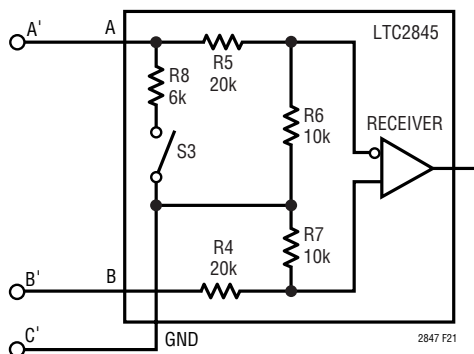


Figure 21. V.10 Receiver Configuration

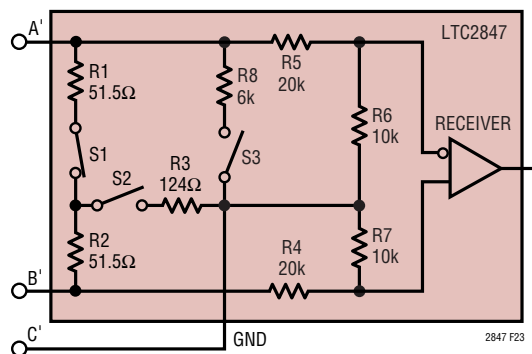


Figure 23. V.11 Receiver Configuration

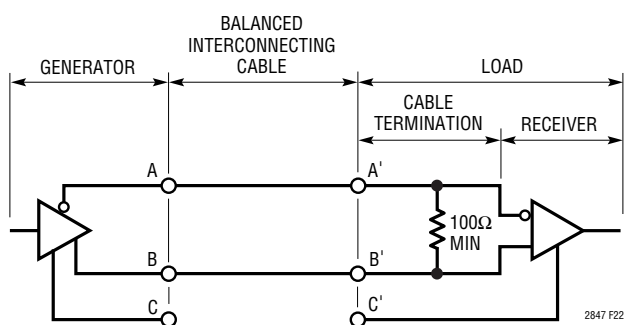


Figure 22. Typical V.11 Interface

The cable termination is then the 30k input impedance to ground of the LTC2845 V.10 receiver.

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 22. A V.11 differential generator with outputs A and B and ground C is connected to a differential receiver with input A' connected to A, input B' connected to B, and ground C' connected via the signal return to ground C. The V.11 interface has a differential termination at the receiver end that has a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is essential to prevent reflections from corrupting the data. The receiver inputs must also be compliant with the impedance curve shown in Figure 20.

In V.11 mode, all switches are off except S1 of the LTC2847's receivers which connects a 103Ω differential

termination impedance to the cable as shown in Figure 23¹. The LTC2845 only handles control signals, so no termination other than its V.11 receivers' 30k input impedance is necessary.

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 24. A V.28 single-ended generator with output A and ground C is connected to a single-ended receiver with input A' connected to A and ground C' connected via the signal return to ground C.

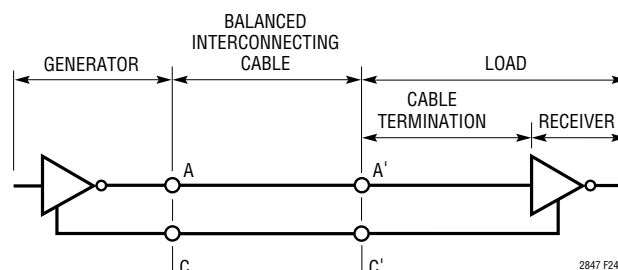


Figure 24. Typical V.28 Interface

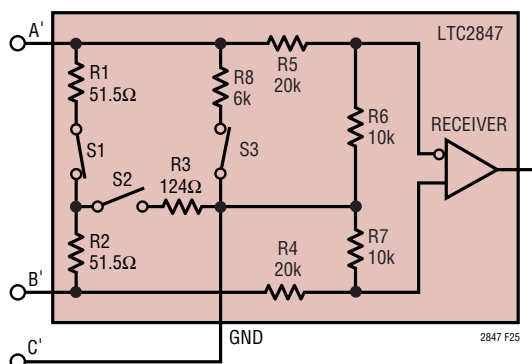


Figure 25. V.28 Receiver Configuration

¹Actually, there is no switch S1 in receivers R2 and R3. However, for simplicity, all termination networks on the LTC2847 can be treated identically if it is assumed that an S1 switch exists and is always closed on the R2 and R3 receivers.

APPLICATIONS INFORMATION

In V.28 mode, S3 is closed inside the LTC2847/LTC2845 which connects a 6k (R8) impedance to ground in parallel with 20k (R5) plus 10k (R6) for a combined impedance of 5k as shown in Figure 25. Proper termination is only provided when the B input of the receivers is floating, since S1 of the LTC2847's R2 and R3 receivers remains on in V.28 mode¹. The noninverting input is disconnected inside the LTC2847/LTC2845 receiver and connected to a TTL level reference voltage to give a 1.4V receiver trip point.

V.35 Interface

A typical V.35 balanced interface is shown in Figure 26. A V.35 differential generator with outputs A and B and ground C is connected to a differential receiver with input A' connected to A, input B' connected to B, and ground C' connected via the signal return to ground C. The V.35 interface requires a T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be $100\Omega \pm 10\Omega$, and the impedance between shorted terminals (A' and B') and ground (C') must be $150\Omega \pm 15\Omega$.

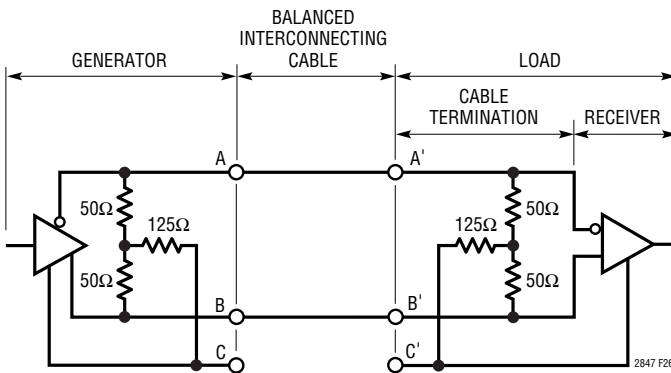


Figure 26. Typical V.35 Interface

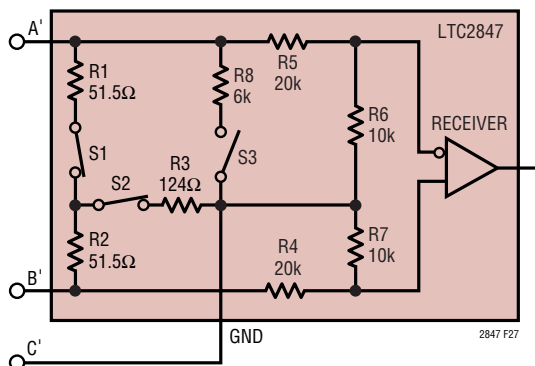


Figure 27. V.35 Receiver Configuration

In V.35 mode, both switches S1 and S2 inside the LTC2847 are on, connecting a T network impedance as shown in Figure 27. The 30k input impedance of the receiver is placed in parallel with the T network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω and the impedance between shorted terminals (A and B) and ground (C) must be $150\Omega \pm 15\Omega$.

No-Cable Mode

The no-cable mode ($M0 = M1 = M2 = 1$) is intended for the case when the cable is disconnected from the connector. The charge pump, bias circuitry, drivers and receivers are turned off, the driver outputs are forced into a high impedance state, and the V_{CC} supply current to the transceiver drops to less than $300\mu A$ while its V_{IN} supply current drops to less than $10\mu A$. Note that the LTC2847's R2 and R3 receivers continue to be terminated by a 103Ω differential impedance.

Charge Pump

The LTC2847 uses an internal capacitive charge pump to generate V_{DD} and V_{EE} as shown in Figure 28. A voltage doubler generates about 8V on V_{DD} and a voltage inverter generates about $-7.5V$ on V_{EE} . Four $1\mu F$ surface mounted tantalum or ceramic capacitors are required for C1, C2, C3 and C5. The V_{EE} capacitor C4 should be a minimum of $3.3\mu F$. All capacitors are 16V and should be placed as close as possible to the LTC2847 to reduce EMI.

Receiver Fail-Safe

All LTC2847/LTC2845 receivers feature fail-safe operation in all modes. If the receiver inputs are left floating or are shorted together by a termination resistor, the receiver output will always be forced to a logic high.

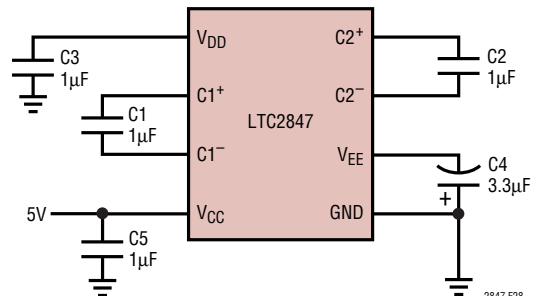


Figure 28. Charge Pump

TYPICAL APPLICATIONS

DTE vs DCE Operation

The DCE/ $\overline{\text{DTE}}$ pin acts as an enable for Driver 3/Receiver 1 in the LTC2847, and Driver 3/Receiver 1 in the LTC2845.

The LTC2847/LTC2845 can be configured for either DTE or DCE operation in one of two ways: a dedicated DTE or DCE port with a connector of appropriate gender or a port with one connector that can be configured for DTE or DCE operation by rerouting the signals to the LTC2847/LTC2845 using a dedicated DTE cable or dedicated DCE cable.

A dedicated DTE port using a DB-25 male connector is shown in Figure 29. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{IN} or GND on the mode select pins. A dedicated DCE port using a DB-25 female connector is shown in Figure 30.

A port with one DB-25 connector, that can be configured for either DTE or DCE operation is shown in Figure 31. The configuration requires separate cables for proper signal routing in DTE or DCE operation. For example, in DTE mode, the TXD signal is routed to Pins 2 and 14 via the LTC2847's Driver 1. In DCE mode, Driver 1 now routes the RXD signal to Pins 2 and 14.

Power Dissipation Calculations

The LTC2847 takes in $5V V_{\text{CC}}$. V_{DD} and V_{EE} are in turn produced from V_{CC} with an internal charge pump at approximately 80% and 70% efficiency respectively. Current drawn internally from V_{DD} or V_{EE} translates directly into a higher I_{CC} . The LTC2847 dissipates power according to the equation:

$$P_{\text{DISS}(2847)} = V_{\text{CC}} \cdot I_{\text{CC}} - N_{\text{D}} \cdot P_{\text{RT}} + N_{\text{R}} \cdot P_{\text{RT}} \quad (1)$$

P_{RT} refers to the power dissipated by each driver in a receiver termination on the far end of the cable while N_{D} is the number of drivers. Conversely, current from the far end drivers dissipate power $N_{\text{R}} \cdot P_{\text{RT}}$ in the internal receiver termination where N_{R} is the number of receivers.

LTC2847 Power Dissipation

Consider an LTC2847 in X.21, DCE mode (three V.11 drivers and two V.11 receivers). From the Electrical Characteristics Table, I_{CC} at no load = 14mA, I_{CC} at full load = 100mA. Each receiver termination is 100Ω (R_{RT}) and

current going into each receiver termination = $(100\text{mA} - 14\text{mA})/3 = 28.7\text{mA}$ (I_{RT}).

$$P_{\text{RT}} = (I_{\text{RT}})^2 \cdot R_{\text{RT}} \quad (2)$$

From Equation (2), $P_{\text{RT}} = 82.4\text{mW}$ and from Equation (1), DC power dissipation $P_{\text{DISS}(2847)} = 5V \cdot 100\text{mA} - 3 \cdot 82.4\text{mW} + 2 \cdot 82.4\text{mW} = 418\text{mW}$.

Consider the above example running at a baud rate of 10MBd. From the Typical Characteristic for "V.11 Mode I_{CC} vs Data Rate," the I_{CC} at 10MBd is 160mA. I_{CC} increases with baud rate due to driver transient dissipation. From Equation (1), AC power dissipation $P_{\text{DISS}(2847)} = 5V \cdot 160\text{mA} - 3 \cdot 82.4\text{mW} + 2 \cdot 82.4\text{mW} = 718\text{mW}$.

LTC2845 Power Dissipation

If a LTC2845 is used to form a complete DCE port with the LTC2847, it will be running in the X.21 mode (three V.11 drivers and two V.10 drivers, two V.11 receivers and two V.10 receivers, all with internal 30k termination). In addition to V_{CC} , it uses the V_{DD} and V_{EE} outputs from the LTC2847. Negligible power is dissipated in the large internal receiver termination of the LTC2845 so the $N_{\text{R}} \cdot P_{\text{RT}}$ term of Equation (1) can be omitted. Thus Equation (1) is modified as follows:

$$P_{\text{DISS}(2845)} = (V_{\text{CC}} \cdot I_{\text{CC}}) + (V_{\text{DD}} \cdot I_{\text{DD}}) + (V_{\text{EE}} \cdot I_{\text{EE}}) - N_{\text{D}} \cdot P_{\text{RT}} \quad (3)$$

Since power is drawn from the supplies of the LTC2847 (V_{DD} and V_{EE}) at less than 100% efficiency, the LTC2847 dissipates extra power to source $P_{\text{DISS}(2845)}$ and P_{RT} :

$$P_{\text{DISS1}(2847)} = 125\% \cdot (V_{\text{DD}} \cdot I_{\text{DD}}) + 143\% \cdot (V_{\text{EE}} \cdot I_{\text{EE}}) - P_{\text{DISS}(2845)} - N_{\text{D}} \cdot P_{\text{RT}} \\ = 25\% \cdot (V_{\text{DD}} \cdot I_{\text{DD}}) + 43\% \cdot (V_{\text{EE}} \cdot I_{\text{EE}}) \quad (4)$$

From the LTC2845 Electrical Characteristics Table, for $V_{\text{CC}} = 5V$, $V_{\text{DD}} = 8V$ and $V_{\text{EE}} = -5.5V$:

I_{CC} at no load	2.7mA
I_{CC} at full load with all drivers high	110mA
I_{EE} at no load	2mA
I_{EE} at full load with both V.10 drivers low	23mA
I_{DD} at no load	0.3mA
I_{DD} at full load	0.3mA

TYPICAL APPLICATIONS

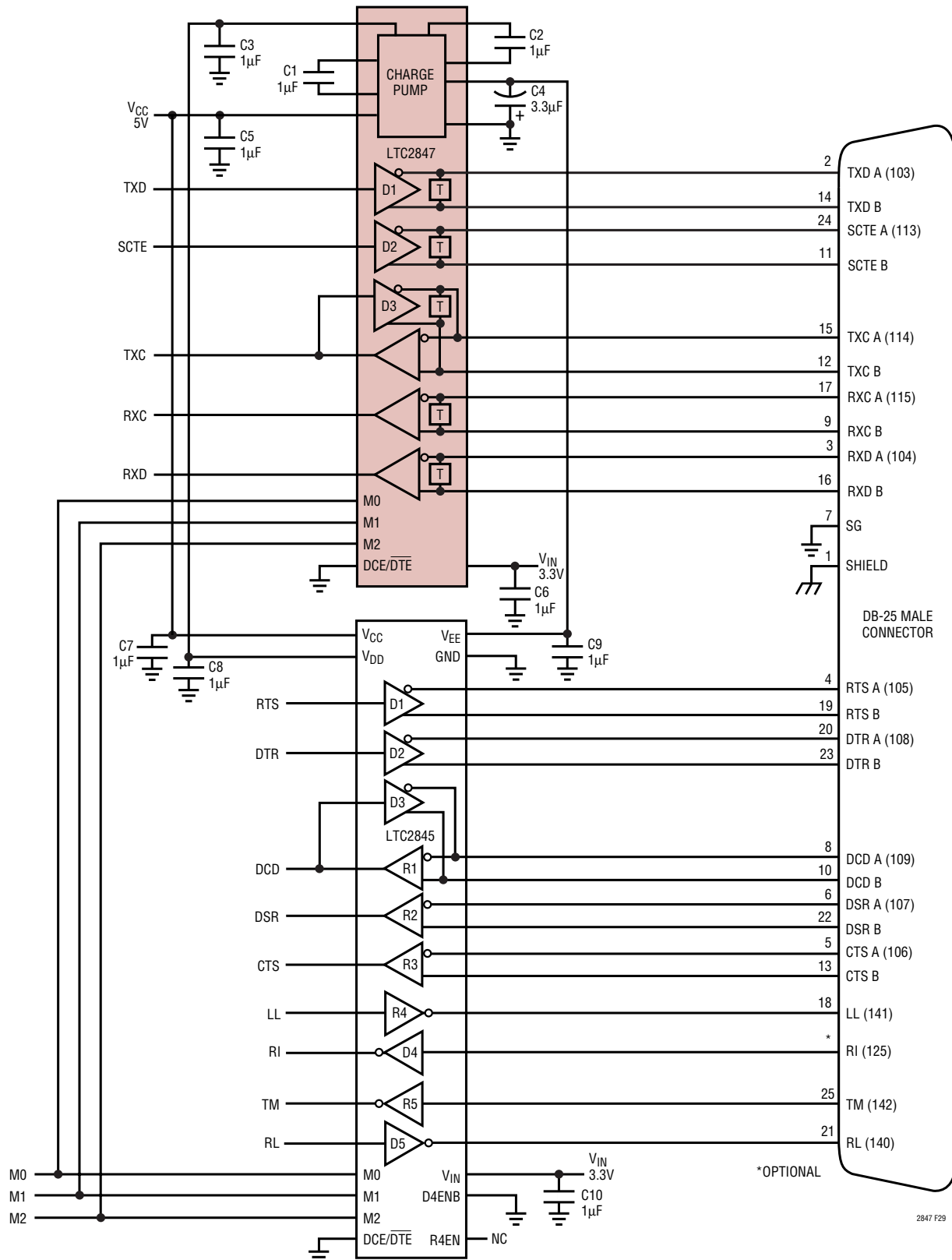


Figure 29. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector

TYPICAL APPLICATIONS

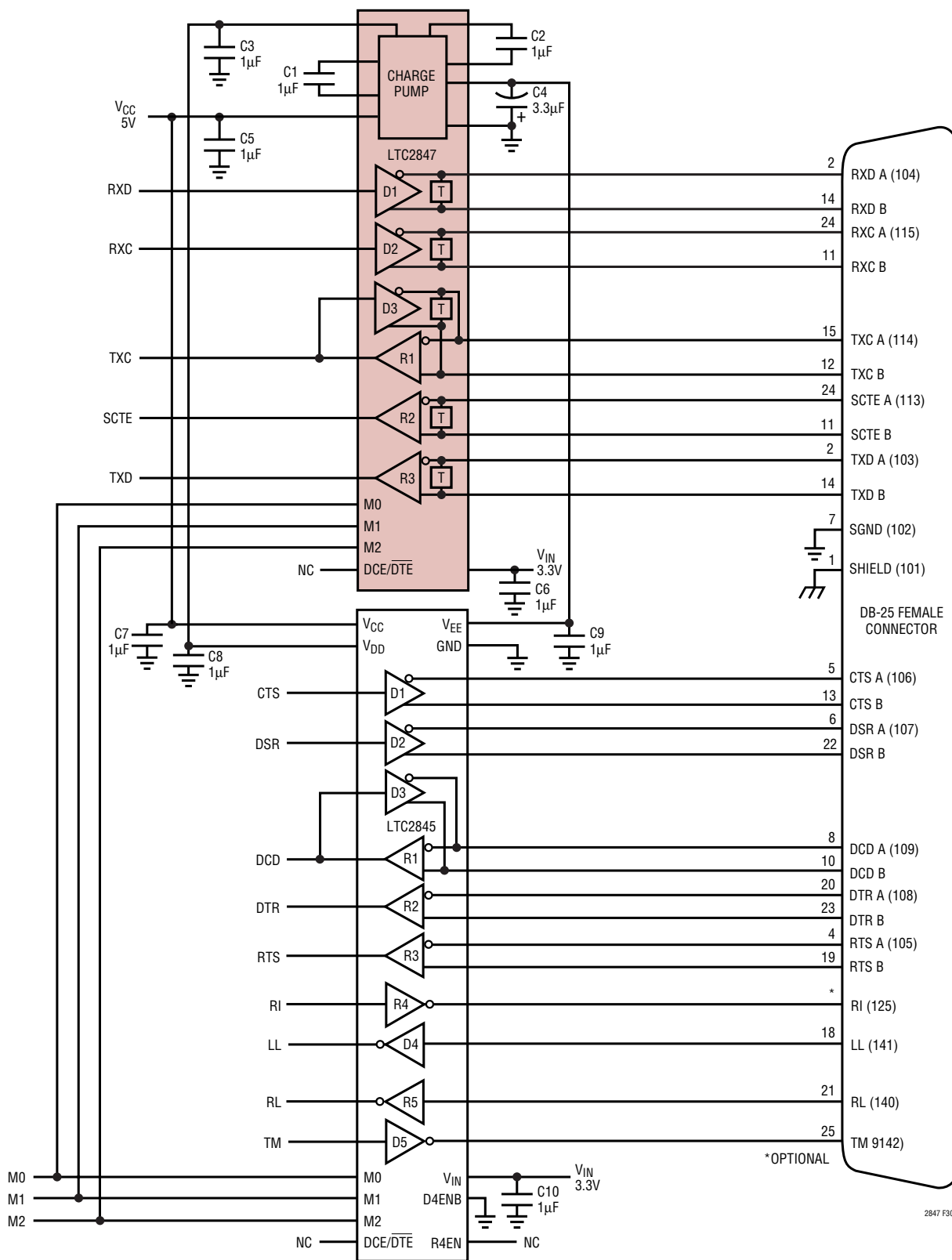


Figure 30. Controller-Selectable DCE Port with DB-25 Connector

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TYPICAL APPLICATIONS

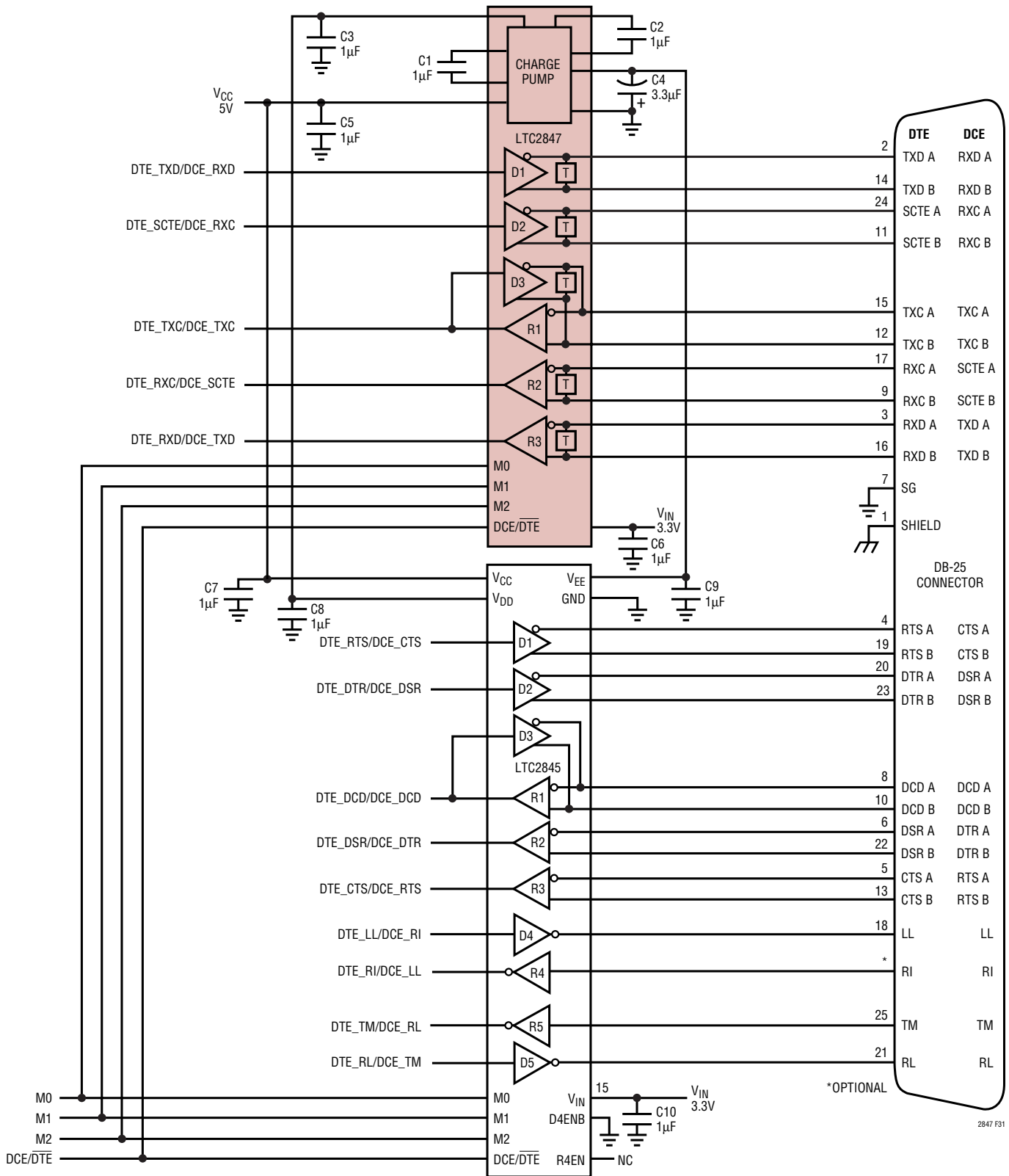
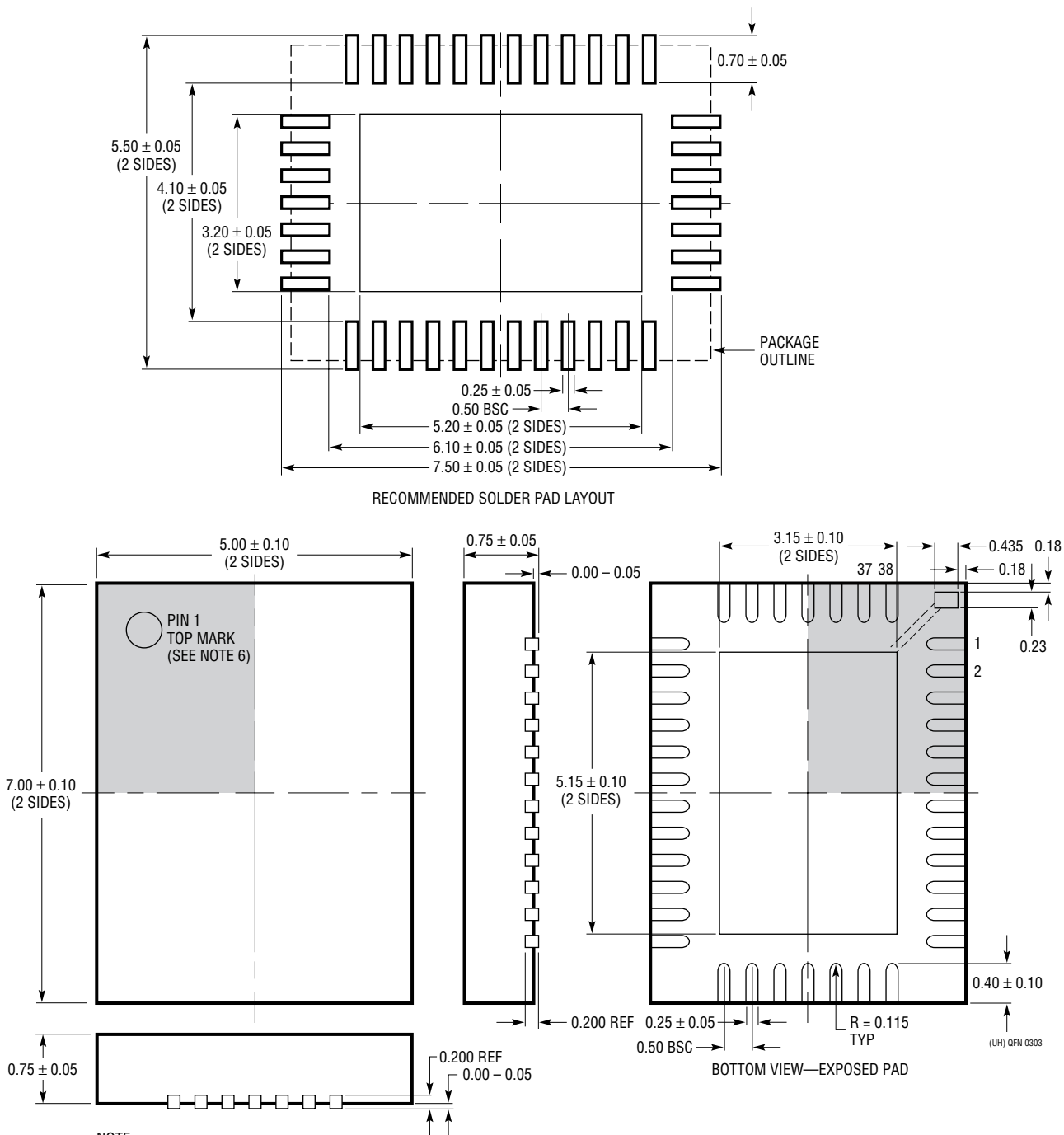


Figure 31. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

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PACKAGE DESCRIPTION

UHF Package 38-Lead Plastic QFN (5mm × 7mm) (Reference LTC DWG # 05-08-1701)



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE