

# 20Mbps RS485 Transceivers with Integrated Switchable Termination

## FEATURES

- **Integrated, Logic-Selectable 120Ω Termination Resistor**
- **20Mbps Max Data Rate**
- **No Damage or Latchup to ESD: ±15kV HBM**
- **High Input Impedance Supports 256 Nodes (C-, I-Grades)**
- **Operation Up to 105°C (LTC2859H)**
- **250kbps Low-EMI Mode**
- **Guaranteed Failsafe Receiver Operation Over the Entire Common Mode Range**
- **Current Limited Drivers and Thermal Shutdown**
- **Delayed Micropower Shutdown (5μA Max)**
- **Power Up/Down Glitch-Free Driver Outputs**
- **Low Operating Current (900μA Max in Receive Mode)**
- **Meets All TIA/EIA-485-A Specifications**
- **Available in 10-Pin 3mm × 3mm DFN, 12-Pin 4mm × 3mm DFN and 16-Pin SSOP Packages**

## APPLICATIONS

- **Low Power RS485/RS422 Transceiver**
- **Level Translator**
- **Backplane Transceiver**

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## DESCRIPTION

The LTC<sup>®</sup>2859 and LTC2861 are low power, 20Mbps RS485/422 transceivers operating on 5V supplies. The receiver includes a logic-selectable 120Ω termination, one-eighth unit load supporting up to 256 nodes per bus (C-, I-grades), and a failsafe feature that guarantees a high output state under conditions of floating or shorted inputs.

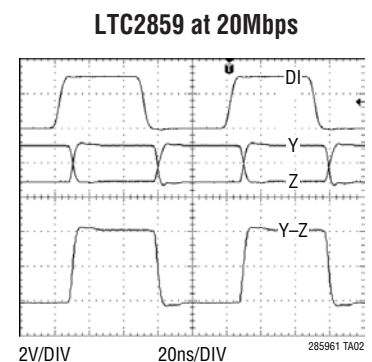
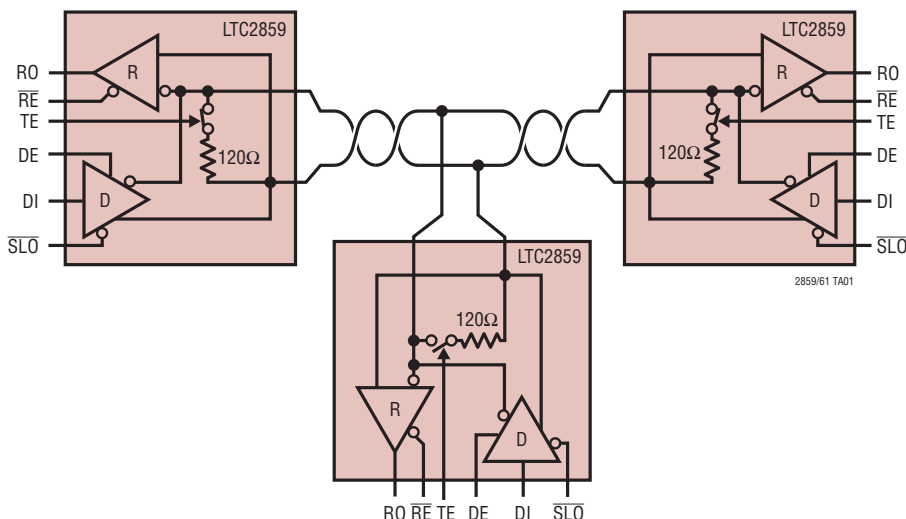
The driver features a logic-selectable low-EMI 250kbps operating mode, and maintains a high output impedance over the entire common mode range when disabled or when the supply is removed. Excessive power dissipation caused by bus contention or a fault is prevented by current limiting all outputs and by a thermal shutdown.

Enhanced ESD protection allows the LTC2859 and LTC2861 to withstand ±15kV (human body model) on the transceiver interface pins without latchup or damage.

## PRODUCT SELECTION GUIDE

PART NUMBER	DUPLEX	PACKAGE
LTC2859	Half	DFN-10
LTC2861	Full	SSOP-16, DFN-12

## TYPICAL APPLICATION



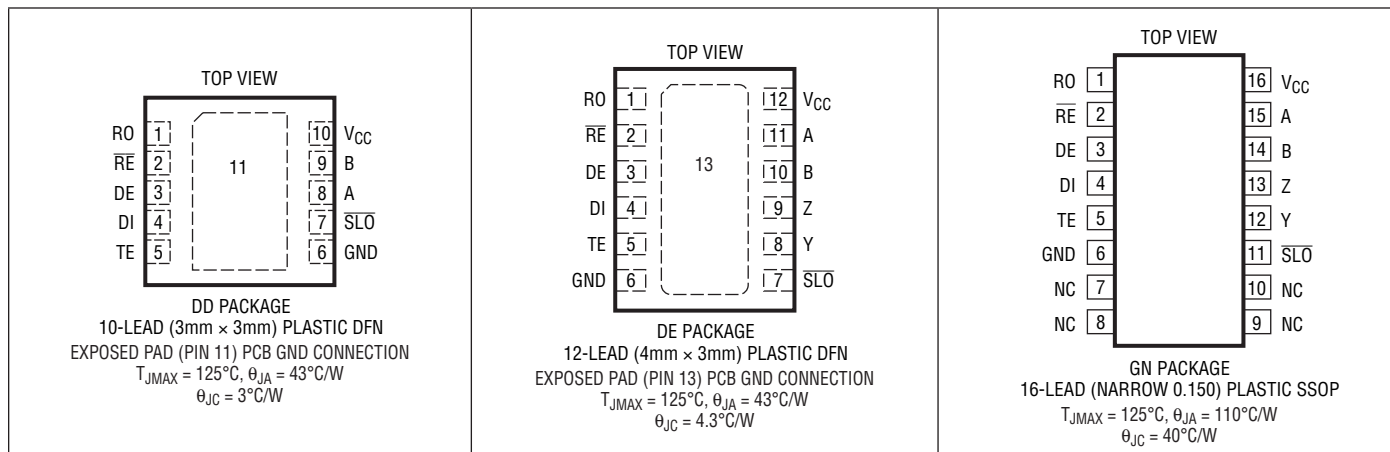
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# LTC2859/LTC2861

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.3V to 7V	Operating Temperature (Note 4)	
Logic Input Voltages ( $\overline{RE}$ , DE, DI, TE, $\overline{SLO}$ )	-0.3V to 7V	LTC2859C, LTC2861C	0°C to 70°C
Interface I/O:		LTC2859I, LTC2861I	-40°C to 85°C
A, B, Y, Z	( $V_{CC}$ - 15V) to +15V	LTC2859H	-40°C to 105°C
(A-B) or (B-A) with Terminator Enabled	6V	Storage Temperature Range	-65°C to 125°C
Receiver Output Voltage (RO)	-0.3V to ( $V_{CC}$ + 0.3V)	Lead Temperature (Soldering, 10 sec)	
		GN Package	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2861CDE#PBF	LTC2861CDE#TRPBF	2861	12-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2861IDE#PBF	LTC2861IDE#TRPBF	2861	12-Lead (4mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2861CGN#PBF	LTC2861CGN#TRPBF	2861	16-Lead Plastic SSOP	0°C to 70°C
LTC2861IGN#PBF	LTC2861IGN#TRPBF	2861I	16-Lead Plastic SSOP	-40°C to 85°C
LTC2859CDD#PBF	LTC2859CDD#TRPBF	LBNX	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2859IDD#PBF	LTC2859IDD#TRPBF	LBNX	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2859HDD#PBF	LTC2859HDD#TRPBF	LBNX	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$  unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Driver</b>						
$ V_{OD} $	Differential Driver Output Voltage	$R = \infty$ , $I_O = 0\text{mA}$ , $V_{CC} = 4.5\text{V}$ (Figure 1) $R = 27\Omega$ (RS485), $V_{CC} = 4.5\text{V}$ (Figure 1) $R = 50\Omega$ (RS422), $V_{CC} = 4.5\text{V}$ (Figure 1)	● ● ●	1.5 2.0	$V_{CC}$ $V_{CC}$ $V_{CC}$	V V V
$\Delta V_{OD} $	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$ (Figure 1)	●		0.2	V
$V_{OC}$	Driver Common Mode Output Voltage	$R = 27\Omega$ or $R = 50\Omega$ (Figure 1)	●		3.0	V
$\Delta V_{OC} $	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$ (Figure 1)	●		0.2	V
$I_{OZD}$	Driver Three-State (High Impedance) Output Current on Y and Z	$DE = 0\text{V}$ , $V_O = -7\text{V}$ , $+12\text{V}$ (LTC2861 Only)	●		$\pm 10$	$\mu\text{A}$
$I_{OSD}$	Maximum Driver Short-Circuit Current	$-7\text{V} \leq (Y \text{ or } Z) \leq 12$ (Figure 2)	●	$\pm 120$	$\pm 250$	$\text{mA}$
<b>Receiver</b>						
$I_{IN2}$	Receiver Input Current (A, B)	$DE = TE = 0\text{V}$ , $V_{CC} = 0\text{V}$ or $5\text{V}$ , $V_A$ or $V_B = 12\text{V}$ , Other at $0\text{V}$ (H-Grade) $DE = TE = 0\text{V}$ , $V_{CC} = 0\text{V}$ or $5\text{V}$ , $V_A$ or $V_B = -7\text{V}$ , Other at $0\text{V}$ (H-Grade)	● ● ● ●		125 250	$\mu\text{A}$ $\mu\text{A}$
$V_{TH}$	Receiver Differential Input Threshold Voltage	$-7\text{V} \leq V_{CM} \leq 12$	●		$\pm 0.2$	V
$\Delta V_{TH}$	Receiver Input Hysteresis	$V_{CM} = 0\text{V}$		25		$\text{mV}$
$V_{OH}$	Receiver Output HIGH Voltage	$I_O = -4\text{mA}$ , $V_{ID} = 200\text{mV}$ , $V_{CC} = 4.5\text{V}$	●	2.4		V
$V_{OL}$	Receiver Output LOW Voltage	$I_O = 4\text{mA}$ , $V_{ID} = -200\text{mV}$ , $V_{CC} = 4.5\text{V}$	●		0.4	V
$I_{OZR}$	Receiver Three-State (High Impedance) Output Current on RO	$\overline{RE} = 5\text{V}$ , $0\text{V} \leq V_O \leq V_{CC}$	●		$\pm 1$	$\mu\text{A}$
$R_{IN}$	Receiver Input Resistance	$\overline{RE} = 5\text{V}$ or $0\text{V}$ , $DE = TE = 0\text{V}$ $-7\text{V} \leq V_A = V_B \leq 12\text{V}$ (H-Grade)	● ●	96 48	125 125	$\text{k}\Omega$ $\text{k}\Omega$
$R_{TERM}$	Receiver Input Terminating Resistor	$TE = 5\text{V}$ , $V_{AB} = 2\text{V}$ , $V_B = -7, 0, 10\text{V}$ (Figure 7)	●	108	120 156	$\Omega$
<b>Logic</b>						
$V_{IH}$	Logic Input High Voltage	$DE, DI, \overline{RE}, TE, \overline{SLO}$ , $V_{CC} = 4.5\text{V}$	●	2		V
$V_{IL}$	Logic Input Low Voltage	$DE, DI, \overline{RE}, TE, \overline{SLO}$ , $V_{CC} = 4.5\text{V}$	●		0.8	V
$I_{IN1}$	Logic Input Current	$DE, DI, \overline{RE}, TE, \overline{SLO}$	●		0 $\pm 10$	$\mu\text{A}$
<b>Supplies</b>						
$I_{SHDN}$	Supply Current in Shutdown Mode	$DE = 0\text{V}$ , $\overline{RE} = V_{CC}$ , $TE = 0\text{V}$	●	0	5	$\mu\text{A}$
$I_{CCR}$	Supply Current in Receive Mode	No Load, $DE = 0\text{V}$ , $\overline{RE} = 0\text{V}$ , $TE = 0\text{V}$	●	540	900	$\mu\text{A}$
$I_{CCT}$	Supply Current in Transmit Mode	No Load, $DE = V_{CC}$ , $\overline{RE} = V_{CC}$ , $\overline{SLO} = V_{CC}$ , $TE = 0\text{V}$	●	630	1000	$\mu\text{A}$
$I_{CCTS}$	Supply Current in Transmit SLO Mode	No Load, $DE = V_{CC}$ , $\overline{RE} = V_{CC}$ , $\overline{SLO} = 0\text{V}$ , $TE = 0\text{V}$	●	670	1100	$\mu\text{A}$
$I_{CCL}$	Supply Current in Loopback Mode (Both Driver and Receiver Enabled)	No Load, $DE = V_{CC}$ , $\overline{RE} = 0\text{V}$ , $\overline{SLO} = V_{CC}$ , $TE = 0\text{V}$	●	660	1100	$\mu\text{A}$
$I_{CCRT}$	Supply Current in Termination Mode	$DE = 0\text{V}$ , $\overline{RE} = V_{CC}$ , $TE = V_{CC}$ , $\overline{SLO} = V_{CC}$	●	640	1180	$\mu\text{A}$

## SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $T_E = 0$  unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Driver in Normal Mode (SLO HIGH)</b>						
$f_{MAX}$	Maximum Data Rate	Note 3	●	20		Mbps
$t_{PLHD}$ , $t_{PHLD}$	Driver Input to Output	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	10	50	ns
$\Delta t_{PD}$	Driver Input to Output Difference $ t_{PLHD} - t_{PHLD} $	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	1	6	ns
$t_{SKEWD}$	Driver Output Y to Output Z	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	1	$\pm 6$	ns
$t_{RD}$ , $t_{FD}$	Driver Rise or Fall Time	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	4	12.5	ns
$t_{ZLD}$ , $t_{ZHD}$ , $t_{LZD}$ , $t_{HZD}$	Driver Enable or Disable Time	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , $\overline{RE} = 0$ (Figure 4)	●		70	ns
$t_{ZHSD}$ , $t_{ZLSD}$	Driver Enable from Shutdown	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , $\overline{RE} = V_{CC}$ (Figure 4)	●		8	$\mu\text{s}$
$t_{SHDN}$	Time to Shutdown	$(DE = \downarrow, \overline{RE} = V_{CC})$ or $(DE = 0, \overline{RE} \uparrow)$ (Figure 4)	●		100	ns
<b>Driver in SLO Mode (SLO LOW)</b>						
$f_{MAXS}$	Maximum Data Rate	Note 3	●	250		kbps
$t_{PLHDS}$ , $t_{PHLDS}$	Driver Input to Output	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	0.95	1.5	$\mu\text{s}$
$\Delta t_{PDS}$	Driver Input to Output Difference $ t_{PLHR} - t_{PHLR} $	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	50	500	ns
$t_{SKEWDS}$	Driver Output A to Output B	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3) (H-Grade)	● ●	200 200	$\pm 500$ $\pm 750$	ns ns
$t_{RDS}$ , $t_{FDS}$	Driver Rise or Fall Time	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 3)	●	0.9	1.5	$\mu\text{s}$
$t_{ZHDS}$ , $t_{ZLDS}$	Driver Enable Time	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , $\overline{RE} = 0$ (Figure 4)	●		300	ns
$t_{LZDS}$ , $t_{HZDS}$	Driver Disable Time	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , $\overline{RE} = 0$ (Figure 4)	●		70	ns
$t_{ZHSDS}$ , $t_{ZLSDS}$	Driver Enable from Shutdown	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ , $\overline{RE} = V_{CC}$ (Figure 4)	●		8	$\mu\text{s}$
$t_{SHDNS}$	Time to Shutdown	$(DE = 0, \overline{RE} = \uparrow)$ or $(DE = \downarrow, \overline{RE} = V_{CC})$ (Figure 4)	●		500	ns
<b>Receiver</b>						
$t_{PLHR}$ , $t_{PHLR}$	Receiver Input to Output	$C_L = 15\text{pF}$ , $V_{CM} = 1.5\text{V}$ , $ V_{AB}  = 1.5\text{V}$ , $t_R$ and $t_F < 4\text{ns}$ (Figure 5)	●	50	70	ns
$t_{SKEWR}$	Differential Receiver Skew $ t_{PLHR} - t_{PHLR} $	$C_L = 15\text{pF}$ (Figure 5)	●	1	6	ns
$t_{RR}$ , $t_{FR}$	Receiver Output Rise or Fall Time	$C_L = 15\text{pF}$ (Figure 5)	●	3	12.5	ns
$t_{ZLR}$ , $t_{ZHR}$ , $t_{LZR}$ , $t_{HZR}$	Receiver Enable/Disable	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ , $DE = V_{CC}$ (Figure 6) $DI = 0$ or $V_{CC}$	●		50	ns
$t_{ZHRS}$ , $t_{ZLSR}$	Receiver Enable from Shutdown	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ , $DE = 0\text{V}$ (Figure 6) $DI = 0$ or $V_{CC}$	●		8	$\mu\text{s}$
$t_{RTEN}$ , $t_{RTZ}$	Termination Enable or Disable Time	$V_B = 0\text{V}$ , $V_{AB} = 2\text{V}$ , $\overline{RE} = V_{CC}$ , $DE = 0\text{V}$ (Figure 7)	●		100	$\mu\text{s}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

**Note 3:** Maximum data rate is guaranteed by other measured parameters and is not tested directly.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

TEST CIRCUITS

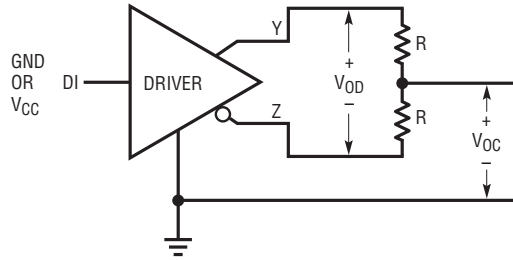


Figure 1. Driver DC Characteristics

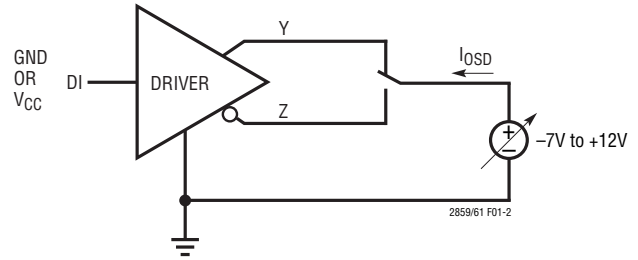


Figure 2. Driver Output Short-Circuit Current

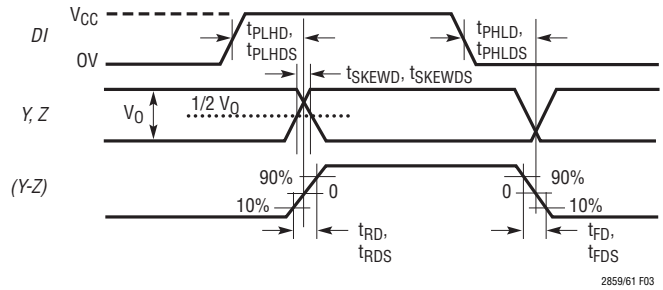
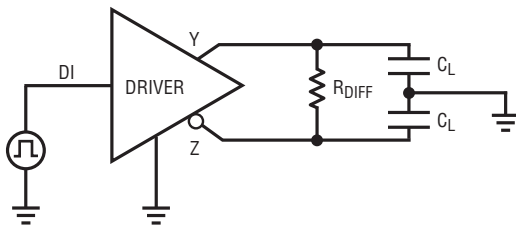


Figure 3. Driver Timing Measurement

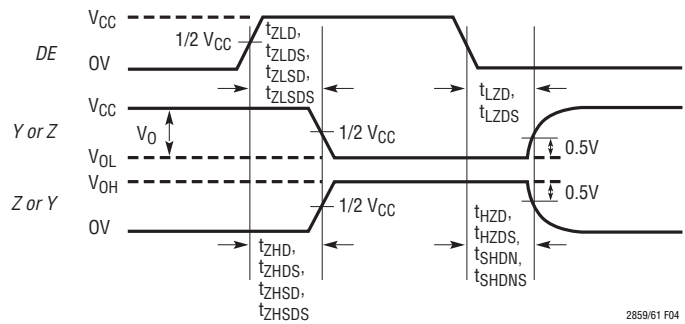
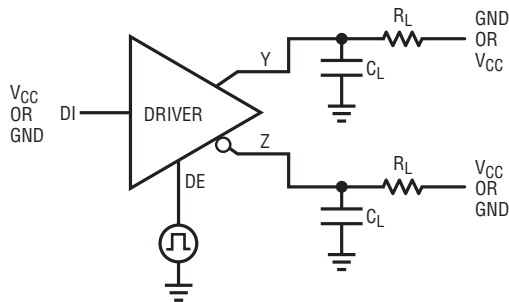
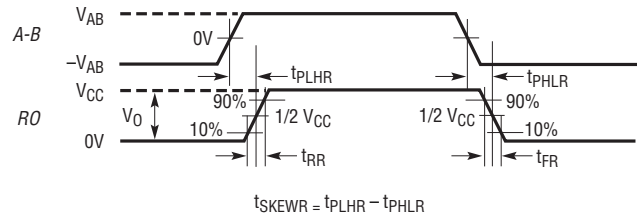
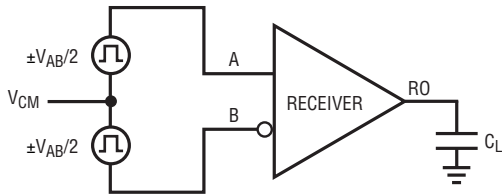


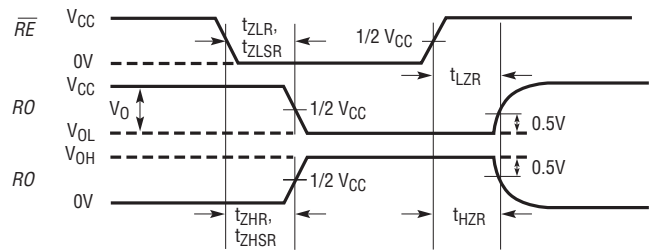
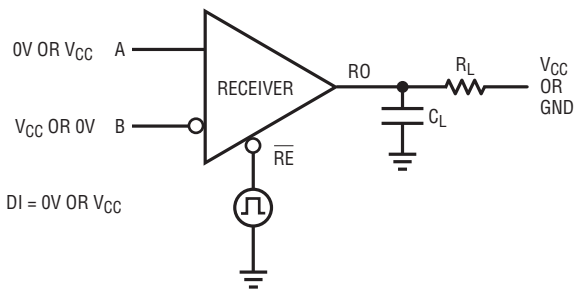
Figure 4. Driver Enable and Disable Timing Measurement

## TEST CIRCUITS



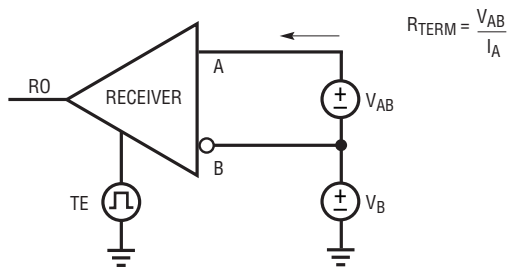
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Figure 5. Receiver Propagation Delay Measurements

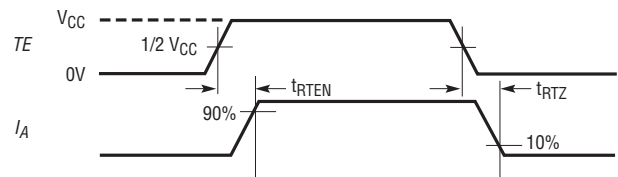


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Figure 6. Receiver Enable/Disable Time Measurements



$$R_{TERM} = \frac{V_{AB}}{I_A}$$

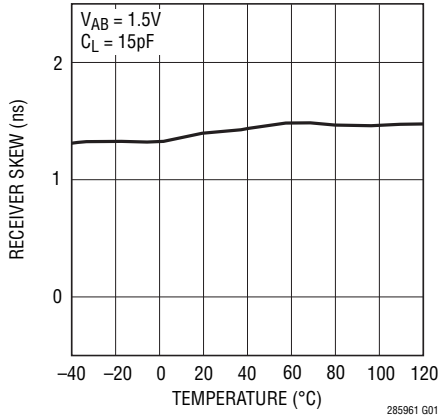


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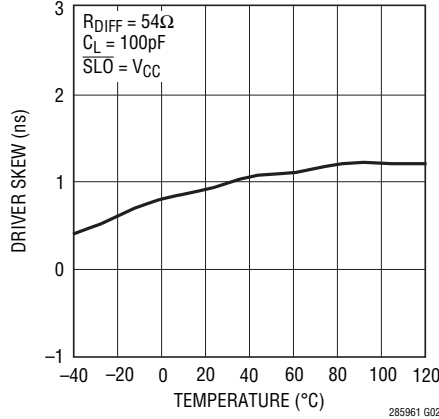
Figure 7. Termination Resistance and Timing Measurements

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ , unless otherwise noted.

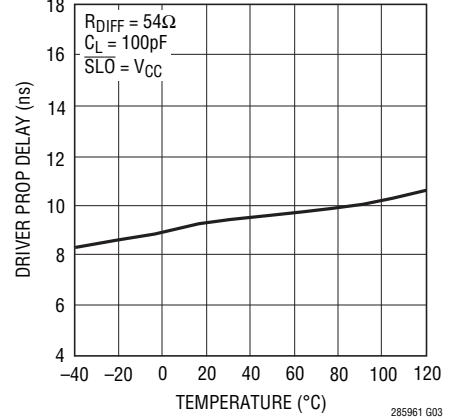
**Receiver Skew vs Temperature**



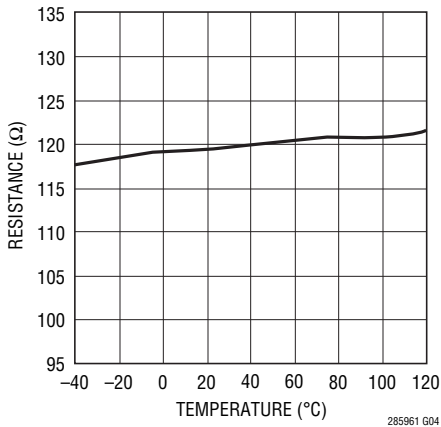
**Driver Skew vs Temperature**



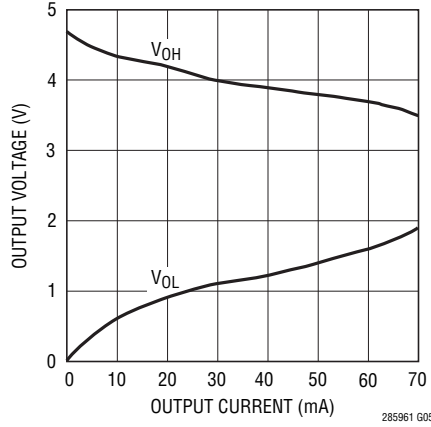
**Driver Propagation Delay vs Temperature**



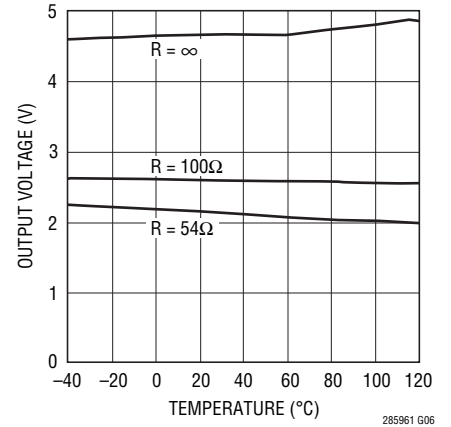
**$R_{TERM}$  vs Temperature**



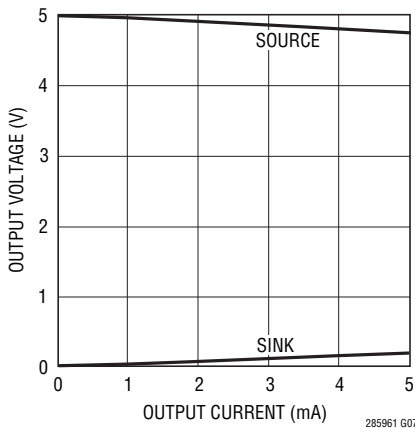
**Driver Output Low/High Voltage vs Output Current**



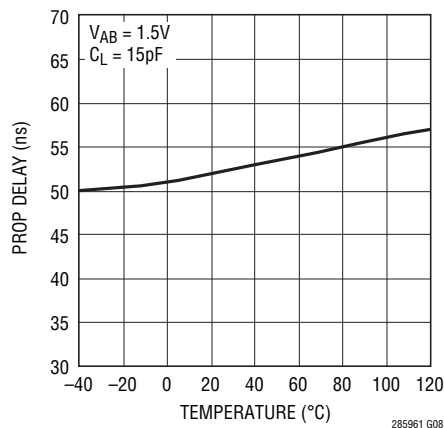
**Driver Differential Output Voltage vs Temperature**



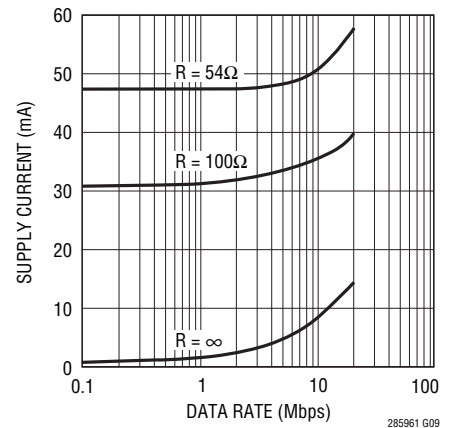
**Receiver Output Voltage vs Output Current (Source and Sink)**



**Receiver Propagation Delay vs Temperature**



**Supply Current vs Data Rate**



## PIN FUNCTIONS (DD/DE/GN)

**RO (Pin 1):** Receiver Output. If the receiver output is enabled ( $\overline{RE}$  low) and  $A > B$  by 200mV, then RO will be high. If  $A < B$  by 200mV, then RO will be low. If the receiver inputs are open, shorted, or terminated without a valid signal, RO will be high.

**$\overline{RE}$  (Pin 2):** Receiver Enable. A low enables the receiver. A high input forces the receiver output into a high impedance state.

**DE (Pin 3):** Driver Enable. A high on DE enables the driver. A low input will force the driver outputs into a high impedance. If  $\overline{RE}$  is high with DE and TE LOW, the part will enter a low power shutdown state.

**DI (Pin 4):** Driver Input. If the driver outputs are enabled (DE HIGH), then a low on DI forces the driver positive output LOW and negative output HIGH. A high on DI, with the driver outputs enabled, forces the driver positive output HIGH and negative output LOW.

**TE (Pin 5):** Internal Termination Resistance Enable. A high input will connect a termination resistor (120 $\Omega$  typical) between pins A and B.

**GND (Pins 6,11/6,13/6):** Ground. Pins 11 and 13 are backside thermal pad, connected to Ground.

**$\overline{SLO}$  (Pins 7/7/11):** Driver Slew Rate Control. A low input will force the driver into a reduced slew rate mode.

**Y (Pins -/8/12):** Positive Driver Output for LTC2861.

**Z (Pins -/9/13):** Negative Driver Output for LTC2861.

**B (Pins 9/10/14):** Negative Receiver Input (and Negative Driver Output for LTC2859).

**A (Pins 8/11/15):** Positive Receiver Input (and Positive Driver Output for LTC2859).

**V<sub>CC</sub> (Pins 10/12/16):** Positive Supply.  $4.5V < V_{CC} < 5.5V$ . Bypass with 0.1 $\mu$ F ceramic capacitor.



## FUNCTION TABLES

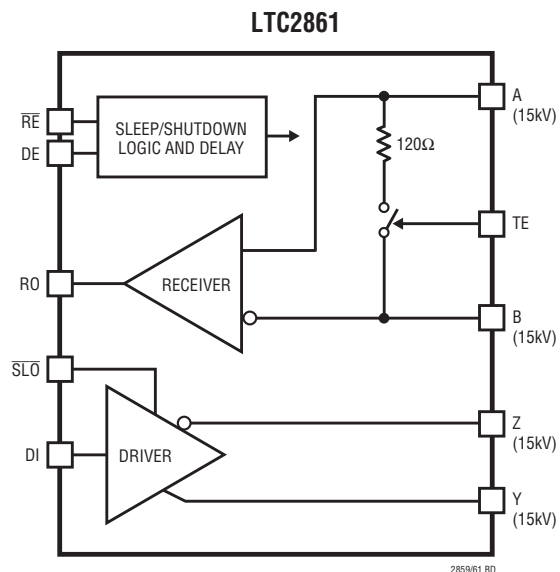
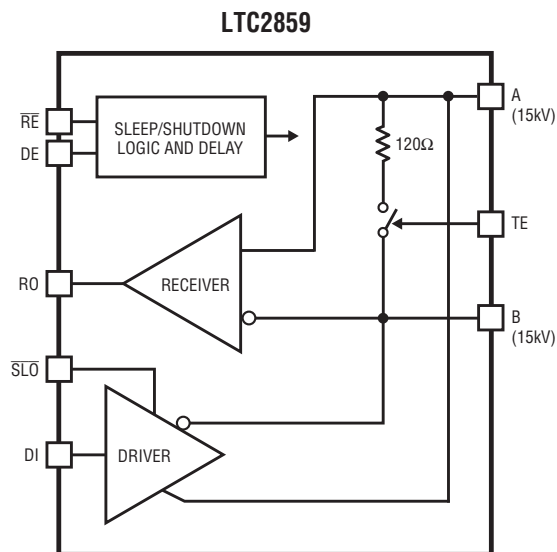
## LTC2859

LOGIC INPUTS			MODE	A, B	RO	TERMINATOR
DE	$\overline{RE}$	TE				
0	0	0	Receive	$R_{IN}$	Enabled	Off
0	0	1	Receive with Term	$R_{IN}$	Enabled	On
0	1	0	Shutdown	$R_{IN}$	Hi-Z	Off
0	1	1	Term Only	$R_{IN}$	Hi-Z	On
1	0	0	Transmit with Receive	Driven	Enabled	Off
1	0	1	Transmit with Receive and Term	Driven	Enabled	On
1	1	0	Transmit	Driven	Hi-Z	Off
1	1	1	Transmit with Term	Driven	Hi-Z	On

## LTC2861

LOGIC INPUTS			MODE	A, B	Y, Z	RO	TERMINATOR
DE	$\overline{RE}$	TE					
0	0	0	Receive	$R_{IN}$	Hi-Z	Enabled	Off
0	0	1	Receive with Term	$R_{IN}$	Hi-Z	Enabled	On
0	1	0	Shutdown	$R_{IN}$	Hi-Z	Hi-Z	Off
0	1	1	Term Only	$R_{IN}$	Hi-Z	Hi-Z	On
1	0	0	Transmit with Receive	$R_{IN}$	Driven	Enabled	Off
1	0	1	Transmit with Receive and Term	$R_{IN}$	Driven	Enabled	On
1	1	0	Transmit	$R_{IN}$	Driven	Hi-Z	Off
1	1	1	Transmit with Term	$R_{IN}$	Driven	Hi-Z	On

## BLOCK DIAGRAMS



285961 RD

285961fc

## APPLICATIONS INFORMATION

### Driver

The driver provides full RS485 and RS422 compatibility. When enabled, if DI is high, Y-Z is positive for the full duplex device (LTC2861) and A-B is positive for the half-duplex device (LTC2859).

When the driver is disabled, both outputs are high-impedance. For the full duplex LTC2861, the leakage on the driver output pins is guaranteed to be less than  $10\mu\text{A}$  over the entire common mode range of  $-7\text{V}$  to  $+12\text{V}$ . On the half-duplex LTC2859, the impedance is dominated by the receiver input resistance,  $R_{\text{IN}}$ .

### Driver Overvoltage and Overcurrent Protection

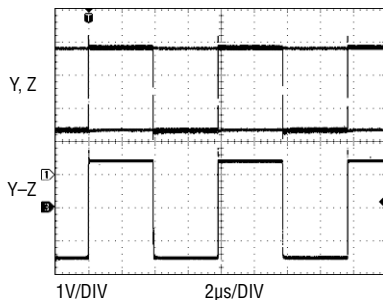
The driver outputs are protected from short circuits to any voltage within the Absolute Maximum range of ( $V_{\text{CC}} - 15\text{V}$ ) to  $+15\text{V}$ . The maximum current in this condition is  $250\text{mA}$ . If the pin voltage exceeds about  $\pm 10\text{V}$ , current limit folds back to about half of the peak value to reduce overall power dissipation and avoid damaging the part.

The LTC2859/LTC2861 also feature thermal shutdown protection that disables the driver, terminator, and receiver in case of excessive power dissipation.

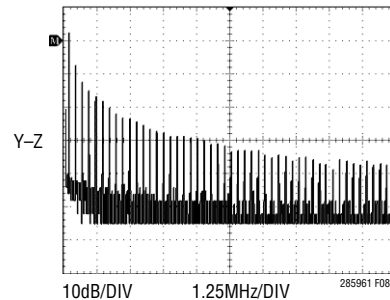
### $\overline{\text{SLO}}$ Mode: Slew Limiting for EMI Emissions Control

The LTC2859/LTC2861 feature a logic-selectable reduced-slew mode ( $\overline{\text{SLO}}$  mode) that softens the driver output edges to control the high frequency EMI emissions from equipment and data cables. The reduced slew rate mode is entered by taking the  $\overline{\text{SLO}}$  pin low, where the data rate is limited to about  $250\text{kbps}$ . Slew limiting also mitigates the adverse effects of imperfect transmission line termination caused by stubs or mismatched cables.

Figures 8a and 8b show the LTC2861 driver outputs in normal and  $\overline{\text{SLO}}$  mode with their corresponding frequency spectrums operating at  $250\text{kbps}$ .  $\overline{\text{SLO}}$  mode significantly reduces the high frequency harmonics.

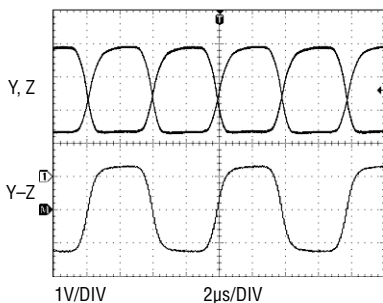


Driver Output at  $125\text{kHz}$  into  $100\Omega$  Resistor

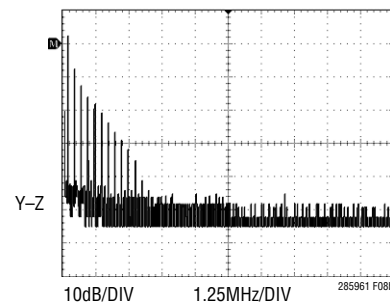


Frequency Spectrum of the Same Signal

Figure 8a. Driver Output in Normal Mode



Driver Output at  $125\text{kHz}$  into  $100\Omega$  Resistor



Frequency Spectrum of the Same Signal

Figure 8b. Driver Output in  $\overline{\text{SLO}}$  Mode

## APPLICATIONS INFORMATION

### Receiver and Failsafe

With the receiver enabled, when the absolute value of the differential voltage between the A and B pins is greater than 200mV, the state of RO will reflect the polarity of (A-B).

The LTC2859/LTC2861 have a failsafe feature that guarantees the receiver output to be in a logic HIGH state when the inputs are either shorted, left open, or terminated (externally or internally), but not driven for more than about 3 $\mu$ s. The delay prevents signal zero crossings from being interpreted as shorted inputs and causing RO to go high inadvertently. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of -7V to +12V.

The receiver output is internally driven high (to  $V_{CC}$ ) or low (to ground) with no external pull-up needed. When the receiver is disabled the RO pin becomes Hi-Z with leakage of less than  $\pm 1\mu$ A for voltages within the supply range.

### Receiver Input Resistance

The receiver input resistance from A or B to ground is greater than 96k permitting up to a total of 256 receivers per system without exceeding the RS485 receiver load-

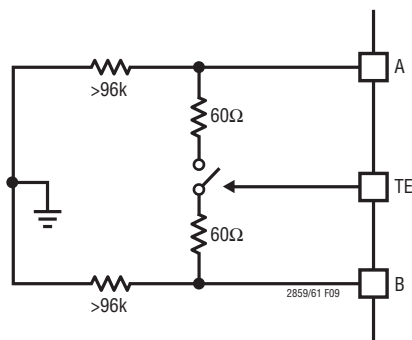


Figure 9. Equivalent Input Resistance into A and B (on the LTC2859, Valid if Driver is Disabled)

ing specification. High temperature H-Grade operation reduces the minimum input resistance to 48k permitting 128 receivers on the bus. The input resistance of the receiver is unaffected by enabling/disabling the receiver or by powering/unpowering the part. The equivalent input resistance looking into A and B is shown in Figure 9.

### Switchable Termination

Proper cable termination is very important for good signal fidelity. If the cable is not terminated with its characteristic impedance, reflections will result in distorted waveforms.

The LTC2859/LTC2861 are the first RS485 transceivers to offer integrated switchable termination resistors on the receiver input pins. This provides the tremendous advantage of being able to easily change, through logic control, the proper line termination for optimal performance when configuring transceiver networks.

When the TE pin is high, the termination resistor is enabled and the differential resistance from A to B is  $120\Omega$ . Figure 10 shows the I/V characteristics between pins A and B with the termination resistor enabled and disabled. The resistance is maintained over the entire RS485 common mode range of -7V to +12V as shown in Figure 11.

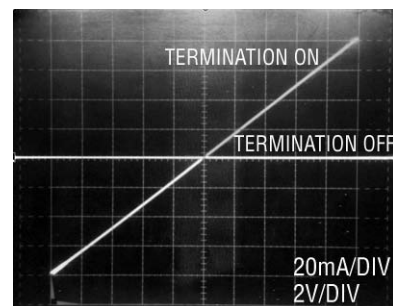


Figure 10. Curve Trace Between A and B with Termination Enabled and Disabled

## APPLICATIONS INFORMATION

The integrated termination resistor has a high frequency response which does not limit performance at the maximum specified data rate. Figure 12 shows the magnitude and phase of the termination impedance vs frequency. The termination resistor cannot be enabled by TE if the device is unpowered or in thermal shutdown mode.

### Supply Current

The unloaded static supply currents in the LTC2859/LTC2861 are very low—typically under 700 $\mu$ A for all modes of operation without the internal terminator enabled. In applications with resistively terminated cables, the supply current is dominated by the driver load. For example, when using two 120 $\Omega$  terminators with a differential driver output voltage of 2V, the DC current is 33mA, which is sourced by the positive voltage supply. This is true whether the terminators are external or internal such as in the LTC2859/LTC2861. Power supply current increases with toggling data due to capacitive loading and this term can increase significantly at high data rates. Figure 13 shows supply current vs data rate for two different capacitive loads (for the circuit configuration of Figure 3).

### High Speed Considerations

A ground plane layout is recommended for the LTC2859/LTC2861. A 0.1 $\mu$ F bypass capacitor less than one quarter inch away from the  $V_{CC}$  pin is also recommended. The PC board traces connected to signals A/B and Z/Y (LTC2861) should be symmetrical and as short as possible to maintain good differential signal integrity. To minimize capacitive effects, the differential signals should be separated by more than the width of a trace and should not be routed on top of each other if they are on different signal planes.

Care should be taken to route outputs away from any sensitive inputs to reduce feedback effects that might cause noise, jitter, or even oscillations. For example, in the full duplex LTC2861, DI and A/B should not be routed near the driver or receiver outputs.

The logic inputs of the LTC2859/LTC2861 have 50mV of hysteresis to provide noise immunity. Fast edges on the outputs can cause glitches in the ground and power supplies which are exacerbated by capacitive loading. If a logic input is held near its threshold (typically 1.5V), a noise glitch

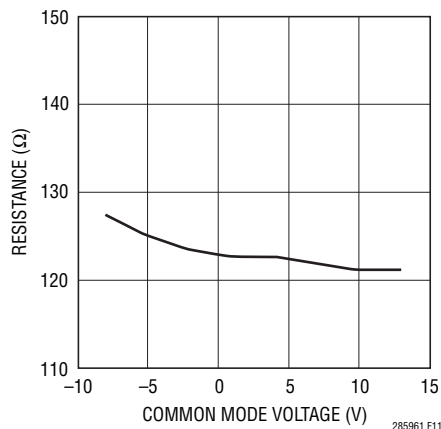


Figure 11. Termination Resistance vs Common Mode Voltage

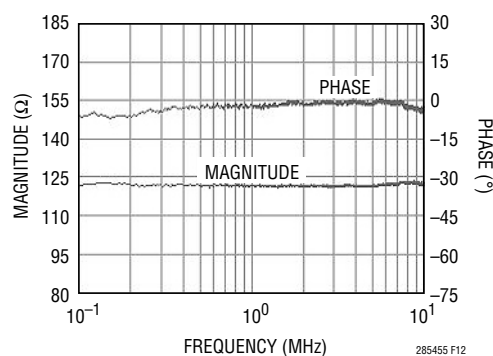


Figure 12. Termination Magnitude and Phase vs Frequency

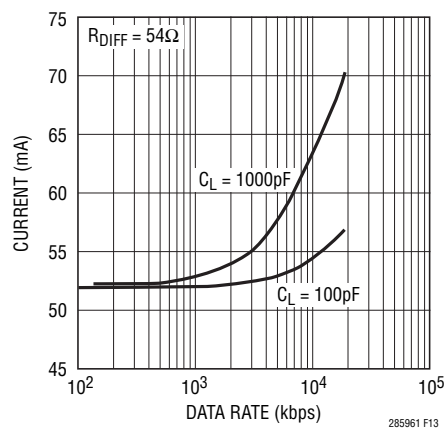


Figure 13. Supply Current vs Data Rate

## APPLICATIONS INFORMATION

from a driver transition may exceed the hysteresis levels on the logic and data inputs pins causing an unintended state change. This can be avoided by maintaining normal logic levels on the pins and by slewing inputs through their thresholds by faster than  $1V/\mu s$  when transitioning. Good supply decoupling and proper line termination also reduces glitches caused by driver transitions.

### Cable Length vs Data Rate

For a given data rate, the maximum transmission distance is bounded by the cable properties. A typical curve of cable length vs data rate compliant with the RS485 standard is shown in Figure 14. Three regions of this curve reflect different performance limiting factors in data transmission. In the flat region of the curve, maximum distance is determined by resistive losses in the cable. The downward sloping region represents limits in distance and data rate due to AC losses in the cable. The solid vertical line

represents the specified maximum data rate in the RS485 standard. The dashed lines at 250kbps and 20Mbps show the maximum data rates of the LTC2859/LTC2861 in Low-EMI and normal modes, respectively.

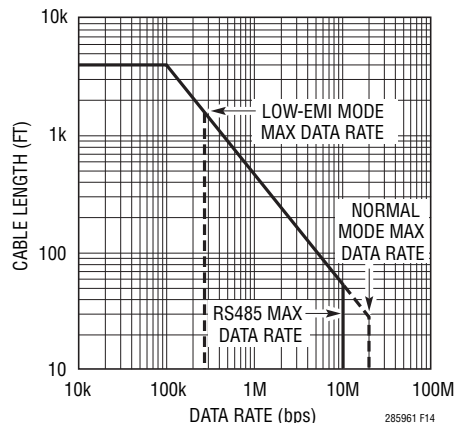
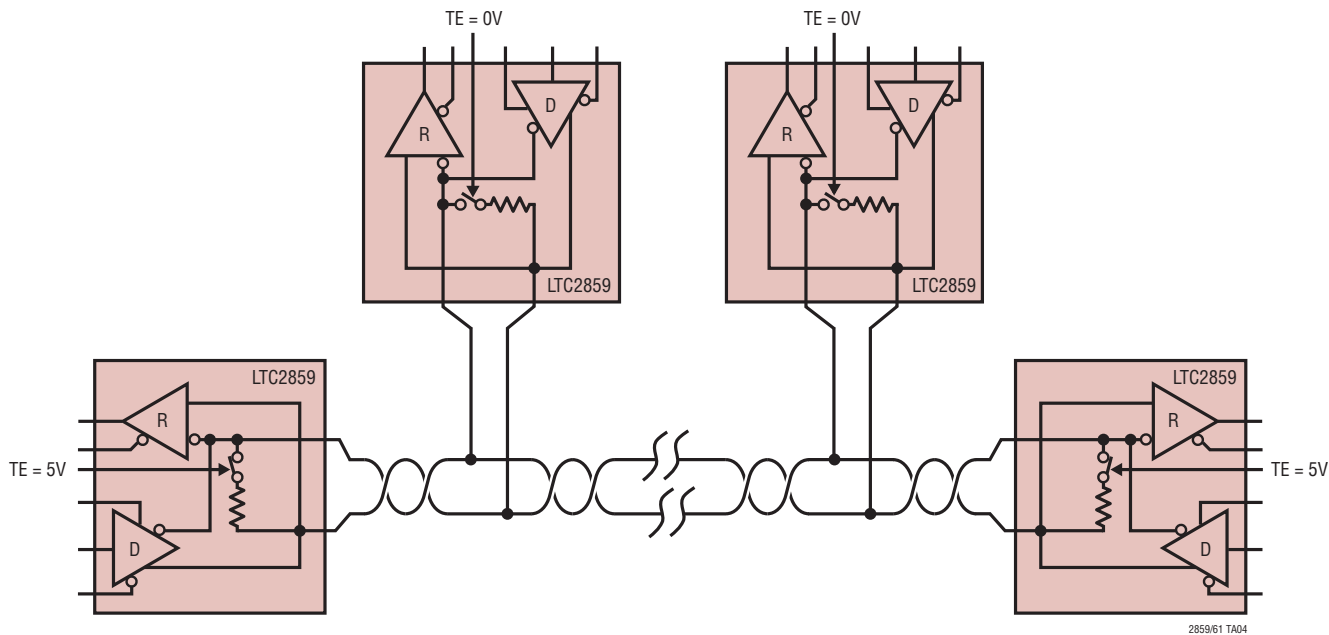


Figure 14. Cable Length vs Data Rate (RS485 Standard Shown in Solid Lines)

## TYPICAL APPLICATIONS

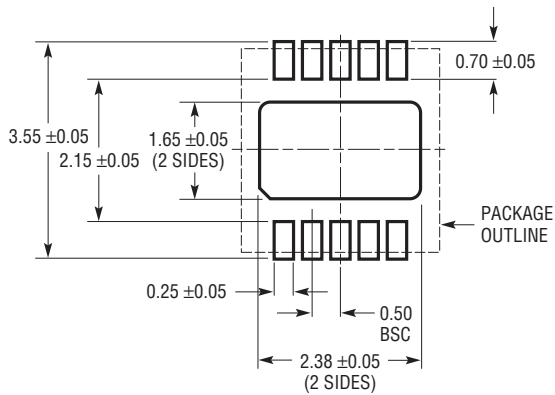
### Multi-Node Network with End Termination Using LTC2859



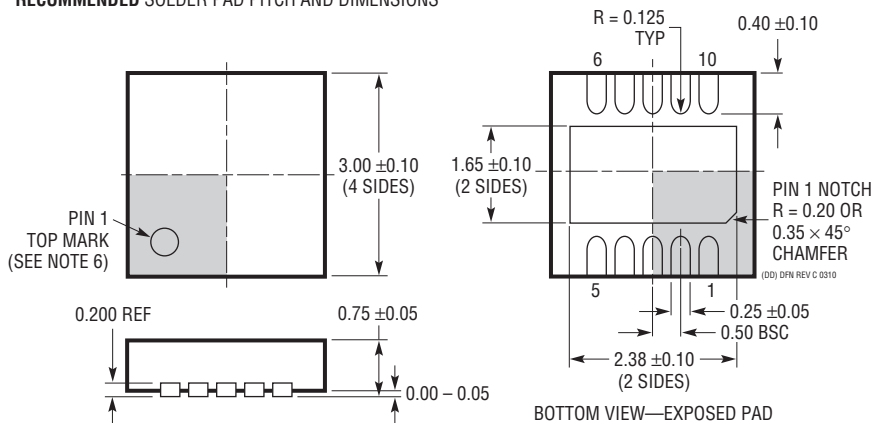
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**DD Package**  
**10-Lead Plastic DFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1699 Rev C)



**RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS**



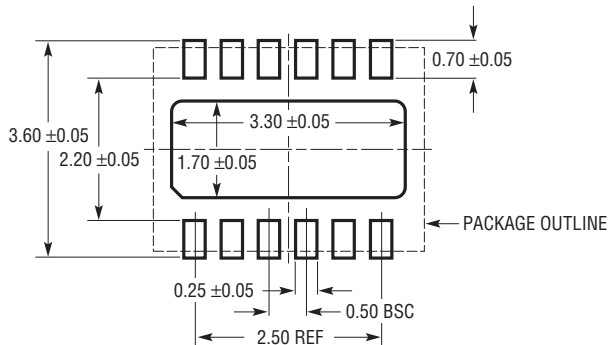
**NOTE:**

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

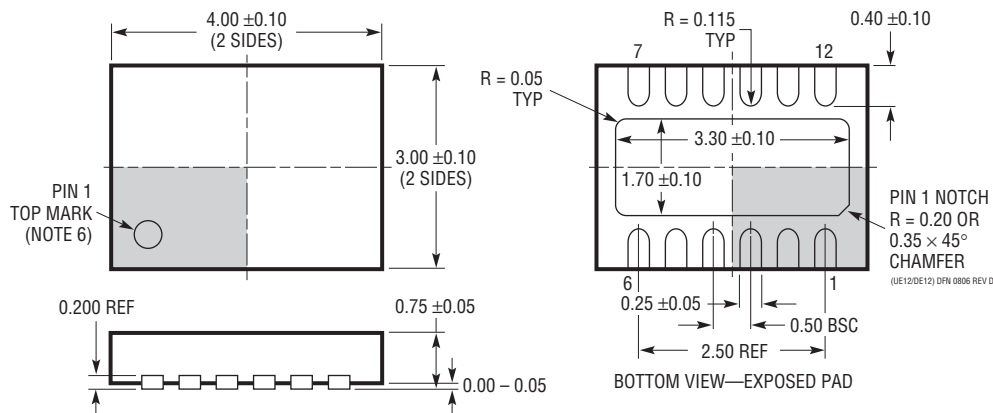
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

### DE/UE Package 12-Lead Plastic DFN (4mm × 3mm) (Reference LTC DWG # 05-08-1695 Rev D)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



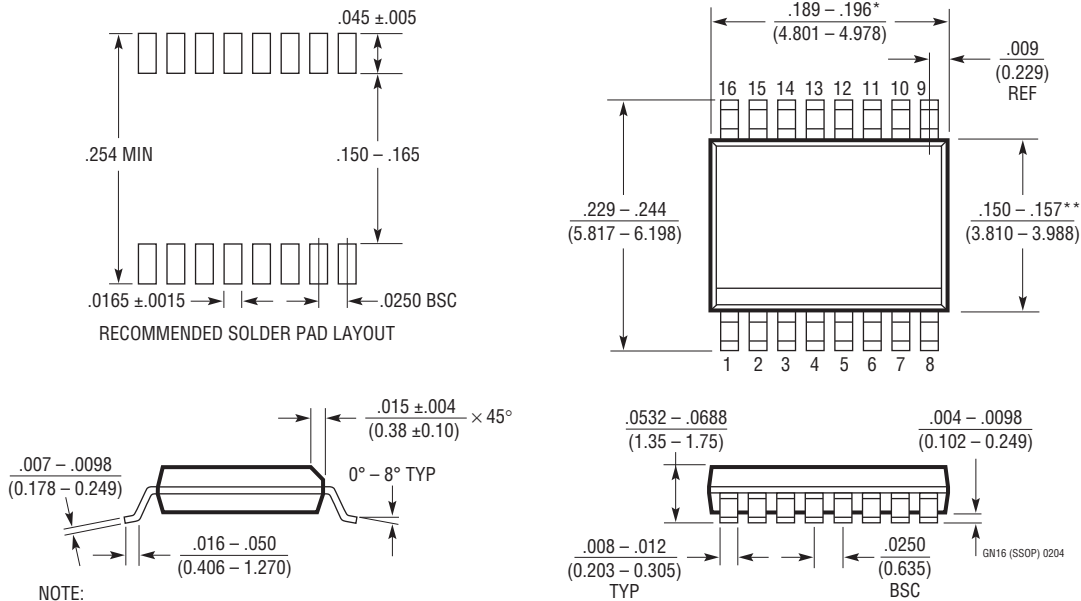
#### NOTE:

1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

### GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



**NOTE:**

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
3. DRAWING NOT TO SCALE

\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE



**REVISION HISTORY** (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	3/12	Added H-grade Order Information and Electrical Characteristics parameters	2, 3, 4
		Revised Receiver Input Resistance section	11
		Replaced Figure 12	12
		Added Termination Resistor restriction information	12