±60V Fault Protected 3V to 5.5V RS485/RS422 Transceiver with Level 4 IEC ESD

FEATURES

- **Protected from Overvoltage Line Faults to ±60V**
- **3V to 5.5V Supply Voltage**
- **20Mbps or Low EMI 250kbps Data Rate**
- **±40kV HBM ESD Interface Pins, ±15kV Other Pins**
- **Enhanced Receiver and Failsafe Noise Immunity**
- **IEC Level 4 ESD and EFT on Interface Pins**
- **Extended Common Mode Range: ±25V**
- Guaranteed Failsafe Receiver Operation
- High Input Impedance Supports 224 Nodes
- MP-Grade Option Available (–55°C to 125°C)
- Fully Balanced Differential Receiver Thresholds for Low Duty Cycle Distortion
- Current Limited Drivers and Thermal Shutdown
- Compliant with TIA/EIA-485-A
- Pin Compatible with LTC2862 and LT®1785
- Available in DFN and Leaded Packages
- AEC-Q100 Qualified for Automotive Applications (LTC2862A#W)

APPLICATIONS

- Supervisory Control and Data Acquisition (SCADA)
- Industrial Control and Instrumentation Networks
- Automotive and Transportation Electronics
- Building Automation, Security Systems and HVAC
- Medical Equipment
- Lighting and Sound System Control

DESCRIPTION

The LTC®2862A is a low power, 20Mbps or 250kbps RS485/RS422 transceiver operating on 3V to 5.5V supplies with ±60V overvoltage fault protection on the interface pins during all modes of operation, including power-down. Improvements were made to the LTC2862 for greater robustness and signal integrity: ±40kV HBM and Level 4 IEC ESD protection on the interface pins; increased resistance to electrical overstress; increased receiver noise immunity; additional receiver noise filtering on the LTC2862A-2; and an improved failsafe function optimized for high speed in the LTC2862A-1 and noise rejection in the LTC2862A-2. Low EMI slew rate limited data transmission is available in the 250kbps LTC2862A-2 option, while the LTC2862A-1 operates to 20Mbps.

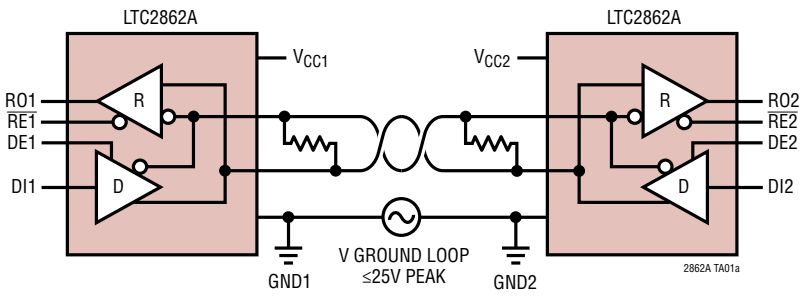
Extended ±25V input common mode range and full failsafe operation improve data communication reliability in electrically noisy environments and in the presence of large ground loop voltages.

PRODUCT SELECTION GUIDE

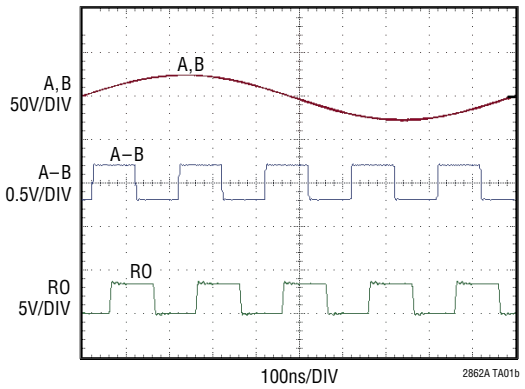
PART NUMBER	DUPLEX	ENABLES	MAX DATA RATE (bps)
LTC2862A-1	HALF	YES	20M
LTC2862A-2	HALF	YES	250k

TYPICAL APPLICATION

RS485 Link With Large Ground Loop Voltage



LTC2862A-1 Receiving 10Mbps ±200mV Differential Signal with 1MHz ±25V Common Mode Sweep



Rev. A

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltages
- V_{CC} ..... –0.3 to 6V

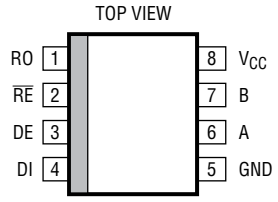
Logic Input Voltages ($\overline{RE}$, DE, DI) ..... –0.3 to 6V
Interface I/O: A, B ..... –60V to +60V
Receiver Output (RO) ..... –0.3V to (V_{CC}+0.3V)

Operating Ambient Temperature Range (Note 4)
- LTC2862AC ..... 0°C to 70°C
- LTC2862AI ..... –40°C to 85°C
- LTC2862AH ..... –40°C to 125°C
- LTC2862AMP ..... –55°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

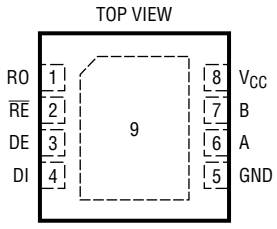
PIN CONFIGURATION

LTC2862A-1, LTC2862A-2



S8 PACKAGE
8-LEAD (150mil) PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 120°C/W, θ_{JC} = 39°C/W

LTC2862A-1, LTC2862A-2



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
EXPOSED PAD (PIN 9) CONNECT TO PCB GND
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2862ACS8-1#PBF	LTC2862ACS8-1#TRPBF	2862A1	8-Lead (150mil) Plastic SO	0°C to 70°C
LTC2862AIS8-1#PBF	LTC2862AIS8-1#TRPBF	2862A1	8-Lead (150mil) Plastic SO	–40°C to 85°C
LTC2862AHS8-1#PBF	LTC2862AHS8-1#TRPBF	2862A1	8-Lead (150mil) Plastic SO	–40°C to 125°C
LTC2862AMPS8-1#PBF	LTC2862AMPS8-1#TRPBF	2862A1	8-Lead (150mm) Plastic SO	–55°C to 125°C
LTC2862ACS8-2#PBF	LTC2862ACS8-2#TRPBF	2862A2	8-Lead (150mil) Plastic SO	0°C to 70°C
LTC2862AIS8-2#PBF	LTC2862AIS8-2#TRPBF	2862A2	8-Lead (150mil) Plastic SO	–40°C to 85°C
LTC2862AHS8-2#PBF	LTC2862AHS8-2#TRPBF	2862A2	8-Lead (150mil) Plastic SO	–40°C to 125°C
LTC2862AMPS8-2#PBF	LTC2862AMPS8-2#TRPBF	2862A2	8-Lead (150mm) Plastic SO	–55°C to 125°C
LTC2862ACDD-1#PBF	LTC2862ACDD-1#TRPBF	LGYK	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2862AIDD-1#PBF	LTC2862AIDD-1#TRPBF	LGYK	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2862AHDD-1#PBF	LTC2862AHDD-1#TRPBF	LGYK	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2862ACDD-2#PBF	LTC2862ACDD-2#TRPBF	LGYM	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2862AIDD-2#PBF	LTC2862AIDD-2#TRPBF	LGYM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2862AHDD-2#PBF	LTC2862AHDD-2#TRPBF	LGYM	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**				
LTC2862AIS8-1#WPBF	LTC2862AIS8-1#WTRPBF	2862A1	8-Lead (150mil) Plastic SO	–40°C to 85°C
LTC2862AIS8-2#WPBF	LTC2862AIS8-2#WTRPBF	2862A1	8-Lead (150mil) Plastic SO	–40°C to 85°C
LTC2862AHS8-1#WPBF	LTC2862AHS8-1#WTRPBF	2862A1	8-Lead (150mil) Plastic SO	–40°C to 125°C
LTC2862AHS8-2#WPBF	LTC2862AHS8-2#WTRPBF	2862A1	8-Lead (150mil) Plastic SO	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{CC}	Primary Power Supply		●	3		5.5	V
I_{CCS}	Supply Current in Shutdown Mode (C-, I-Grade)	DE = 0V, $\overline{RE}$ = V_{CC}	●		0	10	µA
	Supply Current in Shutdown Mode (H-, MP-Grade)	DE = 0V, $\overline{RE}$ = V_{CC}	●		0	40	µA
I_{CCTR}	Supply Current with Both Driver and Receiver Enabled (LTC2862A-1)	No Load, DE = V_{CC}, $\overline{RE}$ = 0V	●		1.1	1.6	mA
I_{CCR}	Supply Current with Receiver Enabled (LTC2862A-1)	No Load, DE = $\overline{RE}$ = 0V	●		1.0	1.4	mA
I_{CCTRS}	Supply Current with Both Driver and Receiver Enabled (LTC2862A-2)	No Load, DE = V_{CC}, $\overline{RE}$ = 0V	●		3.5	8	mA
I_{CCRS}	Supply Current with Receiver Enabled (LTC2862A-2)	No Load, DE = $\overline{RE}$ = 0V	●		1.3	1.8	mA
Driver							
$\|V_{OD}\|$	Differential Driver Output Voltage	R = ∞ (Figure 1)	●	1.5	3	V_{CC}	V
		R = 27Ω (Figure 1)	●	1.5	2	5	V
		R = 50Ω (Figure 1)	●	2	2.3	V_{CC}	V
$\Delta\|V_{OD}\|$	Change in Magnitude of Driver Differential Output Voltage	R = 27Ω or 50Ω (Figure 1)	●		0	0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or 50Ω (Figure 1)	●		2	3	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Driver Common-Mode Output Voltage	R = 27Ω or 50Ω (Figure 1)	●		0	0.2	V
I_{OSD}	Maximum Driver Short-Circuit Current	–60V ≤ (A or B) ≤ 60V (Figure 2)	●		±150	±250	mA
Receiver							
I_{IN}	Receiver Input Current (A, B)	V_{CC} = 0V or 3.3V, V_{IN} = 12V (Figure 3)	●			143	µA
		V_{CC} = 0V or 3.3V, V_{IN} = –7V (Figure 3)	●	–100			µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{IN}	Receiver Input Resistance	$0 \le V_{CC} \le 5.5V$, V_{IN} = –25V or 25V (Figure 3)			112		kΩ
V_{CM}	Receiver Common Mode Input Voltage (A + B)/2		●	–25		25	V
V_{TH}^+	Positive Differential Input Signal Threshold Voltage (A – B)	$-25V \le V_{CM} \le 25V$	●		125	200	mV
V_{TH}^-	Negative Differential Input Signal Threshold Voltage (A – B)	$-25V \le V_{CM} \le 25V$	●	–200	–125		mV
ΔV_{TH}	Differential Input Signal Hysteresis ($V_{TH}^+ - V_{TH}^-$)	V_{CM} = 0V			250		mV
V_{TFS}	Differential Input Failsafe Threshold Voltage	$-25V \le V_{CM} \le 25V$	●	–200	–75	–10	mV
ΔV_{TFS}	Differential Input Failsafe Hysteresis ($V_{TFS} - V_{TH}^-$)	V_{CM} = 0V			50		mV
V_{OH}	Receiver Output High Voltage	I(RO) = –3mA (Sourcing)	●	V_{CC} –0.4V	V_{CC} –0.2V		V
V_{OL}	Receiver Output Low Voltage	I(RO) = 3mA (Sinking)	●		0.2	0.4	V
I_{OZR}	Receiver Three-State (High Impedance) Output Current on RO	$\overline{RE}$ = High, V_{CC} = 5V, RO = 0V or V_{CC}	●	–32		5	µA
I_{OSR}	Receiver Short-Circuit Current	$\overline{RE}$ = Low, RO = 0V or V_{CC}	●			±20	mA
C_{IN}	Input Capacitance (A and B)	(Note 5)			50		pF
Logic							
V_{TH}	Input Threshold Voltage (DE, DI, $\overline{RE}$)	$3.0 \le V_{CC} \le 5.5V$	●	0.33 • V_{CC}		0.67 • V_{CC}	V
I_{INL}	Logic Input Current (DE, DI, $\overline{RE}$)	$0 \le V_{IN} \le V_{CC}$	●		0	±5	µA
ESD (Note 5)							
	ESD Protection Level of Interface Pins (A,B), Powered or Unpowered	Human Body Model, A or B to GND, V_{CC}, B or A, 1µF Between V_{CC} and GND			±40kV		kV
		IEC 61000-4-2 ESD Level 4, Contact, 1µF Between V_{CC} and GND			±8kV		kV
	ESD Protection Level of All Other Pins (RO, $\overline{RE}$, DE, DI, V_{CC}, GND)	Human Body Model			±15kV		kV

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Driver – High Speed (LTC2862A-1)							
f_{MAX}	Maximum Data Rate	(Note 3)	●	20			Mbps
t_{PLHD}, t_{PHLD}	Driver Input to Output	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		25	50	ns
Δt_{PD}	Driver Input to Output Difference $\lvert t_{PLHD} - t_{PHLD} \rvert$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		2	5	ns
t_{SKEWD}	Driver Output A to Output B	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●			±10	ns
t_{RD}, t_{FD}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		4	15	ns
t_{ZLD}, t_{ZHD}	Driver Enable Time	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = 0V (Figure 5)	●		25	50	ns
t_{LZD}, t_{HZD}	Driver Disable Time	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = 0V (Figure 5)	●		45	75	ns
t_{ZHSD}, t_{ZLSD}	Driver Enable from Shutdown	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = High (Figure 5)	●		5	10	µs
t_{SHDND}	Time to Shutdown	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = High (Figure 5)	●		50	90	ns
Driver – Slew Rate Limited (LTC2862A-2)							
f_{MAXS}	Maximum Data Rate	(Note 3)	●	250			kbps
t_{PLHDS}, t_{PHLDS}	Driver Input to Output	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		850	1500	ns
Δt_{PDS}	Driver Input to Output Difference $\lvert t_{PLHDS} - t_{PHLDS} \rvert$	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●		10	150	ns
t_{SKEWDS}	Driver Output A to Output B	R_{DIFF} = 54Ω, C_L = 100pF (Figure 4)	●			±500	ns
t_{RDS}, t_{FDS}	Driver Rise or Fall Time	R_{DIFF} = 54Ω, C_L =100pF (Figure 4)	●	500	800	1200	ns
t_{ZLDS}, t_{ZHDS}	Driver Enable Time	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = 0V (Figure 5)	●		400	800	ns
t_{LZDS}, t_{HZDS}	Driver Disable Time	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = 0V (Figure 5)	●		45	75	ns
t_{ZHSDS}, t_{ZLSDS}	Driver Enable from Shutdown	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = High (Figure 5)	●		6	11	µs
t_{SHDNDS}	Time to Shutdown	R_L = 27Ω, C_L = 100pF, $\overline{RE}$ = High (Figure 5)	●		50	90	ns
Receiver							
t_{PLHR}, t_{PHLR}	Receiver Input to Output (LTC2862A-1)	C_L = 15pF, V_{CM} = 0V, $\lvert V_{AB} \rvert$ = 1.5V, t_R and t_F < 4ns (Figure 6)	●		50	65	ns
t_{PLHRS}, t_{PHLRS}	Receiver Input to Output (LTC2862A-2)	C_L = 15pF, V_{CM} = 0V, $\lvert V_{AB} \rvert$ = 1.5V, t_R and t_F < 4ns (Figure 6)	●		400	700	ns
t_{SKEWR}	Differential Receiver Skew $\lvert t_{PLHR} - t_{PHLR} \rvert$ (LTC2862A-1)	C_L = 15pF (Figure 6)	●		1	5	ns
t_{SKEWRS}	Differential Receiver Skew $\lvert t_{PLHRS} - t_{PHLRS} \rvert$ (LTC2862A-2)	C_L = 15pF (Figure 6)	●		5	30	ns
t_{PFSN}	Failsafe Enter Delay (LTC2862A-1)	C_L = 15pF, V_{CM} = 0V, $\lvert V_{AB} \rvert$ = 1.5V, t_R and t_F < 4ns (Figure 8)	●		80	110	ns
t_{PFSNS}	Failsafe Enter Delay (LTC2862A-2)	C_L = 15pF, V_{CM} = 0V, $\lvert V_{AB} \rvert$ = 1.5V, t_R and t_F < 4ns (Figure 8)	●		1.5	2.3	µs

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PFSX}	Failsafe Exit Delay (LTC2862A-1)	C_L = 15pF, V_{CM} = 0V, $\|V_{AB}\|$ = 1.5V, t_R and t_F < 4ns (Figure 8)	●		45	60	ns
t_{PFSXS}	Failsafe Exit Delay (LTC2862A-2)	C_L = 15pF, V_{CM} = 0V, $\|V_{AB}\|$ = 1.5V, t_R and t_F < 4ns (Figure 8)	●		0.7	1.3	µs
t_{RR}, t_{FR}	Receiver Output Rise or Fall Time	C_L = 15pF (Figure 6)	●		3	6	ns
t_{ZLR}, t_{ZHR}	Receiver Enable Time	R_L = 500Ω, C_L = 15pF, DE = High (Figure 7)	●		18	30	ns
t_{LZR}, t_{HZR}	Receiver Disable Time	R_L = 500Ω, C_L = 15pF, DE = High (Figure 7)	●		29	40	ns
t_{ZHSR}, t_{ZLSR}	Receiver Enable from Shutdown	R_L = 500Ω, C_L = 15pF, DE = High (Figure 7)	●		5	10	µs
t_{SHDNR}	Time to Shutdown	R_L = 500Ω, C_L = 15pF, DE = High (Figure 7)	●		24	40	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

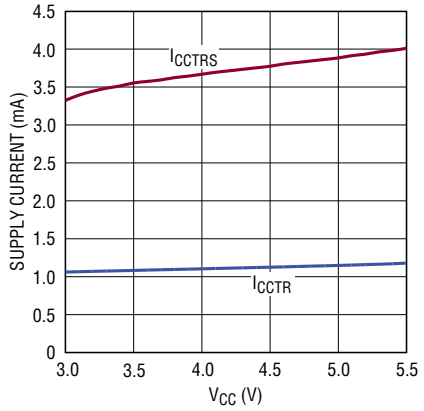
Note 3: Maximum data rate is guaranteed by other measured parameters and is not tested directly.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may result in device degradation or failure.

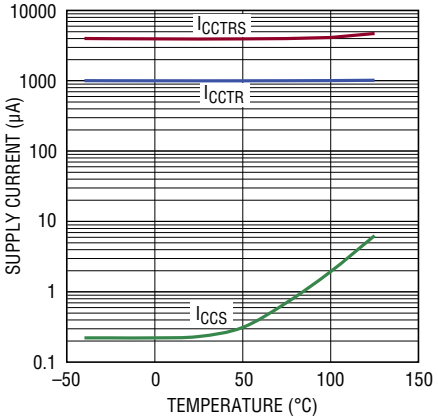
Note 5: Not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{CC} = 3.3V, unless otherwise noted.

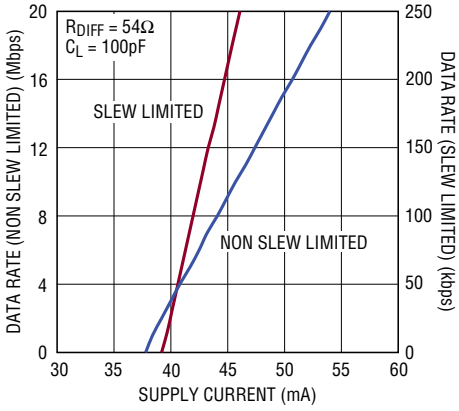
Supply Current vs V_{CC}



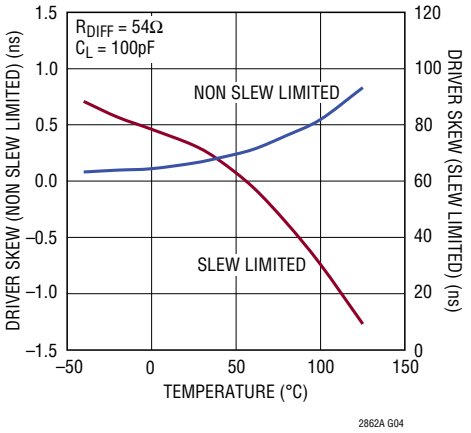
Supply Current vs Temperature



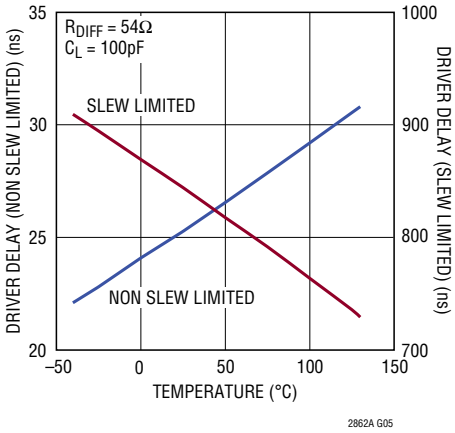
Supply Current vs Data Rate



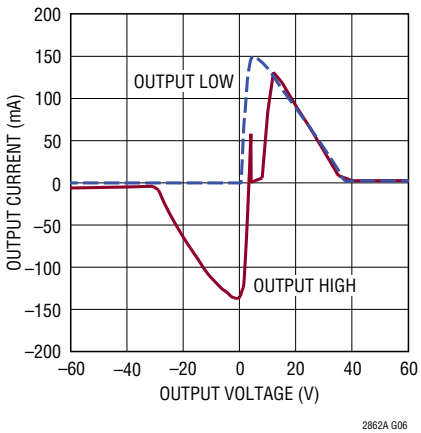
Driver Skew vs Temperature



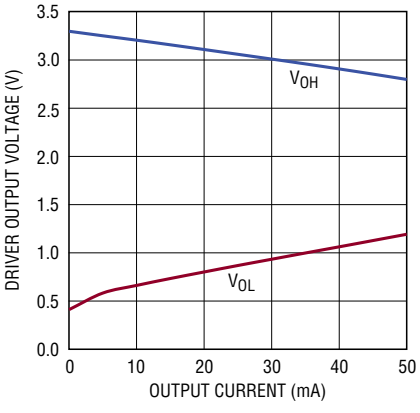
Driver Propagation Delay vs Temperature



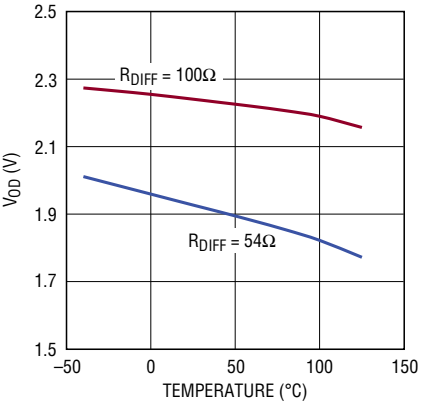
Driver Output Short-Circuit Current vs Voltage



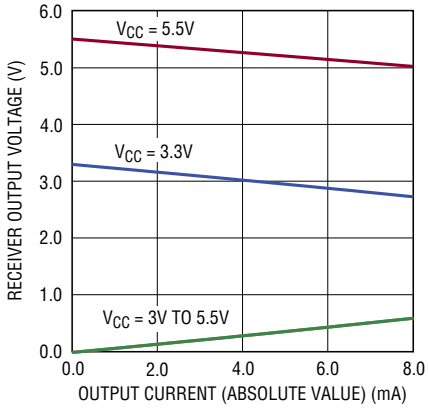
Driver Output Low/High Voltage vs Output Current



Driver Differential Output Voltage vs Temperature

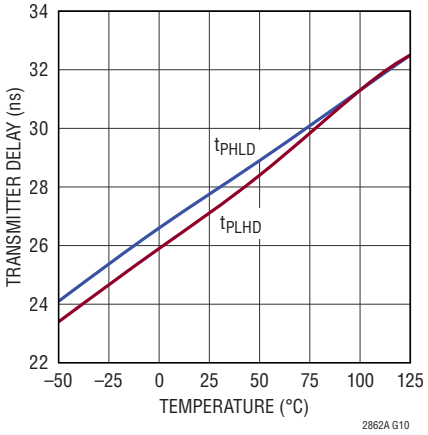


Receiver Output Voltage vs Output Current (Source and Sink)

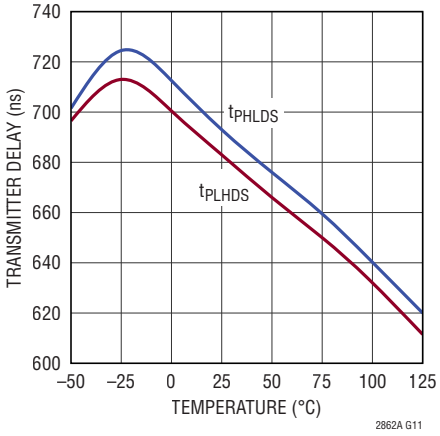


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_{CC} = 3.3V, unless otherwise noted.

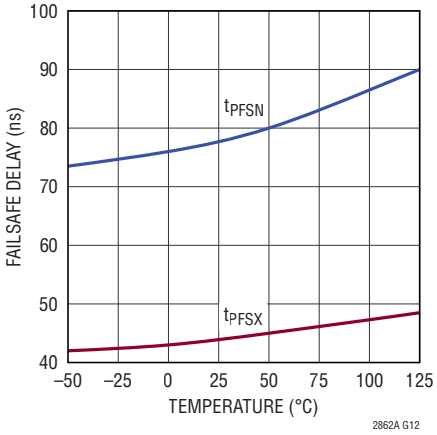
Transmitter Propagation Delay vs Temperature (LTC2862A-1)



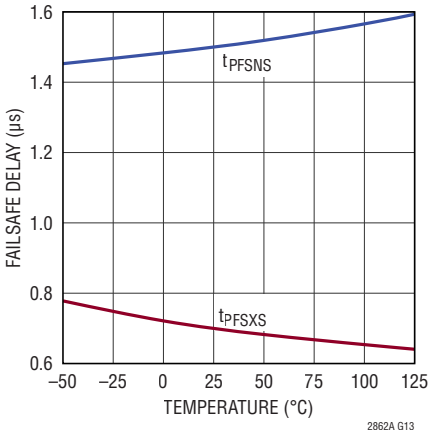
Transmitter Propagation Delay vs Temperature (LTC2862A-2)



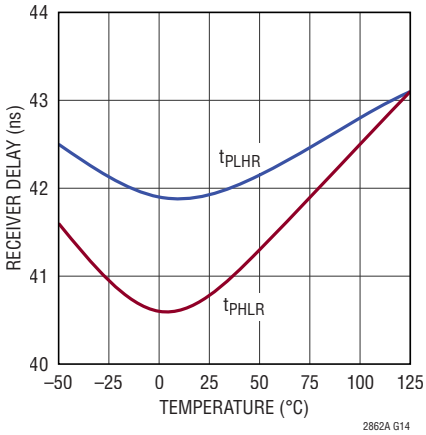
Failsafe Enter and Exit Delay vs Temperature (LTC2862A-1)



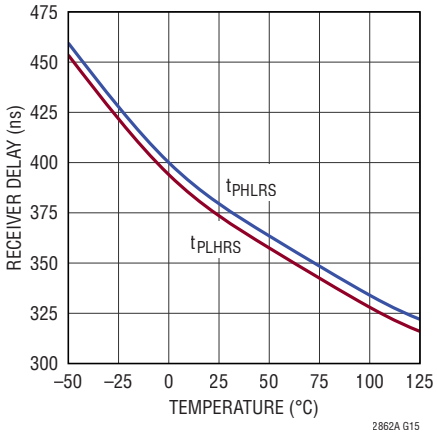
Failsafe Enter and Exit Delay vs Temperature (LTC2862A-2)



Receiver Propagation Delay vs Temperature (LTC2862A-1)



Receiver Propagation Delay vs Temperature (LTC2862A-2)



PIN FUNCTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
RO	1	Receiver Output. If the receiver output is enabled ($\overline{RE}$ low) and A–B > 200mV, then RO will be high. If A–B < –200mV, then RO will be low. If the receiver inputs are open, shorted, or terminated without a signal, RO will be high. Integrated 250kΩ pull-up to V_{CC}.
$\overline{RE}$	2	Receiver Enable. A low input enables the receiver. A high input forces the receiver output into a high impedance state. If $\overline{RE}$ is high with DE low, the part will enter a low power shutdown state.
DE	3	Driver Enable. A high input on DE enables the driver. A low input will force the driver outputs into a high impedance state. If DE is low with $\overline{RE}$ high, the part will enter a low power shutdown state.
DI	4	Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the driver noninverting output A low and inverting output B high. A high on DI, with the driver outputs enabled, forces the driver noninverting output A high and inverting output B low.
GND	5	Ground.
Exposed Pad	9	Connect the exposed pad on the DFN packages to GND.
B	7	Inverting Receiver Input and Inverting Driver Output. Impedance is ~112kΩ in receive mode or unpowered.
A	6	Noninverting Receiver Input and Noninverting Driver Output. Impedance is ~112kΩ in receive mode or unpowered.
V_{CC}	8	Power Supply. 3V < V_{CC} < 5.5V. Bypass with 1µF ceramic capacitor to GND for best ESD performance.

FUNCTION TABLE

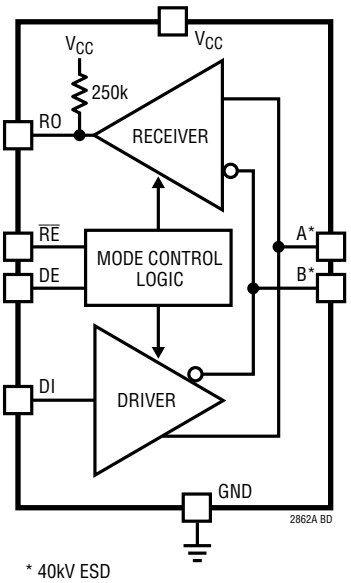
LTC2862A

LOGIC INPUTS		MODE	A, B	RO
DE	$\overline{RE}$			
0	0	Receive	R_{IN}	Active
0	1	Shutdown	R_{IN}	High-Z*
1	0	Transceive	Active	Active
1	1	Transmit	Active	High-Z*

* 250kΩ pull-up to V_{CC}.

BLOCK DIAGRAM

LTC2862A



* 40kV ESD
ALL OTHER PINS 15kV

TEST CIRCUITS

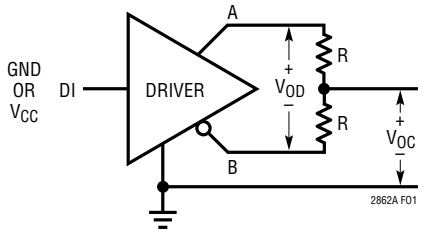


Figure 1. Driver DC Characteristics

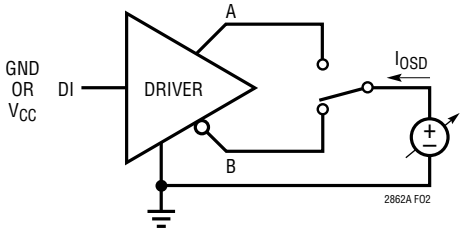
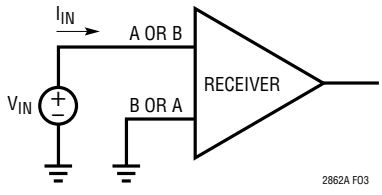


Figure 2. Driver Output Short-Circuit Current



$R_{IN} = \frac{V_{IN}}{I_{IN}}$

Figure 3. Receiver Input Current and Input Resistance

TEST CIRCUITS

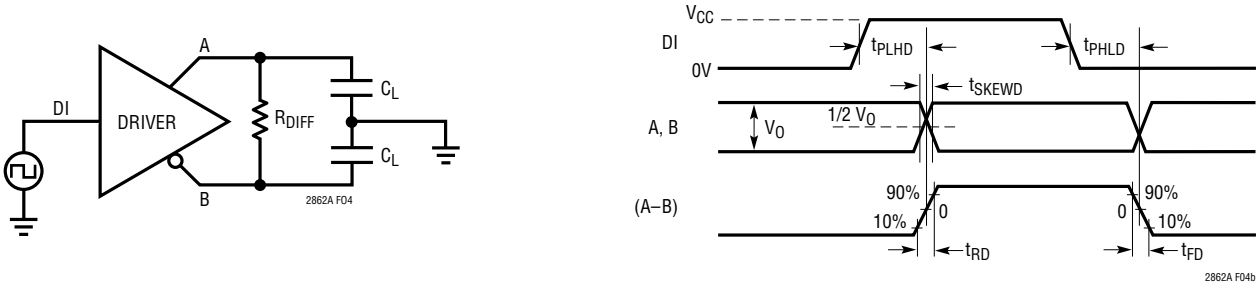


Figure 4. Driver Timing Measurement

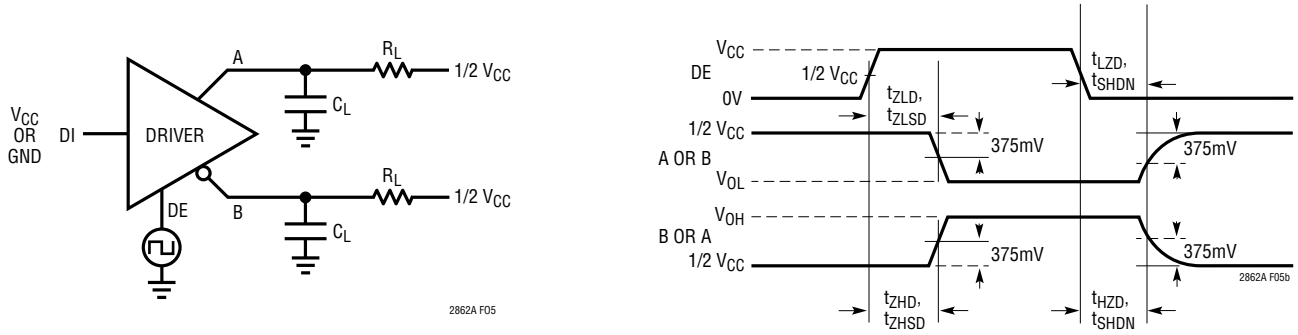


Figure 5. Driver Enable and Disable Timing Measurements

TEST CIRCUITS

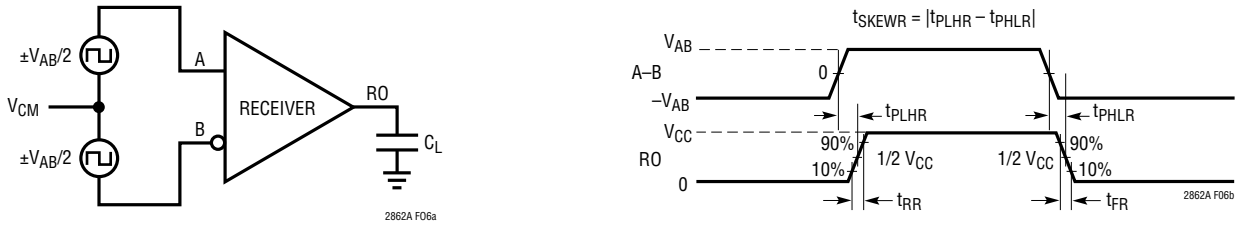


Figure 6. Receiver Propagation Delay Measurements

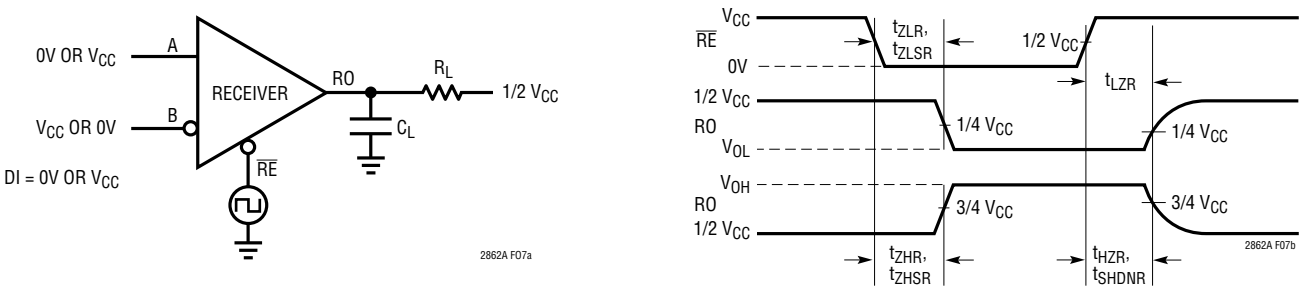


Figure 7. Receiver Enable/Disable Time Measurements

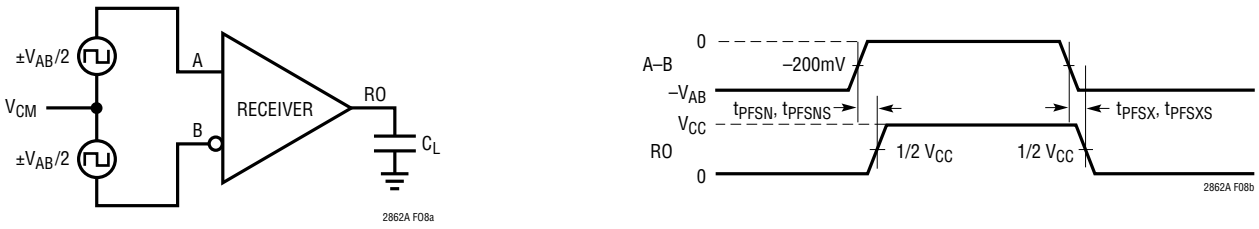


Figure 8. Failsafe Delay Measurements

APPLICATIONS INFORMATION

±60V Fault Protection

The LTC2862A is an improved overvoltage fault-tolerant RS485/RS422 transceiver that operates from 3V to 5.5V power supplies. Industrial installations may encounter common mode voltages between nodes far greater than the –7V to 12V range specified by the RS485 standards. Standard RS485 transceivers can be damaged by voltages above their typical absolute maximum ratings of –8V to 12.5V. The limited overvoltage tolerance of standard RS485 transceivers makes implementation of effective external protection networks difficult without interfering with proper data network performance within the –7V to 12V region of RS485 operation. Replacing standard RS485 transceivers with the rugged LTC2862A devices may eliminate field failures due to overvoltage faults without using costly external protection devices.

The ±60V fault protection of the LTC2862A is achieved by using a high-voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered-off and high-impedance conditions. The driver outputs use a progressive foldback current limit design to protect against overvoltage faults while still allowing high current output drive.

The LTC2862A is protected from ±60V faults even with the loss of GND or V_{CC} (GND open faults not tested in production). Additional precautions must be taken in the case of V_{CC} present and GND open. The LTC2862A chip will protect itself from damage, but the chip ground current may flow out through the ESD diodes on the logic I/O pins and into associated circuitry. The system designer should examine the susceptibility of the associated circuitry to damage if the condition of a GND open fault with V_{CC} present is anticipated.

The high voltage rating of the LTC2862A makes it simple to extend the overvoltage protection to higher levels using external protection components. Compared to lower voltage RS485 transceivers, external protection devices with higher breakdown voltages can be used, so as not to interfere with data transmission in the presence of large common mode voltages. The Typical Applications section shows a protection network against faults up to ±360V peak, while still maintaining the extended ±25V common mode range on the signal lines.

±25V Extended Common Mode Range

To further increase the reliability of operation and extend functionality in environments with high common mode voltages due to electrical noise or local ground potential differences due to ground loops, the LTC2862A features an extended common mode operating range of –25V to 25V. This extended common mode range allows the LTC2862A to transmit and receive under conditions that would cause data errors and possible device damage in competing products.

±40kV ESD Protection

The LTC2862A features exceptionally robust ESD protection. The transceiver interface pins (A,B) feature protection to ±40kV HBM with respect to GND, V_{CC} (with a 1µF capacitor to GND), A or B without latchup or damage, during all modes of operation or while unpowered. All the other pins are protected to ±15kV HBM to make this a component capable of reliable operation under severe environmental conditions.

Level 4 IEC ESD and EFT Protection

The improved ESD protection of the LTC2862A provides a high level of protection in the IEC ESD and EFT (Electrical Fast Transient) tests. The IEC ESD stress exceeds that of the HBM test in peak current, amplitude, and rise time, while the EFT test provides a prolonged repetitive stress. Combined with the HBM test, the IEC tests help ensure that the LTC2862A is robust under a wide range of real world hazards. The LTC2862A passes the following tests on the A, B pins:

- IEC 61000-4-2 Edition 2.0 2008-12 ESD Level 4: ±8kV contact (A or B to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a test card with a low impedance ground discharge path from board GND to ESD gun return lead, per Figure 4 of the standard)
- IEC 61000-4-4 Second Edition 2004-07 EFT Level 4: ±5kV (line to GND, 5kHz repetition rate, 15ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard)

APPLICATIONS INFORMATION

Enhanced EOS Protection

The improved ESD protection of the LTC2862A also provides superior resistance to electrical overstress (EOS) damage in the presence of large fault voltages applied from low impedance faults. The LTC2862A employs thyristor type ESD protection on the A, B pins. While thyristors have the low on-state impedance and high robustness needed to achieve the very high levels of ESD protection of the LTC2862A, they have the disadvantage of snapping back to a low voltage conduction state after they have been triggered by an initial voltage that exceeds ~±80V. In the presence of a high voltage, high current fault source, the large resulting currents will blow the bond wires inside the LTC2862A package, resulting in a failed chip.

The LTC2862A mitigates the probability of this type of failure by establishing a very high trigger current in addition to a higher trigger voltage. In order to trigger the ESD cell, the fault must not only exceed the ~±80V trigger voltage, but must be able to source ~±500mA at that voltage to initiate the snapback of the ESD cell. This makes the LTC2862A much less susceptible to snapback induced failures created by high voltage noise spikes or voltage transients caused by inductive overshoot when the A,B pins are shorted to a fault voltage source. (The snapback characteristics of the ESD protection are not tested during production.)

Driver

The driver provides full RS485/RS422 compatibility. When enabled, if DI is high, A–B is positive. When the driver is disabled, both transmitter outputs are high impedance, and the impedance is dominated by the receiver input resistance, R_{IN}.

Driver Overvoltage and Overcurrent Protection

The driver outputs are protected from short circuits to any voltage within the Absolute Maximum range of –60V to 60V. The maximum current in a fault condition is ±250mA. The driver includes a progressive foldback current limiting circuit that continuously reduces the driver current limit with increasing output fault voltage. The fault current is less than ±15mA for fault voltages over ±40V.

All devices also feature thermal shutdown protection that disables the driver and receiver in case of excessive power dissipation (see Note 4). (Thermal shutdown is not tested during production.)

Full Failsafe Operation

When the absolute value of the differential voltage between the A and B pins is greater than 200mV with the receiver enabled, the state of RO will reflect the polarity of (A–B).

These parts have a failsafe feature that guarantees the receiver output will be in a logic 1 state (the idle state) when the inputs are shorted, left open, or terminated but not driven. The delay allows normal data signals to transition through the threshold region without being interpreted as a failsafe condition. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of –25V to 25V.

Most competing devices achieve the failsafe function by a simple negative offset of the input threshold voltage. This causes the receiver to interpret a zero differential voltage as a logic 1 state. The disadvantage of this approach is the input offset can introduce duty cycle asymmetry at the receiver output that becomes increasingly worse with low input signal levels and slow input edge rates.

Other competing devices use internal biasing resistors to create a positive bias at the receiver inputs in the absence of an external signal. This type of failsafe biasing is ineffective if the network lines are shorted, or if the network is terminated but not driven by an active transmitter.

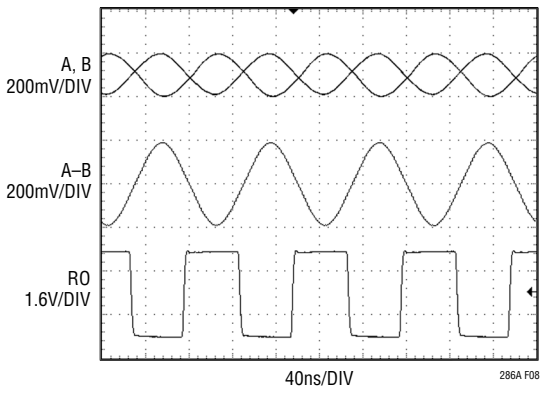


Figure 9. Duty Cycle of Balanced Receiver with ±200mV 10Mbps Input Signal

APPLICATIONS INFORMATION

The LTC2862A uses fully symmetric positive and negative receiver thresholds V_{TH}^- and V_{TH}^+ (typically ±125mV) to maintain good duty cycle symmetry at low signal levels. The failsafe operation is performed with a window comparator to determine when the differential input voltage falls above the V_{TFS} failsafe threshold (typically –75mV) but below the V_{TH}^+ threshold. If this condition persists for more than about 40ns for the LTC2862A-1 or 1.2µs for the LTC2862A-2 the failsafe condition is asserted and the RO pin is forced to the logic 1 state. This circuit provides full failsafe operation and a large dynamic signal hysteresis of ~250mV between V_{TH}^- and V_{TH}^+ with no negative impact to receiver duty cycle symmetry, as shown in Figure 9. The input signal in Figure 9 was obtained by driving a 10Mbps RS485 signal through 1000 feet of cable, thereby attenuating it to a ±200mV signal with slow rise and fall times. Good duty cycle symmetry is observed at RO despite the degraded input signal.

The failsafe circuit has been enhanced with noise filtering to exit the failsafe state. In the absence of noise filtering, a noise transient that momentarily forces the A-B differential voltage below the V_{TH}^- receiver threshold will cause the RO output to go low, which may be interpreted as a false start character by the microcontroller. The LTC2862A receiver reduces these false signals by low pass filtering the signal to exit the failsafe state. The noise filtering in the failsafe circuit of the LTC2862A-2 is much greater than in the LTC2862A-1, commensurate with its lower data rate. For example, the LTC2862A-1 exits the failsafe state when a –1V differential pulse of about 3ns duration is applied, while the LTC2862A-2 requires a –1V pulse of about 400ns duration to exit the failsafe state. (The minimum pulse widths to enter or exit the failsafe state are not tested in production, but the underlying filtering is reflected in the t_{FSN}, t_{FSX}, t_{FSNS}, and t_{FSXS} measurements).

Enhanced Receiver Noise Immunity

An additional benefit of the fully symmetric receiver thresholds is enhanced receiver noise immunity. The differential input signal must go above the positive threshold to register as a logic 1 and go below the negative threshold to register as a logic 0. This provides a hysteresis of 250mV (typical) at the receiver inputs for any valid data signal. (An invalid data condition such as a DC sweep of the receiver inputs will produce a different observed hysteresis due to the activation of the failsafe circuit.) Competing devices that employ a negative offset of the input threshold voltage generally have a much smaller hysteresis and subsequently have lower receiver noise immunity.

The LTC2862A-2 provides additional noise immunity by adding low-pass filtering to the differential signal in its receiver. Commensurate with its maximum data rate of 250kbps, the LTC2862A-2 receiver attenuates high frequency signals above approximately 660kHz. This low-pass filter removes high frequency noise transients that might otherwise be interpreted as data. (High frequency noise filtering is not tested in production, but the underlying filtering is reflected in the t_{PLHR}, t_{PHLR}, t_{PLHRS}, and t_{PHLRS} measurements).

RS485 Network Biasing

RS485 networks are usually biased with a resistive divider to generate a differential voltage of ≥200mV on the data lines, which establishes a logic 1 state (the idle state) when all the transmitters on the network are disabled. The values of the biasing resistors are not fixed, but depend on the number and type of transceivers on the line and the number and value of terminating resistors. Therefore, the values of the biasing resistors must be customized to each specific network installation, and may change if nodes are added to or removed from the network.

The internal failsafe feature of the LTC2862A eliminates the need for external network biasing resistors provided they are used in a network of transceivers with similar internal failsafe features. The LTC2862A transceivers will operate correctly on biased, unbiased, or under-biased networks.

Hi-Z State

The receiver output is internally driven high (to V_{CC}) or low (to GND) with no external pull-up needed. When the receiver is disabled the RO pin becomes Hi-Z with a 250k pull-up resistor to V_{CC}.

APPLICATIONS INFORMATION

High Receiver Input Resistance

The bus receiver input load from A or B to GND is less than one-seventh unit load, permitting a total of 224 receivers per system without exceeding the RS485 receiver loading specification. The input load of the receiver is unaffected by enabling/disabling the receiver or by powering/unpowering the part.

Supply Current

The unloaded static supply currents in these devices are low — typically 1.1mA for non slew limited devices and 3.5mA for slew limited devices. In applications with resistively terminated cables, the supply current is dominated by the driver load. For example, when using two 120Ω terminators with a differential driver output voltage of 2V, the DC load current is 33mA, which is sourced by the positive voltage supply. Power supply current increases with toggling data due to capacitive loading and this term can increase significantly at high data rates. A plot of the supply current vs data rate is shown in the Typical Performance Characteristics of this data sheet.

During fault conditions with a positive voltage larger than the supply voltage applied to the transmitter pins, or during transmitter operation with a high positive common mode voltage, positive current of up to 80mA may flow from the transmitter pins back to V_{CC}. If the system power supply or loading cannot sink this excess current, a 5.6V 1W 1N4734 Zener diode may be placed between V_{CC} and GND to prevent an overvoltage condition on V_{CC}.

The LTC2862A contains a supply undervoltage lockout circuit that enables the transmitter and receiver outputs when V_{CC} exceeds ~2.7V and disables the transmitter and receiver outputs when V_{CC} falls below ~2.5V.

When the LTC2862A is unpowered, the logic inputs (DE, DI, $\overline{RE}$) are high impedance for voltages > 0V. Each input has a diode clamp to GND that will conduct if a negative voltage sufficient to forward bias the diode (~ –0.6V at 25°C) is applied to the pad. The RO output contains a CMOS driver with parasitic diodes to GND and V_{CC}. The diode to GND will conduct if forward biased by a negative voltage below GND, while the diode to V_{CC} will conduct if forward biased by a positive voltage above V_{CC}. If V_{CC} is low, this will result in the RO line being clamped to approximately 0.6V above V_{CC}. The impedance of the logic inputs and the RO output are not tested with the LTC2862A unpowered.

Shutdown Mode Delay

The LTC2862A features a low power shutdown mode that is entered when both the driver and the receiver are simultaneously disabled (pin DE low and $\overline{RE}$ high). A shutdown mode delay of approximately 250ns (not tested in production) is imposed after this state is received before the chip enters shutdown. If either DE goes high or $\overline{RE}$ goes low during this delay, the delay timer is reset and the chip does not enter shutdown. This reduces the chance of accidentally entering shutdown if DE and $\overline{RE}$ are driven in parallel by a slowly changing signal or if DE and $\overline{RE}$ are driven by two independent signals with a timing skew between them.

This shutdown mode delay does not affect the outputs of the transmitter and receiver, which start to switch to the high impedance state upon the reception of their respective disable signals as defined by the parameters t_{SHDND} and t_{SHDNR}. The shutdown mode delay affects only the time when all the internal circuits that draw DC power from V_{CC} are turned off.

High Speed Considerations

A ground plane layout with a 0.1µF bypass capacitor placed less than 7mm away from the V_{CC} pin is recommended. The PC board traces connected to signals A/B should be symmetrical and as short as possible to maintain good differential signal integrity. To minimize capacitive effects, the differential signals should be separated by more than the width of a trace and should not be routed on top of each other if they are on different signal planes.

Care should be taken to route outputs away from any sensitive inputs to reduce feedback effects that might cause noise, jitter, or even oscillations.

The logic inputs have a typical hysteresis of 100mV to provide noise immunity. Fast edges on the outputs can cause glitches in the ground and power supplies which are exacerbated by capacitive loading. If a logic input is held near its threshold (typically $V_{CC}/2$), a noise glitch from a

APPLICATIONS INFORMATION

driver transition may exceed the hysteresis levels on the logic and data input pins, causing an unintended state change. This can be avoided by maintaining normal logic levels on the pins and by slewing inputs faster than 1V/µs. Good supply decoupling and proper driver termination also reduce glitches caused by driver transitions.

RS485 Cable Length vs Data Rate

Many factors contribute to the maximum cable length that can be used for RS485 or RS422 communication, including driver transition times, receiver threshold, duty cycle distortion, cable properties and data rate. A typical curve of cable length versus maximum data rate is shown in Figure 10. Various regions of this curve reflect different performance limiting factors in data transmission.

At frequencies below 100kbps, the maximum cable length is determined by DC resistance in the cable. In this example, a cable longer than 4000ft will attenuate the signal at the far end to less than what can be reliably detected by the receiver.

For data rates above 100kbps the capacitive and inductive properties of the cable begin to dominate this relationship. The attenuation of the cable is frequency and length dependent, resulting in increased rise and fall times at the far end of the cable. At high data rates or long cable lengths, these transition times become a significant part of the signal bit time. Jitter and intersymbol interference aggravate this so that the time window for capturing valid data at the receiver becomes impossibly small.

The boundary at 20Mbps in Figure 10 represents the guaranteed maximum operating rate of the LTC2862A-1. The dashed vertical line at 10Mbps represents the specified maximum data rate in the RS485 standard. This boundary is not a limit, but reflects the maximum data rate that the specification was written for.

It should be emphasized that the plot in Figure 10 shows a typical relation between maximum data rate and cable length. Results with the LTC2862A will vary, depending on cable properties such as conductor gauge, characteristic impedance, insulation material, and solid versus stranded conductors.

Low EMI 250kbps Data Rate

The LTC2862A-2 features slew rate limited transmitters for low electromagnetic interference (EMI) in sensitive applications. The slew rate limit circuit maintains consistent control of transmitter slew rates across voltage and temperature to ensure low EMI under all operating conditions. Figure 11 demonstrates the reduction in high frequency content achieved by the 250kbps mode compared to the 20Mbps mode.

The 250kbps mode has the added advantage of reducing signal reflections in an unterminated network, and thereby increasing the length of a network that can be used without termination. Using the rule of thumb that the rise time of the transmitter should be greater than four times the one-way delay of the signal, networks of up to 140 feet can be driven without termination.

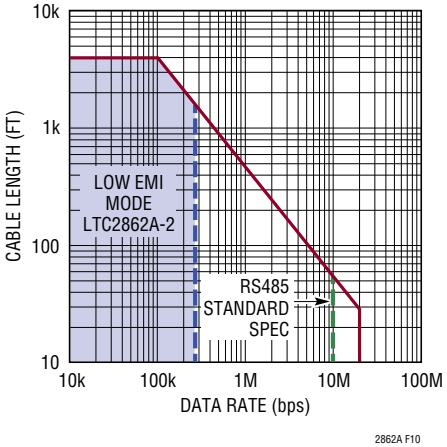


Figure 10. Cable Length vs Data Rate (RS485/RS422 Standard Shown in Vertical Dashed Line)

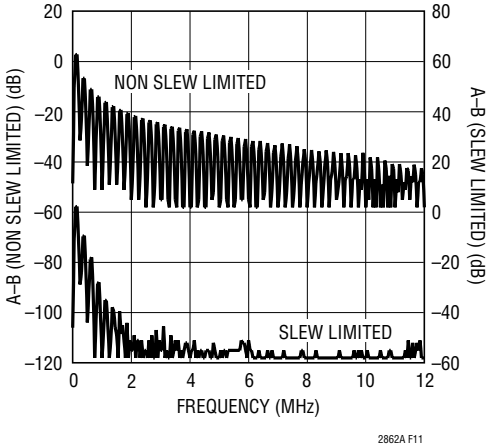


Figure 11. High Frequency EMI Reduction of Slew Limited 250kbps Mode Compared to Non Slew Limited 20Mbps Mode

APPLICATIONS INFORMATION

PROFIBUS Compatible Interface

PROFIBUS is an RS485-based field bus. In addition to the specifications of TIA/EIA-485-A, the PROFIBUS specification contains additional requirements for cables, interconnects, line termination, and signal levels. The following discussion applies to the PROFIBUS Type A cables with associated connectors and termination. The Type A cable is a twisted pair shielded cable with a characteristic impedance of 135Ω to 165Ω and a loop resistance of < 110Ω/km.

The LTC2862A RS485 transceiver may be used in PROFIBUS compatible equipment if the following considerations are implemented. (Please refer to the schematic of the PROFIBUS Compatible Interface in the Typical Applications Section.)

1. The polarity of the PROFIBUS signal is opposite to the polarity convention used in this data sheet. The PROFIBUS B wire is driven by a non-inverted signal, while the A wire is driven by an inverted signal. Therefore, it is necessary to swap the output connections from the transceiver. Pin A is connected to the PROFIBUS B wire, and Pin B is connected to the PROFIBUS A wire.
2. Each end of the PROFIBUS line is terminated with a 220Ω resistor between B and A, a 390Ω pull-up resistor between B and V_{CC}, and a 390Ω pull-down resistor between A and GND. This provides suitable termination for the 150Ω twisted pair transmission cable.
3. The peak to peak differential voltage V_{OD} received at the end of a 100m cable with the cable and terminations described above must be greater than 4V and less than 7V. The LTC2862A produces signal levels in excess of 7V when driving this network directly. 8.2Ω resistors may be inserted between the A and B pins of the transceiver and the B and A pins of the PROFIBUS cable to attenuate the transmitted signal to meet the PROFIBUS upper limit of 7V while still providing enough drive strength to meet the lower limit of 4V.
4. The LTC2862A transceiver should be powered by a 5% tolerance 5V supply (4.75V to 5.25V) to ensure that the PROFIBUS V_{OD} tolerances are met.

Auxiliary Protection for 5kV Surge, 5kV EFT, and 30kV IEC ESD

An interface transceiver used in an industrial setting may be exposed to extremely high levels of electrical overstress due to phenomena such as lightning surge, electrical fast transient (EFT) from switching high current inductive loads, and electrostatic discharge (ESD) from the discharge of electrically charged personnel or equipment. Test methods to evaluate immunity of electronic equipment to these phenomena are defined in the IEC standards 61000-4-2, 61000-4-4, and 61000-4-5, which address ESD, EFT, and surge, respectively. The transients produced by the EFT and particularly the surge tests contain much more energy than the ESD transients. The LTC2862A is designed for high robustness against ESD, but the on-chip protection is not able to absorb the energy associated with the 61000-4-5 surge transients. Therefore, a properly designed external protection network is necessary to achieve a high level of surge protection, and can also extend the ESD and EFT performance of the LTC2862A to extremely high levels.

In addition to providing surge, EFT and ESD protection, an external network should preserve or extend the ability of the LTC2862A to withstand overvoltage faults, operate over a wide common mode, and communicate at high frequencies. In order to meet the first two requirements, protection components with suitably high conduction voltages must be chosen. A means to limit current must be provided to prevent damage in case a secondary protection device or the ESD cell on the LTC2862A fires and conducts. The capacitance of these components must be kept low in order to permit high frequency communication over a network with multiple nodes. Meeting the requirements for conducting very high energy electrical transients while maintaining high hold-off voltages and low capacitance is a considerable challenge.

APPLICATIONS INFORMATION

A protection network shown in the Typical Applications section (Network for IEC Level 4 Protection Against 5kV Surge, 5kV EFT and 30kV IEC ESD Plus ±360V Overvoltage Protection) meets this challenge. The network provides the following protection:

- IEC 61000-4-2 ESD Level 4: ±30kV contact, ±30kV air (line to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a ground referenced test card per Figure 4 of the standard)
- IEC 61000-4-4 EFT Level 4: ±5kV (line to GND, 5kHz repetition rate, 15ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard)
- IEC 61000-4-5 Surge Level 4: ±5kV (line to GND, line to line, 8/20µs waveform, each line coupled to generator through 80Ω resistor per Figure 14 of the standard)

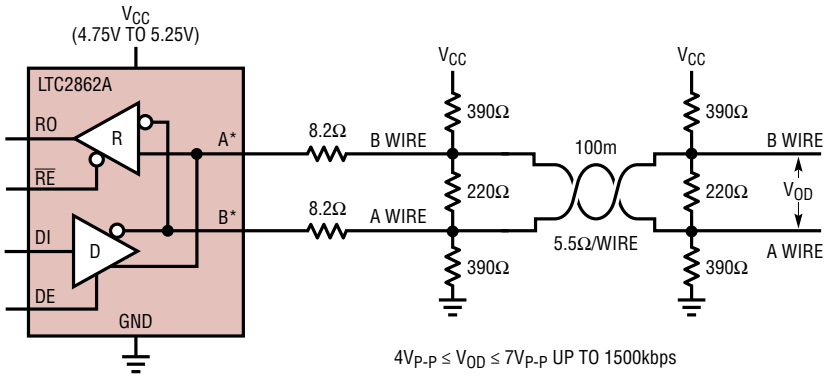
This protection circuit adds only ~8pF of capacitance per line (line to GND), thereby providing an extremely high level of protection without significant impact to the performance of the LTC2862A transceivers at high data rates.

The gas discharge tubes (GDTs) provide the primary protection against electrical surges. These devices provide a very low impedance and high current carrying capability when they fire, safely discharging the surge current to GND. The transient blocking units (TBUs) are solid state devices that switch from a low impedance pass through state to a high impedance current limiting state when a specified current level is reached. These devices limit the current and power that can pass through to the secondary protection. The secondary protection consists of a bidirectional thyristor, which triggers above 35V to protect the bus pins of the LTC2862A transceiver. The high trigger voltage of the secondary protection maintains the full ±25V common mode range of the receivers. The final component of the network is the metal oxide varistors (MOVs) which are used to clamp the voltage across the TBUs to protect them against fast ESD and EFT transients which exceed the turn-on time of the GDT.

The high performance of this network is attributable to the low capacitance of the GDT and thyristor primary and secondary protection devices. The high capacitance MOV floats on the line and is shunted by the TBU, so it contributes no appreciable capacitive load on the signal.

TYPICAL APPLICATIONS

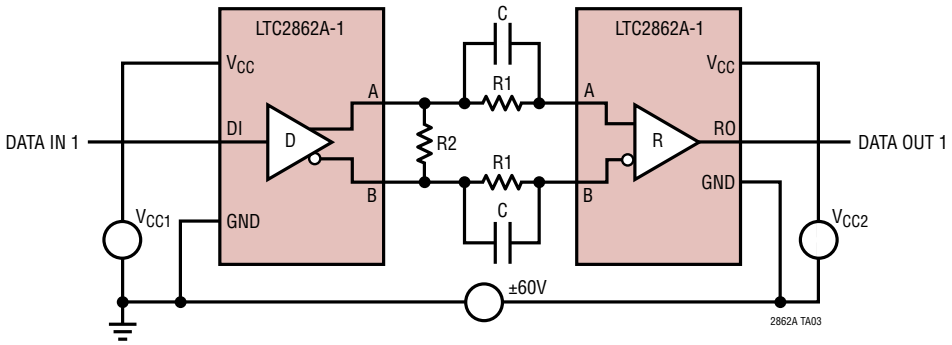
PROFIBUS Compatible Line Interface



* THE POLARITY OF A AND B IN THIS DATA SHEET IS OPPOSITE THE POLARITY DEFINED BY PROFIBUS.

2862A TA02

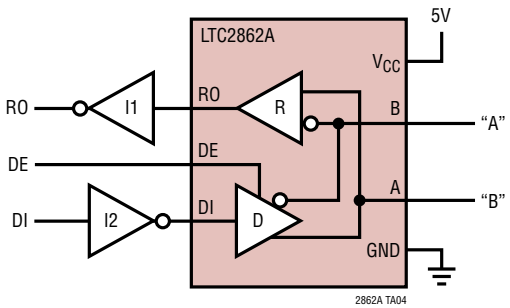
±60V 20Mbps Level Shifter/Isolator



2862A TA03

R1 = 200k 1%. PLACE R1 RESISTORS NEAR A AND B PINS OF RECEIVER.
R2 = 10k
C = 47pF, 5%, 50 WVDC. MAY BE OMITTED FOR DATA RATES < 100kbps.

Failsafe 0 Application (Idle State = Logic 0)

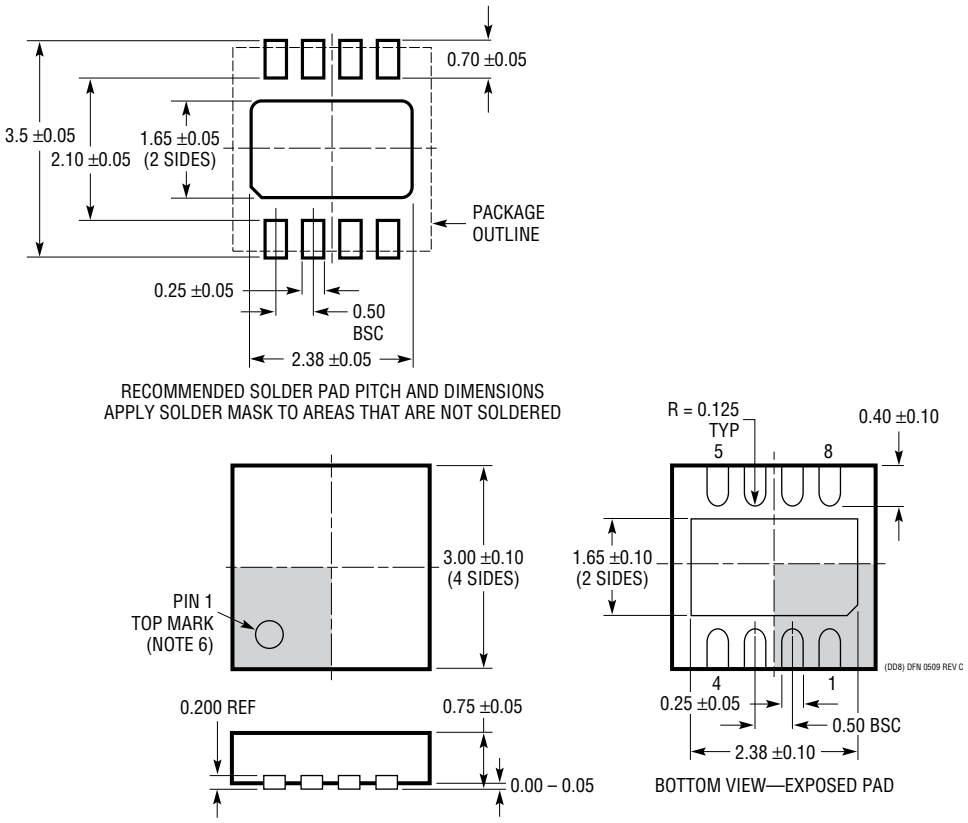


2862A TA04

Rev. A

PACKAGE DESCRIPTION

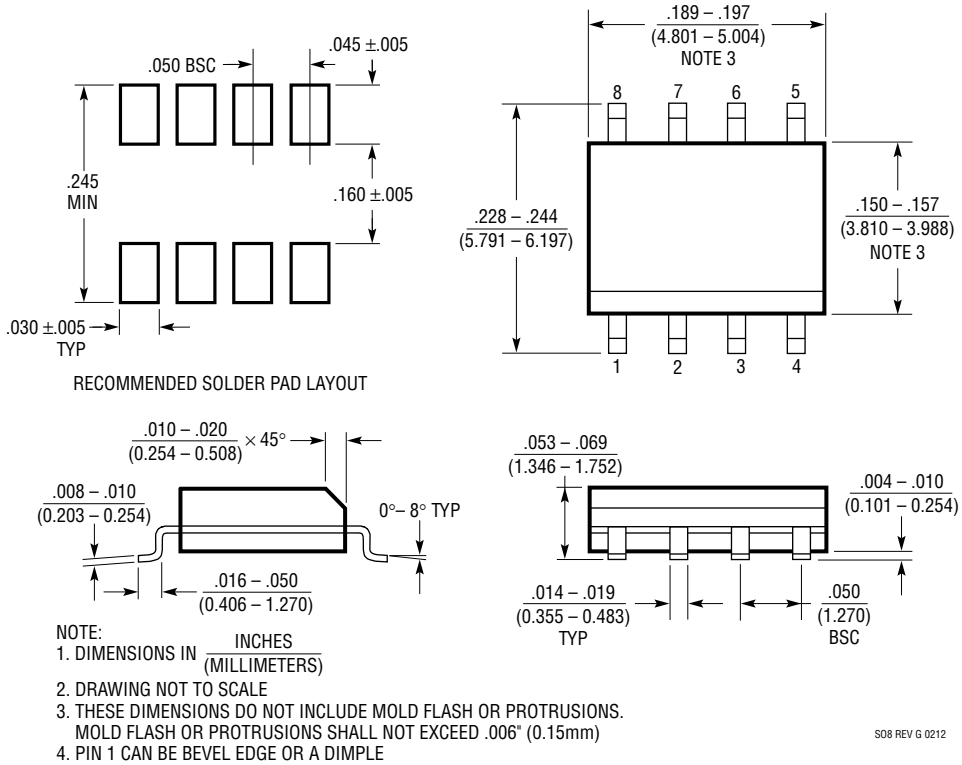
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/21	Add automotive grade.	1, 3