±60V Fault Protected 3.3V or 5V 25kV ESD High Speed CAN FD Transceiver

FEATURES

- **Protected from Overvoltage Line Faults to ±60V**
- **3.3V or 5V Supply Voltage**
- **High Speed CAN FD Operation Up to 4Mbps**
- **±25kV ESD Interface Pins, ±8kV All Other Pins**
- **Variable Slew Rate Driver with Active Symmetry Control and SPLIT Pin for Low Electromagnetic Emission (EME)**
- **Extended Common Mode Range (±36V)**
- Ideal Passive Behavior to CAN Bus with Supply Off
- Current Limited Drivers and Thermal Shutdown
- Power-Up/Down Glitch-Free Driver Outputs
- Micropower Shutdown Mode
- Transmit Data (TXD) Dominant Timeout Function
- ISO 11898-2 and CAN FD Compliant
- DeviceNet Compatible
- Up to MP-Grade Available (–55°C to 125°C)
- 3mm × 3mm 8-Lead DFN and SO-8 Packages

APPLICATIONS

- Industrial Control and Instrumentation Networks
- Automotive and Transportation Electronics
- Building Automation, Security Systems, HVAC
- Medical Equipment

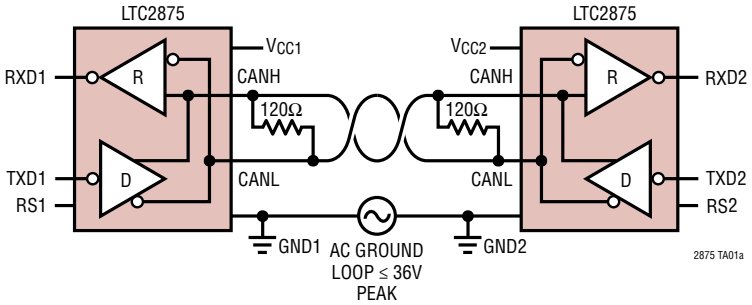
DESCRIPTION

The LTC®2875 is a robust high speed, low power CAN transceiver operating on 3.3V or 5V supplies that features ±60V overvoltage fault protection on the data transmission lines during all modes of operation, including power-down. The maximum data rate has been extended to 4Mbps to support high speed protocols based on the CAN physical layer. Supports up to 4Mbps CAN with Flexible Data Rate (CAN FD). Enhanced ESD protection allows these parts to withstand ±25kV HBM on the transceiver interface pins without latchup or damage.

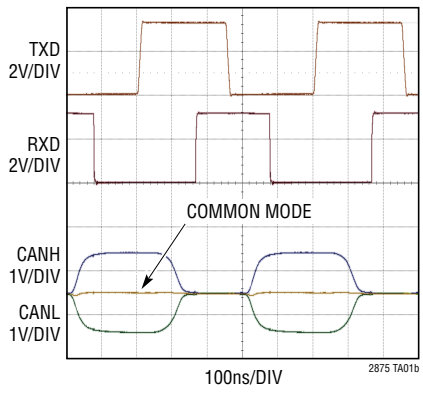
Extended ±36V input common mode range and high common mode rejection on the CAN receiver provides tolerance of large ground loop voltages. A sophisticated CAN driver with active symmetry control maintains tight control of the common mode voltage for excellent electromagnetic emission, while the variable slew rate and split termination support allow additional EME reduction.

TYPICAL APPLICATION

CAN Bus Link with Large Ground Loop Voltage



LTC2875 Transmitting at 4Mbps from a 3.3V Supply



ABSOLUTE MAXIMUM RATINGS

(Note 1)

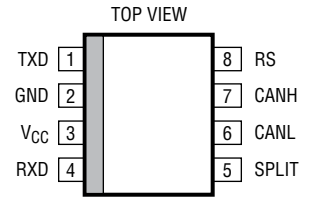
Supply Voltages
- V_{CC} ..... –0.3V to 6V

Logic Input Voltages (TXD, RS) ..... –0.3V to 6V
Interface I/O: CANH, CANL, SPLIT ..... –60V to 60V
Receiver Output (RXD) ..... –0.3V to (V_{CC} + 0.3V)
Bus Differential Voltage (CANH-CANL) ..... –120V to 120V

Operating Ambient Temperature Range (Note 4)
- LTC2875I ..... –40°C to 85°C
- LTC2875H ..... –40°C to 125°C
- LTC2875MP ..... –55°C to 125°C

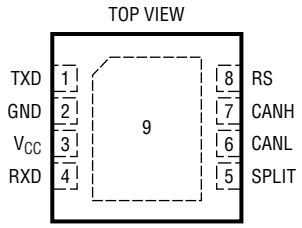
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



S8 PACKAGE
8-LEAD (150mil) PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 120°C/W, θ_{JC} = 39°C/W



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 9) CONNECT TO PCB GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2875IDD#PBF	LTC2875IDD#TRPBF	LGKG	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2875HDD#PBF	LTC2875HDD#TRPBF	LGKG	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2875MPDD#PBF	LTC2875MPDD#TRPBF	LGKG	8-Lead (3mm × 3mm) Plastic DFN	–55°C to 125°C
LTC2875IS8#PBF	LTC2875IS8#TRPBF	2875	8-Lead (150 mil) Plastic SO	–40°C to 85°C
LTC2875HS8#PBF	LTC2875HS8#TRPBF	2875	8-Lead (150 mil) Plastic SO	–40°C to 125°C
LTC2875MPS8#PBF	LTC2875MPS8#TRPBF	2875	8-Lead (150 mil) Plastic SO	–55°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V or 5V, Figure 1 applies with R_L = 60Ω, RS = 0V, TYP values at V_{CC} = 5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
Supplies									
V_{CC}	Supply Voltage		3.3V V_{CC} Range		●	3	3.3	3.6	V
			5V V_{CC} Range		●	4.5	5	5.5	V
$I_{CC(R)}$	Supply Current (Recessive)				●	1	1.8	3	mA
$I_{CC(D)}$	Supply Current (Dominant)				●	25	42	60	mA
I_{CCS}	Supply Current in Shutdown Mode (I-Grade)		RS = TXD = V_{CC}, RXD Open, T ≤ 85°C		●		1	5	µA
	Supply Current in Shutdown Mode (H-, MP-Grade)		RS = TXD = V_{CC}, RXD Open, T ≤ 125°C		●		1	15	µA
Driver									
$V_{O(D)}$	Bus Output Voltage (Dominant)	CANH	t < t_{TOTXD}	V_{CC} = 5V	●	2.75	3.6	4.5	V
				V_{CC} = 3.3V	●	2.15	2.9	3.3	V
		CANL	t < t_{TOTXD}	V_{CC} = 5V	●	0.5	1.4	2.25	V
				V_{CC} = 3.3V	●	0.5	0.9	1.65	V
$V_{O(R)}$	Bus Output Voltage (Recessive)		V_{CC} = 5V, No Load (Figure 1)		●	2	2.5	3	V
			V_{CC} = 3.3V, No Load (Figure 1)		●	1.45	1.95	2.45	V
$V_{OD(D)}$	Differential Output Voltage (Dominant)		R_L = 50Ω to 65Ω (Figure 1)		●	1.5	2.2	3.0	V
$V_{OD(R)}$	Differential Output Voltage (Recessive)		No Load (Figure 1)		●	–500	0	50	mV
$V_{OC(D)}$	Common Mode Output Voltage (Dominant)		V_{CC} = 5V, (Figure 1)		●	2	2.5	3	V
			V_{CC} = 3.3V, (Figure 1)		●	1.45	1.95	2.45	V
$I_{OS(D)}$	Bus Output Short-Circuit Current (Dominant)	CANH	CANH = 0V		●	–100	–75	–40	mA
		CANH	–60V ≤ CANH ≤ 60V		●	–100		3	mA
		CANL	CANL = 5V		●	40	75	100	mA
		CANL	–60V ≤ CANL ≤ 60V		●	–3		100	mA
Receiver									
V_{CM}	Bus Common Mode Voltage = (CANH + CANL)/2 for Data Reception		V_{CC} = 5V		●			±36	V
			V_{CC} = 3.3V		●			±25	V
V_{TH}^+	Bus Input Differential Threshold Voltage (Positive-Going)		V_{CC} = 5V, –36V ≤ V_{CM} ≤ 36V		●		775	900	mV
			V_{CC} = 3.3V, –25V ≤ V_{CM} ≤ 25V		●		775	900	mV
V_{TH}^-	Bus Input Differential Threshold Voltage (Negative-Going)		V_{CC} = 5V, –36V ≤ V_{CM} ≤ 36V		●	500	625		mV
			V_{CC} = 3.3V, –25V ≤ V_{CM} ≤ 25V		●	500	625		mV
ΔV_{TH}	Bus Input Differential Hysteresis Voltage		V_{CC} = 5V, –36V ≤ V_{CM} ≤ 36V				150		mV
			V_{CC} = 3.3V, –25V ≤ V_{CM} ≤ 25V				150		mV
R_{IN}	Input Resistance (CANH and CANL)		TXD = V_{CC}; R_{IN} = ΔV/ΔI; ΔI = ±20µA		●	25	40	50	kΩ
R_{ID}	Differential Input Resistance		TXD = V_{CC}; R_{IN} = ΔV/ΔI; ΔI = ±20µA		●	50	80	100	kΩ
ΔR_{IN}	Input Resistance Matching		R_{IN} (CANH) to R_{IN} (CANL)		●			±1	%
C_{IH}	Input Capacitance to GND (CANH)		(Note 6)				32		pF
C_{IL}	Input Capacitance to GND (CANL)		(Note 6)				8		pF
C_{ID}	Differential Input Capacitance		(Note 6)				8.4		pF
I_L	Bus Leakage Current (Power Off) (I-Grade)		V_{CC} = 0V, CANH = CANL = 5V, T ≤ 85°C		●			±10	µA
	Bus Leakage Current (Power Off) (H-, MP-Grade)		V_{CC} = 0V, CANH = CANL = 5V, T ≤ 125°C		●			±40	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V or 5V, Figure 1 applies with R_L = 60Ω, RS = 0V, TYP values at V_{CC} = 5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Common Mode Stabilization Output SPLIT								
V_{O_SPLIT}	SPLIT Output Voltage	–500µA ≤ I(SPLIT) ≤ 500µA	V_{CC} = 5V	●	1.5	2.5	3.5	V
			V_{CC} = 3.3V	●	0.9	1.9	2.9	V
I_{OS_SPLIT}	SPLIT Short-Circuit Current	–60V ≤ SPLIT ≤ 60V		●	–3		3	mA
Receiver Output RXD								
V_{OH_RXD}	Receiver Output High Voltage	I(RXD) = –3mA (Sourcing)		●	V_{CC} – 0.4V			V
V_{OL_RXD}	Receiver Output Low Voltage	I(RXD) = 3mA (Sinking)		●			0.4	V
I_{OS_RXD}	Receiver Short-Circuit Current	RXD = 0V or V_{CC}		●		±11	±18	mA
Logic Input TXD								
V_{IH_TXD}	High Level Input Voltage	V_{CC} = 3.3V or 5V		●	0.67 • V_{CC}			V
V_{IL_TXD}	Low Level Input Voltage	V_{CC} = 3.3V or 5V		●			0.33 • V_{CC}	V
I_{IN_TXD}	Logic Input Current	0 ≤ TXD ≤ V_{CC}		●	–20	0	10	µA
Logic / Slew Control Input RS								
V_{IH_RS}	High Level Input Voltage	V_{CC} = 3.3V or 5V		●	0.9 • V_{CC}			V
V_{IL_RS}	Low Level Input Voltage	V_{CC} = 3.3V or 5V		●			0.5 • V_{CC}	V
I_{IN_RS}	Logic Input Current	0 ≤ RS ≤ V_{CC}		●	–170	0	10	µA

SWITCHING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 3.3V or 5V, Figure 1 applies with R_L = 60Ω, C_L = 100pF, RSL = 0Ω, RS = 0V, TYP values at V_{CC} = 5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Transceiver Timing								
f_{MAX}	Maximum Data Rate			●	4			Mbps
t_{PTXBD}	TXD to Bus Dominant Propagation Delay	(Figure 2, 3)	V_{CC} = 3.3V	●	45	80	130	ns
			V_{CC} = 5V	●	45	75	115	ns
t_{PTXBR}	TXD to Bus Recessive Propagation Delay	(Figure 2, 3)	V_{CC} = 3.3V	●	80	120	170	ns
			V_{CC} = 5V	●	60	90	120	ns
t_{PTXBDS}	TXD to Bus Dominant Propagation Delay, Slow Slew	RSL=200kΩ (Figure 2, 3)	V_{CC} = 3.3V	●	200	540	1220	ns
			V_{CC} = 5V	●	220	560	1200	ns
t_{PTXBRS}	TXD to Bus Recessive Propagation Delay, Slow Slew	RSL=200kΩ (Figure 2, 3)	V_{CC} = 3.3V	●	400	960	2010	ns
			V_{CC} = 5V	●	480	1040	2240	ns
t_{PBDRX}	Bus Dominant to RXD Propagation Delay	(Figure 2, 3)		●	25	40	65	ns
t_{PBRRX}	Bus Recessive to RXD Propagation Delay	(Figure 2, 3)		●	25	45	80	ns
t_{PTXRXD}	TXD to RXD Dominant Propagation Delay	(Figure 2, 3)	V_{CC} = 3.3V	●	80	120	180	ns
			V_{CC} = 5V	●	75	115	165	ns
t_{PTXRXR}	TXD to RXD Recessive Propagation Delay	(Figure 2, 3)	V_{CC} = 3.3V	●	115	165	215	ns
			V_{CC} = 5V	●	95	135	185	ns
$t_{PTXRXDS}$	TXD to RXD Dominant Propagation Delay, Slow Slew	RSL = 200kΩ (Figure 2, 3)	V_{CC} = 3.3V	●	190	500	1110	ns
			V_{CC} = 5V	●	210	530	1090	ns
$t_{PTXRXRS}$	TXD to RXD Recessive Propagation Delay, Slow Slew	RSL = 200kΩ (Figure 2, 3)	V_{CC} = 3.3V	●	420	940	1910	ns
			V_{CC} = 5V	●	480	1020	2110	ns
t_{TOTXD}	TXD Timeout Time	(Figure 2, 4)		●	0.5	2	4	ms
$t_{BIT(RXD),2M}$	Receiver Output Recessive Bit Time, 2Mbps, Loop Delay Symmetry	(Figure 7)	V_{CC2} = 3.3V	●	400	455	550	ns
			V_{CC2} = 5V	●	400	475	550	ns
$t_{BIT(RXD),4M}$	Receiver Output Recessive Bit Time, 4Mbps	(Figure 7)	V_{CC2} = 5V	●	200	225	275	ns
t_{ENRX}	RXD Enable from Shutdown	(Figure 5)		●			40	µs
t_{ENTX}	TXD Enable from Shutdown	(Figure 2, 6) (Note 5)		●			40	µs
t_{SHDNRX}	Time to Shutdown, RXD	(Figure 5)		●			250	ns
t_{SHDNTX}	Time to Shutdown, TXD	(Figure 2, 6)		●			250	ns
Transmitter Drive Symmetry (Common Mode Voltage Fluctuation)								
V_{SYM}	Driver Symmetry (CANH + CANL – $2V_{O(R)}$) (Dynamic Peak Measurement)	RL = 60Ω/Tol. < 1%, C_{SPLIT} = 4.7nF/5%, fTXD = 250kHz, Input Impedance of Oscilloscope: ≤ 20pF/ ≥ 1MΩ (Figure 2)		●			±500	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: Not tested in production.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may result in device degradation or failure.

Note 5: TXD must make a high to low transition after this time to assert a bus dominant state.

Note 6: Pin capacitance given for reference only and is not tested in production.

TEST CIRCUITS

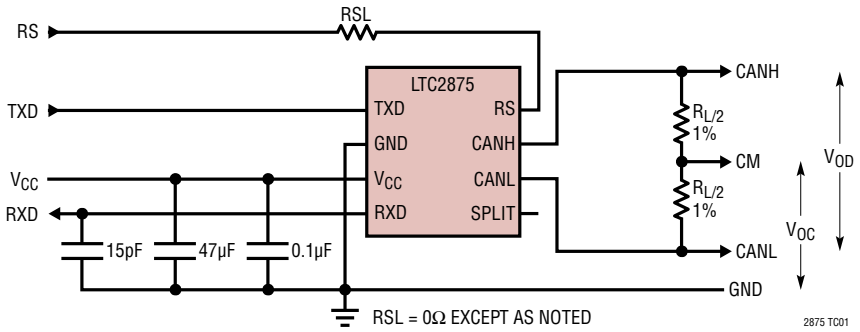


Figure 1. All Electrical Characteristic Measurements

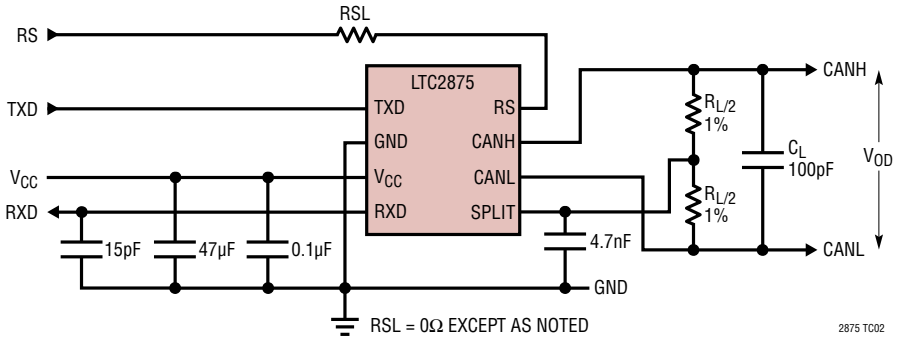


Figure 2. All Switching Characteristic Measurements Except Receiver Enable/Disable Times

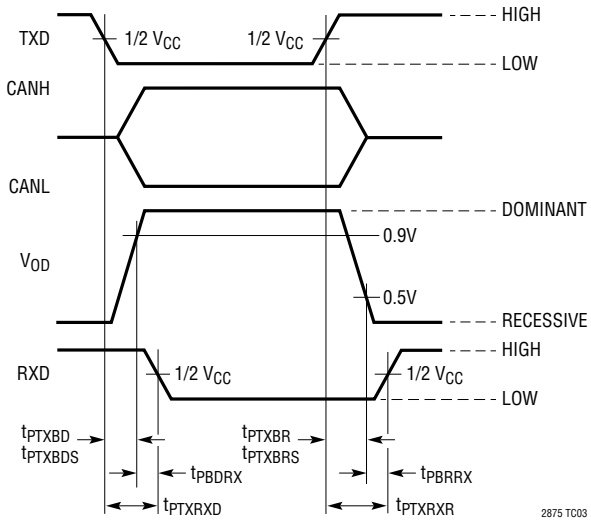


Figure 3. CAN Transceiver Data Propagation Timing Diagram

TEST CIRCUITS

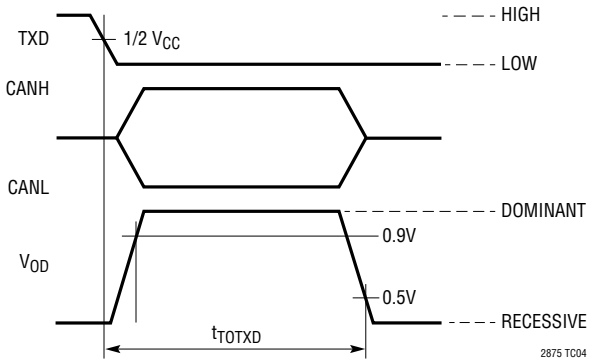


Figure 4. TXD Dominant Timeout Time

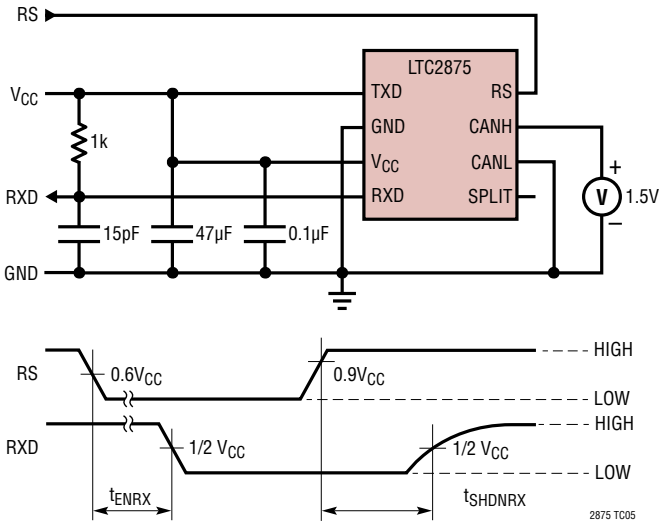


Figure 5. RXD Enable and Disable Timing

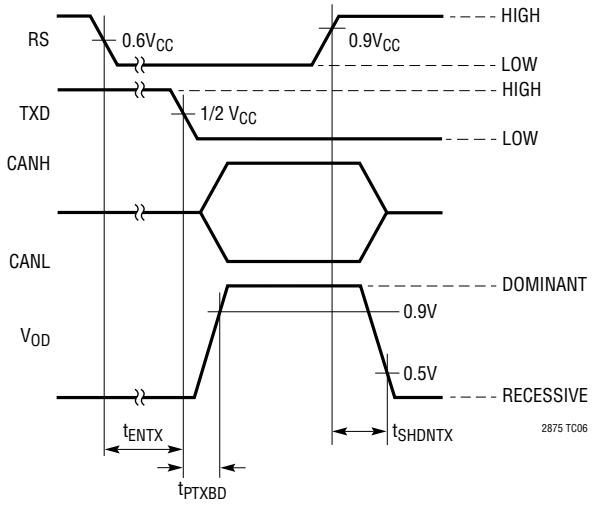


Figure 6. TXD Enable and Disable Timing

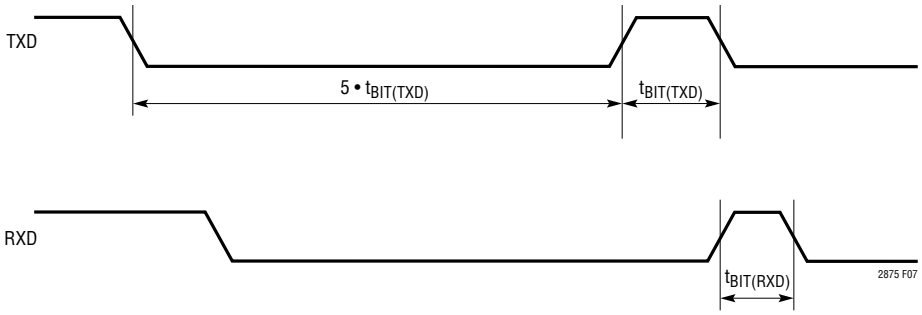
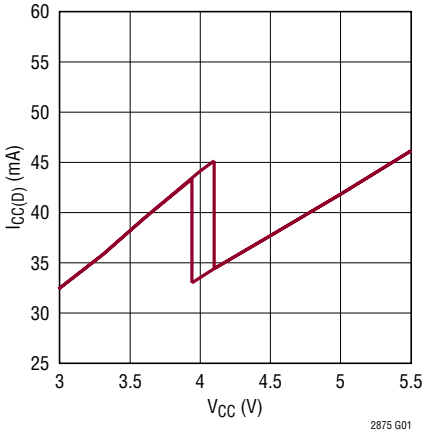


Figure 7. Loop Delay Symmetry

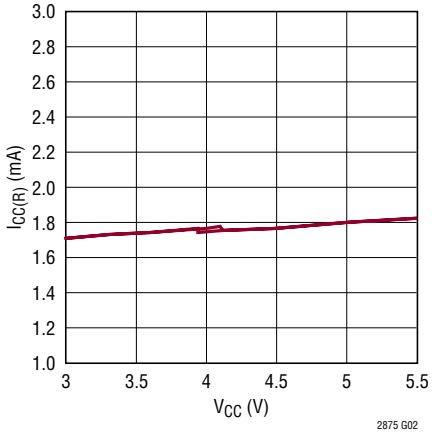
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V or 5V, R_L = 60Ω, C_L = 100pF, RSL = 0Ω, RS = 0V unless otherwise noted.

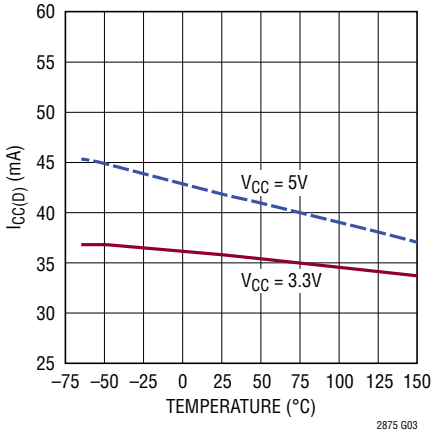
Supply Current (Dominant) vs V_{CC}



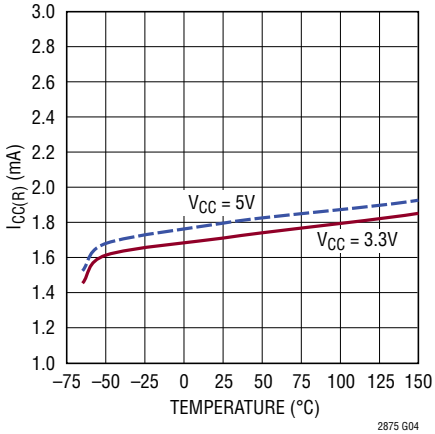
Supply Current (Recessive) vs V_{CC}



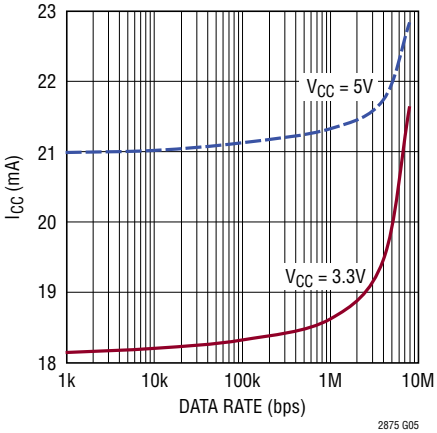
Supply Current (Dominant) vs Temperature



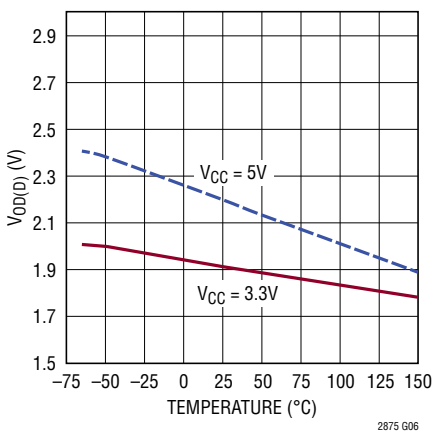
Supply Current (Recessive) vs Temperature



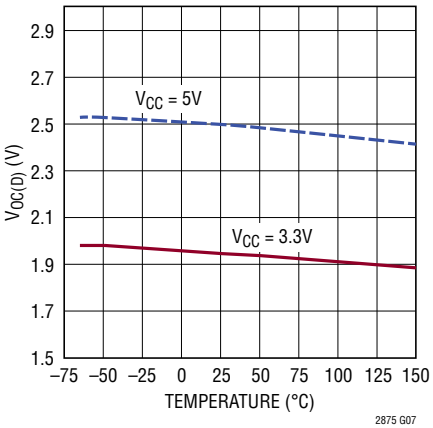
Supply Current vs Data Rate



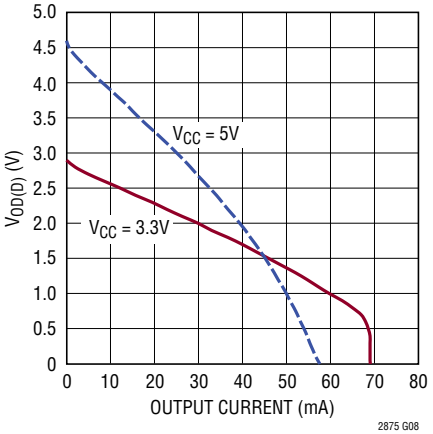
Driver Differential Output Voltage (Dominant) vs Temperature



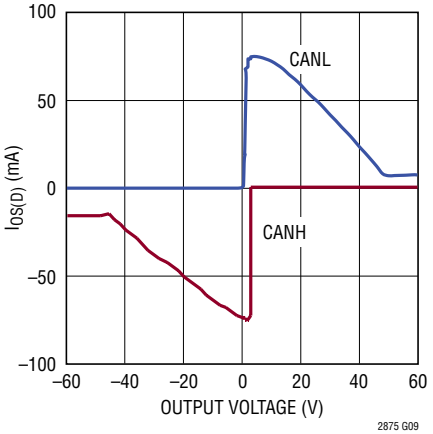
Common Mode Output Voltage (Dominant) vs Temperature



Driver Differential Output Voltage (Dominant) vs Output Current



Driver Output Short-Circuit Current (Dominant) vs Voltage

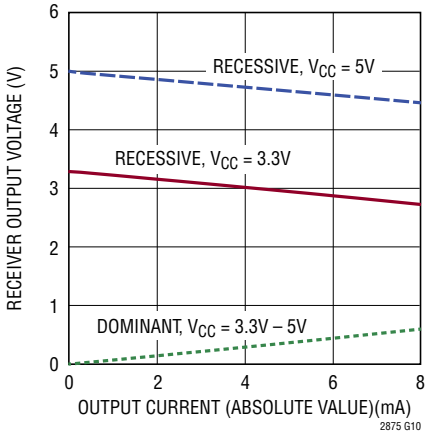


Rev A

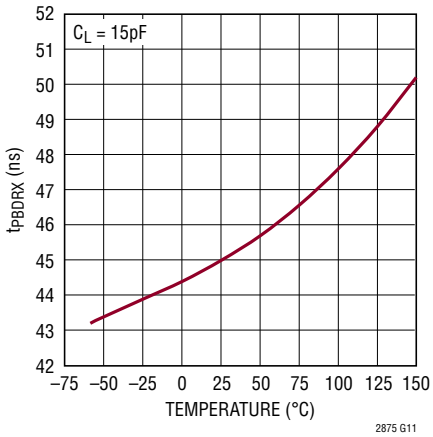
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = 3.3V or 5V, R_L = 60Ω, C_L = 100pF, RSL = 0Ω, RS = 0V unless otherwise noted.

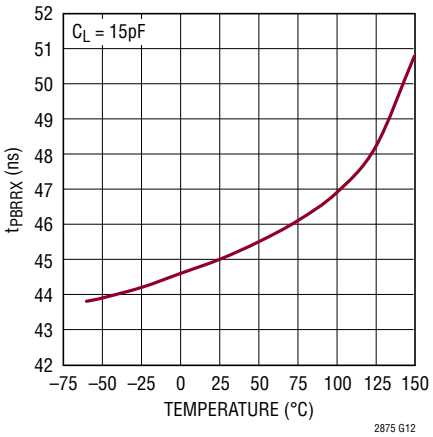
Receiver Output Voltage vs Output Current



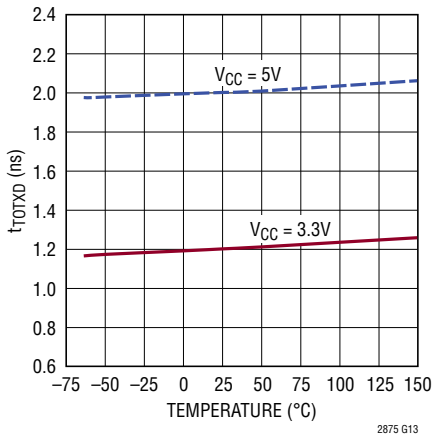
Bus Dominant to RXD Propagation Delay vs Temperature



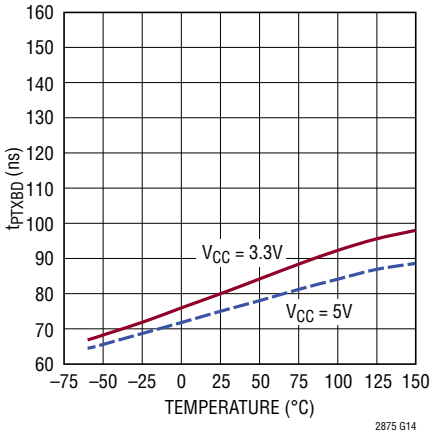
Bus Recessive to RXD Propagation Delay vs Temperature



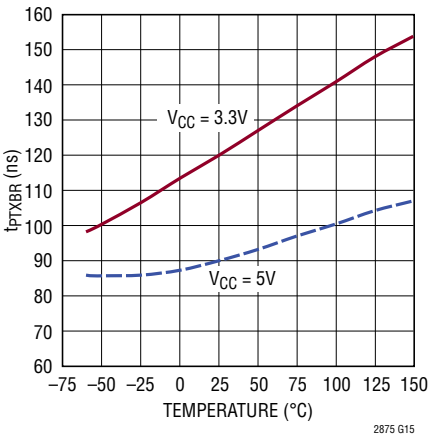
TXD Timeout Time vs Temperature



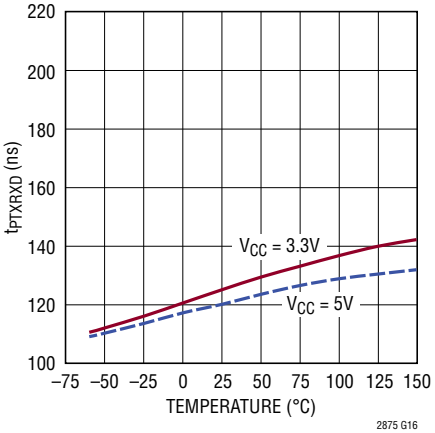
TXD to Bus Dominant Propagation Delay vs Temperature



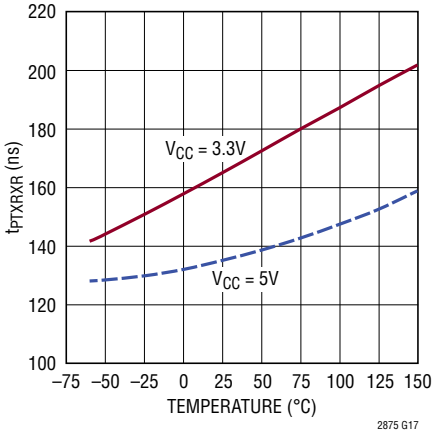
TXD to Bus Recessive Propagation Delay vs Temperature



TXD to RXD Dominant Propagation Delay vs Temperature



TXD to RXD Recessive Propagation Delay vs Temperature



PIN FUNCTIONS

TXD (Pin 1): Transmit Data Input. Low in dominant state. Integrated 500k pull-up to V_{CC}.

GND (Pin 2): Ground.

V_{CC} (Pin 3): Positive Supply. $3V \leq V_{CC} \leq 3.6V$ or $4.5V \leq V_{CC} \leq 5.5V$. Bypass with 0.1µF ceramic capacitor or larger.

RXD (Pin 4): Receiver Data Output. Low in dominant state. Integrated 500k pull-up to V_{CC}.

SPLIT (Pin 5): Common Mode Stabilization Output for Optional Split Termination. ±60V tolerant, 25kV ESD. If unused, leave open.

CANL (Pin 6): Low Level CAN Bus Line. ±60V tolerant, 25kV ESD.

CANH (Pin 7): High Level CAN Bus Line. ±60V tolerant, 25kV ESD.

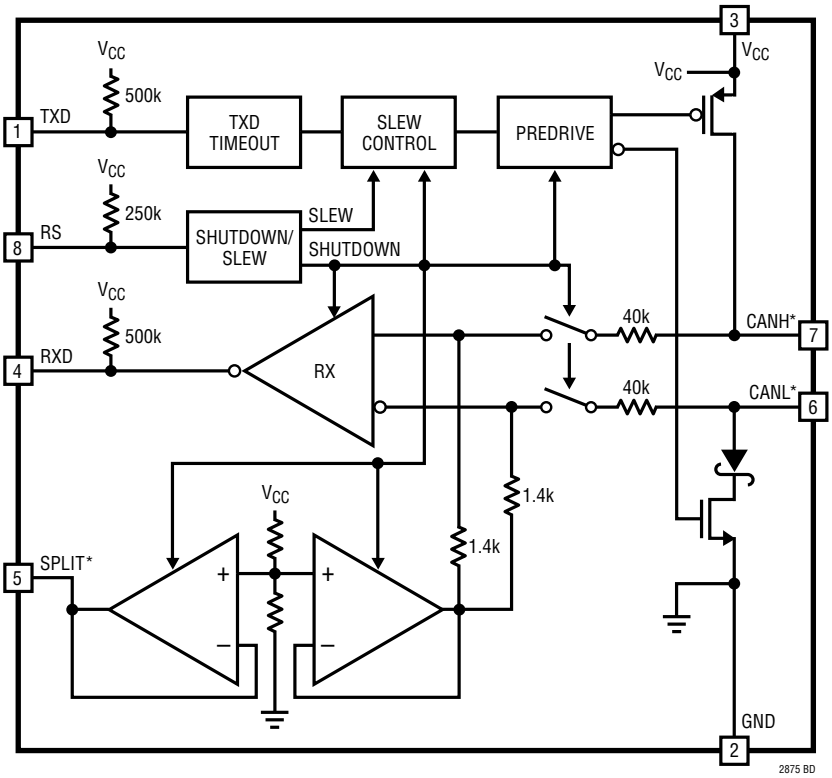
RS (Pin 8): Shutdown Mode/Slew Control Input. A voltage on RS higher than V_{IH_RS} puts the chip in a low power shutdown state. A voltage on RS lower than V_{IL_RS} enables the chip. A resistor between RS and ground can be used to control the slew rate. See Applications section for details.

GND (Pin 9): Exposed pad on the DFN package. Connect to PCB ground.

FUNCTIONAL TABLES

LOGIC INPUTS		MODE	CANH, CANL	RXD
RS	TXD			
0	0	Active	Dominant ($t < t_{TOTXD}$)	0
0	1	Active	Recessive	Receive Bus Data
$\sim 0.9V \leq V_{RS} \leq \sim 1.1V$	–	Slew Control	–	–
1	X	Shutdown	High-Z	High-Z

BLOCK DIAGRAM



*±60V TOLERANT, ±25kV HBM PROTECTED PINS

Figure 8. LTC2875 Simplified Block Diagram

APPLICATIONS INFORMATION

Supply Voltage Ranges

The LTC2875 can operate from 3.3V or 5V supplies. An internal comparator monitors the supply voltage and switches internal reference voltages and output drive strengths at approximately 4.1V. Because of the discontinuity in the internal voltages at this switch point, operation with a supply voltage between 3.6V and 4.5V is not recommended.

±60V Fault Protection

The LTC2875 addresses application needs for an overvoltage tolerant CAN transceiver that can operate from both 3.3V and 5V supplies and provide extended common mode operation, high noise immunity and low electromagnetic emission. Industrial installations may encounter common mode voltages between nodes far greater than the –2V to 7V range specified by the ISO 11898-2 standard. Competing CAN transceivers can be damaged by voltages beyond their typical absolute maximum ratings of –3V to 16V. The limited overvoltage tolerance makes implementation of effective external protection networks difficult without interfering with proper data network performance. Replacing standard CAN transceivers with LTC2875 devices can eliminate field failures due to overvoltage faults without using costly external protection devices.

The ±60V fault protection of the LTC2875 is achieved by using a high voltage BiCMOS integrated circuit technology. The naturally high breakdown voltage of this technology provides protection in powered off and high impedance conditions. The driver outputs use a progressive foldback current limit to protect against overvoltage faults while still allowing high current output drive.

The LTC2875 is protected from ±60V bus faults even with the loss of GND or V_{CC} (GND open faults are not tested in production). In the case of V_{CC} open, or shorted to GND, the LTC2875 is off and the bus pins remain in the high impedance state. Additional precautions must be taken in the case of V_{CC} present and GND open. The LTC2875 chip protects itself from damage but may turn on despite the open GND pin. When the RS or TXD input is pulled low with the GND pin floating, a sneak path to GND is established: through the ESD diode on the RS or TXD pin; out through the RS or TXD pin; and into the external driver that is pulling the pin low (Figure 9).

The current in this path can have a maximum current of –100mA with a maximum voltage of approximately V_{CC} – 2.5V during an overvoltage fault condition on the CANL pin because the entire current that should flow out the GND pin may flow out the input pin instead. If a GND open fault with V_{CC} present is anticipated, the system designer should choose drivers for the RS and TXD inputs that are protected against shorts to V_{CC} – 2.5V.

The high voltage rating of the LTC2875 makes it simple to extend the overvoltage protection to higher levels using external protection components. Compared to lower voltage CAN transceivers, external protection devices with higher breakdown voltages can be used so as not to interfere with data transmission in the presence of large common mode voltages. Figure 14 in the Typical Application section shows a network capable of protecting against IEC Level 4 surge, while still providing up to ±35V common mode range on the signal lines.

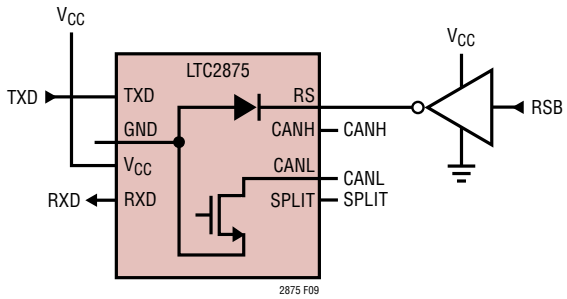


Figure 9. Sneak Path to GND with GND Pin Floating

±36V Extended Common Mode Range

The LTC2875 receiver features an extended common mode range of –36V to 36V when operating from a 5V supply, and –25V to 25V when operating from a 3.3V supply. The wide common mode increases the reliability of operation in environments with high common mode voltages created by electrical noise or local ground potential differences due to ground loops. This extended common mode range allows the LTC2875 to transmit and receive under conditions that would cause data errors and possible device damage in competing products.

APPLICATIONS INFORMATION

±25kV ESD Protection

The LTC2875 features exceptionally robust ESD protection. The transceiver interface pins (CANH, CANL, SPLIT) feature protection with respect to GND to ±25kV HBM without latchup or damage, during all modes of operation or while unpowered. All other pins are protected to ±8kV HBM to make the LTC2875 reliable under severe environmental conditions.

4Mbps Operation

The LTC2865 features a high speed receiver and transmitter capable of operating up to 4 Mbps. In order to operate at this data rate, the transmitter must be set at its maximum slew rate by pulling the RS pin low to ground with no more than 4kΩ of resistance, including the output impedance of the buffer driving the RS input (see RS Pin and Variable Slew Rate Control below).

Driver

The driver provides full CAN compatibility. When TXD is low with the chip enabled (RS low), the dominant state is asserted on the CAN bus lines (subject to the TXD timeout t_{TOTXD}); the CANH driver pulls high and the CANL driver pulls low. When TXD is high and RS is low, the driver is in the recessive state; both the CANH and CANL drivers are in the Hi-Z state and the bus termination resistor equalizes the voltage on CANH and CANL. In the recessive state, the impedance on CANH and CANL is determined by the receiver input resistance, R_{IN}. When RS is high the LTC2875 is in shutdown; the CANH and CANL drivers are in the Hi-Z state, and the receiver input resistance R_{IN} is disconnected from the bus by a FET switch.

Transmit Dominant Timeout Function

The LTC2875 includes a 2ms (typical) timer to limit the time that the transmitter can hold the bus in the dominant state. If TXD is held low, a dominant state is asserted on CANH and CANL until the TXD timer times out at t_{TOTXD}, after which the transmitter reverts to the recessive state. The timer is reset when TXD is brought high. The transmitter asserts a dominant state upon the next TXD low.

The lowest data rate that can be communicated without interference from the transmit dominant timeout timer is 22kbps, corresponding to 11 consecutive dominant bits divided by a bit time equal to the minimum t_{TOTXD} value of 0.5ms. 11 dominant bits is the maximum allowed by the CAN protocol, consisting of 5 dominant bits followed by an error frame of 6 dominant bits.

Driver Overvoltage, Overcurrent, and Overtemperature Protection

The driver outputs are protected from short circuits to any voltage within the absolute maximum range of –60V to 60V. The maximum current in a fault condition is ±100mA. The driver includes a progressive foldback current limiting circuit that continuously reduces the driver current limit with increasing output fault voltage. The fault current is typically ±10mA for fault voltages of ±60V.

The LTC2875 also features thermal shutdown protection that disables the driver in case of excessive power dissipation (see Notes 3 and 4). When the die temperature exceeds 170°C (typical), the transmitter is forced into the recessive state. The receiver remains operational.

Power-Up/Down Glitch-Free Outputs

The LTC2875 employs a supply undervoltage detection circuit to control the activation of the circuitry on-chip. During power-up, the CANH, CANL, RXD and SPLIT outputs remain in the high impedance state until the supply reaches a voltage sufficient to reliably operate the chip. At this point, the chip activates if RS is low. The receiver output goes active after a short delay t_{ENRX} and reflects the state at the CAN bus pins, and the SPLIT output goes active at approximately the same time. The transmitter powers up in the transmit dominant timeout state regardless of the state of the TXD pin, and remains in the recessive state until the first high to low transition on TXD after the TXD enable time t_{ENTX}. This assures that the transmitter does not disturb the bus by glitching to the dominant state during power-up.

During power down, the reverse occurs; the supply undervoltage detection circuit senses low supply voltage and immediately puts the chip into shutdown. CANH, CANL, RXD, and SPLIT outputs go to the high impedance state. The voltage on RXD is pulled high by the 500k pull-up resistor.

APPLICATIONS INFORMATION

Common Mode Voltage vs Supply Voltage

When operating from a 5V supply the LTC2875 adheres to the ISO 11898-2 CAN bus standard by maintaining drive levels that are symmetric around $V_{CC}/2 = 2.5V$. An internal common mode reference of $V_{CC}/2$ is buffered to supply the termination of the receiver input resistors. A second buffer with a high voltage tolerant output supplies $V_{CC}/2$ to the SPLIT output.

When operating from a 3.3V supply the 2.5V nominal common mode voltage specified in the ISO 11898-2 standard is too close to the 3.3V supply to provide symmetric drive levels while maintaining the necessary differential output voltage. To maintain driver symmetry the common mode reference voltage is lowered during 3.3V operation. The typical output common mode voltage is 1.95V in the dominant state. The internal common mode reference is set to $V_{CC}/2 + 0.3V = 1.95V$ to match the dominant state output common mode voltage. This reference is independently buffered to supply the termination of the receiver input resistors and the SPLIT voltage output.

As the LTC2875 operates over a very wide common mode range, this small shift of –0.55V in the common mode when operating from 3.3V does not degrade data transmission or reception. An LTC2875 operating at 3.3V may share a bus with other CAN transceivers operating at 5V. However, the electromagnetic emissions may be larger if transceivers powered by different voltages share a bus, due to the fluctuation in the common mode voltage from 1.95V (when an LTC2875 on a 3.3V supply is dominant) to 2.5V (when a CAN transceiver on a 5V supply is dominant).

RS Pin and Variable Slew Rate Control

The driver features adjustable slew rate for improved EME performance. The slew rate is set by the amount of current that is sourced by the RS pin when it is pulled below approximately 1.1V. This allows the slew rate to be set by a single slew control resistor RSL in series with the RS pin (Figure 1).

The relationship between the series slew control resistor RSL and the transmitter slew rate can be observed in Figure 10. RSL ≤ 4kΩ is recommended for high data rate communication. RSL should be less than 200k to ensure that the RS pin can be reliably pulled below V_{IL_RS} to enable the chip.

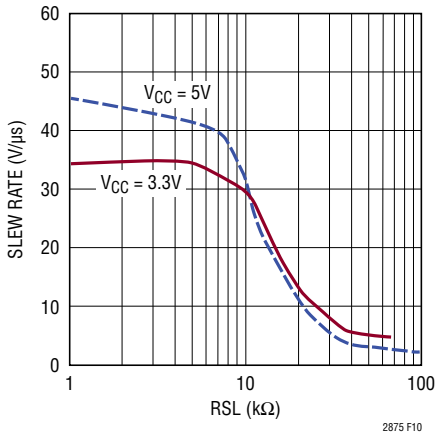


Figure 10. Slew Rate vs Slew Control Resistor RSL

When a voltage between 1.1V and V_{CC} is applied, the RS pin acts as a high impedance receiver. A voltage above V_{IH_RS} puts the chip in shutdown, while a voltage below V_{IL_RS} but above 1.1V activates the chip and sets the transmitter to the minimum slew rate.

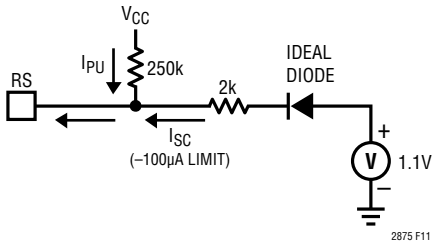


Figure 11. Equivalent Circuit of RS Pin

The slew control circuit on the RS pin is activated at applied voltages below 1.1V. The RS pin can be approximately modeled as a 1.1V voltage source with a series resistance of 2kΩ and a current compliance limit of –100µA, and a 250kΩ pull-up resistor to V_{CC} (Figure 11). Lowering

APPLICATIONS INFORMATION

the voltage on RS increases the slew control current I_{SC} being drawn from the slew control circuit until the voltage reaches ~ 0.9V, where the current drawn from the circuit is ~ –100µA. Below an applied voltage of ~ 0.9V, the slew control circuit sources no additional current, and the current drawn from it remains at ~ –100µA down to 0V.

The total current I_{RS} drawn from the RS pin for input voltage $0.9V \le V_{RS} \le 1.1V$ is the sum of the internal pull-up resistor current I_{RS} and the slew control current I_{SC}.

$$I_{RS(0.9V \le V_{RS} \le 1.1V)} = I_{PU} + I_{SC}$$
$$= \frac{V_{CC} - V_{RS}}{250k} + \frac{1.1V - V_{RS}}{2k}$$

The transmitter slew rate is controlled by the slew control current I_{SC} with increasing current magnitude corresponding to higher slew rates. The slew rate can be controlled using a single slew control resistor RSL in series with the RS pin. When the RS pin is pulled low towards ground by an external driver, RSL limits the amount of current drawn from the RS pin and sets the transmitter slew rate. Alternatively, the slew rate may be controlled by an external voltage or current source.

High Symmetry Driver with Variable Slew Rate

The electromagnetic emissions spectrum of a differential line transmitter is largely determined by the variation in the common mode voltage during switching, as the differential component of the emissions from the two lines cancel, while the common mode emissions of the two lines add. The LTC2875 transmitter has been designed to maintain highly symmetric transitions on the CANH and CANL lines to minimize the perturbation of the common mode voltage during switching (Figure 12), resulting in low EME. The common mode switching symmetry is guaranteed by the V_{SYM} specification.

In addition to full compliance with the ISO 11898-2 standard, LTC2875 meets the more stringent requirements of ISO 11898-5 for bus driver symmetry. This requires that the common mode voltage stay within the limits not only during the static dominant and recessive states, but during the bit transition states as well. Ultra-high speed peak detect circuits are used during manufacturing test to ensure that V_{SYM} limits are not exceeded at any point during the switching cycle.

The high frequency content may be reduced by choosing a lower data rate and a slower slew rate for the signal transitions. The LTC2875 provides an approximate 20 to 1 reduction in slew rate, with a corresponding decrease in the high frequency content. The lowest slew rate is suitable for data communication at 200kbps or below, while the highest slew rate supports 4Mbps. The slew rate limit circuit maintains consistent control of transmitter slew rates across voltage and temperature to ensure predictable performance under all operating conditions. Figure 13 demonstrates the reduction in high frequency content of the common mode voltage achieved by the lowest slew rate compared to the highest slew rate at 200kbps.

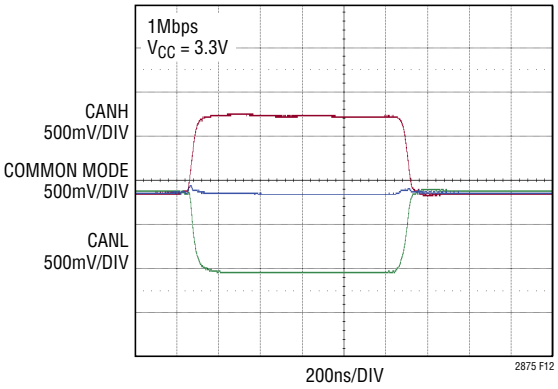


Figure 12. Low Perturbation of Common Mode Voltage During Switching

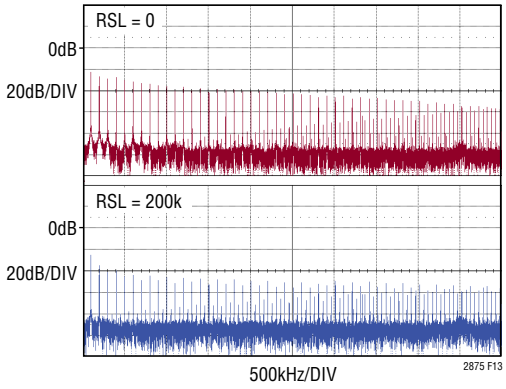


Figure 13. Power Spectrum of Common Mode Voltage Showing High Frequency Reduction of Lowest Slew Rate (RSL=200k) Compared to Highest Slew Rate (RSL=0)

APPLICATIONS INFORMATION

SPLIT Pin Output for Split Termination Support

Split termination is an optional termination technique to reduce common mode voltage perturbations that can produce EME. A split terminator divides the single line-end termination resistor (nominally 120Ω) into two series resistors of half the value of the single termination resistor (Figure 2). The center point of the two resistors is connected to a low impedance voltage source that sets the recessive common mode voltage.

Split termination suppresses common mode voltage perturbations by providing a low impedance load to common mode noise sources such as transmitter noise or coupling to external noise sources. In the case of single resistor termination, the only load on a common mode noise source is the parallel impedance of the input resistors of the CAN transceivers on the bus. This results in a common mode impedance of several kilohms for a small network. The split termination, on the other hand, provides a common mode load equal to the parallel resistance of the two split termination resistors, or ¼ the resistance of the single termination resistor (30Ω). This low common mode impedance results in a reduction of the common mode noise voltage compared to the much higher common mode impedance of the single resistor termination.

The SPLIT pin on the LTC2875 provides a buffered voltage to bias the mid-point of the split termination resistors. The voltage on the SPLIT pin matches the common mode voltage established by the transmitter in the dominant state and the receiver input resistor bias during the recessive state: V_{CC}/2 when V_{CC} = 5V and V_{CC}/2+0.3V when V_{CC} = 3.3V. Decouple SPLIT with a 4.7nF capacitor to ground to lower the AC impedance to better suppress fast transients. SPLIT is a high voltage fault tolerant output that tolerates the same ±60V overvoltage faults and ±25kV ESD discharges as CANH and CANL.

One disadvantage of the SPLIT termination is higher power supply current if the two terminating transceivers differ in their common mode voltage due to differences in V_{CC} or GND potential or to chip to chip variations in the internal reference voltages. This will result in the transceiver with the higher common mode voltage sourcing current into the bus lines through its SPLIT pin, while the transceiver with the lower common mode voltage will sink current through its SPLIT pin.

Ideal Passive Behavior to CAN Bus With Supply Off

When the power supply is removed or the chip is in shutdown, the CANH and CANL pins are in a high impedance state. The receiver inputs are isolated from the CANH and CANL nodes by FET switches which opens in the absence of power, thereby preventing the resistor dividers on the receiver input from loading the bus. The high impedance state of the receiver is maintained over a range determined by the ESD protection of the receiver input, typically –0.3V to 10V. For bus voltages outside this range, the current flowing into the receiver is governed by the conduction voltages of the ESD device and the 40k nominal receiver input resistance.

Micropower Shutdown Mode

The low power shutdown mode is entered by raising the voltage on the RS pin above its V_{IH_RS} threshold. This turns off all circuits that draw DC bias currents and disables all chip functionality. Any remaining supply current in shutdown is due to semiconductor device leakage currents. All the outputs —CANH, CANL, SPLIT, and RXD— are in the high impedance state, with RXD pulled up to V_{CC} through a 500kΩ resistor to ensure it remains in the recessive state.

The chip is enabled by bringing the RS pin below its V_{IL_RS} threshold. The RXD output goes active after the time delay t_{ENRX} (40µs max) and the SPLIT pin goes active at approximately the same time. CANH and CANL switch to the dominant state at the first high-to-low transition of TXD after the t_{ENTX} delay.

Auxiliary Protection for IEC Surge, EFT and ESD

A transceiver used in an industrial setting may be exposed to extremely high levels of electrical overstress due to phenomena such as lightning surge, electrical fast transient (EFT) from switching high current inductive loads, and electrostatic discharge (ESD) from the discharge of electrically charged personnel or equipment. Test methods to evaluate immunity of electronic equipment to these phenomena are defined in the IEC standards 61000-4-2,

APPLICATIONS INFORMATION

61000-4-4, and 61000-4-5, which address ESD, EFT, and surge, respectively. The transients produced by the EFT and particularly the surge tests contain much more energy than ESD transients. The LTC2875 is designed for high robustness against ESD, but the on-chip protection is not able to absorb the energy associated with the 61000-4-5 surge transients. Therefore, a properly designed external protection network is necessary to achieve a high level of surge protection, and can also extend the ESD and EFT performance of the LTC2875 to extremely high levels.

In addition to providing surge, EFT and ESD protection, an external network should preserve the ability of the LTC2875 to operate over a wide common mode and communicate at high frequencies. In order to meet the first requirement, protection components with suitably high conduction voltages must be chosen. A means to limit current must be provided to prevent damage in case a secondary protection device or the ESD cell on the LTC2875 fires and conducts. The capacitance of these components must be kept low in order to permit high frequency communication over a network with multiple nodes.

The protection network shown in Figure 14 in the Typical Application section provides the following protection:

IEC 61000-4-2 Edition 2.0 2008-12 ESD Level 4: ±30kV air, ±15kV contact (line to GND, direct discharge to bus pins with transceiver and protection circuit mounted on a ground referenced test card per Figure 4 of the standard)

IEC 61000-4-4 Second Edition 2004-07 EFT Level 4: ±5kV (line to GND,100kHz repetition rate, 0.75ms burst duration, 60 second test duration, discharge coupled to bus pins through 100pF capacitor per paragraph 7.3.2 of the standard)

IEC 61000-4-5 Second Edition 2005-11 Surge Level 4: ±5kV (line to GND, line to line, 8/20µs waveform, each line coupled to generator through 80Ω resistor per Figure 14 of the standard)

This protection circuit adds only ~36pF of capacitance per line (line to GND), thereby providing an extremely high level of protection without significant impact to the performance of the LTC2875 at high data rates.

The gas discharge tubes (GDTs) provide the primary protection against electrical surges. These devices provide a very low impedance and high current carrying capability when they fire, safely discharging the surge current to GND. The transient blocking units (TBUs) are solid state devices that switch from a low impedance pass through state to a high impedance current limiting state when a specified current level is reached. These devices limit the current and power that can pass through to the secondary protection. The secondary protection consists of a bidirectional TVS diode, which avalanches above 36V to protect the bus pins of the LTC2875 transceiver. The high avalanche voltage of the secondary protection maintains a wide common mode range. The final component of the network is the metal oxide varistors (MOVs) which are used to clamp the voltage across the TBUs to protect them against fast ESD and EFT transients which exceed the turn-on time of the GDT.

The high performance of this network is attributable to the low capacitance of the GDT primary protection devices. The high capacitance MOV floats on the line and is shunted by the TBU, so it contributes no appreciable capacitive load on the signal.

Logic I/O Interface Voltages and Power Supply Sequencing

Logic inputs RS and TXD are protected by ground referenced ESD devices. These inputs do not draw a high current if driven by voltages exceeding V_{CC} as long as the absolute maximum ratings for these pins are not exceeded. The V_{CC} supply for the LTC2875 may be safely brought up before or after the supplies powering the logic driving the RXD and TXD inputs with no adverse consequences.

APPLICATIONS INFORMATION

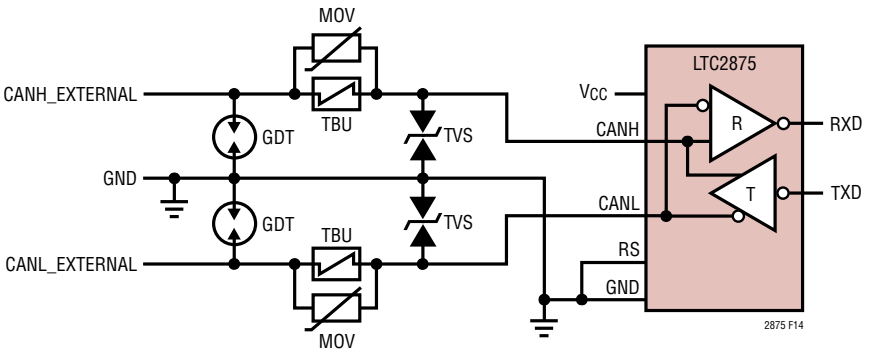
DeviceNet Compatibility

DeviceNet is a network standard based on the CAN bus. The DeviceNet standard places requirements on the transceiver that exceed those of the ISO 11898-2 standard. The LTC2875 meets the following DeviceNet requirements:

PARAMETER	DeviceNet REQUIREMENT	ISO 11898-2 REQUIREMENT	LTC2875
Number of Nodes	64	N/A	166
Minimum Differential Input Resistance	20kΩ	10kΩ	50kΩ
Differential Input Capacitance	25pF (Max)	10pF (Nom)	8.4pF (Typ)
Bus Pin Voltage Range (Survivable)	–25V to 18V	–3V to 16V (for 12V Battery)	–60V to 60V
Bus Pin Voltage Range (Operation)	–5V to 10V	–2V to 7V	–36V to 36V (V_{CC} = 5V)
Connector Mis-Wiring Tests, All Pin-Pin Combinations	±18V	N/A	±60V (See Below)
Transmitter Propagation Delay	120ns (Max)	N/A	120ns (V_{CC} = 5V)
Receiver Propagation Delay	130ns (Max)	N/A	65ns (V_{CC} = 5V)

DeviceNet employs a 5-pin connector with conductors for Power+, Power–, CANH, CANL, and Drain. The power is 24V DC, and the Drain wire is connected to the cable shield for shielded cables. DeviceNet devices that are powered from the 24V DC line voltage contain a step-down regulator to power the CAN transceiver and associated circuitry, and blocking diodes to prevent damage in case of power polarity reversal.

The DeviceNet mis-wiring tests involve connecting an 18V supply to each of the 20 possible pin pair/polarity combinations on the 5-pin connector. The ±60V tolerance of the LTC2875 with V_{CC} and/or GND open or grounded ensure that the LTC2875 will pass all the mis-wiring tests without damage as long as its V_{CC} pin is protected from overvoltage and reverse polarity by other circuitry in the DeviceNet device.

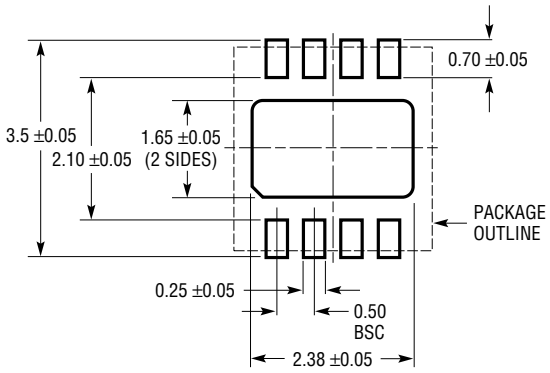


GDT: BOURNS 2031-15T-SM; 150V GAS DISCHARGE TUBE
TBU: BOURNS TBU-CA050-300-WH; 500V TRANSIENT BLOCKING UNIT
MOV: BOURNS MOV-7D201K; 200V 13J METAL OXIDE VARISTOR
TVS: BOURNS CDSOD323-T36SC; 36V BIDIRECTIONAL TVS DIODE

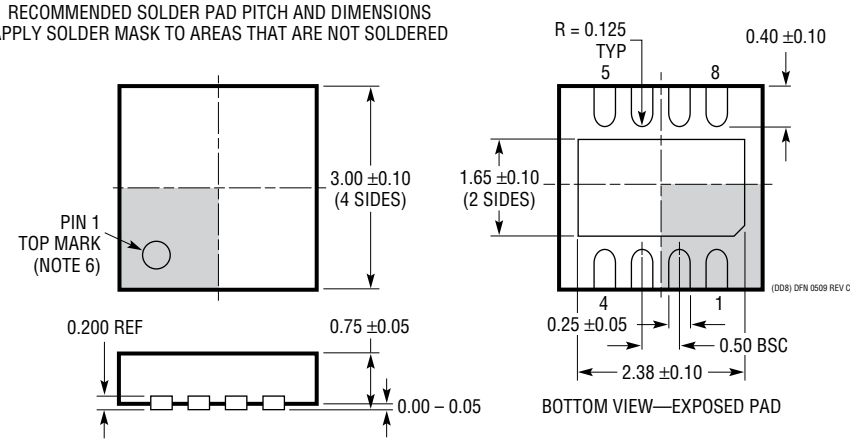
Figure 14. Network for IEC Level 4 Protection Against Surge, EFT and ESD

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

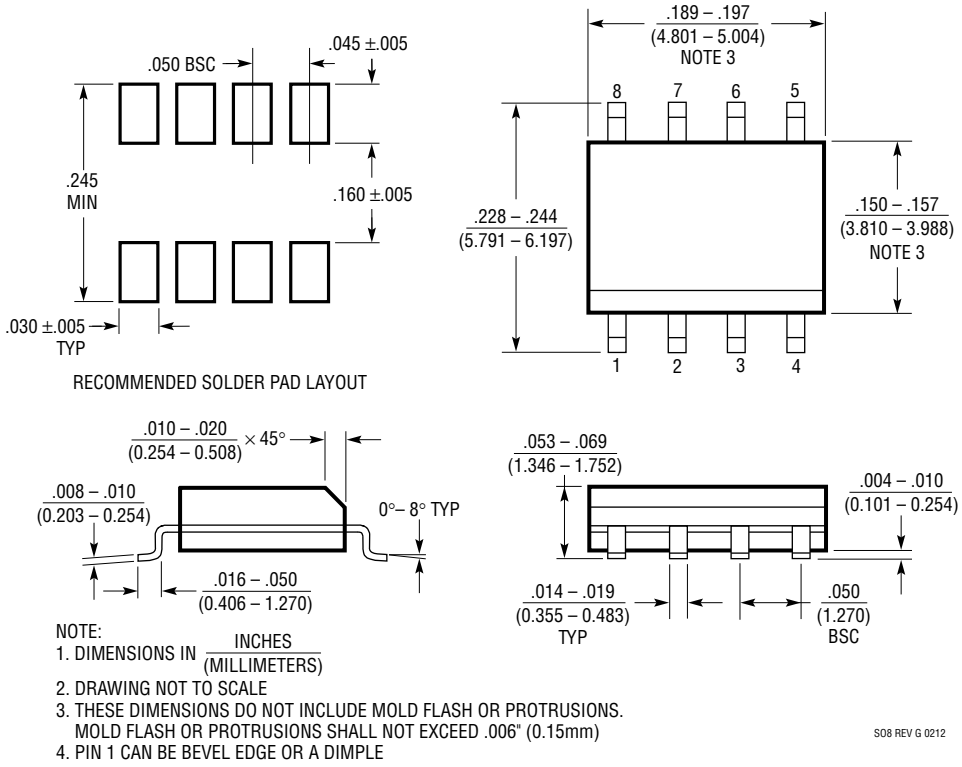


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/19	Added CAN FD claims to title, features, and description	1
		Added t_{BIT} specifications to Switching Characteristics table	5
		Inserted new Figure 7: Loop Delay Symmetry	7
		Corrected lowest data rate in “Transmit Dominant Timeout Function”	13