Voltage Supervisor with 27 Selectable Thresholds and Watchdog Timer

FEATURES

- **9 Selectable Supply Voltages**
  12V, 5V, 3.3V, 2.5V, 1.8V
  1.5V, 1.2V, 1V, +ADJ (0.5V)
- **3 Selectable Tolerances**
  –5%, –10%, –15% (LTC2917)
- **Manual Reset Input (LTC2918)**
- **1.5V to 5.5V Supply Operation**
- **Adjustable Watchdog Timeout**
- **Windowed Watchdog Timeout for Higher Reliability Applications (LTC2917-B, LTC2918-B)**
- **6.2V Shunt Regulator for High Voltage Operation**
- **Guaranteed Operation to 125°C**
- Guaranteed Threshold Accuracy: ±1.5%
- Low Quiescent Current: 30µA Typical
- Power Supply Glitch Immunity
- Guaranteed $\overline{RST}$ for $V_{CC} \geq 0.8V$
- 10-Lead MSOP Packages and (3mm × 2mm) DFN Packages

APPLICATIONS

- Handheld Devices
- Cell Phone Base Stations
- Automotive Control Systems
- Network Servers
- Optical Networking Systems

DESCRIPTION

The LTC®2917-A/LTC2917-B and LTC2918-A/LTC2918-B are low voltage single-supply monitors with selectable thresholds and an adjustable watchdog timer. The parts operate from 1.5V to 5.5V and consume a quiescent current of only 30µA.

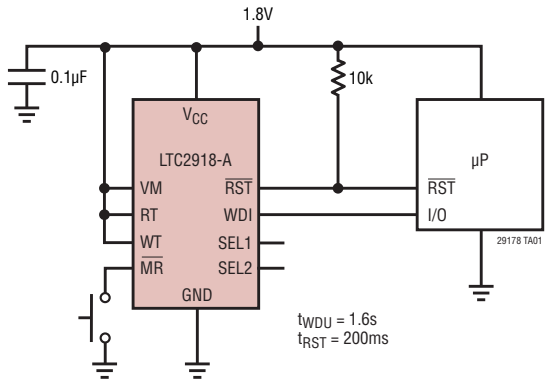
Two three state inputs select one of nine internally programmed thresholds without the need for external resistors. For the LTC2917, an additional three state input determines the tolerance (–5%, –10%, –15%). The tolerance for the LTC2918 is fixed at –5%. Threshold accuracy is guaranteed at ±1.5% over the entire operating temperature range. Glitch filtering ensures reliable reset operation without false triggering.

The reset timeout and the watchdog timeout may be set with no external components, or adjusted using an external capacitor. A windowed watchdog feature is available for high-reliability applications (B1 versions). A separate manual reset input on the LTC2918-A/LTC2918-B allows a simple push button interface.

Operation to 125°C makes the LTC2917-A/LTC2917-B and LTC2918-A/LTC2918-B suitable for automotive applications.

TYPICAL APPLICATION

1.8V Supply Monitor with Manual Reset and Internal Timers Selected



Monitor Selection Table

NOMINAL VOLTAGE	SEL1	SEL2
12V	V_{CC}	V_{CC}
5V	V_{CC}	Open
3.3V	V_{CC}	GND
2.5V	Open	V_{CC}
1.8V	Open	Open
1.5V	Open	GND
1.2V	GND	V_{CC}
1V	GND	Open
ADJ (0.5V)	GND	GND

ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Terminal Voltages
- V_{CC} (Note 3) ..... –0.3V to 5.7V
- SEL1, SEL2, TOL, WDI, $\overline{MR}$, $\overline{RST}$ ..... –0.3V to 7.5V
- VM ..... –0.3V to 15V
- RT, WT ..... –0.3V to (V_{CC} + 0.3)V

Terminal Currents
- V_{CC} (Note 3) ..... ±5mA

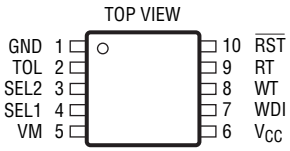
Operating Temperature Range
- LTC2917C/LTC2918C ..... 0°C to 70°C
- LTC2917I/LTC2918I ..... –40°C to 85°C
- LTC2917H/LTC2918H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- MSOP ..... 300°C

PIN CONFIGURATION

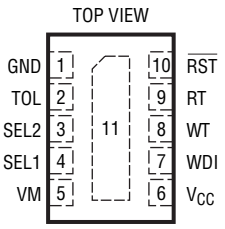
LTC2917



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W
LTC2917

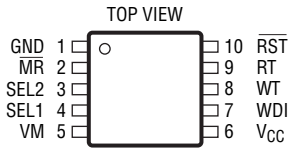
LTC2917



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB GND
CONNECTION OPTIONAL
LTC2917

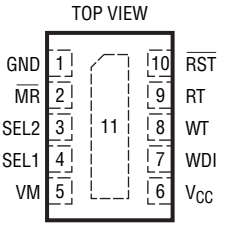
LTC2918



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W
LTC2918

LTC2918



DDB PACKAGE
10-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) PCB GND
CONNECTION OPTIONAL
LTC2918

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2917CMS-B1#PBF	LTC2917CMS-B1#TRPBF	LTCQP	10-Lead Plastic MSOP	0°C to 70°C
LTC2917IMS-B1#PBF	LTC2917IMS-B1#TRPBF	LTCQP	10-Lead Plastic MSOP	–40°C to 85°C
LTC2917HMS-B1#PBF	LTC2917HMS-B1#TRPBF	LTCQP	10-Lead Plastic MSOP	–40°C to 125°C
LTC2917CMS-A1#PBF	LTC2917CMS-A1#TRPBF	LTDGD	10-Lead Plastic MSOP	0°C to 70°C
LTC2917IMS-A1#PBF	LTC2917IMS-A1#TRPBF	LTDGD	10-Lead Plastic MSOP	–40°C to 85°C
LTC2917HMS-A1#PBF	LTC2917HMS-A1#TRPBF	LTDGD	10-Lead Plastic MSOP	–40°C to 125°C
LTC2918CMS-B1#PBF	LTC2918CMS-B1#TRPBF	LTDCT	10-Lead Plastic MSOP	0°C to 70°C
LTC2918IMS-B1#PBF	LTC2918IMS-B1#TRPBF	LTDCT	10-Lead Plastic MSOP	–40°C to 85°C
LTC2918HMS-B1#PBF	LTC2918HMS-B1#TRPBF	LTDCT	10-Lead Plastic MSOP	–40°C to 125°C
LTC2918CMS-A1#PBF	LTC2918CMS-A1#TRPBF	LTDGG	10-Lead Plastic MSOP	0°C to 70°C
LTC2918IMS-A1#PBF	LTC2918IMS-A1#TRPBF	LTDGG	10-Lead Plastic MSOP	–40°C to 85°C
LTC2918HMS-A1#PBF	LTC2918HMS-A1#TRPBF	LTDGG	10-Lead Plastic MSOP	–40°C to 125°C
TAPE AND REEL (MINI)	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2917CDDB-B1#TRMPBF	LTC2917CDDB-B1#TRPBF	LCQR	10-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2917IDDB-B1#TRMPBF	LTC2917IDDB-B1#TRPBF	LCQR	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2917HDDB-B1#TRMPBF	LTC2917HDDB-B1#TRPBF	LCQR	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC2917CDDB-A1#TRMPBF	LTC2917CDDB-A1#TRPBF	LDGF	10-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2917IDDB-A1#TRMPBF	LTC2917IDDB-A1#TRPBF	LDGF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2917HDDB-A1#TRMPBF	LTC2917HDDB-A1#TRPBF	LDGF	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC2918CDDB-B1#TRMPBF	LTC2918CDDB-B1#TRPBF	LDCV	10-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2918IDDB-B1#TRMPBF	LTC2918IDDB-B1#TRPBF	LDCV	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2918HDDB-B1#TRMPBF	LTC2918HDDB-B1#TRPBF	LDCV	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC2918CDDB-A1#TRMPBF	LTC2918CDDB-A1#TRPBF	LDGH	10-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2918IDDB-A1#TRMPBF	LTC2918IDDB-A1#TRPBF	LDGH	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2918HDDB-A1#TRMPBF	LTC2918HDDB-A1#TRPBF	LDGH	10-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(MIN)}$	Minimum Supply Voltage	$\overline{RST}$ in Correct Logic State	●	0.8			V
$V_{CC(UVLO)}$	Supply Undervoltage Lockout		●			1.5	V
$V_{CC(SHUNT)}$	Shunt Regulation Voltage	I_{VCC} = 0.5mA	●	5.7	6.2	7.0	V
I_{CC}	V_{CC} Pin Current	SEL1, SEL2, TOL, $\overline{MR}$ = Open SEL1, SEL2, TOL = GND (LTC2917) $\overline{MR}$ = V_{CC} (LTC2918)	● ●		30 45	50 80	µA µA
Monitor Input (VM)							
V_{MT120}	12V, 5% Reset Threshold 12V, 10% Reset Threshold 12V, 15% Reset Threshold		● ● ●	11.04 10.44 9.84	11.22 10.62 10.02	11.40 10.80 10.20	V V V
V_{MT50}	5V, 5% Reset Threshold 5V, 10% Reset Threshold 5V, 15% Reset Threshold		● ● ●	4.600 4.350 4.100	4.675 4.425 4.175	4.750 4.500 4.250	V V V
V_{MT33}	3.3V, 5% Reset Threshold 3.3V, 10% Reset Threshold 3.3V, 15% Reset Threshold		● ● ●	3.036 2.871 2.706	3.086 2.921 2.756	3.135 2.970 2.805	V V V
V_{MT25}	2.5V, 5% Reset Threshold 2.5V, 10% Reset Threshold 2.5V, 15% Reset Threshold		● ● ●	2.300 2.175 2.050	2.338 2.213 2.088	2.375 2.250 2.125	V V V
V_{MT18}	1.8V, 5% Reset Threshold 1.8V, 10% Reset Threshold 1.8V, 15% Reset Threshold		● ● ●	1.656 1.566 1.476	1.683 1.593 1.503	1.710 1.620 1.530	V V V
V_{MT15}	1.5V, 5% Reset Threshold 1.5V, 10% Reset Threshold 1.5V, 15% Reset Threshold		● ● ●	1.380 1.305 1.230	1.403 1.328 1.253	1.425 1.350 1.275	V V V
V_{MT12}	1.2V, 5% Reset Threshold 1.2V, 10% Reset Threshold 1.2V, 15% Reset Threshold		● ● ●	1.104 1.044 0.984	1.122 1.062 1.002	1.140 1.080 1.020	V V V
V_{MT10}	1V, 5% Reset Threshold 1V, 10% Reset Threshold 1V, 15% Reset Threshold		● ● ●	0.920 0.870 0.820	0.935 0.885 0.835	0.950 0.900 0.850	V V V
V_{MTADJ}	ADJ (0.5V), 5% Reset Threshold ADJ (0.5V), 10% Reset Threshold ADJ (0.5V), 15% Reset Threshold		● ● ●	460.0 435.0 410.0	467.5 442.5 417.5	475.0 450.0 425.0	mV mV mV
R_{VM}	VM Input Impedance (Note 4)	Fixed Threshold Modes	●	0.5		8	MΩ
$I_{VM(ADJ)}$	ADJ Input Current	VM = 0.5V	●			±15	nA
Three-State Inputs (SEL1, SEL2), (TOL, LTC2917)							
$V_{TPIN,LOW}$	Low Level Input Voltage		●			0.5	V
$V_{TPIN,HIGH}$	High Level Input Voltage		●	1.4			V
$V_{TPIN,Z}$	Pin Voltage when Open	I = 0µA			0.9		V
$I_{TPIN,Z}$	Allowable Leakage in Open State		●			±5	µA
$I_{TPIN,H/L}$	Pin Input Current	V_{TPIN} = 0V, V_{CC}	●			±20	µA
Reset Timer Control (RT)							
$I_{RT(UP)}$	RT Pull-Up Current	V_{RT} = 0.25V	●	–2	–3	–4	µA
$I_{RT(DOWN)}$	RT Pull-Down Current	V_{RT} = 1.1V	●	2	3	4	µA
$I_{RT(INT)}$	Internal RT V_{CC} Detect Current	V_{RT} = V_{CC}	●		1	8	µA
$V_{RT(INT, LH)}$	RT Internal Timer Threshold	V_{RT} Rising, Referenced to V_{CC}	●	–100	–160	–300	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Output ($\overline{RST}$)							
$t_{RST(INT)}$	Internal Reset Timeout Period	$V_{RT} = V_{CC}$	●	150	200	260	ms
$t_{RST(EXT)}$	Adjustable Reset Timeout Period	C_{RT} = 2.2nF	●	16	20	25	ms
t_{UV}	VM Undervoltage Detect to $\overline{RST}$ Asserted	VM Less Than Reset Threshold V_{MTX} by More Than 5%	●	10	80	150	µs
V_{OL}	Output Voltage Low $\overline{RST}$	V_{CC} = 3.3V, I_{RST} = 2.5mA V_{CC} = 1V, I_{RST} = 100µA V_{CC} = 0.8V, I_{RST} = 15µA	● ● ●		0.15 0.15 0.05	0.4 0.3 0.2	V V V
$I_{OH(RST)}$	$\overline{RST}$ Output Voltage High Leakage	$\overline{RST} = V_{CC}$	●			±1	µA
Watchdog Timer Control (WT)							
$I_{WT(UP)}$	WT Pull-Up Current	V_{WT} = 0.25V	●	–2	–3	–4	µA
$I_{WT(DOWN)}$	WT Pull-Down Current	V_{WT} = 1.1V	●	2	3	4	µA
$V_{WT(INT, LH)}$	WT Internal Timer Threshold	V_{WT} Rising, Referenced to V_{CC}	●	–100	–160	–300	mV
$I_{WT(INT)}$	Internal WT V_{CC} Detect Current	$V_{WT} = V_{CC}$	●		1	8	µA
$I_{WT(DIS)}$	Watchdog Disable Hold Current	V_{WT} = 0V			–3.5		µA
Watchdog Input (WDI)							
$t_{WDU(INT)}$	Internal Watchdog Upper Boundary	$V_{WT} = V_{CC}$	●	1.3	1.6	2	s
$t_{WDL(INT)}$	Internal Watchdog Lower Boundary (Note 5)	B Versions, $V_{WT} = V_{CC}$	●	37.5	50	62.5	ms
$t_{WDU(EXT)}$	External Watchdog Upper Boundary	C_{WT} = 2.2nF	●	130	160	200	ms
$t_{WDL(EXT)}$	External Watchdog Lower Boundary (Note 5)	B Versions, C_{WT} = 2.2nF	●		$t_{WDU(EXT)}/32$		ms
$V_{IL(WDI)}$	Input Low Voltage		●			0.4	V
$V_{IH(WDI)}$	Input High Voltage		●	1.1			V
$t_{PW(WDI)}$	Input Pulsewidth		●	400			ns
	WDI Leakage Current		●			±1	µA
Manual Reset Input (LTC2918)							
$V_{IL(MR)}$	Input Low Voltage		●			0.2 • V_{CC}	V
$V_{IH(MR)}$	Input High Voltage		●	0.8 • V_{CC}			V
R_{PU}	Pull-Up Resistance		●	50	100	150	kΩ
$t_{PW(MR)}$	Pulsewidth		●	250			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

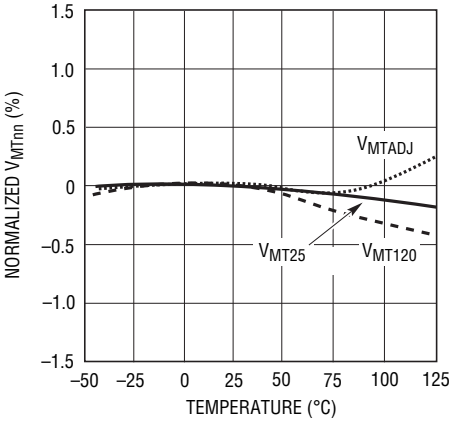
Note 3: V_{CC} maximum pin voltage is limited by input current. Since the V_{CC} pin has an internal 6.2V shunt regulator, a low impedance supply which exceeds 5.7V may exceed the rated terminal current. Operation from higher voltage supplies requires a series dropping resistor. See Applications Information.

Note 4: Input impedance is dependent on the configuration of the SEL pins.

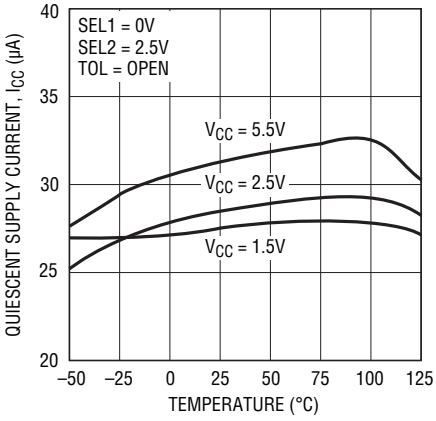
Note 5: In the LTC2917-B/LTC2918-B, edges must occur on WDI with a period between the lower and upper boundary or $\overline{RST}$ is invoked. For the LTC2917-A/LTC2918-A, the edges must simply occur before the upper boundary. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS

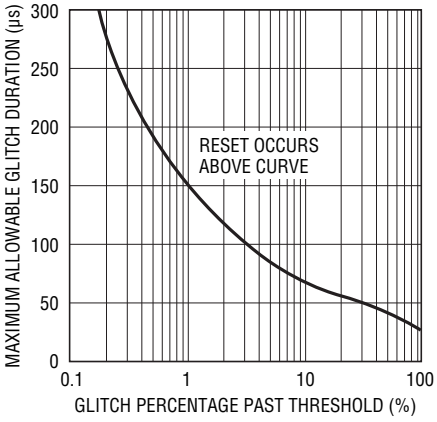
Threshold Voltage vs Temperature



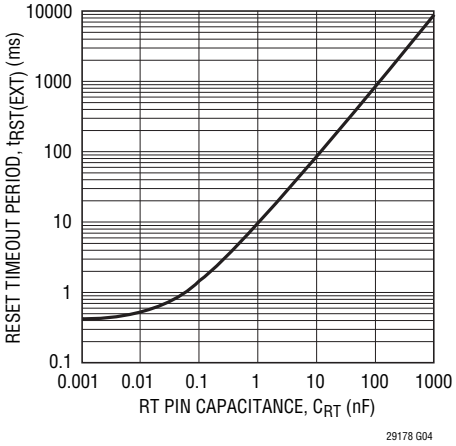
Quiescent Supply Current vs Temperature



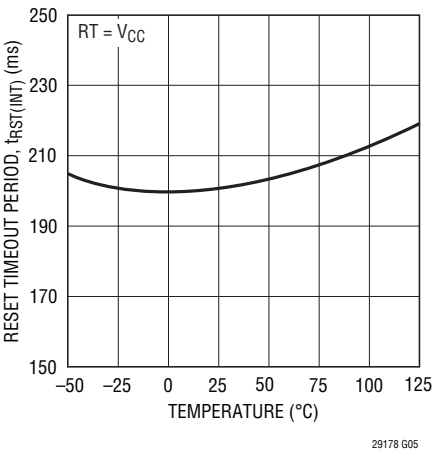
Allowable Glitch Duration vs Magnitude



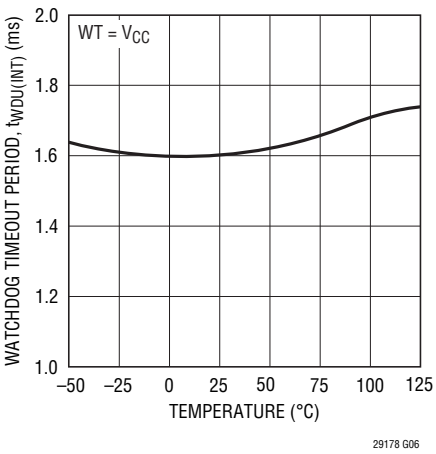
Reset Timeout Period vs RT Capacitance



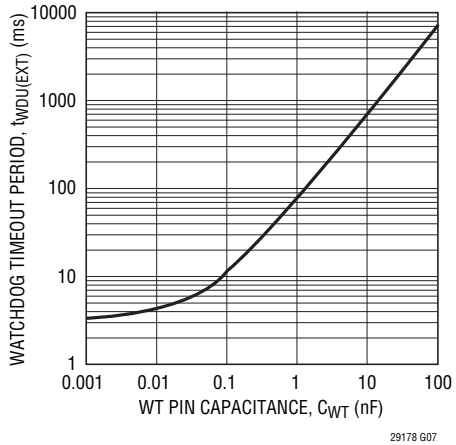
Internal Reset Timeout Period vs Temperature



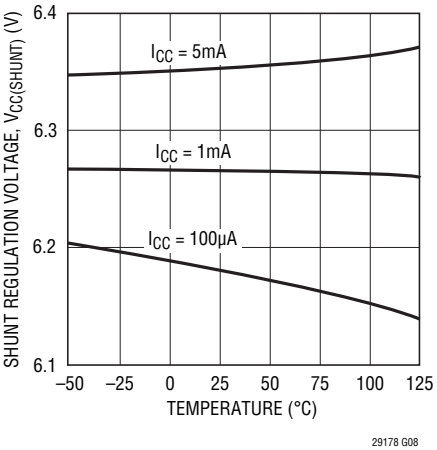
Internal Watchdog Timeout Period vs Temperature



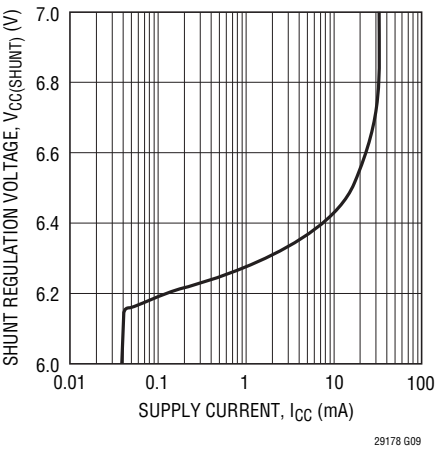
Watchdog Timeout Period vs Capacitance



Shunt Regulation Voltage vs Temperature

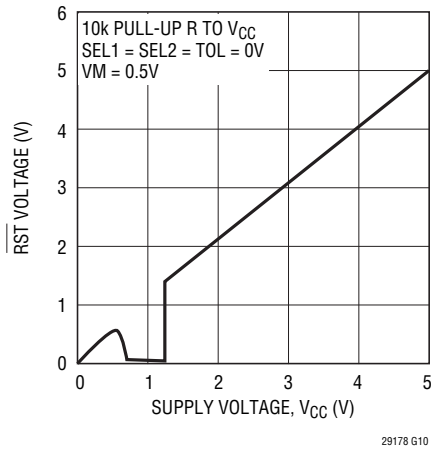


Shunt Regulation Voltage vs Supply Current

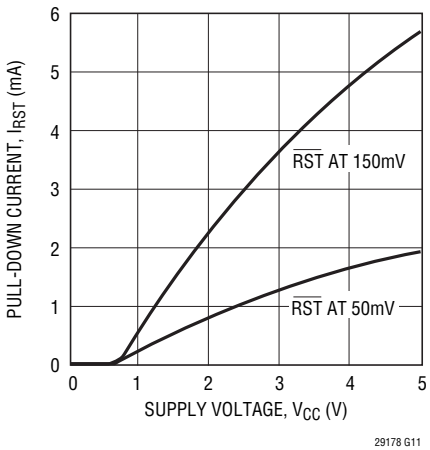


TYPICAL PERFORMANCE CHARACTERISTICS

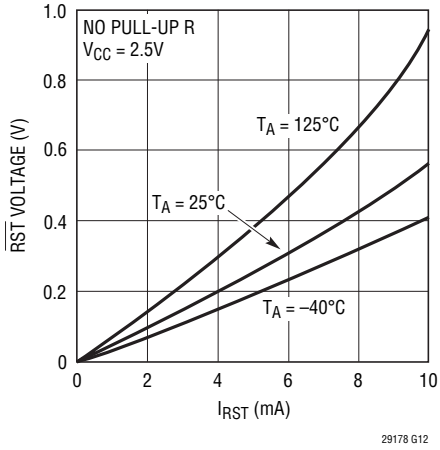
$\overline{RST}$ Output Voltage vs V_{CC}



$\overline{RST}$ Pull-Down Current vs V_{CC}



$\overline{RST}$ V_{OL} vs I_{RST}



PIN FUNCTIONS

GND: Device Ground.

$\overline{MR}$ (LTC2918 only): Manual Reset Input (Active Low). A low level on the $\overline{MR}$ input causes the part to issue a reset, which is released one reset timeout after the input goes high. The pin has an internal 100k pull-up to V_{CC}, and thus may interface directly to a momentary pushbutton. Leave open if unused.

$\overline{RST}$: Open Drain $\overline{RST}$ Output. Asserts low when VM is below the threshold selected by SEL1, SEL2 and TOL input pins. Held low for an adjustable timeout after VM input is above threshold.

RT: Reset Timeout Control Pin. Attach an external capacitor (C_{RT}) to GND to set a reset timeout of 9ms/nF. Leave RT open to generate a reset timeout of approximately 400µs. Tie RT to V_{CC} to generate a reset timeout of approximately 200ms.

SEL1, SEL2: Monitor Voltage Select Three-State Input. SEL1, and SEL2 control the nominal threshold voltage that VM is set to monitor. Connect to V_{CC}, GND or leave unconnected in open state. (See Table 1).

TOL (LTC2917 only): Three-State Input for Supply Tolerance Selection (–5%, –10% or –15%). Controls the tolerance band at which the VM supply is monitored. Connect to V_{CC}, GND, or leave unconnected in open state. (See Table 2)

V_{CC}: Power Supply input. Bypass this pin to ground with a 0.1µF ceramic capacitor. A minimum of 1.5V on V_{CC} ensures that the part is out of under voltage lockout and that the voltage thresholds are accurate. Operates as a direct supply input for voltages up to 5.5V. Operates as a shunt regulator for supply voltages greater than 5.7V and should have a resistor between this pin and the supply to limit V_{CC} input current to no greater than 5mA. When used without a current-limiting resistor, pin voltage must not exceed 5.7V.

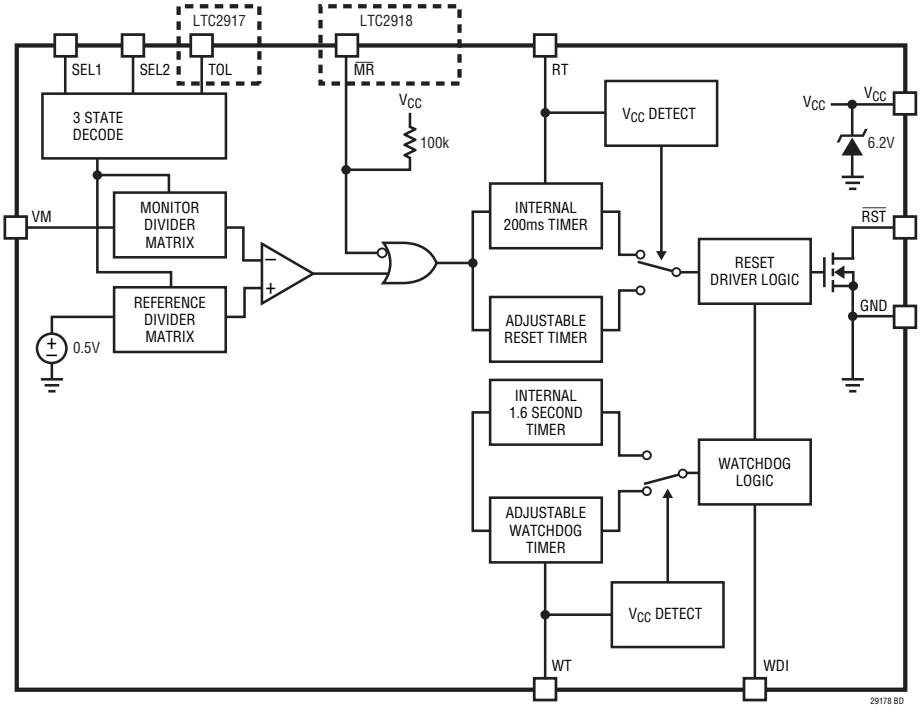
VM: Voltage Monitor Input to $\overline{RST}$ comparator. SEL1, SEL2 and TOL inputs select the exact threshold that asserts the $\overline{RST}$ output.

WDI: Watchdog Input. This pin must be driven to change state within a time less than the watchdog upper boundary time, or $\overline{RST}$ will be asserted low. On the LTC2917-B, LTC2918-B, the period must also be greater than the watchdog lower boundary time, and only falling edges are considered. Tie WT and WDI to GND to disable the watchdog timer.

WT: Watchdog Timer Control Pin. Attach an external capacitor (C_{WT}) to GND to set a watchdog upper boundary timeout time of 72ms/nF. Tie WT to V_{CC} to generate a timeout of approximately 1.6s. Leave WT open to generate a timeout of approximately 3.2ms. Tie WT and WDI to GND to disable the watchdog timer.

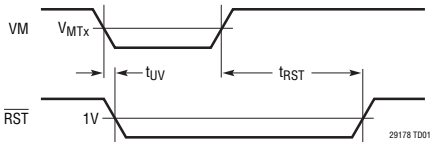
Exposed Pad (DFN Only): Exposed Pad may be left open or connected to device ground.

BLOCK DIAGRAM

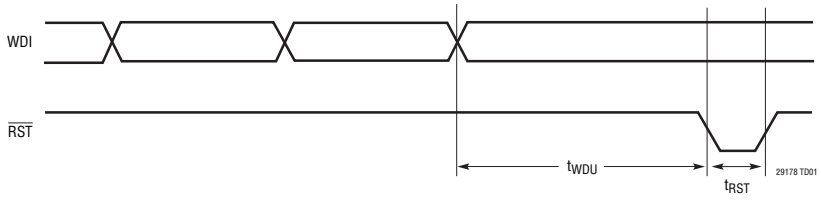


TIMING DIAGRAMS

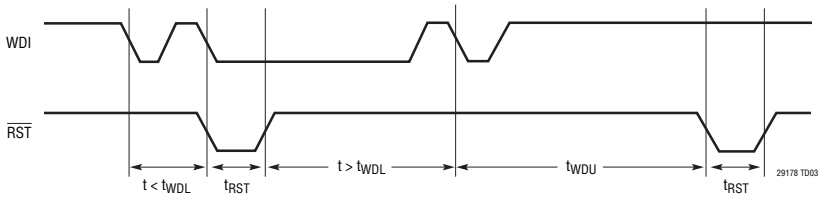
Monitor Input Timing



Watchdog Timing (LTC2917-A, LTC2918-A)



Watchdog Timing (LTC2917-B, LTC2918-B)



APPLICATIONS INFORMATION

Supply Monitoring

The LTC2917/LTC2918 are low voltage single supply monitors with selectable thresholds. Two three-state inputs select one of nine internally programmed thresholds. For the LTC2917, a third three-state input selects the tolerance at which the supply connected to the VM pin is monitored (–5%, –10%, –15%). The tolerance for the LTC2918 is fixed at –5%. Threshold accuracy is guaranteed at ±1.5% over the entire operating temperature range.

The LTC2917/LTC2918 asserts the $\overline{RST}$ output low when VM is below the programmed threshold, and for a reset timeout period (t_{RST}) after VM goes above the threshold. The reset timeout can be configured to use one of two internal timers with no external components, or an adjusted timer programmed by placing an external capacitor from RT to ground. Glitch filtering ensures reliable reset operation without false triggering.

Power-Up

V_{CC} powers the drive circuits for the $\overline{RST}$ pin. Therefore, as soon as V_{CC} reaches 0.8V during power up, the $\overline{RST}$ output asserts low.

Until V_{CC} reaches the undervoltage lockout threshold (guaranteed less than 1.5V), $\overline{RST}$ is held low regardless of the state of VM.

Once V_{CC} is above the undervoltage lockout threshold and VM is above the programmed threshold, the reset timer is started. After the reset timeout, the open drain pull-down releases $\overline{RST}$ and the external pull-up resistor pulls high.

Power-Down

On power-down, once VM drops below its threshold or V_{CC} drops below the undervoltage lockout, $\overline{RST}$ asserts logic low.

Monitor Threshold Control

The monitor threshold on the VM pin is controlled by the SEL1, SEL2 and TOL three-state pins. The SEL1 and SEL2 pins select one of nine preset nominal voltages (including one externally adjustable threshold) as shown in Table 1.

The SEL1 and SEL2 three-state input pins should be connected to GND, V_{CC} or left unconnected during normal operation. Note that when left unconnected, the maximum leakage allowable from the pin to either GND or V_{CC} is ±5µA.

The tolerance at which the monitored supply is measured is set by the TOL pin (LTC2917 only) as shown in Table 2. If desired (e.g. for margining purposes), the TOL pin may be driven by a three-state buffer. That three-state buffer must have a V_{OL} and V_{OH} which meet the V_{IL} and V_{IH} of the TOL pin specified in the Electrical Characteristics, and maintain less than 5µA of leakage in the open state.

Table 1. Voltage Threshold Settings

NOMINAL VOLTAGE	SEL1	SEL2
12V	V_{CC}	V_{CC}
5V	V_{CC}	Open
3.3V	V_{CC}	GND
2.5V	Open	V_{CC}
1.8V	Open	Open
*1.5V	Open	GND
*1.2V	GND	V_{CC}
*1V	GND	Open
*ADJ (0.5V)	GND	GND

*Require a separate supply for V_{CC}

Table 2. System Voltage Tolerance Settings

TOLERANCE	TOL
–5%	V_{CC}
–10%	Open
–15%	GND

APPLICATIONS INFORMATION

Threshold Accuracy

The trip threshold for the supplies monitored is selected by configuring the three-state input pins. When using the adjustable input, a external resistive divider sets the trip threshold, allowing the user complete control over the trip point. Selection of this trip voltage is crucial to the reliability of the system.

Any power supply has some tolerance band within which it is expected to operate (e.g. 5V±10%). It is generally undesirable that a supervisor issue a reset when the power supply is inside this tolerance band. Such a "nuisance" reset reduces reliability by preventing the system from functioning under normal conditions.

To prevent nuisance resets, the supervisor threshold must be guaranteed to lie outside the power supply tolerance band. To ensure that the threshold lies outside the power supply tolerance range, the nominal threshold must lie outside that range by the monitor's accuracy specification.

All 27 of the selectable thresholds have the same relative threshold accuracy of ±1.5% of the programmed nominal input voltage (over the full operating temperature range). Consider the example of monitoring a 5V supply with a 10% tolerance. The nominal threshold internal to the LTC2917 is 11.5% below the 5V input at 4.425V. With ±1.5% accuracy, the trip threshold range is 4.425V±75mV over temperature (i.e. 10% to 13% below 5V). The monitored system must thus operate reliably down to 4.35V or 13% below 5V over temperature.

Glitch Immunity

The above discussion is concerned only with the DC value of the monitored supply. Real supplies also have relatively high-frequency variation, from sources such as load transients, noise, and pickup. These variations should not be considered by the monitor in determining whether a supply voltage is valid or not. The variations may cause spurious outputs at $\overline{RST}$, particularly if the supply voltage is near its trip threshold.

Two techniques are used to combat spurious reset without sacrificing threshold accuracy. First, the timeout period helps prevent high-frequency variation whose frequency is above 1/ t_{RST} from appearing at the $\overline{RST}$ output.

When the voltage at VM goes below the threshold, the $\overline{RST}$ pin asserts low. When the supply recovers past the threshold, the reset timer starts (assuming it is not disabled), and $\overline{RST}$ does not go high until it finishes. If the supply becomes invalid any time during the timeout period, the timer resets and starts a fresh when the supply next becomes valid.

While the reset timeout is useful at preventing toggling of the reset output in most cases, it is not effective at preventing nuisance resets due to short glitches (due to load transients or other effects) on a valid supply.

To reduce sensitivity to these short glitches, the comparator has additional anti-glitch circuitry. Any transient at the input of the comparator needs to be of sufficient magnitude and duration t_{UV} before it can change the monitor state.

The combination of the reset timeout and anti-glitch circuitry prevents spurious changes in output state without sacrificing threshold accuracy.

Adjustable Input

When the monitor threshold is configured as ADJ, the internal comparator input is connected to the pin without a resistive divider, and the pin is high-impedance. Thus, any desired threshold may be chosen by attaching VM to a tap point on an external resistive divider between the monitored supply and ground, as shown in Figure 1.

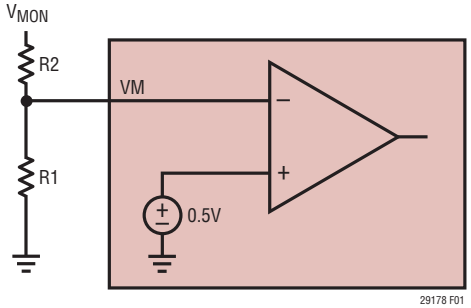


Figure 1. Setting the Trip Point Using the Adjustable Threshold.

APPLICATIONS INFORMATION

The reference input of the comparator is controlled by the tolerance pin. The external resistive divider should make the voltage at VM = 0.5V when the supply is at nominal value. The actual threshold of VM accounts for the supply tolerance of ±1.5% guaranteed over the full operating temperature range. The resulting tolerances are –6.5%, –11.5%, –16.5% which correspond to 0.468V, 0.443V, 0.418V respectively.

Typically, the user will pick a value of R1 based on acceptable current draw. Current used by the resistor divider will be approximately:

$$R1=\left(\frac{0.5V}{I}\right)$$

Recommended range of R1 is 1k—1M. Higher values of resistance exacerbate the degradation of threshold accuracy due to leakage currents.

If the nominal value of the supply being monitored is V_{NOM}, then

$$R2 = R1(2V_{NOM} - 1)$$

Resistor tolerances must be taken into account when determining the overall accuracy.

Selecting the Reset Timing Capacitor

The reset timeout period can be set to one of two fixed internal timers or set with a capacitor in order to accommodate a variety of applications. Connecting a capacitor, C_{RT}, between the RT pin and ground sets the reset timeout period, t_{RST}. The following formula approximates the value of capacitor needed for a particular timeout:

$$C_{RT} = t_{RST} \bullet 110\ [pF/ms]$$

For example, using a standard capacitor value of 2.2nF would give a 20ms timeout.

Figure 2 shows the desired reset timeout period as a function of the value of the timer capacitor.

Leaving RT open with no external capacitor generates a reset timeout of approximately 400µs. Shorting RT to V_{CC} generates a reset timeout of approximately 200ms.

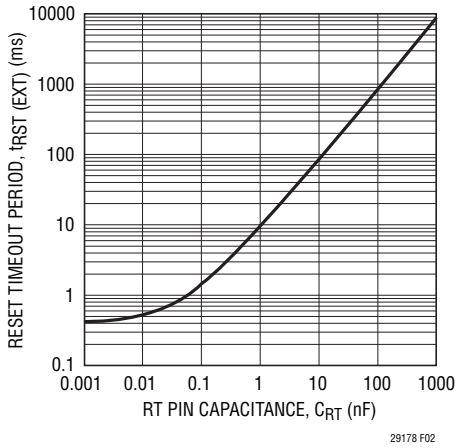


Figure 2. Reset Timeout Period vs RT Capacitance

$\overline{RST}$ Output Characteristics

The DC characteristics of the $\overline{RST}$ pull-down strength are shown in the Typical Performance Characteristics section. $\overline{RST}$ is an open-drain pin and thus requires an external pull-up resistor to the logic supply. $\overline{RST}$ may be pulled above V_{CC}, providing the voltage limits of the pin are observed.

The open-drain of the $\overline{RST}$ pin allows for wired-OR connection of several LTC2917/LTC2918's.

Watchdog

LTC2917-A/LTC2918-A

A standard watchdog function is used to ensure that the system is in a valid state by continuously monitoring the microprocessor's activity. The microprocessor must toggle the logic state of the WDI pin periodically (within upper boundary) in order to clear the watchdog timer. If timeout occurs, the LTC2917-A/LTC2918-A asserts $\overline{RST}$ low for the reset timeout period, issuing a system reset. Once the reset timeout completes, $\overline{RST}$ is released to go high and the watchdog timer starts again.

During power-up, the watchdog timer remains cleared while $\overline{RST}$ is asserted low. As soon as the reset timer times out, $\overline{RST}$ goes high and the watchdog timer is started.

APPLICATIONS INFORMATION

LTC2917-B/LTC2918-B

For applications in which reliability is even more critical, the LTC2917-B/LTC2918-B implements a windowed watchdog function by adding a lower boundary condition to the standard watchdog function. If the WDI input receives a falling edge prior to the watchdog lower boundary, the part considers this a watchdog failure, and asserts $\overline{RST}$ low (releasing again after the reset timeout period as described above). The LTC2917-B/LTC2918-B WDI input only responds to falling edges.

Setting the Watchdog Timeout Period

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog timeout period is adjusted by connecting a capacitor between WT and ground. Given a specified watchdog timeout period, the capacitor is determined by:

$$C_{WT} = t_{WD} \bullet 13.8\ [nF/s]$$

For example, using a standard capacitor value of 0.047µF would give a 3.4s watchdog timeout period.

Leaving WT open with no external capacitor generates a timeout of approximately 3.2ms. Shorting WT to V_{CC} generates a timeout of approximately 1.6s. Connecting WT to GND disables the watchdog function.

Manual Reset (LTC2918 Only)

The LTC2918 includes the $\overline{MR}$ pin for applications where a manual reset is desired. $\overline{MR}$ is internally pulled up, making it ready to interface with a push button with no external components required. Asserting $\overline{MR}$ low when $\overline{RST}$ is high initiates a reset, resulting in $\overline{RST}$ being asserted low for the reset timeout time.

Shunt Regulator

The LTC2917 and LTC2918 contain an internal 6.2V shunt regulator on the V_{CC} pin to allow operation from a high voltage supply. To operate the part from a supply higher than 5.7V, the V_{CC} pin must have a series resistor, R_{CC}, to the supply. See Figure 3. This resistor should be sized according to the following equation:

$$\frac{V_{S(MAX)} - 5.7V}{5mA} \le R_{CC} \le \frac{V_{S(MIN)} - 7V}{250\mu A}$$

where $V_{S(MIN)}$ and $V_{S(MAX)}$ are the operating minimum and maximum of the supply.

As an example, consider operation from an automobile battery which might dip as low as 10V or spike to 60V. We must then pick a resistance between 10.86k and 12k.

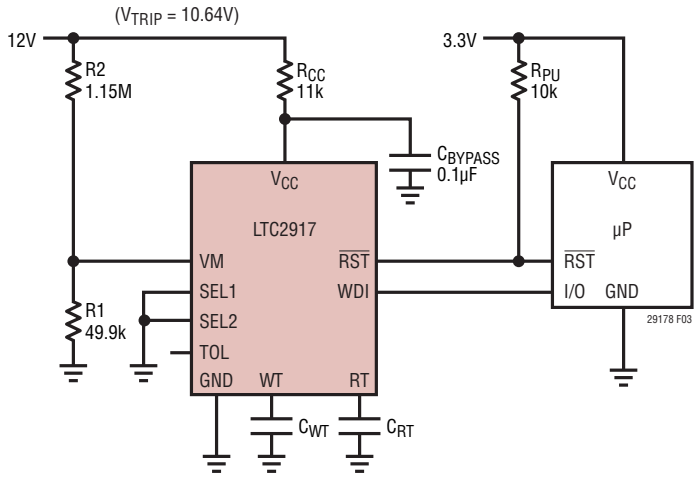
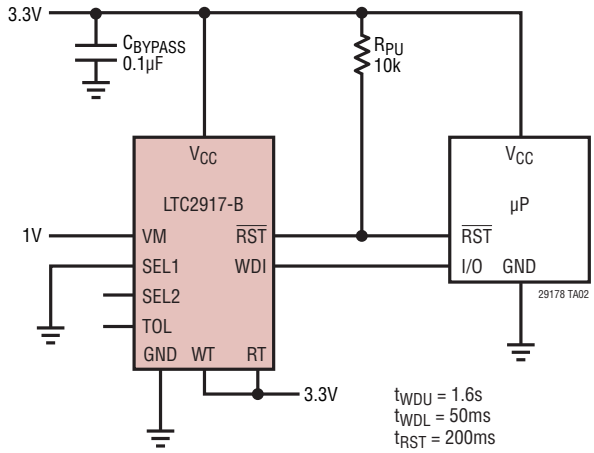


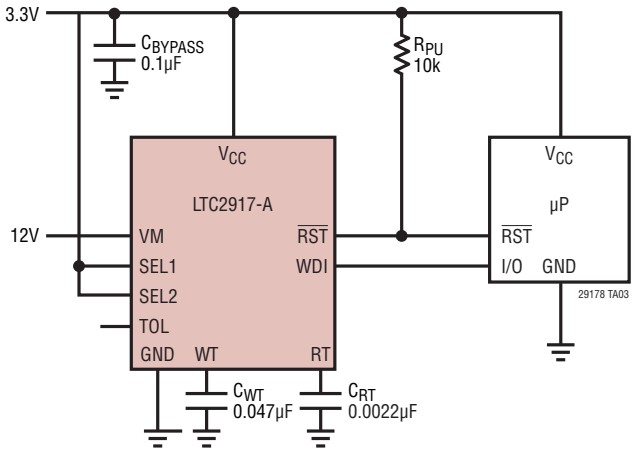
Figure 3. 12V Supply Monitor Powered From 12V, Utilizing the Internal Shunt Regulator with 3.3V Logic Out

TYPICAL APPLICATIONS

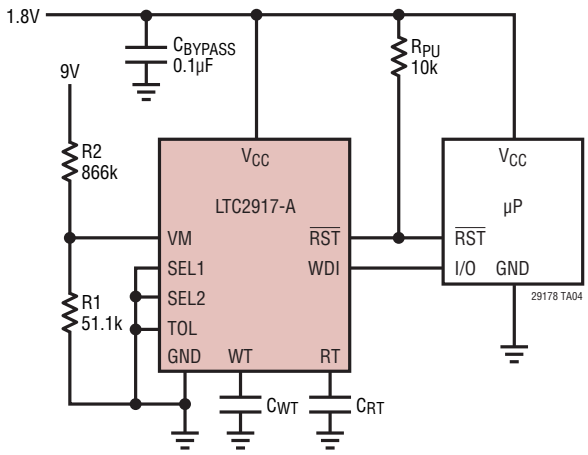
1V Supply Monitor with Windowed Watchdog Timeout and Internal Timers Selected



12V Supply Monitor with 20ms Reset Timeout and 3.4s Watchdog Timeout, with 3.3V Logic Out

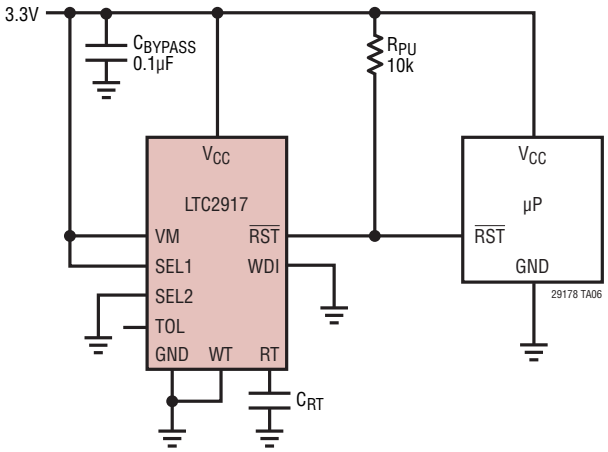


9V, –15% Tolerance Supply Monitor ith 1.8V Logic Out

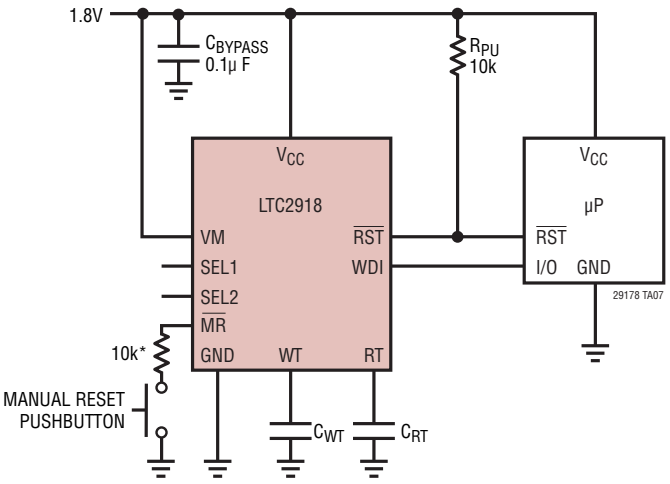


TYPICAL APPLICATIONS

3.3V, –10% Tolerance Supply Monitor with Disabled Watchdog

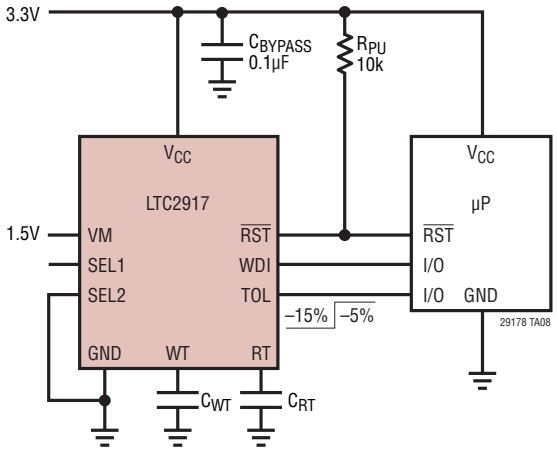


1.8V, –5% Supply Monitor with Manual Reset



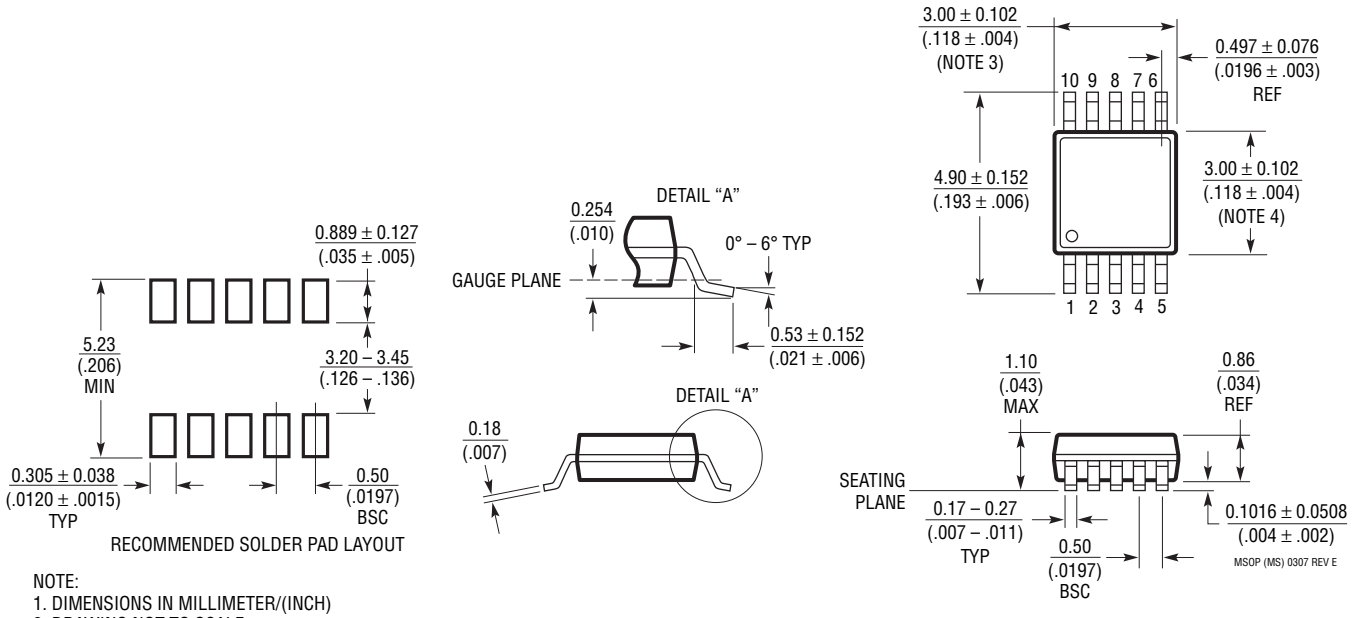
*OPTIONAL RESISTOR RECOMMENDED TO EXTEND ESD TOLERANCE

1.5V Supply Monitor with Tolerance Control for Margining, –5% Operation with –15% Margining



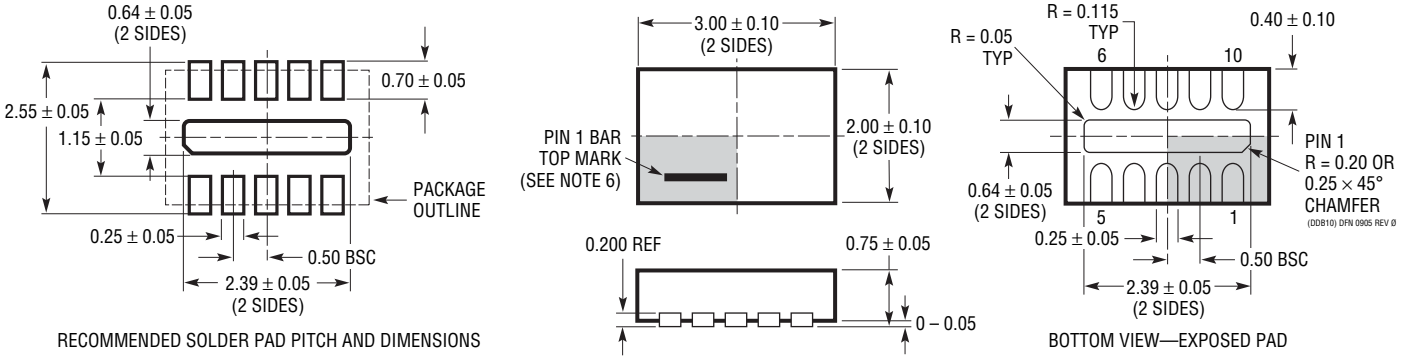
PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

DDB Package
10-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1722 Rev Ø)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE