Power Supply Tracker with Input Monitors

FEATURES

- **Tracks Multiple Supplies with MOSFET Switches**
- **Monitors 5 Input Voltages Including V_{CC}**
- **Guaranteed Threshold Accuracy: ±1% at 0.5V**
- **Automatic Remote Sense Switching**
- **Adjustable Supply Ramp Rate**
- Overvoltage Monitor
- Adjustable Electronic Circuit Breaker
- Adjustable Power-Good Delay
- Available for V_{CC} Supply Voltages of 5V, 3.3V and 2.5V
- Available in 16-Pin Narrow SSOP (LTC2921 Series) and 20-Pin TSSOP (LTC2922 Series)

APPLICATIONS

- Desktop Computers
- Plug-In Cards
- Telecom Infrastructure
- Supply Sequencing
- Instruments

DESCRIPTION

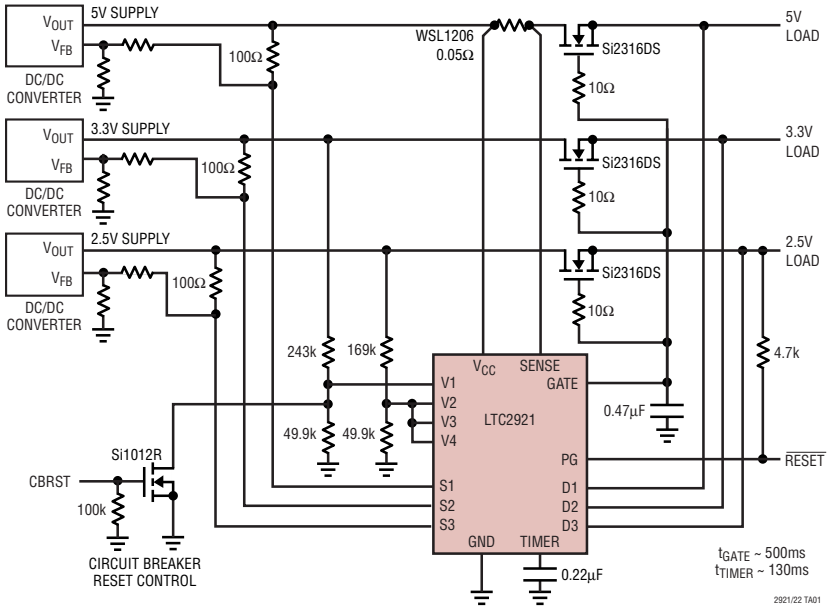
The LTC®2921 and LTC2922 monitor up to five supplies and force them to track on power-up in multiple supply systems. Using external N-channel pass transistors, the supplies can be ramped up at an adjustable rate. Automatic remote sense switching allows the DC/DC converters to compensate for series voltage drops in the wiring. An incorrect level on one or more of the supplies triggers disconnect of all supplies. Tight 1% accuracy and glitch immunity on the low 0.5V monitoring level ensure no false error disconnects.

The LTC2921 and LTC2922 each feature an adjustable electronic circuit breaker to protect the V_{CC} supply against short circuits. Capacitance at the TIMER pin programs the delays in the monitoring sequence.

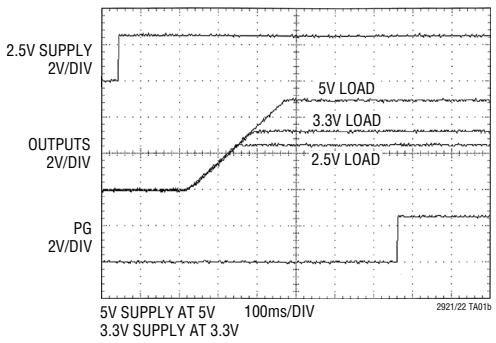
The LTC2921 includes three remote sense switches in a 16-pin narrow SSOP package, while the LTC2922 includes five remote sense switches in a 20-pin TSSOP package. Both parts are available for V_{CC} supply voltages of 5V, 3.3V, and 2.5V.

TYPICAL APPLICATION

Three-Supply Tracker and Monitor (5V, 3.3V, 2.5V)



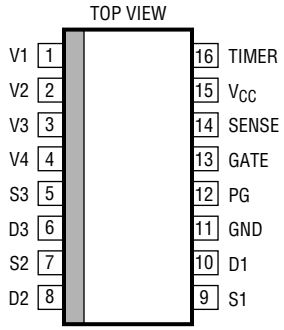
Load Voltage Ramp-Up and Power-Good Activation



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} Supply Voltage ..... –0.3V to 7V
V1, V2, V3, V4 Voltages ..... –0.3V to 7V
SENSE Voltage ..... –0.3V to 7V
TIMER Voltage ..... –0.3V to (V_{CC} + 0.3V)
Charge Pumped Output Voltages
GATE, PG ..... –0.3V to 12.2V
Switch Voltages
S0, D0, S4, D4 (LTC2922 Series) ..... –0.3V to 7V
S1, D1, S2, D2, S3, D3 ..... –0.3V to 7V
Switch Currents (DC, RMS)
S0, D0, S4, D4 (LTC2922 Series) 30mA
S1, D1, S2, D2, S3, D3 ..... 30mA
Operating Ambient Temperature Range
LTC2921C/LTC2922C ..... 0°C to 70°C
LTC2921I/LTC2922I ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



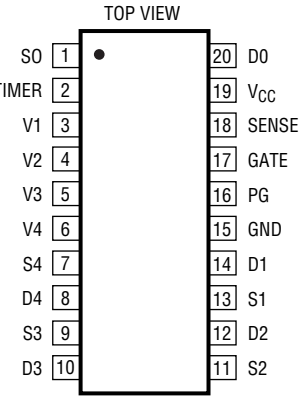
GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC2921CGN
LTC2921CGN-3.3
LTC2921CGN-2.5
LTC2921IGN
LTC2921IGN-3.3
LTC2921IGN-2.5

GN PART MARKING

2921
292133
292125
2921I
921I33
921I25



F PACKAGE
20-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 90°C/W

ORDER PART NUMBER

LTC2922CF
LTC2922CF-3.3
LTC2922CF-2.5
LTC2922IF
LTC2922IF-3.3
LTC2922IF-2.5

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V for LTC2921/LTC2922, V_{CC} = 3.3V for LTC2921-3.3/LTC2922-3.3, and V_{CC} = 2.5V for LTC2921-2.5/LTC2922-2.5, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Pin							
V_{CC}	Supply Voltage	Typical Operating Range					
		LTC2921/LTC2922		4.50	5.00	5.50	V
		LTC2921-3.3/LTC2922-3.3		2.97	3.30	3.63	V
		LTC2921-2.5/LTC2922-2.5		2.37	2.50	2.63	V
I_{CC}	Supply Current				2		mA
$V_{CC(MON)}$	Supply Monitor Threshold Voltage	LTC2921/LTC2922	●	4.285	4.350	4.415	V
		LTC2921-3.3/LTC2922-3.3	●	2.828	2.871	2.914	V
		LTC2921-2.5/LTC2922-2.5	●	2.265	2.300	2.335	V
$V_{CC(OV)}$	Supply Overvoltage Threshold	LTC2921/LTC2922	●	5.82	6.13	6.43	V
		LTC2921-3.3/LTC2922-3.3	●	3.84	4.04	4.24	V
		LTC2921-2.5/LTC2922-2.5	●	3.08	3.24	3.40	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V for LTC2921/LTC2922, V_{CC} = 3.3V for LTC2921-3.3/LTC2922-3.3, and V_{CC} = 2.5V for LTC2921-2.5/LTC2922-2.5, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(UVLO)}$	Supply Undervoltage Lockout	V_{CC} Rising	●	2.08	2.20	2.30	V
$V_{CC(UVH)}$	Supply Undervoltage Hysteresis	V_{CC} Falling			120		mV
Electronic Circuit Breaker							
ΔV_{SENSE}	Circuit Breaker Trip Voltage	$\Delta V_{SENSE} = V_{CC} - V_{SENSE}$	●	45	50	55	mV
I_{SENSE}	SENSE Pin Input Current				150	500	nA
$t_{V1(DLY)}$	Circuit Breaker Trip Delay Time	$V_{CC} - V_{SENSE}$ = 150mV LTC2921/LTC2922 LTC2921-3.3/LTC2922-3.3 LTC2921-2.5/LTC2922-2.5		 0.5 0.5 0.5	 1.5 1.5 1.5	 3.0 3.0 6.0	 µs µs µs
$t_{V1(RST)}$	Circuit Breaker Reset Pulse Width	Guaranteed Not to Reset Guaranteed to Reset	● ●	 150		50	µs µs
$V_{V1(RST)}$	Circuit Breaker Reset Threshold Voltage		●	0.490	0.500	0.510	V
Monitor Inputs							
V_{MON}	V1-V4 Monitor Threshold Voltages		 ●	0.495 0.492	0.500 0.500	0.505 0.508	V V
V_{OV}	V1-V4 Overvoltage Thresholds		●	0.665	0.700	0.735	V
I_{MON}	V1-V4 Input Currents					±0.1	µA
TIMER Pin							
$V_{TIMER(TH)}$	TIMER Ramp Threshold Voltage		●	1.15	1.20	1.25	V
$I_{TIMER(PU)}$	TIMER Pull-Up Current	V_{TIMER} = 1V	●	–1.3	–2.0	–2.5	µA
$I_{TIMER(PD)}$	TIMER Pull-Down Current	V_{CC} = 2.35V, V_{TIMER} = 0.4V		100			µA
$V_{TIMER(CLR)}$	TIMER Cleared Threshold Voltage	V_{TIMER} Falling			150	250	mV
GATE Pin							
V_{GATE}	GATE Drive Output Voltage	LTC2921/LTC2922 LTC2921-3.3/LTC2922-3.3 LTC2921-2.5/LTC2922-2.5	● ● ●	10.0 8.4 6.1	11.1 9.1 6.8	12.2 9.8 7.5	V V V
$I_{GATE(PU)}$	GATE Pull-Up Current	$V_{GATE} = V_{CC}$	●	–6.5	–10.0	–12.5	µA
$I_{GATE(PD)}$	GATE Pull-Down Current	V_{CC} = 2.35V, V_{GATE} = 2.35V		10			mA
Remote Sense Switches							
$R_{DS(FB)}$	Feedback Switch Resistances (Note 3)	$V_D = V_{CC}$	●		2	10	Ω
PG Pin							
$I_{PG(PU)}$	PG Pull-Up Current	$V_{PG} = V_{CC}$	●	–2.6	–4.0	–5.0	µA
$I_{PG(PD)}$	PG Pull-Down Current	V_{CC} = 2.35V, V_{PG} = 2.35V		10			mA
$V_{PG(OL)}$	PG Output Low Voltage	V_{CC} = 2.35V, I_{PG} = 5mA	●			0.4	V
V_{PG}	PG Output Voltage (Note 4)	LTC2921/LTC2922 LTC2921-3.3/LTC2922-3.3 LTC2921-2.5/LTC2922-2.5	● ● ●	10.0 8.4 6.1	11.1 9.1 6.8	12.2 9.8 7.5	V V V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LTC2921 Series: $T_J = T_A + (P_D \bullet 110°C/W)$

LTC2922 Series: $T_J = T_A + (P_D \bullet 90°C/W)$

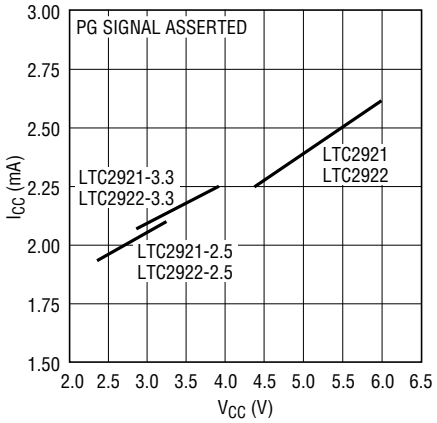
Note 3: This specification applies to all switches, and is measured with $V_S < V_D$.

Note 4: The PG pin will rise to approximately the same voltage as the GATE pin when not pulled up or pulled down by external resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

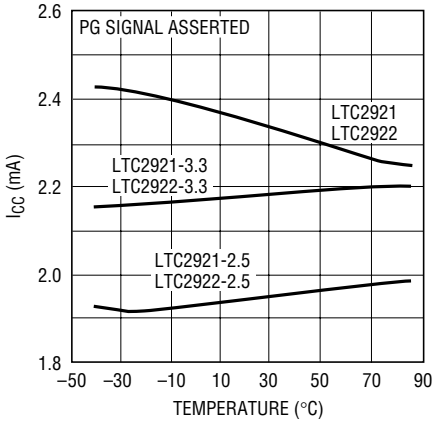
Specifications are at T_A = 25°C unless otherwise noted.

Supply Current vs Supply Voltage



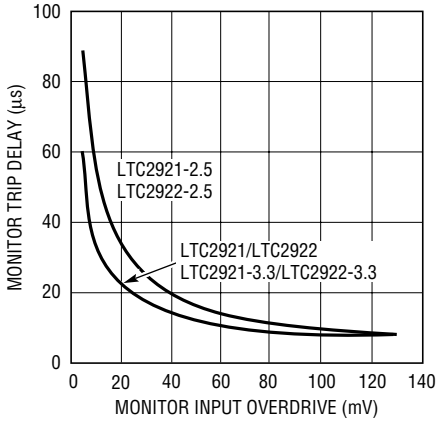
2921/2 G01

Supply Current vs Temperature



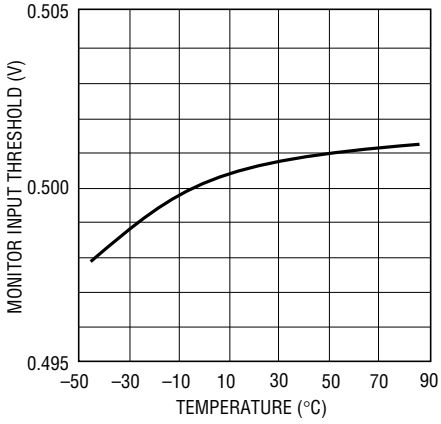
2921/2 G02

Monitor Trip Delay vs Monitor Input Overdrive



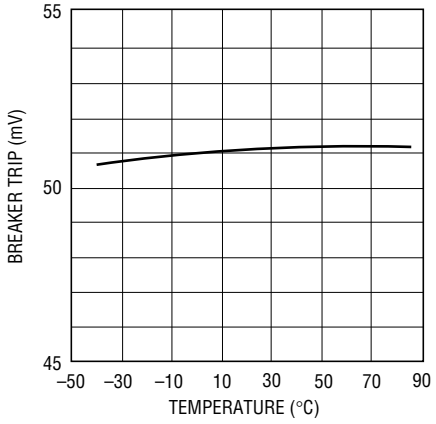
2921/2 G03

Monitor Input Threshold vs Temperature



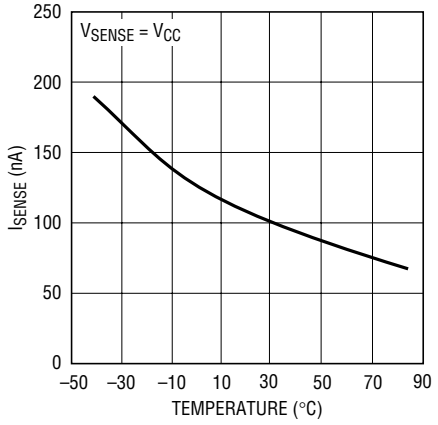
2921/2 G04

Circuit Breaker Trip Voltage vs Temperature



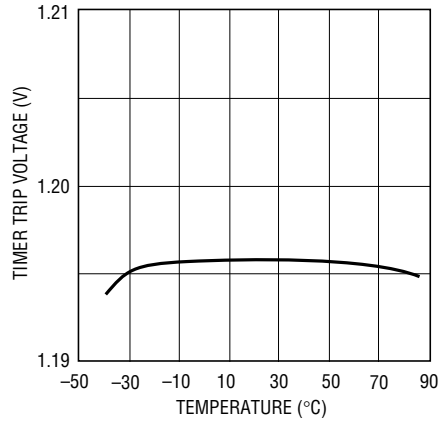
2921/2 G05

SENSE Input Current vs Temperature



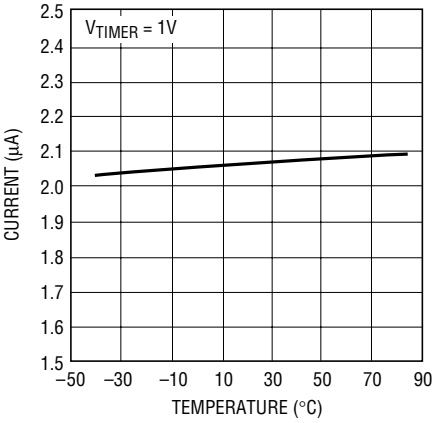
2921/2 G06

TIMER Trip Voltage vs Temperature



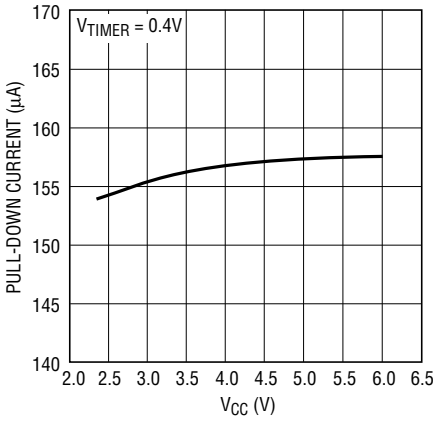
2921/2 G07

TIMER Pull-Up Current vs Temperature



2921/2 G08

TIMER Pull-Down Current vs Supply Voltage

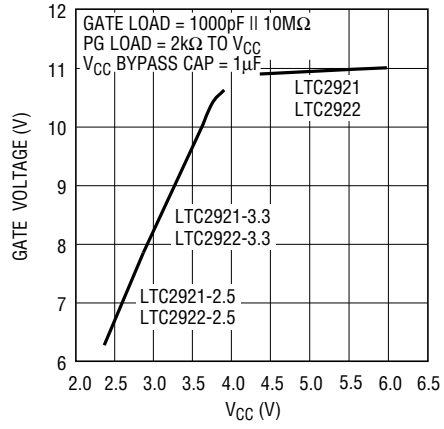


2921/2 G09

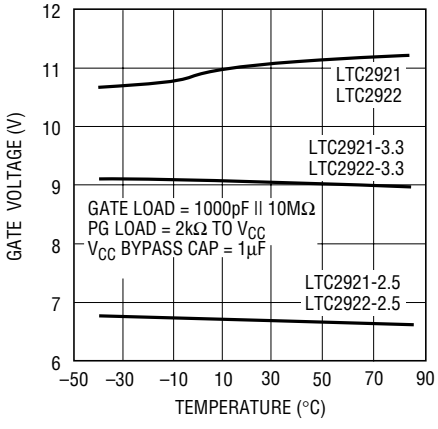
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

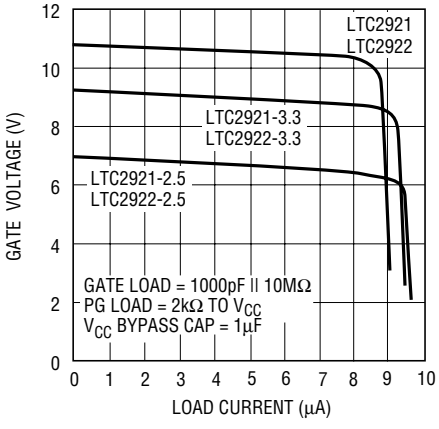
Gate Voltage vs Supply Voltage



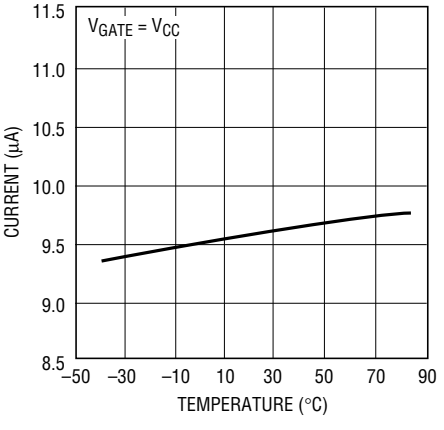
Gate Voltage vs Temperature



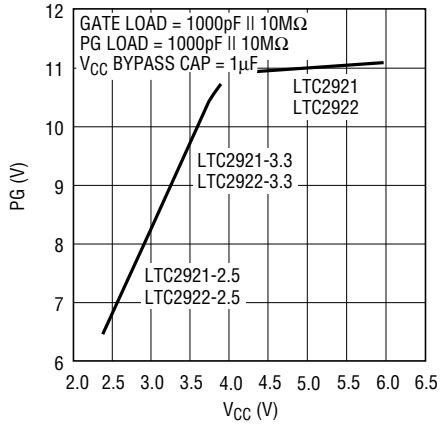
Gate Voltage vs Load Current



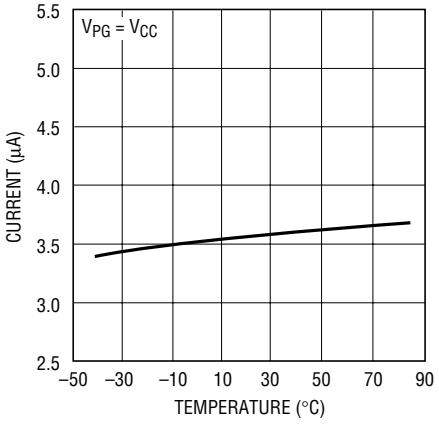
GATE Pull-Up Current vs Temperature



PG Voltage vs Supply Voltage



PG Pull-Up Current vs Temperature



PIN FUNCTIONS (LTC2921/LTC2922 or [LTC2922 Only])

S0, D0 (Pins 1, 20 [LTC2922]): Remote Switch 0. These pins are the terminals of an internal N-channel FET switch that is enabled after the GATE pin is fully ramped up. This switch can be used to connect a remote sense line to compensate for IR drop across the external FETs. The gate of the internal switch ramps up at a nominal rate of 8V/ms. The pins are interchangeable, either switch pin can be tied to the load side. Tie both pins to ground if unused.

S4, D4 (Pins 7, 8 [LTC2922]): Remote Sense Switch 4. Tie to GND if unused.

S3, D3 (Pins 5, 6/Pins 9, 10): Remote Sense Switch 3. Tie to GND if unused.

S2, D2 (Pins 7, 8/Pins 11, 12): Remote Sense Switch 2. Tie to GND if unused.

S1, D1 (Pins 9, 10/Pins 13, 14): Remote Sense Switch 1. Tie to GND if unused.

TIMER (Pin 16/Pin 2): Timing Delay Input. Connect a capacitor between this pin and ground to set a 600ms/µF delay at two points in the monitoring sequence. This sets the delay after all monitors are good, before the start of GATE ramping, and the delay after the remote sense switches are on, before PG is activated. TIMER must fall below 150mV before a timing delay can start. The TIMER pin is pulled to ground at other points in the sequence.

V1-V4 (Pins 1-4/Pins 3-6): Supply Monitor Inputs. All four inputs must lie above the monitor threshold level (0.5V) and below the monitor overvoltage level (0.7V) for a turn-on sequence to commence or continue. When any monitor input falls outside those levels, the GATE and PG pins are pulled low, disconnecting all the loads. Glitch filtering on the 0.5V monitor threshold prevents low-energy voltage spikes from affecting the comparators' results. V1 also serves as an active-low reset pin for the circuit breaker. Tie unused monitor inputs to used monitor inputs.

GND (Pin 11/Pin 15): Circuit Ground.

PG (Pin 12/Pin 16): Power Good Output. A 4µA current source from the internal charge pump rail (V_{PUMP}) pulls PG up after the turn-on sequence is complete. The output is pulled to ground before turn-on is complete, when any monitor is out of compliance, when the circuit breaker trips, and when V_{CC} is undervoltage. An external resistor can be added to pull up to a lower voltage and to improve pull up speed. This pin can also be configured as a gate drive for external N-channel FETs in sequencing applications. In applications not requiring the PG output, leave the pin unconnected.

GATE (Pin 13/Pin 17): Gate Drive for External N-Channel FETs. A 10µA current source from the internal charge pump rail (V_{PUMP}) ramps the gates of the external N-channel MOSFETs forcing all supplies to track on. The resistor and capacitor network from this pin to ground sets the supplies' ramp rate and enhances control loop stability.

SENSE (Pin 14/Pin 18): Circuit Breaker Sense Input. An external resistor between V_{CC} and SENSE sets the electronic circuit breaker trip current. The breaker trips when the voltage across the resistor exceeds 50mV for 1µs. To disable the circuit breaker tie SENSE to V_{CC}. To reset the circuit breaker after the current falls below the trip point, pull the V1 pin below 0.5V for >150µs or go into undervoltage lockout for >10µs.

V_{CC} (Pin 15/Pin 19): Supply Voltage. The voltage at V_{CC} is monitored through an internal resistive divider in a manner similar to the V1-V4 inputs. An undervoltage lockout circuit disables the part until the voltage at V_{CC} is greater than 2.2V. The V_{CC} pin must be connected to the highest supply voltage. Bypass the V_{CC} pin to ground with a 10µF capacitor.

FUNCTIONAL DIAGRAM

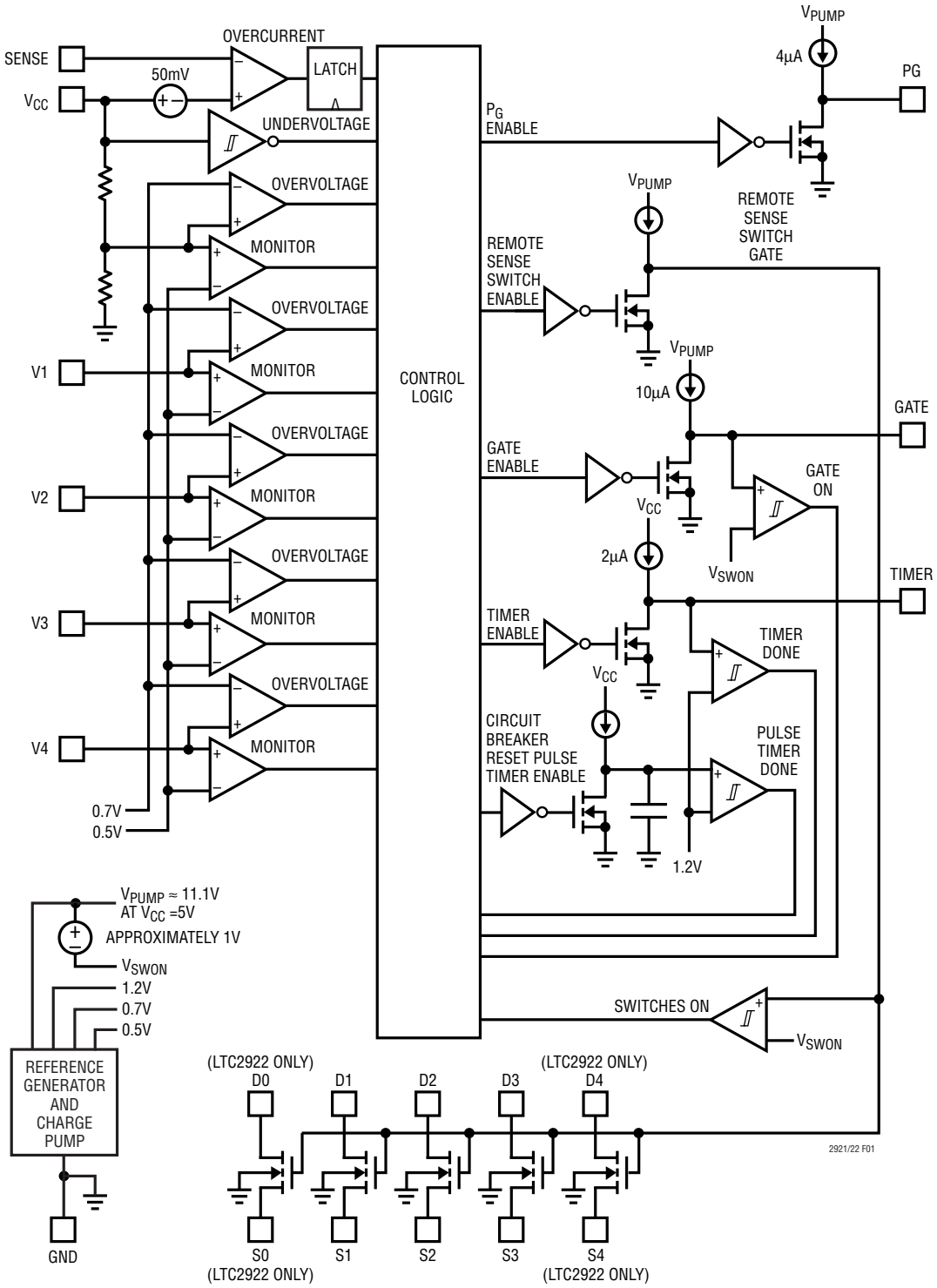


Figure 1. LTC2921 and LTC2922 Functional Diagram

OPERATION

General Operation

The LTC2921 and LTC2922 track multiple supplies, monitor multiple inputs, and provide integrated switches for remote sensing. Once all input voltages lie between monitoring and overvoltage threshold levels, in-line FETs are turned on to simultaneously ramp power to the loads. The automatic remote sense switches are then activated, and the power good signal is asserted. After initial power-on the LTC2921 and LTC2922 continue monitoring the inputs. Several types of events will trigger interruption, any of which will disconnect all supplies, deactivate the power good signal, and open the remote sense switches.

Monitoring Sequence

A normal power-on sequence comprises the following steps:

Step 0) Wait for V_{CC} to exceed the undervoltage lockout threshold. Continue checking V_{CC}.

Step 1) Confirm that the circuit breaker has not tripped and wait for all monitored supplies, including V_{CC}, to be between their programmed monitor and overvoltage thresholds. Continue checking these conditions.

Step 2) Check that the TIMER pin voltage starts below 150mV. Create a delay by ramping up the TIMER pin until it trips an internal comparator.

Step 3) Ramp the GATE pin to turn on the external N-channel FETs, simultaneously ramping the supplies into their loads. Await confirmation of full GATE enhancement, i.e., GATE voltage within ~1V of V_{PUMP}. Continue checking this condition.

Step 4) Activate the remote sense switches. Await confirmation of full Feedback Switch Gate enhancement.

Step 5) Wait again for another TIMER cycle delay.

Step 6) Release the pull-down on the PG output. Continue checking V_{CC}, the circuit breaker, the input voltages, and the GATE voltage.

Interrupting Events

Three events can interrupt the sequence and trigger immediate disconnect of all supplies, pull-down of the PG signal, and deactivation of the remote sense switches. The three interrupting events are a lockout, a fault, and an error.

A lockout occurs when V_{CC} falls below the undervoltage threshold (including hysteresis). Escape from lockout requires sufficient V_{CC} voltage. Leaving lockout, the sequence begins at Step 1. A lockout condition supersedes faults and errors.

A fault occurs when the circuit breaker trips. Escape from a fault requires pulsing the V1 pin below the reset threshold of 0.5V(nom) for more than 150µs after the current falls below the trip point. When V1 returns high, the sequence begins from Step 1. An undervoltage lockout of >10µs also clears the circuit breaker fault latch. A fault condition supersedes errors.

An error occurs when one or more of the monitor inputs (V1-V4 pins) or V_{CC} falls below its monitor threshold, or rises above its overvoltage threshold. A loss of voltage on the GATE pin, once it has fully ramped up, also causes an error. An error sends the sequence to Step 1.

Feedback Switches for Remote Sensing

The integrated N-channel switches of the LTC2921/LTC2922 automatically compensate for the voltage drops caused by the $R_{DS(ON)}$ of the external load-control MOSFET switches. This is accomplished by modifying the normal feedback path of each power supply that is controlled by the LTC2921/LTC2922. When the load-control switches are off, the remote sense switches are also off, and the power supply uses its normal feedback path to sense its output voltage. After the load-control switches are turned on, the remote sense switches are turned on to create dominating feedback paths. The feedback loops include the load-control switches, thus compensating for their voltage drops.

In order to eliminate glitching on the output of the power supply, the remote sense switches are turned on at a controlled rate of about 8V/ms. The gates of these integrated N-channel devices are pulled up above V_{CC} to V_{PUMP} so as to provide a low-resistance path for a wide range of voltages.

OPERATION

Electronic Circuit Breaker

Placing a resistor between the V_{CC} and SENSE pins allows the part to detect shorts and excessive currents on the V_{CC} supply. The electronic circuit breaker trips when the voltage across the resistor is >50mV for more than 1µs. A trip causes a fault condition which interrupts the monitor sequence, and which requires reset of the circuit breaker latch (see Interrupting Events section). Breaker reset is achieved by pulling V1 below the reset threshold for >150µs after the current falls below the trip point, or by returning from undervoltage lockout on V_{CC}.

TIMING DIAGRAMS

The timing of a typical start-up sequence for the LTC2921/LTC2922 is shown in Figure 2. V_{CC} exceeds the undervoltage lockout level at time 0. All monitor inputs settle between the 0.5V monitor threshold and the 0.7V overvoltage threshold by time 1, then a TIMER cycle starts. The TIMER pin reaches 1.2V at time 2, and GATE ramping begins. When the GATE ramp completes at time 3, the automatic remote sense switches close. Another TIMER delay begins at time 4 and finishes at time 5, at which time PG is activated.

The timing of a monitor failure and subsequent regular turn-on is shown in Figure 3. Prior to time 1, a successful turn-on sequence had completed. At time 1, monitor V2 falls below the 0.5V reference, triggering an error. The GATE pin, PG pin, and the remote sense switches fall at rates determined by the pull-down currents and loading conditions of each (times 2, 3, 4). At time 5, monitor V2 recovers, and a normal turn-on sequence begins.

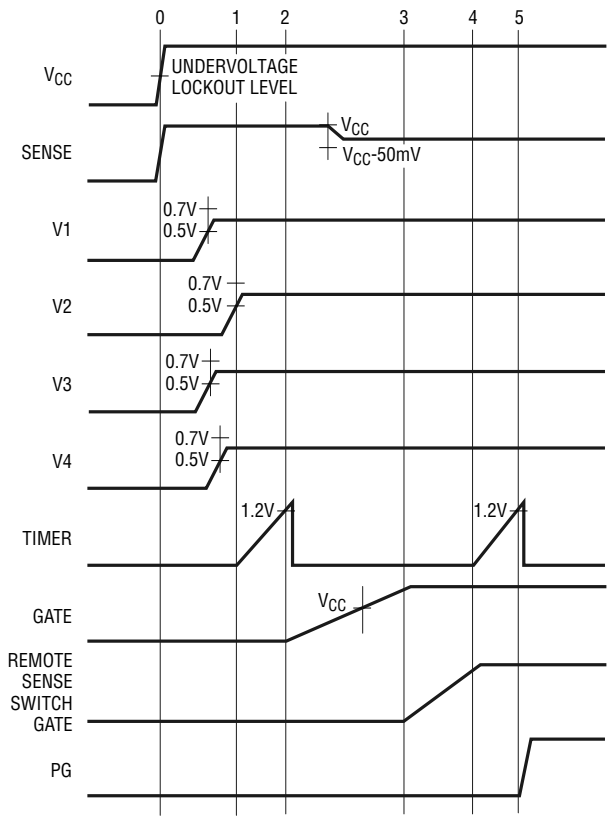


Figure 2. Typical Start-Up Sequence

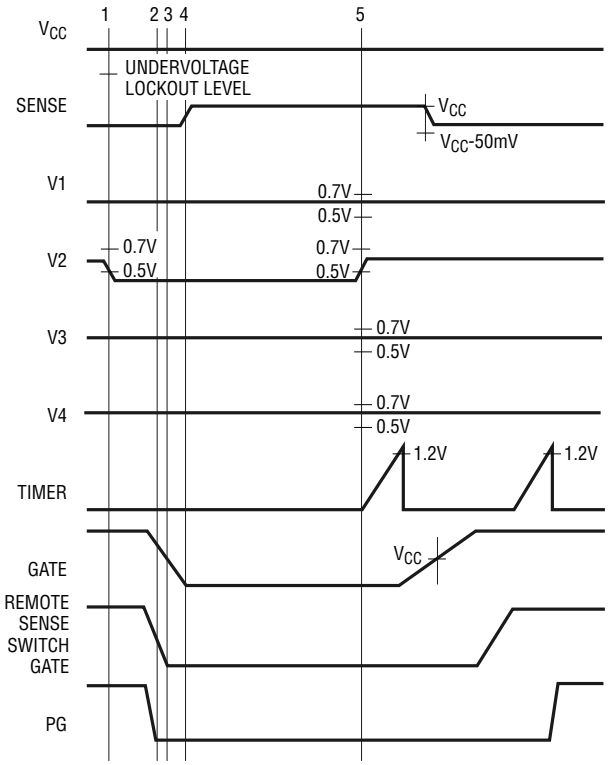


Figure 3. Monitor Failure and Start-Up Sequence Timing

TIMING DIAGRAMS

The timing of a circuit breaker trip and reset, and a subsequent regular turn-on are shown in Figure 4. Prior to time 1, a successful turn-on sequence had completed. At time 1, excessive current pulls SENSE more than 50mV below V_{CC}. The GATE pin, PG pin, and the remote sense switches fall at rates determined by the pull-down currents and loading conditions of each (times 2, 3, 4). Note that the excessive current condition ceases at time 4. A circuit breaker reset pulse is initiated at time 5. The latch resets at time 6 since the V1 pulse is wide enough. A normal turn-on begins when V1 rises above the monitor threshold (time 7 onward).

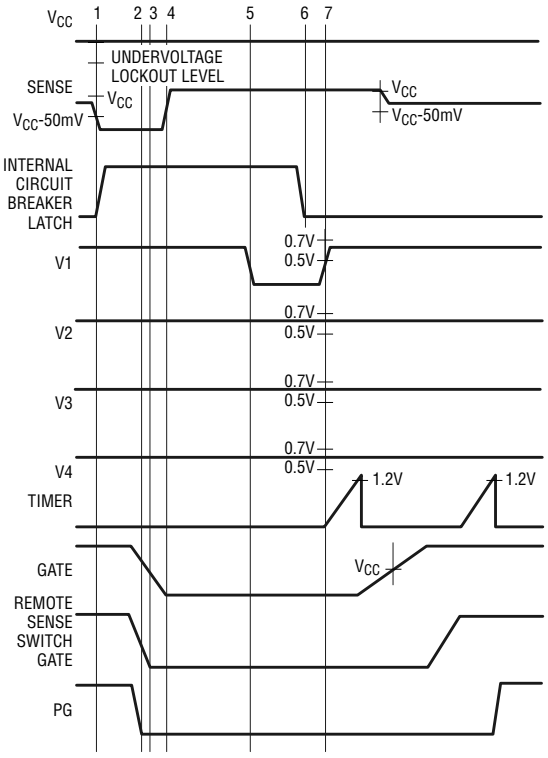


Figure 4. Circuit Breaker Trip, Reset and Start-Up Sequence Timing

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Multiple supply systems have become common to accommodate circuits on the same board with different voltage requirements. Desktop PC motherboards, instrumentation circuits and plug-in boards of all kinds often require tracking and control of several supply voltages.

The LTC2921 and LTC2922 ramp and monitor up to five supply voltages in such systems. External resistive voltage dividers independently program four monitor levels, while an internal divider sets the V_{CC} pin supply monitor level. Time delays in the monitoring sequence are set by an external capacitor at the TIMER pin.

The GATE pin provides a high side drive voltage appropriate to logic-level and sublogic-level N-channel power MOSFETs. The external RC network on GATE programs the supply ramp rate and eliminates possible high frequency oscillations in the power path. Featured in the LTC2921/LTC2922 series are sub-10Ω internal remote sense switches to compensate for voltage drops between the supplies and the loads.

At the end of a successful power-on sequence, the LTC2921/LTC2922 asserts the PG output. A typical application uses an external pull-up resistor between PG and the load side of a supply. In applications where supply power-on sequencing is required, the PG pin can function as a second, separate high side driver.

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Setting the Supply Monitor Levels

The LTC2921 and LTC2922 series both feature low 0.5V monitoring thresholds with tight 1% accuracy. To set a supply monitoring level tightly, design a precision ratio resistive divider to relate the lowest valid supply voltage to the maximum specified monitor threshold voltage. Use resistors with 1% tolerance or better to limit the error due to mismatch. The basic resistive divider connection for supply monitoring is shown in Figure 5.

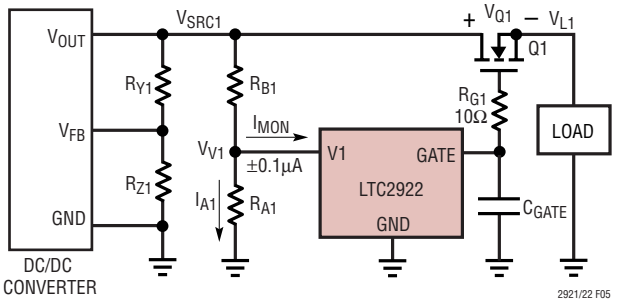

Figure 5. Basic Monitor Connection

First, divide the nominal monitor threshold voltage by an acceptable bias current (I_{A1}), and choose a nearby standard value for resistor R_{A1} (see Equation 1).

Next, calculate the bounds on the value of R_{B1} that guarantee that the divided minimum supply voltage exceeds the maximum specified monitor threshold voltage, and that the minimum specified overvoltage threshold exceeds the divided maximum supply voltage. Use Equations 2 and 3 to calculate $R_{B1(MAX)}$ and $R_{B1(MIN)}$ from R_{A1}, the resistor tolerance (RTOL), the supply voltage, the monitor threshold and overvoltage specifications, and the monitor pin leakage current specification.

When the integrated remote sensing switch is closed, the DC/DC converter will compensate for the IR drop from drain to source of the external N-channel FET ($V_{Q1(ON)}$) by increasing the supply voltage by the same amount. Calculate with $V_{Q1(ON)(MAX)}$ = 0V if the remote sense switch is not used.

$$R_{A1} = \frac{0.500V}{I_{A1}} \quad (1)$$

$$R_{B1(MAX)} = R_{A1} \bullet \left(\frac{1-RTOL}{1+RTOL}\right) \bullet \left(\frac{V_{SRC1(MIN)} - 0.505V}{0.505V + 0.1\mu A \bullet R_{A1}}\right) \quad (2)$$

$$R_{B1(MIN)} = R_{A1} \bullet \left(\frac{1+RTOL}{1-RTOL}\right) \bullet \left(\frac{V_{SRC1(MAX)} + V_{Q1(ON)(MAX)} - 0.665V}{0.665V - 0.1\mu A \bullet R_{A1}}\right) \quad (3)$$

Choose a standard resistor value for R_{B1} that satisfies the inequality of Equation 4.

$$R_{B1(MIN)} \le R_{B1} \le R_{B1(MAX)} \quad (4)$$

When several standard values meet the requirement, choose the value closest to $R_{B1(MAX)}$ to set the tightest monitor threshold. This also allows more headroom for larger $V_{Q1(ON)(MAX)}$. Alternatively, choose the standard value closest to $R_{B1(MIN)}$ to set the tightest overvoltage threshold.

All four monitor input voltages must be between the monitor threshold and the overvoltage threshold for the turn-on sequence to begin. Connect unneeded monitor input pins to any of the utilized monitor input pins.

Selecting the External N-Channel MOSFETs

The GATE pin drives the gate of external N-channel MOSFETs above V_{CC} to connect the supplies to the loads. The GATE drive voltage provided by the LTC2921/LTC2922 series is best suited to logic-level and sublogic-level power MOSFETs. To achieve the lowest switch resistance, the V_{CC} pin must be connected to the highest supply voltage.

Consider the application requirements for current, turnoff speed, on-resistance, gate-source voltage specification, etc. Refer to the Electrical Specifications and Typical Performance Curves to determine the GATE voltages for given V_{CC} voltages over the required range of conditions. Calculate the minimum gate drive voltage for each monitored supply for use in selecting the FETs. Check the maximum GATE voltage against the FETs' gate-source

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voltage specifications. On-resistance is a critical parameter when choosing power MOSFETs. The integrated remote sense switches compensate for IR drops, but minimizing $V_{Q(MAX)}$ leaves more margin for designing the resistive voltage divider for the monitors.

Setting the GATE Ramp Rate

Application of power to the loads is controlled by setting the voltage ramping rate with an external capacitor on the GATE pin. During Step 3 of the monitoring sequence, a 10µA pull-up ramps the GATE pin capacitance up to V_{PUMP}, the internal charge pump voltage. Use Equation 5 to calculate the nominal GATE pin capacitance necessary to achieve a given ramp rate, $\Delta V/\Delta t$:

$$C_{GATE} = \frac{10\mu A}{\Delta V / \Delta t} \quad (5)$$

Alternatively, to calculate the GATE capacitor to achieve a desired nominal ramp time, use Equation 6. The GATE drive voltage (V_{GATE}) varies with V_{CC} voltage. Consult the Electrical Characteristics table and Typical Performance curves to choose an appropriate value to insert for V_{GATE}.

$$C_{GATE} = \frac{10\mu A \bullet t_{RAMP}}{V_{GATE}} \quad (6)$$

When the GATE pin drives several FETs in parallel, the load voltages ramp together at the same rate until the lowest supply reaches its full value. The other supplies continue to track until the next lowest supply reaches its full value, and so on.

The GATE pin must not be forced above the level it reaches when fully ramped. An internal clamp limits the GATE voltage to ≤12.2V relative to ground.

Damp possible ramp-on oscillations by including a 10Ω resistor in series with each external N-channel gate, and as necessary, a 0.1µF capacitor on each external N-channel drain, as shown in Figure 6.

Setting the Sequence Delay Timer

The turn-on sequence includes two programmable delays set by the capacitance on the TIMER pin. More precisely, a single delay value is used at two points in the sequence.

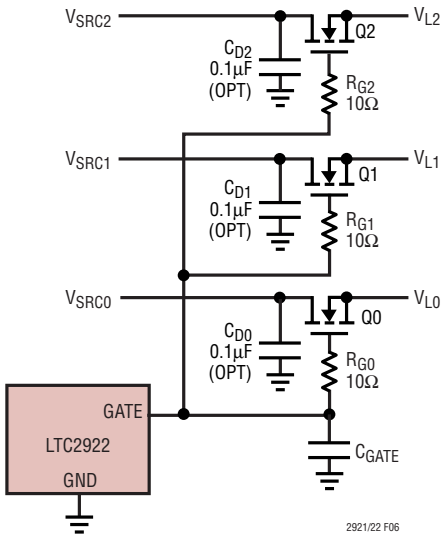

Figure 6. Ramping and Damping Components on GATE Pin

In both cases, the delay provides a measure of confidence that conditions are stable enough for the sequence to advance.

The first TIMER delay begins once all monitor voltages comply with their thresholds, the electronic circuit breaker has not tripped, and V_{CC} is not undervoltage. The TIMER pin sources 2µA into an external capacitor, which ramps its voltage. A comparator trips when the TIMER pin voltage reaches the internal 1.2V reference, then the GATE ramp begins, and TIMER is pulled to ground. The second TIMER delay begins after the gate of the remote sense switches is fully ramped up. After the TIMER ramp completes, the PG pin is activated. An internal circuit pulls-down the TIMER pin with >100µA of current at all times, except during the ramping periods, and when V_{CC} is undervoltage.

Calculate the nominal value for the timing capacitor by inserting the desired delay into Equation 7:

$$C_{TIMER} = \frac{2\mu A}{1.2V} \bullet t_{DLY} \quad (7)$$

For delay times below 60µs, be sure to limit stray capacitances on the TIMER pin by using good PCB design practices. To program essentially no delay (<1µs), float the TIMER pin.

Internal circuitry guarantees that the TIMER pin is pulled below 150mV (typical) before a delay cycle can begin.

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Electronic Circuit Breaker

The LTC2921/LTC2922's electronic circuit breaker protects against excessive current on V_{CC}. The circuit breaker trips when the SENSE pin falls more than 50mV below the V_{CC} pin for more than 1µs. When the breaker trips, the remote sense switches are opened and the PG and GATE pins are pulled to ground, disconnecting the supplies. An internal latch guarantees that the monitoring sequence cannot start until the breaker is reset. To reset the circuit breaker, cycle the V1 input below 0.5V(nom) for more than 150µs. V_{CC} falling below the undervoltage threshold also resets the breaker. After reset, the sequence returns to Step 1, awaiting valid monitor levels.

Figure 7 shows an equivalent schematic for the electronic circuit breaker function. Using Equation 8, set the circuit breaker by selecting R_{SENSE} to drop less than the minimum ΔV_{SENSE} at the desired trip current:

$$R_{SENSE} \leq \frac{\Delta V_{SENSE(MIN)}}{I_{LO(TRIP)}} \quad (8)$$

After selecting a resistor, use Equations 9a and 9b to calculate the actual minimum and maximum trip current threshold limits:

$$I_{TRIP(MIN)} = \frac{\Delta V_{SENSE(MIN)}}{R_{SENSE(MAX)}} \quad (9a)$$

$$I_{TRIP(MAX)} = \frac{\Delta V_{SENSE(MAX)}}{R_{SENSE(MIN)}} \quad (9b)$$

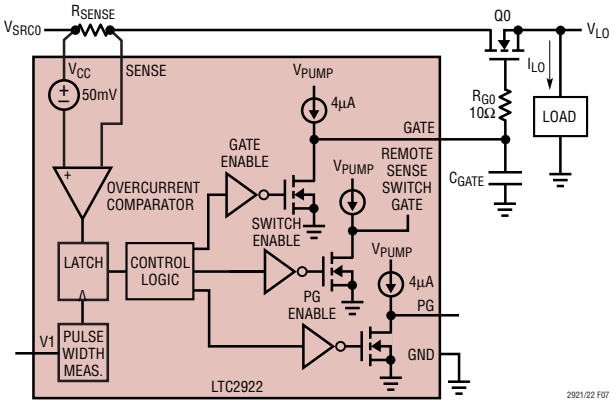

Figure 7. Circuit Breaker Functional Schematic

Be mindful of thermal effects and power ratings when choosing a resistor. Place R_{SENSE} as close as possible to the LTC2921/LTC2922 pins to reduce noise pickup, and use Kelvin sensing to ensure accurate measurement of the voltage drop. In applications not requiring the current sensing circuit breaker, tie the SENSE pin to the V_{CC} pin.

Configuring the PG Pin Output

The LTC2921 and LTC2922 each include a power good indicator, the PG pin. During the turn-on sequence, and upon detection of errors, a strong FET pulls PG to ground with >10mA of current. When all supplies have satisfied their monitor and overvoltage thresholds, the circuit breaker has not tripped, the GATE pin has reached its peak, and the remote sense switches have turned on, a 4µA current source from V_{PUMP} pulls up PG.

Configure PG as a logic signal by adding an external pull-up resistor to a voltage source. For example, create a negative-logic system reset signal by adding an external pull-up resistor to the load side of a supply voltage, as in Figure 8. Calculate the minimum pull-up resistor value that meets the output low voltage specification for $V_{PG(OL)}$:

$$R_{PG(MIN)} = \frac{V_{LO(MAX)} - 0.4V}{5mA} \quad (10)$$

Do not pull PG above the GATE pin's fully ramped voltage. An internal clamp limits the PG voltage to ≤12.2V relative to ground. In applications that do not require the PG output, leave the pin unconnected.

The PG output can also be used as the gate drive for external N-channel MOSFETs, as in Figure 9. The delay between the GATE ramp and the PG activation makes a supply sequencer, useful when two supplies (or two groups of supplies) need to be ramped one after another. Choose the FETs and design the ramp rate in the same way as for the GATE pin. Refer to Equations 5 and 6, substituting 4µA for 10µA, to choose capacitor C_{PG}.

Integrated Switches for Remote Sensing

A significant feature of the LTC2921/LTC2922 series is a set of remote sense switches that allow for compensation of voltage drops in the load path. Switch activation occurs in the turn-on sequence after the GATE

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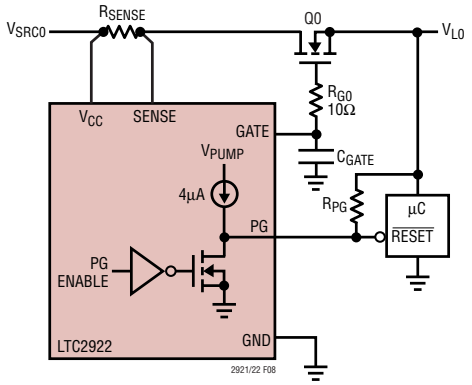

Figure 8. PG Pin as Logic Output

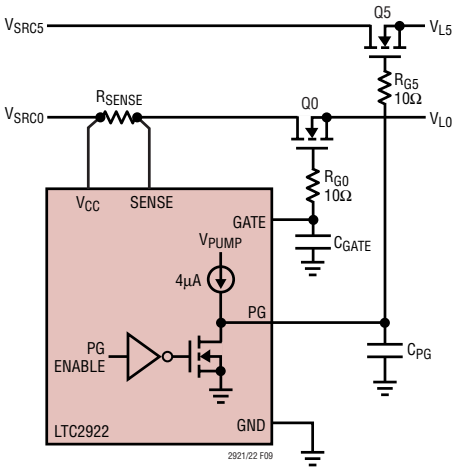

Figure 9. PG Pin as Sequenced N-Channel Gate Driver

pin has fully ramped up. The switches are N-channel MOSFETs whose gates are ramped from ground to V_{PUMP} at a nominal rate of 8V/ms. The PG pin is activated upon completion of the TIMER delay cycle that follows GATE ramp-up and remote sense switch activation. When conditions indicate a supply disconnect, the switches shut off in less than 10µs.

Figure 10 shows an example of how to connect a switch to remote sense the load voltage. Although only one remote sense switch is referred to in this section, the calculations and comments apply to all.

Before the activation of Q1 and the internal switch, resistor R_{X1} provides a direct path between the DC/DC converter's output voltage and its feedback network (R_{Y1} and R_{Z1}). Once Q1 activates, the supply energizes the load. When the internal switch turns on, it provides a remote sense path between the load voltage and the converter's feedback network.

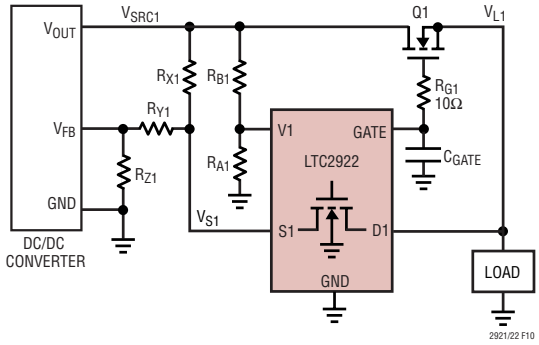

Figure 10. Automatic Remote Sense Switching Connection

To choose a value for resistor R_{X1}, consider the remote sense switch connection equivalent network in Figure 11. Resistor $R_{Q1(ON)}$ represents the on-resistance of Q1, and resistor $R_{FB1(ON)}$ represents the on-resistance of the internal switch.

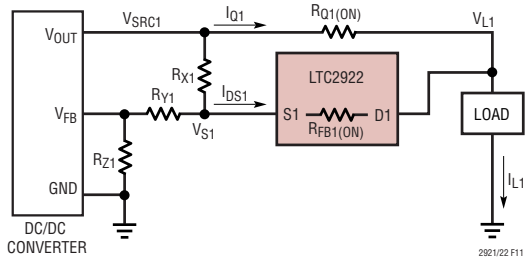

Figure 11. Remote Sense Switch Connection Equivalent Network

To allow the load voltage to dominate the feedback to the converter when the internal switch is closed, make $R_{X1} >> R_{FB1(ON)}$. To set the converter feedback ratio accurately with R_{Y1} and R_{Z1}, make both R_{X1} and $R_{FB1(ON)}$ much less than ($R_{Y1} + R_{Z1}$). To ensure that most of the load current flows through the external N-channel FET, choose ($R_{X1} + R_{FB1(ON)}$) >> $R_{Q1(ON)}$. Summarized, these requirements amount to:

$$R_{Q1(ON)}, R_{FB(ON)} << R_{X1} << (R_{Y1} + R_{Z1}) \quad (11)$$

Approach the selection of R_{X1} in the following way: design the DC/DC converter feedback based on the resistive divider formed by R_{Y1} and R_{Z1} with V_{S1} at the desired supply voltage value. When the resistor values satisfy Equation 11, Equations 12 through 15 are valid.

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Before Q1 closes to connect the load, the actual supply voltage relative to V_{S1} is given by Equation 12.

$$\Delta V_{SRC1} = V_{SRC1} - V_{S1} = V_{S1} \bullet \left(\frac{R_{X1}}{R_{X1} + R_{Y1} + R_{Z1}} \right) \quad (12)$$

After both Q1 and the internal remote sense switch have closed, the load voltage relative to V_{S1} is given by Equation 13.

$$\Delta V_{L1} = V_{L1} - V_{S1} = -I_{L1} \bullet R_{Q1(ON)} \bullet \left(\frac{R_{FB1(ON)}}{R_{X1}} \right) \quad (13)$$

A small part of the load current will flow through the remote sense switch. Use Equation 14 to calculate the current, and do not exceed the switch current Absolute Maximum Rating when choosing the value of R_{X1}.

$$I_{DS1} = I_{L1} \bullet \left(\frac{R_{Q1(ON)}}{R_{X1}} \right) \quad (14)$$

In addition, once the remote sensing is active, the supply voltage V_{SRC1} will rise by approximately the drop across the external FET. The effect on the monitor resistive divider design has already been accounted for in the previous section, Setting the Supply Monitor Levels.

$$V_{SRC1} = V_{S1} + I_{L1} \bullet R_{Q1(ON)} \bullet \left(1 - \frac{R_{FB1(ON)}}{R_{X1}} \right) \approx V_{S1} + V_{Q1(ON)} \quad (15)$$

The terminals of each switch are interchangeable; choose the connections to optimize the board layout. Ground all unused switch pins.

Design Example

Consider the design of a three-supply monitoring system, as shown in Figure 12, with specifications as listed in Table 1.

Table 1. Design Example Electrical Specifications

Supply Specifications		
5V ± 7.5%	$V_{SRC0(MAX)}$ = 5.375V $V_{SRC0(MIN)}$ = 4.625V	I_{L0} = 0.8A (max)
3.3V ± 7.5%	$V_{SRC1(MAX)}$ = 3.5475V $V_{SRC1(MIN)}$ = 3.0525V	I_{L1} = 1.6A (max)
2.5V ± 7.5%	$V_{SRC2(MAX)}$ = 2.6875V $V_{SRC2(MIN)}$ = 2.3125V	I_{L2} = 0.4A (max)
External N-channel FET Drain-Source Voltage Specification		
5V Supply	$V_{Q0(ON)(MAX)}$ < 250mV	
3.3V Supply	$V_{Q1(ON)(MAX)}$ < 250mV	
2.5V Supply	$V_{Q2(ON)(MAX)}$ < 150mV	
Timing Specification		
TIMER Delay	t_{DLY} = 150ms (nom)	
GATE Ramp Time	t_{RAMP} = 500ms (nom)	
Bias Current Specification		
Monitor Resistive Divider Current	I_{A1}= 10µA (nom) I_{A2} = 10µA (nom)	
Other Requirements		
• Remote Sense all 3 Load Voltages • Tight Monitoring Levels • Use Circuit Breaker Function • DC/DC Converter Feedback Resistive Divider >100kΩ		

The LTC2921 suits this application because the largest supply in the system is 5V, and only three remote sense switches are required.

Start with the design of the resistive dividers that set the monitor levels. As the largest supply voltage, the 5V supply must be connected to the V_{CC} pin; an internal resistive divider sets that monitor level. Consult the Electrical Characteristics table to confirm that $V_{SRC0(MIN)} > V_{CC(MON)(MAX)}$ and $V_{SRC0(MAX)} < V_{CC(OV)(MIN)}$.

The bias current in the lower resistor for the 3.3V supply's dividers yields a standard 1% value of R_{A1} = 49.9k:

$$R_{A1} = \frac{0.500V}{10\mu A} = 50k \approx 49.9k$$

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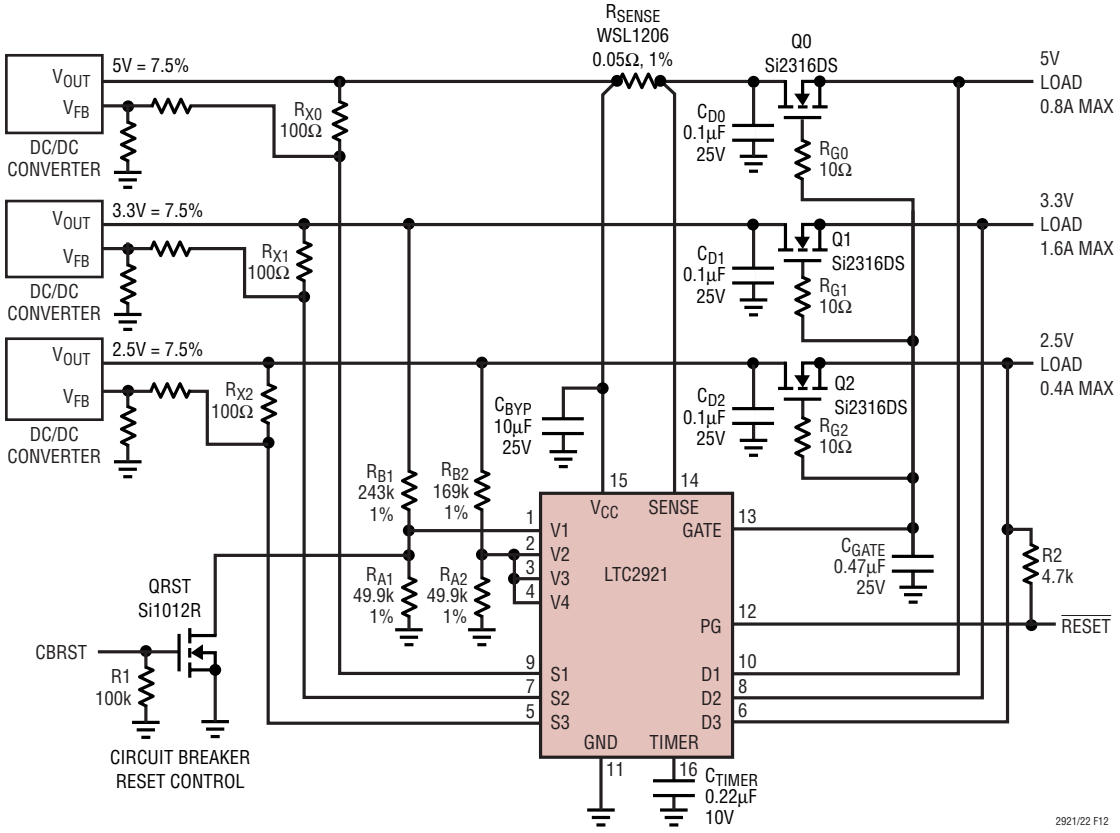

Figure 12. Design Example of a Three-Supply Tracker and Monitor (5V, 3.3V, 2.5V)

Selecting R_{B1} = 243k satisfies the range restrictions below:

$$R_{B1(MAX)} = 49.9k \bullet \left(\frac{1-0.01}{1+0.01}\right) \bullet \left(\frac{3.0525V - 0.505V}{0.505V + 0.1\mu A \bullet 49.9k}\right) = 244.3k$$

$$R_{B1(MIN)} = 49.9k \bullet \left(\frac{1+0.01}{1-0.01}\right) \bullet \left(\frac{3.5475V + 0.250V - 0.665V}{0.665V - 0.1\mu A \bullet 49.9k}\right) = 241.6k$$

Similar calculations for the 2.5V supply yield suitable standard 1% values of R_{A2} = 49.9k and R_{B2} = 169k.

$$R_{A2} = \frac{0.500V}{10\mu A} = 50k \approx 49.9k$$

$$R_{B2(MAX)} = 49.9k \bullet \left(\frac{1-0.01}{1+0.01}\right) \bullet \left(\frac{2.3125V - 0.505V}{0.505V + 0.1\mu A \bullet 49.9k}\right) = 173.3k$$

$$R_{B2(MIN)} = 49.9k \bullet \left(\frac{1+0.01}{1-0.01}\right) \bullet \left(\frac{2.6875V + 0.150V - 0.665V}{0.665V - 0.1\mu A \bullet 49.9k}\right) = 167.6k$$

Tie the unused V3 and V4 monitor pins to V2 for proper operation.

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Next, consider the supply ramping N-channel MOSFETs Q0, Q1 and Q2. Transistor Q0 will have >4.5V of gate-source voltage, even at maximum supply voltage (5.375V) and minimum GATE pin voltage (10V). Considering the voltages, temperatures, and currents involved, the maximum on-resistance ($R_{Q(ON)(MAX)}$) of the Vishay Siliconix Si2316DS is about 150mΩ. Switches Q1 and Q2 will see even higher gate-source voltages, implying even smaller $R_{Q(ON)(MAX)}$ values. Table 2 summarizes the calculated $V_{Q(ON)(MAX)}$ voltages. Include the additional 50mV drop across R_{SENSE} when budgeting for the V_{CC} supply path.

Table 2. External MOSFET Drain-Source Voltage Drops

Supply Voltage	External MOSFET	$R_{Q(ON)}$ Max	I_L Max	$V_{Q(ON)}$ Max
5V	Q0	~150mΩ	0.8A	120mV (+50mV = 170mV)
3.3V	Q1	<150mΩ	1.6A	<240mV
2.5V	Q2	<150mΩ	0.4A	<60mV

The ±20V absolute maximum gate-source voltage rating of the Si2316DS easily accommodates this design.

Next, calculate the necessary capacitance on the GATE pin to realize the desired ramp rate. Use the nominal value of V_{GATE} from the Electrical Specification, and choose a standard value.

$$C_{GATE} = \frac{10\mu A \bullet 500ms}{10.8V} = 0.463\mu F \approx 0.47\mu F$$

Include drain bypass capacitors of 0.1µF and series gate resistors of 10Ω on each external power FET to damp turn-on oscillations.

Find the capacitance at the TIMER pin required to set the delays in the power-on sequence:

$$C_{TIMER} = \frac{2\mu A}{1.2V} \bullet 150ms = 0.25\mu F \approx 0.22\mu F$$

The application requires the use of the circuit breaker function on the V_{CC} supply. First, find the upper limit on the sense resistor value:

$$R_{SENSE} \leq \frac{45mV}{0.8A} = 53.25m\Omega$$

Select a precision power sense resistor, such as the Vishay Dale WSL1206 series. They can be specified to 1%, and exhibit <1% variation over the LTC2921/LTC2922 operating range; choose R_{SENSE} = 50mΩ. Including tolerances, the circuit breaker trip current threshold variation will be:

$$I_{TRIP(MIN)} = \frac{45mV}{51m\Omega} = 0.88A$$

$$I_{TRIP(MAX)} = \frac{55mV}{49m\Omega} = 1.12A$$

The PG pin is configured as a 2.5V negative-logic reset signal for the microcontroller. The minimum pull-up resistance for proper operation is:

$$R_{PG(MIN)} = \frac{2.6875V - 0.4V}{5mA} \approx 460\Omega$$

Figure 13 shows R_{PG} = 4.7k. The value is somewhat arbitrarily chosen, but it does limit the pull-down current to <500µA. Trade off lower pull-down currents against faster pull-up edge rates in other applications.

Recall that proper operation of the remote load sensing function requires:

$$R_{Q(ON)}, R_{FB(ON)} << R_X << (R_Y + R_Z)$$

In this example, the operating conditions and the Si2316DS give $R_{Q(ON)(MAX)}$ = 150mΩ, the Electrical Characteristics table guarantees $R_{FB(ON)}$ < 10Ω, and the example design specification requires that (R_Y + R_Z) <100k. Selecting R_{X0} = R_{X1} = R_{X2} = 100Ω satisfies the inequality.

Before the loads are connected to the supplies, the voltage error due to the R_X resistors will be <0.1% for all three supplies:

$$\Delta V_{SRC} = V_{SRC} \bullet \left(\frac{100\Omega}{100k}\right) = \frac{V_{SRC}}{1000} = 0.1\% \text{ of } V_{SRC}$$

After the remote sense switches close, the load voltage errors due to R_X at maximum loads will be:

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$$\Delta V_{L0} = -0.8A \bullet 150m\Omega \bullet \left(\frac{10\Omega}{100\Omega}\right) = -12mV$$

$$= -0.24\% \text{ of } 5V$$

$$\Delta V_{L1} = -1.6A \bullet 150m\Omega \bullet \left(\frac{10\Omega}{100\Omega}\right) = -24mV$$

$$= -0.73\% \text{ of } 3.3V$$

$$\Delta V_{L2} = -0.4A \bullet 150m\Omega \bullet \left(\frac{10\Omega}{100\Omega}\right) = -6mV$$

$$= -0.24\% \text{ of } 2.5V$$

Confirm that the currents through the remote sense switches are less than the Absolute Maximum Ratings:

$$I_{DS1} = 0.8A \bullet \left(\frac{150m\Omega}{100\Omega}\right) = 1.2mA$$

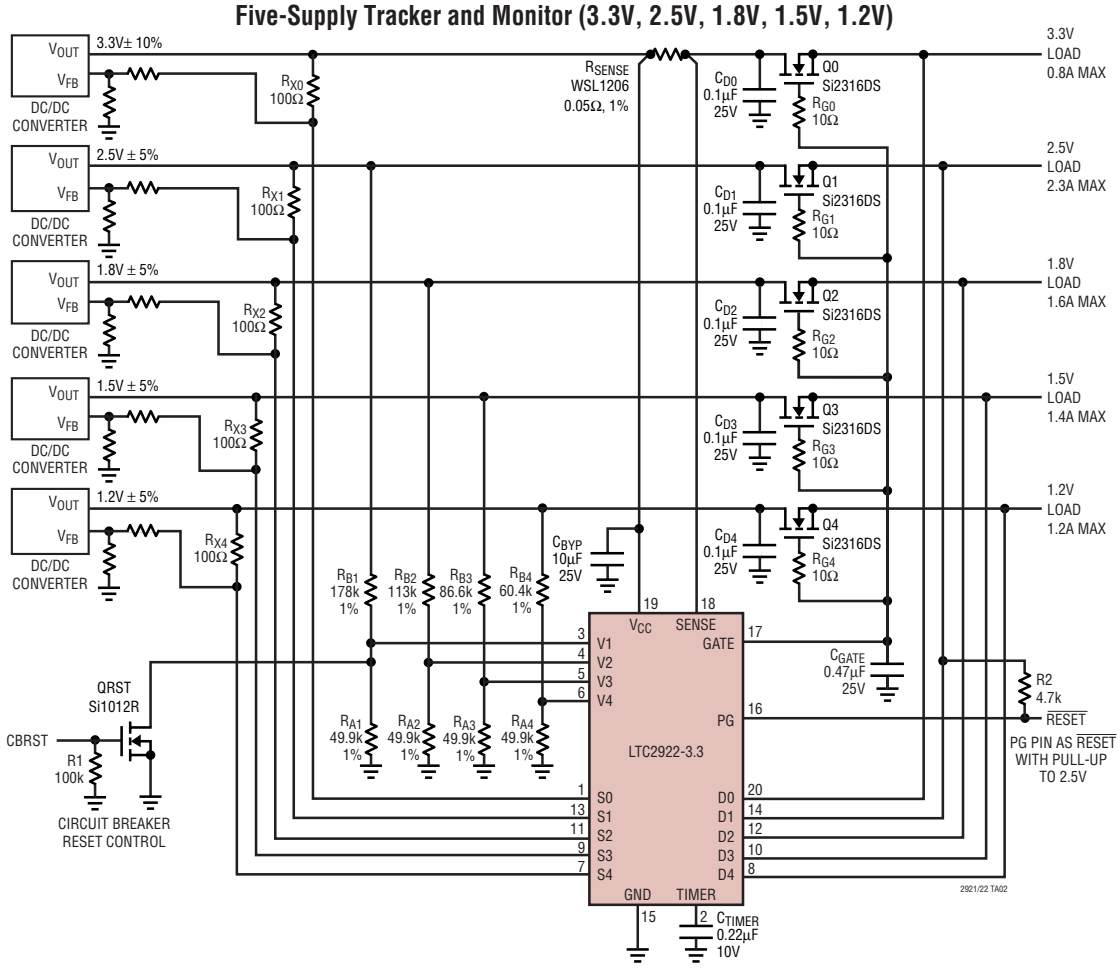
$$I_{DS2} = 1.6A \bullet \left(\frac{150m\Omega}{100\Omega}\right) = 2.4mA$$

$$I_{DS3} = 0.4A \bullet \left(\frac{150m\Omega}{100\Omega}\right) = 0.6mA$$

The pull-down transistor Q5 on the V1 pin is a circuit breaker reset mechanism. Choose the transistor to pull down V_{V1} below the reset threshold under worst-case conditions, and choose a gate-grounding resistor based on speed and current considerations. The Vishay Siliconix Si1012R and a 100k resistor proved sufficient for this design. Finally, bypass the V_{CC} pin with a 10µF capacitor.

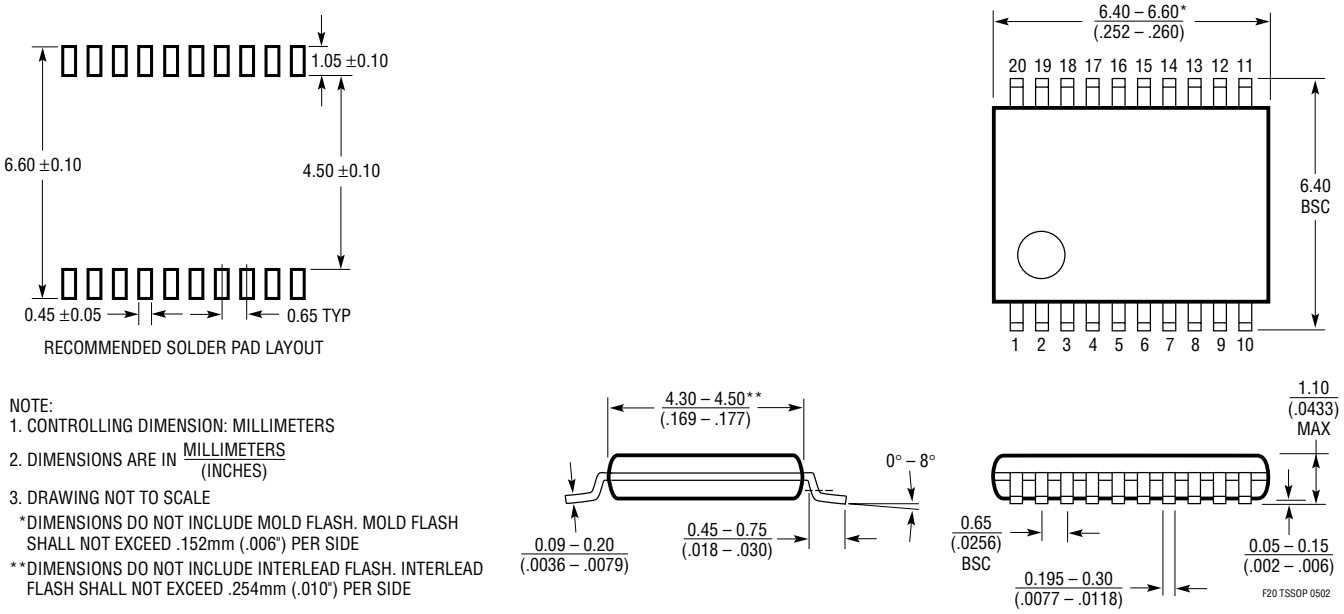
TYPICAL APPLICATIONS

Five-Supply Tracker and Monitor (3.3V, 2.5V, 1.8V, 1.5V, 1.2V)



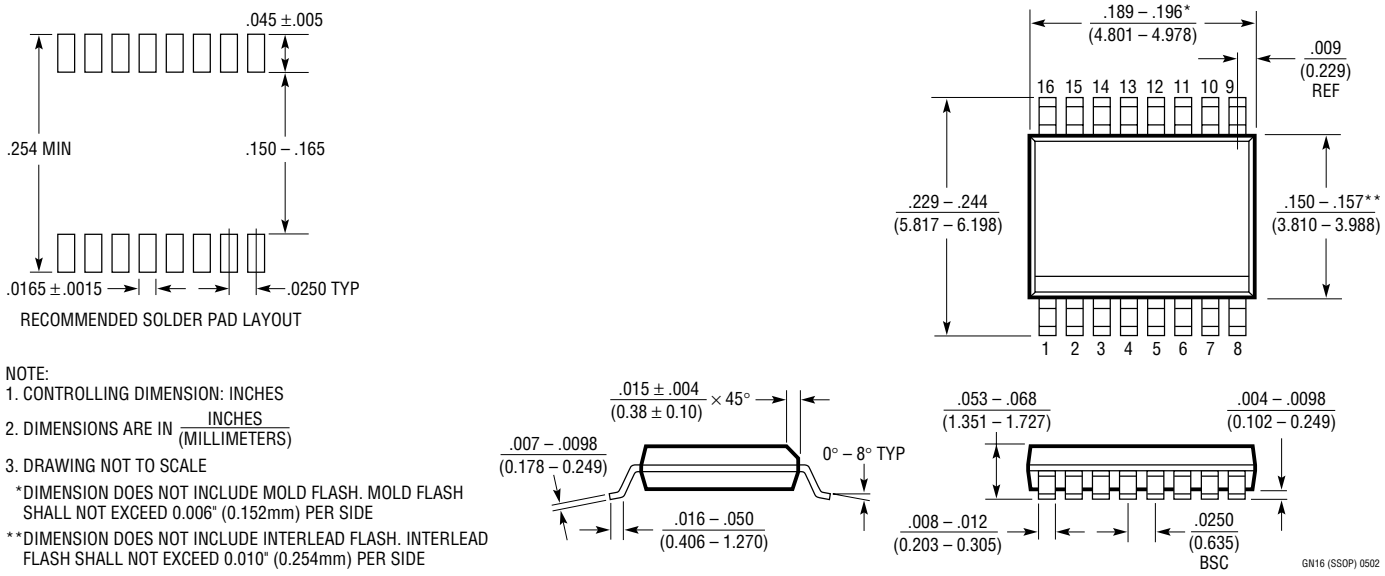
PACKAGE DESCRIPTION

F Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1650)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE