Single Power Supply Tracking Controller

FEATURES

- **Flexible Power Supply Tracking**
- **Tracks Both Up and Down**
- **Power Supply Sequencing**
- **Supply Stability is Not Affected**
- **Low Pin Count**
- Controls Single Supply without Series FETs
- Adjustable Ramp Rate
- Supply Shutdown Output
- Available in 8-Lead ThinSOT™ and 8-Lead (3mm × 2mm) DFN Packages

APPLICATIONS

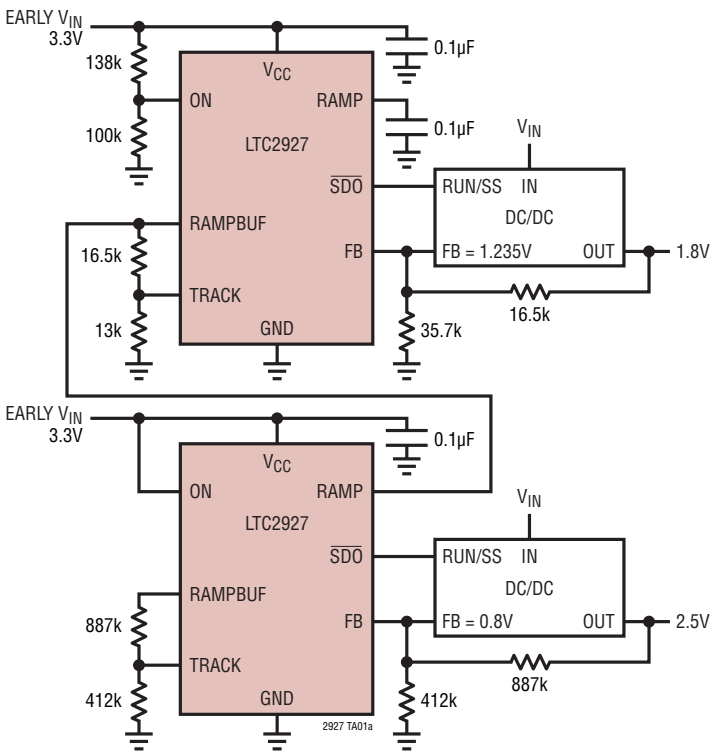
- V_{CORE} and $V_{I/O}$ Supply Tracking
- Microprocessor, DSP and FPGA Supplies
- Multiple Supply Systems
- Point-of-Load Supplies

DESCRIPTION

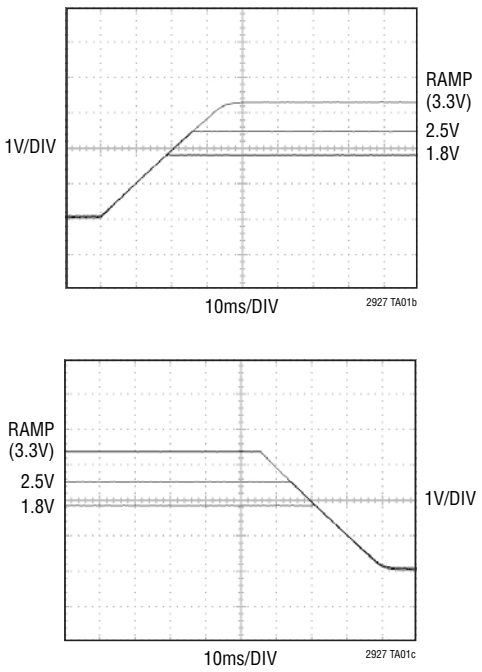
The LTC®2927 provides a simple solution to power supply tracking and sequencing requirements. By selecting a few resistors, the supply can be configured to ramp-up and ramp-down with differing ramp rates, voltage offsets, or time delays relative to other supplies or a master signal.

By forcing current into a feedback node of an independent supply, the LTC2927 causes the output to track a ramp signal without inserting any pass element losses. Because the current is controlled in an open-loop manner, the LTC2927 does not affect the transient response or stability of the supply. The compact solution at point of load minimizes the trace length of the DC/DC circuit sensitive FB node. Furthermore, it presents a high impedance when power-up is complete, effectively removing it from the DC/DC circuit.

TYPICAL APPLICATION



Track-Up and Track-Down Waveforms

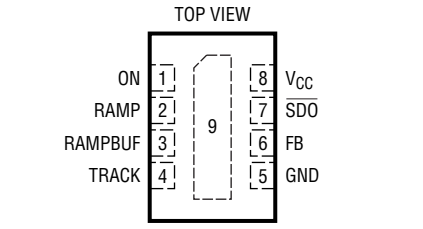


ABSOLUTE MAXIMUM RATINGS (Note 1)

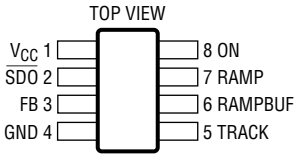
Supply Voltage (V_{CC}) ..... –0.3V to 10V
Input Voltages
ON ..... –0.3V to 10V
TRACK .....–0.3V to V_{CC} + 0.3V
Output Voltages
FB, $\overline{SDO}$ ..... –0.3V to 10V
RAMP, RAMPBUF.....–0.3V to V_{CC} + 0.3V

Average Current
TRACK 5mA
FB 5mA
RAMPBUF.....5mA
Operating Temperature Range
LTC2927C ..... 0°C to 70°C
LTC2927I..... –40°C to 85°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
EXPOSED PAD (PIN 9) PCB GND, CONNECTION OPTIONAL
T_{JMAX} = 125°C, θ_{JA} = 76°C/W



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2927CDDB#PBF	LTC2927CDDB#TRPBF	LBQH	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2927IDDB#PBF	LTC2927IDDB#TRPBF	LBQH	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2927CTS8#PBF	LTC2927CTS8#TRPBF	LTBQJ	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2927ITS8#PBF	LTC2927ITS8#TRPBF	LTBQJ	8-Lead Plastic TSOT-23	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2927CDDB	LTC2927CDDB#TR	LBQH	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC2927IDDB	LTC2927IDDB#TR	LBQH	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2927CTS8	LTC2927CTS8#TR	LTBQJ	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2927ITS8	LTC2927ITS8#TR	LTBQJ	8-Lead Plastic TSOT-23	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.9V < V_{CC} < 5.5V unless otherwise noted (Note 2).

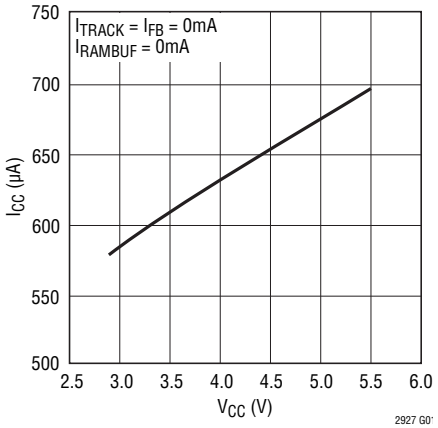
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.9		5.5	V
I_{CC}	Supply Current	I_{FB} = 0mA, I_{TRACK} = 0mA	●	0.25	0.56	1.2	mA
		I_{FB} = –1mA, I_{TRACK} = –1mA, $I_{RAMPBUF}$ = –1mA	●	3	3.6	4.2	mA
$V_{CC(UVLO)}$	Supply Undervoltage Lockout	V_{CC} Rising	●	2.2	2.5	2.7	V
$\Delta V_{CC(UVHYST)}$	Supply Undervoltage Lockout Hysteresis				25		mV
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	1.210	1.230	1.250	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	30	75	150	mV
I_{ON}	ON Pin Input Current	V_{ON} = 1.2V, V_{CC} = 5.5V	●		0	±100	nA
I_{RAMP}	RAMP Pin Input Current	0V < V_{RAMP} < V_{CC}, Ramp On		–9	–10	–11	µA
		0V < V_{RAMP} < V_{CC}, Ramp Off		9	10	11	µA
$V_{RAMPBUF(OL)}$	RAMPBUF Output Low Voltage	$I_{RAMPBUF}$ = 1mA	●		20	100	mV
$V_{RAMPBUF(OH)}$	RAMPBUF Output High Voltage, $V_{RAMPBUF(OH)}$ = V_{CC} – $V_{RAMPBUF}$	$I_{RAMPBUF}$ = –1mA	●		45	150	mV
V_{OS}	Ramp Buffer Offset, V_{OS} = $V_{RAMPBUF}$ – V_{RAMP}	V_{RAMP} = V_{CC}/2, $I_{RAMPBUF}$ = 0mA		–30	0	30	mV
$I_{ERROR(\%)}$	I_{FB} to I_{TRACK} Current Mismatch $I_{ERROR(\%)}$ = (I_{FB} – I_{TRACK})/I_{TRACK}	I_{TRACK} = –10µA	●		0	±5	%
		I_{TRACK} = –1mA	●		0	±5	%
V_{TRACK}	TRACK Pin Voltage	I_{TRACK} = –10µA	●	0.77	0.800	0.82	V
		I_{TRACK} = –1mA	●	0.77	0.800	0.82	V
$I_{FB(LEAK)}$	FB Pin Leakage Current	V_{FB} = 2V, V_{CC} = 5.5V	●		±1	±100	nA
$V_{FB(CLAMP)}$	FB Pin Clamp Voltage	1µA < I_{FB} < 1mA	●	1.5	2	2.3	V
$V_{\overline{SDO}(OL)}$	$\overline{SDO}$ Output Low Voltage	$I_{\overline{SDO}}$ = 1mA, V_{CC} = 2.3V	●		0.1	0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

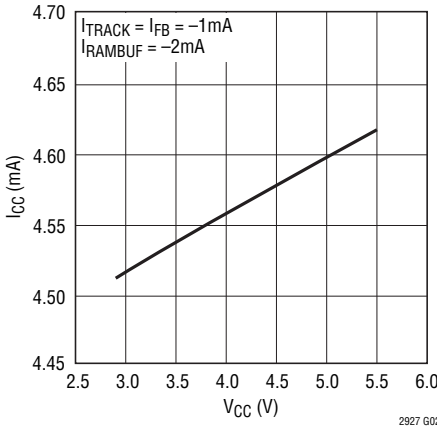
Note 2: All currents into the device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS

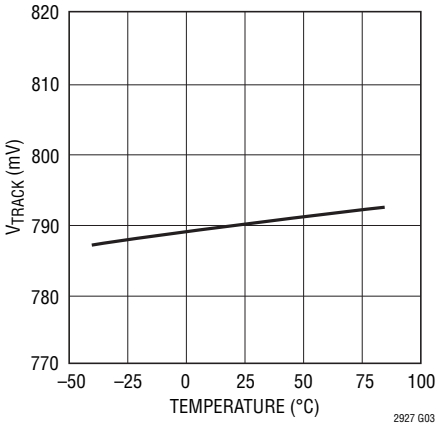
I_{CC} vs V_{CC}



I_{CC} vs V_{CC}

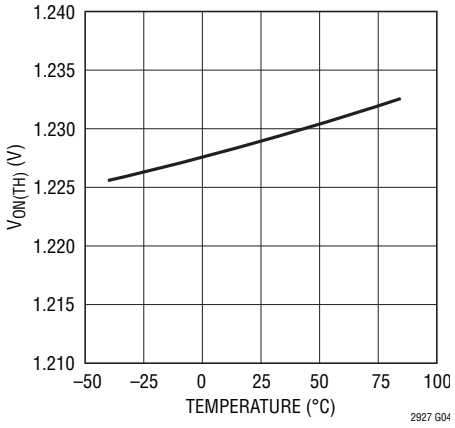


V_{TRACK} vs Temperature

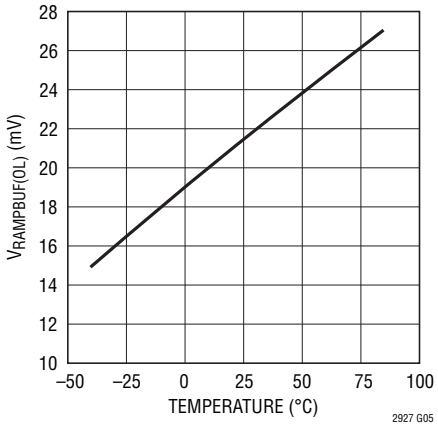


TYPICAL PERFORMANCE CHARACTERISTICS

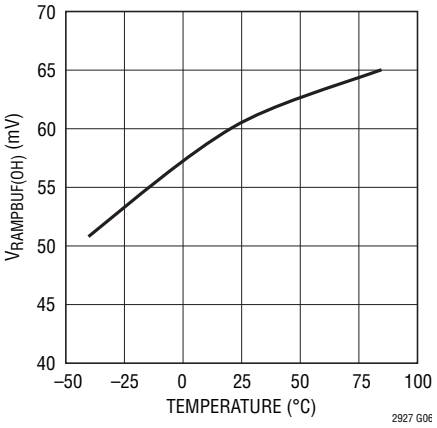
$V_{ON(TH)}$ vs Temperature



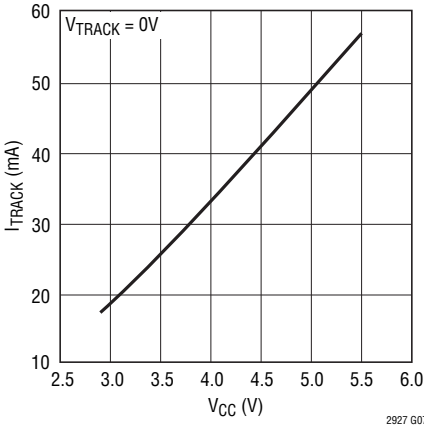
$V_{RAMPBUF(OL)}$ vs Temperature



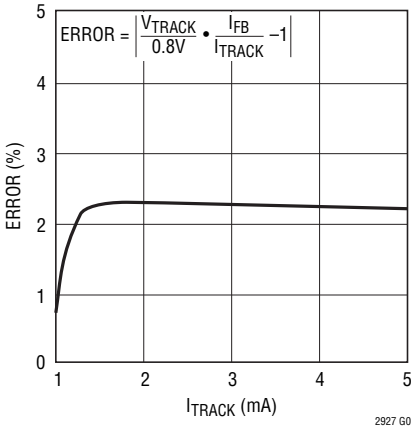
$V_{RAMPBUF(OH)}$ vs Temperature



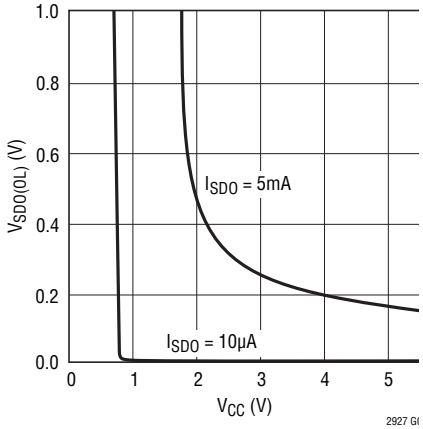
MAX I_{TRACK} vs V_{CC}



Tracking Cell Error vs I_{TRACK}



$V_{\overline{SDO}(OL)}$ vs V_{CC}



PIN FUNCTIONS TSOT/DFN Packages

V_{CC} (Pin 1/Pin 8): Supply Voltage Input. Operating range is from 2.9V to 5.5V. An undervoltage lockout asserts $\overline{SDO}$ until V_{CC} > 2.5V. V_{CC} should be bypassed to GND with a 0.1µF capacitor.

$\overline{SDO}$ (Pin 2/Pin 7): Slave Supply Shutdown Output. $\overline{SDO}$ is an open-drain output that holds the shutdown (RUN/SS) pin of the slave supply low until the V_{CC} pin is pulled above 2.5V, and the ON pin is pulled above 1.23V, or RAMP is above 200mV. $\overline{SDO}$ is pulled low again when both RAMP < 200mV and ON < 1.23V. If the slave supply is capable of operating with an input supply that is lower than the LTC2927's minimum operating voltage of 2.9V, the $\overline{SDO}$ pin can be used to hold off the slave supply. Tie the $\overline{SDO}$ pin to GND if unused.

FB (Pin 3/Pin 6): Feedback Control Output. FB pulls up on the feedback node of the slave supply. Tracking is achieved by mirroring the current from TRACK into FB. A resistive divider connecting RAMPBUF and TRACK will force the output voltage of the slave supply to track RAMP. To prevent damage to the slave supply, the FB pin will not force the slave's feedback node above 2.3V. In addition, the LTC2927 will not actively sink current from this node, even when it is unpowered.

PIN FUNCTIONS TSOT/DFN Packages

GND (Pin 4/Pin 5): Device Ground.

TRACK (Pin 5/Pin 4): Tracking Control Input. A resistive voltage divider between RAMPBUF and TRACK determines the tracking profile of the slave supply. TRACK servos to 0.8V, and the current supplied at TRACK is mirrored at FB. The TRACK pin is capable of supplying at least 1mA when V_{CC} = 2.9V. Under short circuit conditions, the TRACK pin is capable of supplying up to 70mA. Do not connect to GND for extended periods. Limit the capacitance at the TRACK pin to less than 25pF.

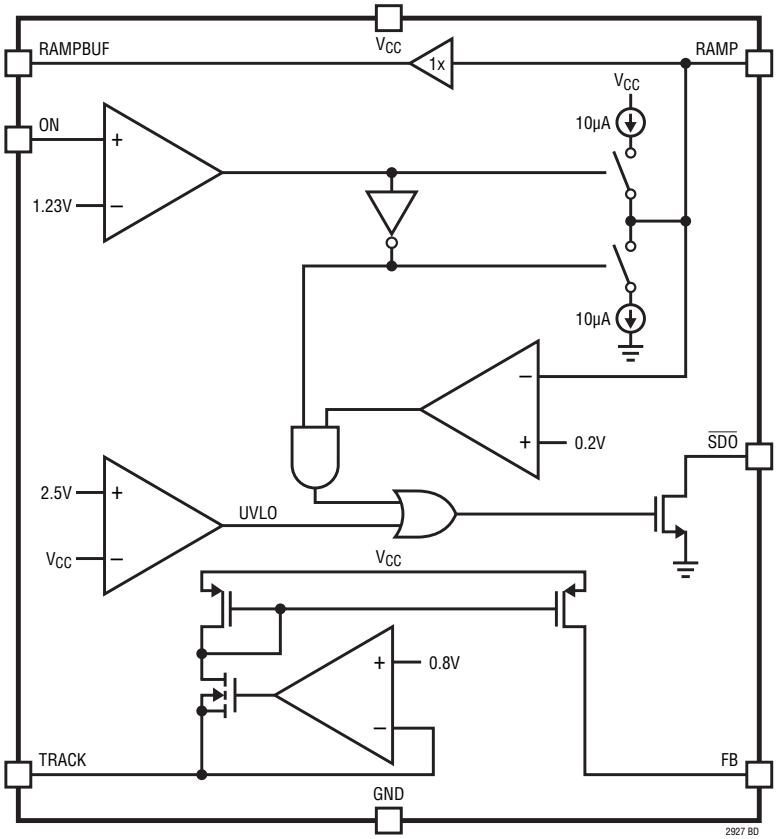
RAMPBUF (Pin 6/Pin 3): Ramp Buffer Output. Provides a low impedance buffered version of the signal on the RAMP pin. This buffered output drives the resistive voltage divider that connects to the TRACK pin. Limit the capacitance at the RAMPBUF pin to less than 100pF. Float RAMPBUF if unused.

RAMP (Pin 7/Pin 2): Ramp Buffer Input. The RAMP pin is the input to the voltage buffer whose output drives a resistive voltage divider connected to the TRACK pin. Connect this input to a capacitor to set the ramp voltage generated from internal 10µA pull-up or pull-down currents. RAMP can also be connected to an external ramping signal for tracking. Ground RAMP if unused.

ON (Pin 8/Pin 1): On Control Input. The voltage level of the ON pin relative to its 1.23V threshold (with 75mV hysteresis) controls the tracking direction of the LTC2927. An active high causes a 10µA pull-up current to flow at the RAMP pin, which charges an external capacitor. An active low at the ON pin causes a 10µA pull-down current at the RAMP pin to discharge the external capacitor relative to GND.

Exposed Pad (NA/Pin 9): Exposed pad may be left open or connected to device ground.

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

Power Supply Tracking and Sequencing

The LTC2927 handles a variety of power-up profiles to satisfy the requirements of digital logic circuits including FPGAs, PLDs, DSPs and microprocessors. These requirements fall into one of the four general categories illustrated in Figures 1 to 4.

Some applications require that the potential difference between two power supplies must never exceed a specified voltage. This requirement applies during power-up and power-down as well as during steady-state operation, often to prevent destructive latch-up in a dual supply ASIC. Typically, this is achieved by ramping the supplies up and down together (Figure 1). In other applications it is desirable to have supplies ramp up and down with fixed voltage offsets between them (Figure 2) or to have them ramp up and down ratiometrically (Figure 3).

Certain applications require one supply to come up after another. For example, a system clock may need to start before a block of logic. In this case, the supplies are sequenced as in Figure 4 where the 2.5V supply ramps up after the 1.8V supply is completely powered.

Operation

The LTC2927 provides a simple solution to all of the power supply tracking and sequencing profiles shown in Figures 1 to 4. A single LTC2927 controls a single supply that tracks to a "master" signal. With two resistors, a slave supply is configured to ramp up as a function of the master signal. This master signal can be a separate supply or it can be a ramp signal generated by tying the RAMP pin to an external capacitor.

Tracking Cell

The LTC2927's operation is based on the tracking cell shown in Figure 5, which uses a proprietary wide-range current mirror. The tracking cell shown in Figure 5 servos the TRACK pin at 0.8V. The current supplied by the TRACK

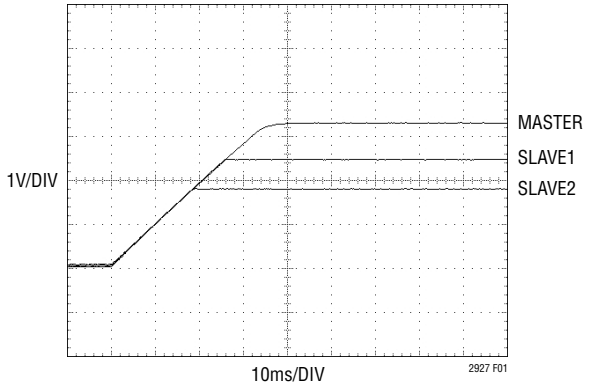


Figure 1. Coincident Tracking

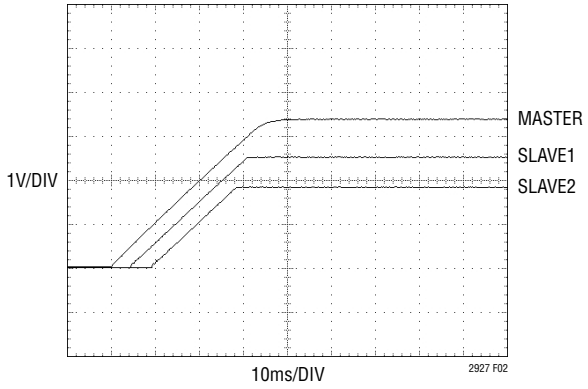


Figure 2. Offset Tracking

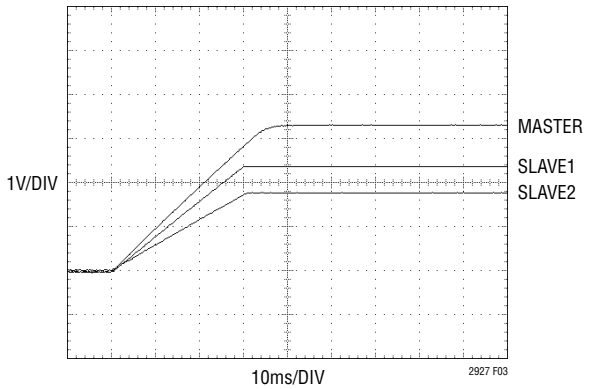


Figure 3. Ratiometric Tracking

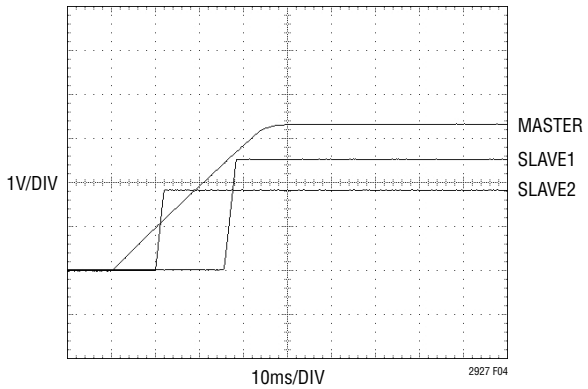


Figure 4. Supply Sequencing

APPLICATIONS INFORMATION

pin is mirrored at the FB pin to establish a voltage at the output of the slave supply. The slave output voltage varies with the master signal, enabling the slave supply to be controlled as a function of the master signal with terms set by R_{TA} and R_{TB}. By selecting appropriate values of R_{TA} and R_{TB}, it is possible to generate any of the profiles in Figures 1 to 4.

Controlling the Ramp-Up and Ramp-Down Behavior

The operation of the LTC2927 is most easily understood by referring to the simplified functional diagram in Figure 6. When the ON pin is low, the master signal at the RAMP pin is pulled to ground. Since the current through R_{TB} is at its maximum when the master signal is low, the current from FB is also at its maximum. This current drives the slave output to its minimum voltage.

When the ON pin rises above 1.23V, the master signal rises and the slave supply tracks the master signal. The ramp rate is set by an external capacitor driven by a 10µA current source at the RAMP pin. Alternatively, the RAMP pin can be connected to a separate supply to be used as the master signal.

In a properly designed system, when the master signal has reached its maximum voltage the current from the TRACK pin is zero. In this case, there is no current from the FB pin and the LTC2927 has no effect on the output voltage accuracy, transient response or stability of the slave supply.

When the ON pin falls below $V_{ON(TH)} – \Delta V_{ON(HYST)}$, typically 1.225V, the RAMP pin pulls down with 10µA and the master signal and slave supplies will fall at the same rate as they rose previously.

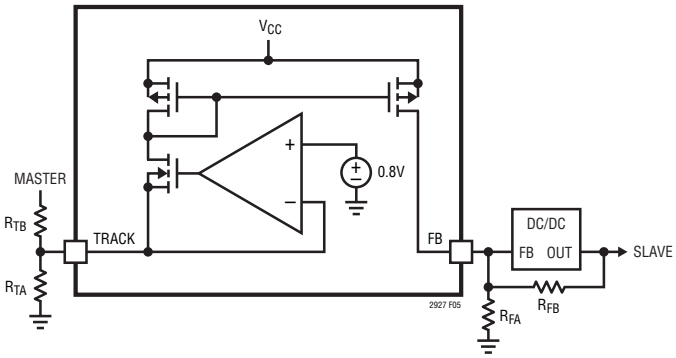


Figure 5. Simplified Tracking Cell

The ON pin can be controlled by a digital I/O pin or it can be used to monitor an input supply. By connecting a resistive divider from an input supply to the ON pin, the supplies will ramp up only after the monitored supply has reached a preset voltage.

If a resistive divider is used to set the ON pin voltage, choose values that will keep this voltage above the maximum ON pin threshold voltage of 1.25V at the lowest operating supply level.

The Ramp Buffer

The RAMPBUF pin provides a buffered version of the RAMP pin voltage that drives the resistive divider on the TRACK pin. The buffered master signal provides up to 2mA to drive the resistors.

Shutdown Output

In some applications it might be necessary to control the shutdown or RUN/SS pins of the slave supplies. The LTC2927 may not be able to supply the rated 1mA of current from the FB pin when V_{CC} is below 2.9V. If the slave power supply is capable of operating at low input voltages, use the open-drain $\overline{SDO}$ output to drive the SHDN or RUN/SS pin of the slave supply (see Figure 7). This will hold the slave supply output low until the ON pin is above 1.23V and V_{CC} is above the 2.5V undervoltage lockout condition.

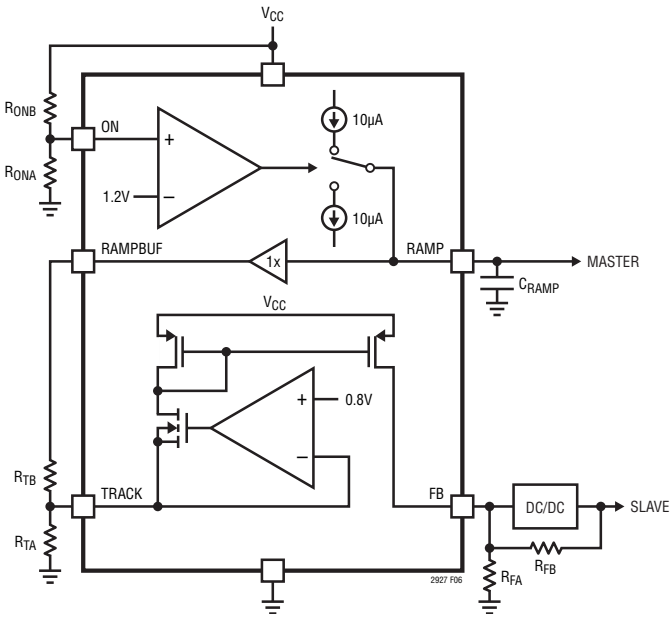


Figure 6. Simplified Functional Diagram

APPLICATIONS INFORMATION

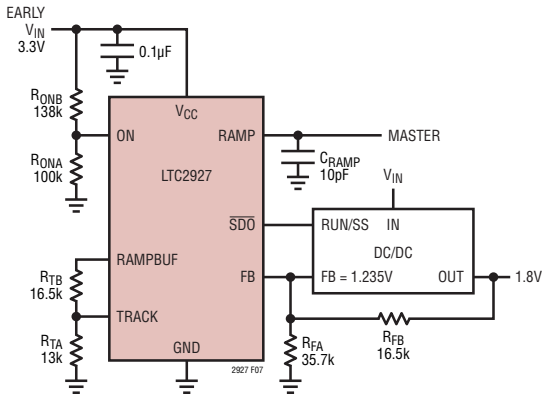


Figure 7. $\overline{SDO}$ Shutdown Application

$\overline{SDO}$ pulls low again when the ON pin is pulled below 1.23V and the RAMP pin is below about 200mV.

3-Step Design Procedure

The following 3-step procedure allows one to complete a design for any of the tracking or sequencing profiles shown in Figures 1 to 4. A basic single supply application circuit is shown in Figure 8.

1. Set the ramp rate of the master signal.

Solve for the value of C_{RAMP} the capacitor on the RAMP pin, based on the desired ramp rate (V/s) of the master supply, S_M.

$$C_{RAMP} = \frac{I_{RAMP}}{S_M} \text{ where } I_{RAMP} \approx 10\mu A \quad (1)$$

2. Solve for the pair of resistors that provide the desired ramp rate of the slave supply, assuming no delay.

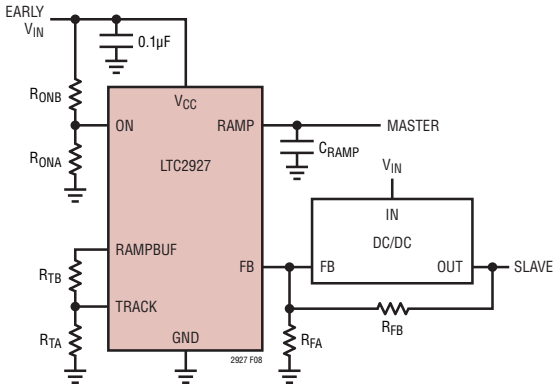


Figure 8. Single Supply Application

Choose a ramp rate for the slave supply, S_S. If the slave supply ramps up coincident with the master signal or with a fixed voltage offset, then the ramp rate equals the master supply's ramp rate. Be sure to use a fast enough ramp rate for the slave supply so that it will finish ramping before the master signal has reached its final supply value. If not, the slave supply will be held below the intended regulation value by the master signal. Use the following formulas to determine the resistor values for the desired ramp rate, where R_{FB} and R_{FA} are the feedback resistors in the slave supply and V_{FB} is the feedback reference voltage of the slave supply:

$$R_{TB} = R_{FB} \bullet \frac{S_M}{S_S} \quad (2)$$

$$R_{TA}' = \frac{V_{TRACK}}{\frac{V_{FB}}{R_{FB}} + \frac{V_{FB}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}}} \quad (3)$$

where $V_{TRACK} \approx 0.8V$.

Note that large ratios of slave ramp rate to master ramp rate, S_S/S_M, may result in negative values for R_{TA}'. If sufficiently large delay is used in step 3, R_{TA} will be positive, otherwise S_S/S_M must be reduced.

3. Choose R_{TA} to obtain the desired delay.

If no delay is required, such as in coincident and ratiometric tracking, then simply set $R_{TA} = R_{TA}'$. If a delay is desired, as in offset tracking and supply sequencing, calculate R_{TA}'' to determine the value of R_{TA} where t_D is the desired delay in seconds.

$$R_{TA}'' = \frac{V_{TRACK} \bullet R_{TB}}{t_D \bullet S_M} \quad (4)$$

$$R_{TA} = R_{TA}' \,||\, R_{TA}'' \quad (5)$$

the parallel combination of R_{TA}' and R_{TA}''.

As noted in step 2, small delays and large ratios of slave ramp rate to master ramp rate (usually only seen in sequencing) may result in solutions with negative values for R_{TA}. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced.

APPLICATIONS INFORMATION

Coincident Tracking Example

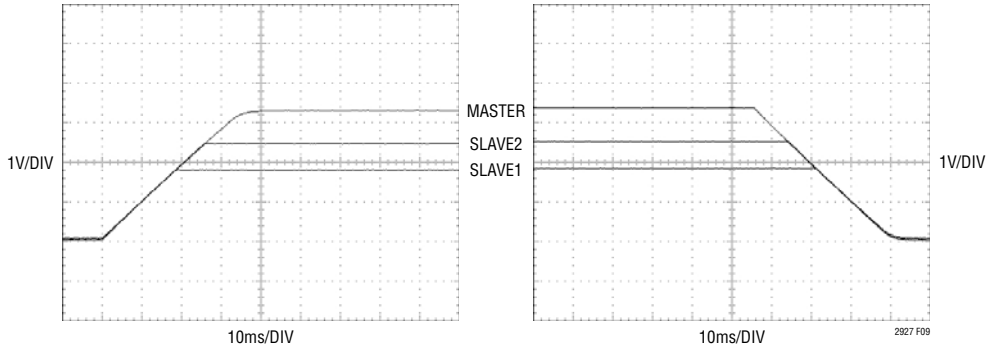


Figure 9. Coincident Tracking (from Figure 10)

A typical application is shown in Figure 10. The master signal is a 3.3V ramp generated by the LTC2927. The slave 1 supply is a 1.8V switching power supply and the slave 2 supply is a 2.5V switching power supply. Both slave supplies track coincidently with the 3.3V ramping master signal. The ramp rate of the supplies is 100V/s. The 3-step design procedure detailed previously can be used to determine component values. Only the slave 1 supply is considered here as the procedure is the same for the slave 2 supply.

1. *Set the ramp rate of the master signal.*

   From Equation 1:

$$C_{RAMP} = \frac{10\mu A}{100V/s} = 0.1\mu F$$

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

   From Equation 2:

$$R_{TB} = 16.5k\Omega \bullet \frac{100V/s}{100V/s} = 16.5k\Omega$$

   From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k\Omega} + \frac{1.235V}{35.7k\Omega} - \frac{0.8V}{16.5k\Omega}} \approx 13k\Omega$$

3. *Choose R_{TA} to obtain desired delay.*

   Since no delay is desired, $R_{TA} = R_{TA}'$

In this example, the supply remains low while the ON pin is held below 1.23V. When the ON pin rises above 1.23V, 10µA pulls up the master signal on C_{RAMP} at 100V/s. The master signal is buffered from the RAMP pin to the RAMPBUF pin. As this output and the RAMPBUF pin rise, the current from the TRACK pin is reduced. Consequently, the voltage at the slave supply's output is increased, and the slave supply tracks the master signal. When the ON pin is again pulled below 1.23V, 10µA will pull down C_{RAMP} at 100V/s. If the loads on the outputs are sufficient, all outputs will track down coincidently at 100V/s.

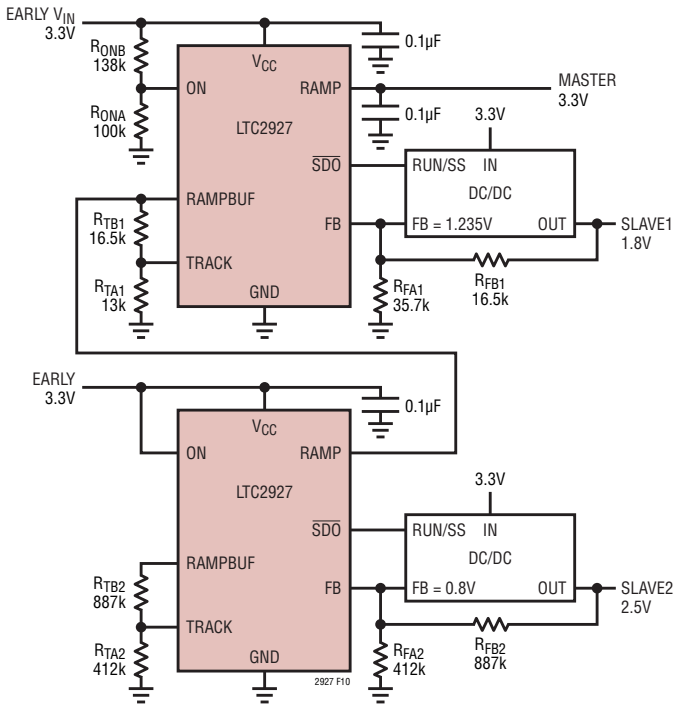


Figure 10. Coincident Tracking Example

APPLICATIONS INFORMATION

Ratiometric Tracking Example

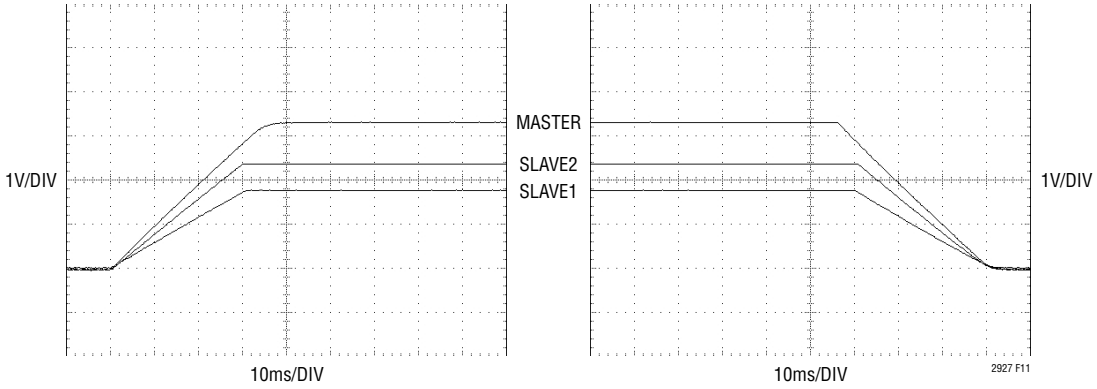


Figure 11. Ratiometric Tracking (from Figure 12)

This example converts the coincident tracking example to the ratiometric tracking profile shown in Figure 11. The ramp rate of the master signal remains unchanged (Step 1) and there is no delay in ratiometric tracking (Step 3), so only the result of step 2 in the 3-step design procedure needs to be considered. In this example, the ramp rate of the 1.8V slave 1 supply ramps up at 60V/s and the 2.5V slave 2 supply ramps up at 85V/s. Always verify that the chosen ramp rate will allow the supplies to ramp-up completely before RAMPBUF reaches V_{CC}. If the 1.8V supply were to ramp-up at 50V/s it would only reach 1.65V because the RAMPBUF signal would reach its final value of V_{CC} = 3.3V before the slave supply reached 1.8V.

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

From Equation 2:

$$R_{TB} = 16.5k\Omega \bullet \frac{100V/s}{60V/s} = 27.4k\Omega$$

From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k\Omega} + \frac{1.235V}{35.7k\Omega} - \frac{0.8V}{27.4k\Omega}} \approx 10k\Omega$$

Step 3 is unnecessary because there is no delay, so $R_{TA} = R_{TA}'$

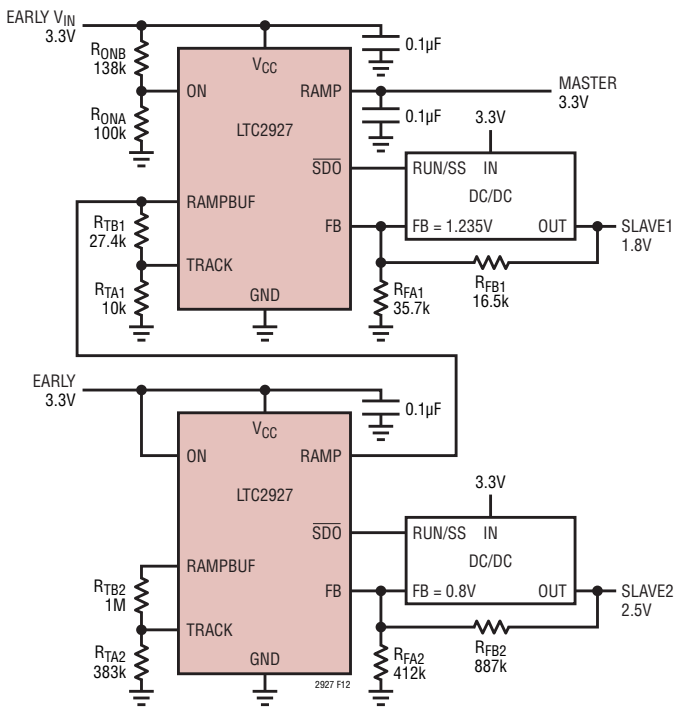


Figure 12. Ratiometric Tracking Example

APPLICATIONS INFORMATION

Offset Tracking Example

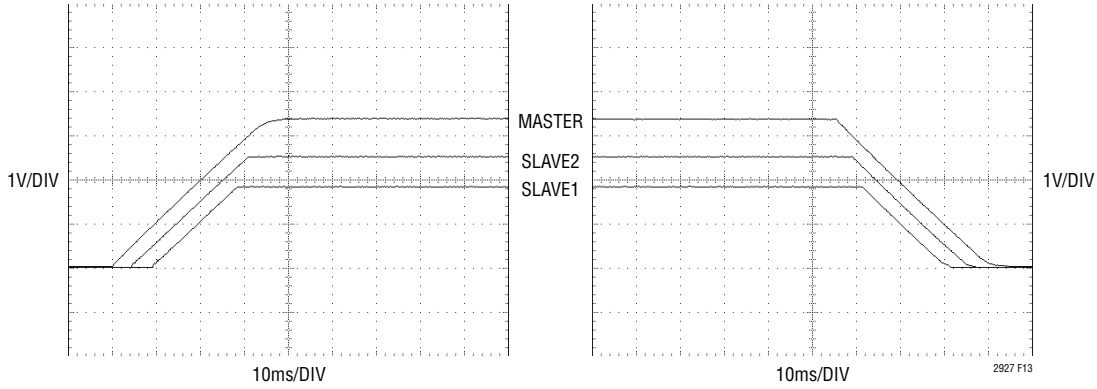


Figure 13. Offset Tracking (from Figure 14)

Converting the circuit in the coincident tracking example to the offset tracking shown in Figure 13 is relatively simple. Here the 1.8V slave 1 supply ramps up 1V below the master. The ramp rate remains the same (100V/s), so there are no changes necessary to steps 1 and 2 of the 3-step design procedure. Only step 3 must be considered. Be sure to verify that the chosen voltage offset will allow the slave supply to ramp up completely. In this example, if the voltage offset were 2V, the slave supply would only ramp to 3.3V – 2V = 1.3V.

3. *Choose R_{TA} to obtain desired delay.*

First, convert the desired voltage offset, V_{OS}, to a delay t_D, using the ramp rate:

$$t_D = \frac{V_{OS}}{S_S} = \frac{1V}{100V/s} = 10ms \quad (6)$$

From Equation 4:

$$R_{TA}'' = \frac{0.8V \bullet 16.5k\Omega}{10ms \bullet 100V/s} = 13.2k\Omega$$

From Equation 5:

$$R_{TA} = 13.1k\Omega \| 13.2k\Omega \approx 6.65k\Omega$$

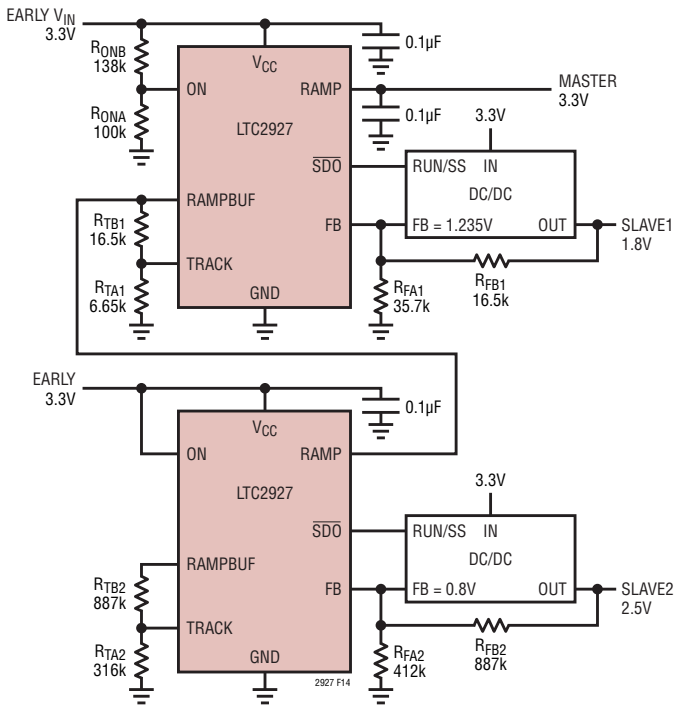


Figure 14. Offset Tracking Example

APPLICATIONS INFORMATION

Supply Sequencing Example

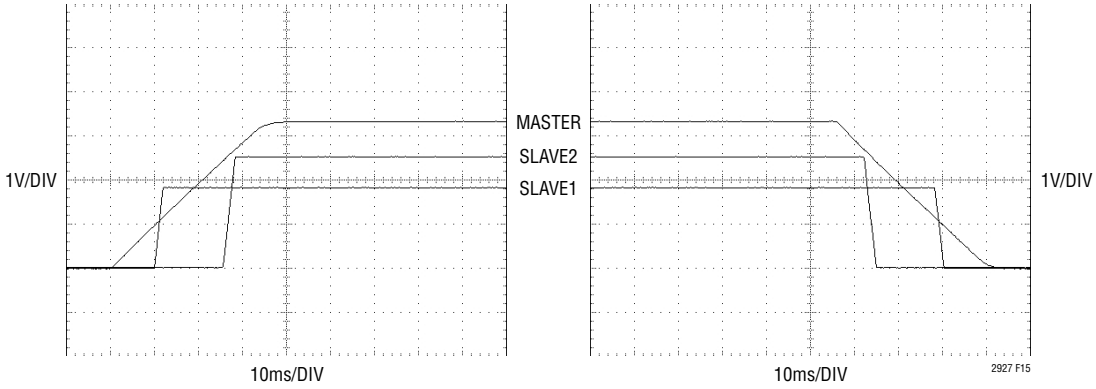


Figure 15. Supply Sequencing (from Figure 16)

In Figure 15, the slave 1 supply and the slave 2 supply are sequenced instead of tracking. The 3.3V master ramps up at 100V/s. The 1.8V slave 1 supply ramps up at 1000V/s beginning 10ms after the master signal starts to ramp up. The 2.5V slave 2 supply ramps up at 1000V/s beginning 25ms after the master signal begins to ramp up. Note that not every combination of ramp rates and delays is possible. Small delays and large ratios of slave ramp rate to master ramp rate may result in solutions that require negative resistors. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced. In this example, solving for the slave supply yields:

1. *Set the ramp rate of the master signal.*

   From Equation 1:

$$C_{RAMP} = \frac{10\mu A}{100V/s} = 0.1\mu F$$

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

$$R_{TB} = 16.5k\Omega \bullet \frac{100V/s}{1000V/s} = 1.65k\Omega$$

   From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k\Omega} + \frac{1.235V}{35.7k\Omega} - \frac{0.8V}{1.65k\Omega}} = -2.13k\Omega$$

3. *Choose R_{TA} to obtain desired delay.*

   From Equation 4:

$$R_{TA}'' = \frac{0.8V \bullet 1.65k\Omega}{10ms \bullet 100V/s} = 1.32k\Omega$$

   From Equation 5:

$$R_{TA} = -2.13k\Omega \| 1.32k\Omega = 3.48k\Omega$$

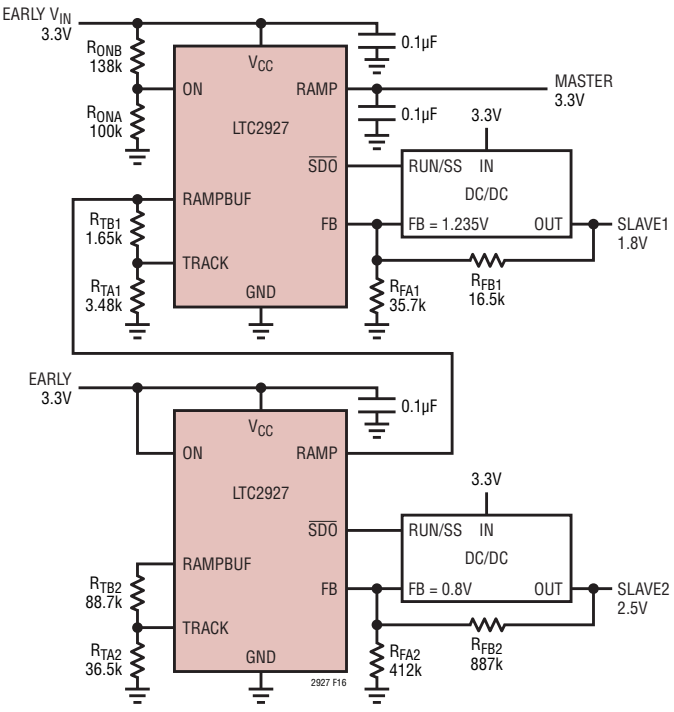


Figure 16. Supply Sequencing Example

APPLICATIONS INFORMATION

Final Sanity Checks

The collection of equations below is useful for identifying unrealizable solutions.

As stated in step 2, the slave supply must finish ramping before the master signal has reached its final voltage. This can be verified by the following equation:

$$V_{TRACK}\left(1+\frac{R_{TB}}{R_{TA}}\right) < V_{MASTER}$$

Here, V_{TRACK} = 0.8V. V_{MASTER} is the final voltage of the master signal (V_{CC} if RAMP pin).

It is possible to choose resistor values that require the LTC2927 to supply more current than the Electrical Characteristics table guarantees. To avoid this condition, check that I_{TRACK} does not exceed 1mA and $I_{RAMPBUF}$ does not exceed ±2mA.

To confirm that I_{TRACK} < 1mA, the TRACK pin's maximum guaranteed current, verify that:

$$\frac{V_{TRACK}}{R_{TA}\|R_{TB}} < 1mA$$

Finally, check that the RAMPBUF pin will not be forced to sink more than 2mA when it is at 0V or be forced to source more than 2mA when it is at V_{MASTER}.

$$\frac{V_{TRACK}}{R_{TB}} < 2mA \text{ and } \frac{V_{MASTER}}{R_{TA}+R_{TB}} < 2mA$$

ON Pin Resistive Divider

Check that the ON pin voltage is above the 1.25V maximum threshold at the lowest possible supply voltage value.

$$\frac{R_{ONB}}{R_{ONA}} < \frac{V_{CC(MIN)}}{1.25V} - 1$$

Also check that the supply voltage is above the minimum LTC2927 operating supply voltage of 2.9V before the ON pin is above the 1.21V minimum threshold voltage.

$$\frac{R_{ONB}}{R_{ONA}} < \frac{2.9V}{1.21V} - 1$$

For example, if the typical application shown on page 1 has a 3.3V ±10% V_{IN}, the lowest possible operating supply voltage will be 2.97.

$$\frac{R_{ONB}}{R_{ONA}} > \frac{2.97V}{1.25V} - 1 = 1.376$$

If R_{ONA} is 100k then R_{ONB} must be greater than 137.6k. Therefore, 138k is chosen. These values must be checked to ensure the supply reaches the LTC2927 minimum operating supply voltage of 2.9V before the ON pin is above the minimum threshold.

$$1.38 < \frac{2.9V}{1.21V} - 1 = 1.389$$

Load Requirements

When the supply is ramped down quickly, either the load or the supply itself must be capable of sinking enough current to support the ramp rate. For example, if there is a large output capacitance on the supply and a weak resistive load, supplies that do not sink current will have their falling ramp rate limited by the RC time constant of the load and the output capacitance. Figure 17 shows the case when the slave supply does not track the master near ground.

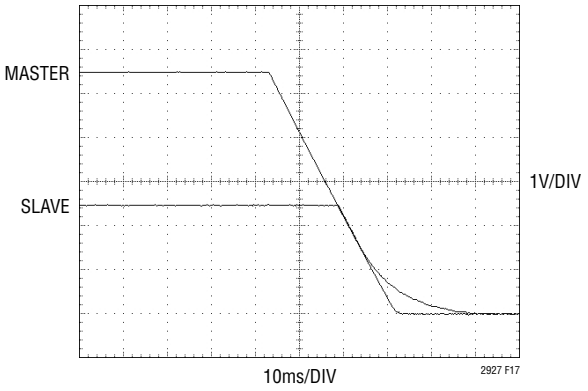


Figure 17. Weak Resistive Load

APPLICATIONS INFORMATION

Start-Up Delays

Often power supplies do not start-up immediately when their input supplies are applied. If the LTC2927 tries to ramp-up these power supplies as soon as the input supply is present, the start-up of the outputs may be delayed, defeating the tracking circuit (Figure 18). Often this delay is intentionally configured by a soft-start capacitor. This can be remedied either by reducing the soft-start capacitor on the slave supply or by including a capacitor in the ON pin's resistive divider to delay the ramp up. See Figure 19.

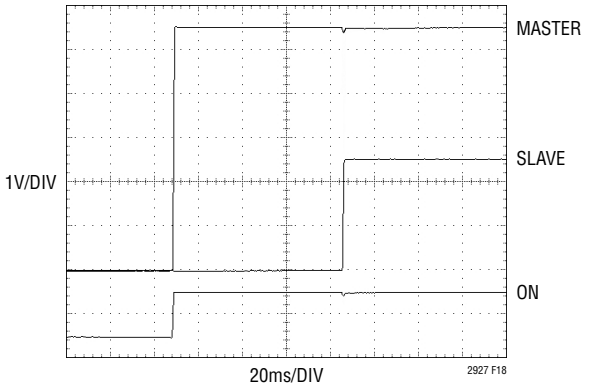


Figure 18. Power Supply Start-Up Delayed

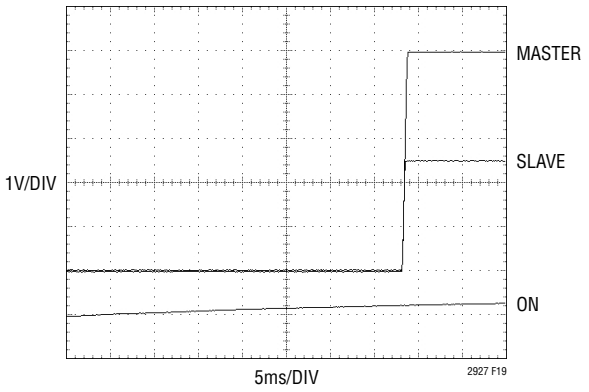


Figure 19. ON Pin Delayed

Layout Considerations

Be sure to place a 0.1µF bypass capacitor as near as possible to the supply pin of the LTC2927.

To minimize the noise on the slave supply's output, keep the trace connecting the FB pin of the LTC2927 and the feedback node of the slave supply as short as possible. In addition, do not route this trace next to signals with fast transition times. In some circumstances it might be advantageous to add a resistor near the feedback node of the slave supply in series with the FB pin of the LTC2927. This resistor must not exceed:

$$R_{SERIES} = \frac{1.5V - V_{FB}}{I_{MAX}} = \left(\frac{1.5V}{V_{FB}} - 1\right)\left(R_{FA} \| R_{FB}\right)$$

This resistor is most effective if there is already a capacitor at the feedback node of the slave supply (often a compensation component). Increasing the capacitance on a slave supply's feedback node will further improve the noise immunity, but could affect the stability and transient response of the supply.

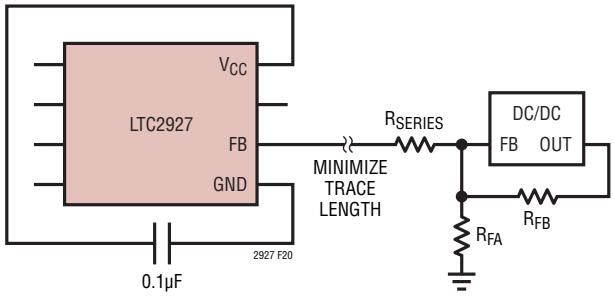
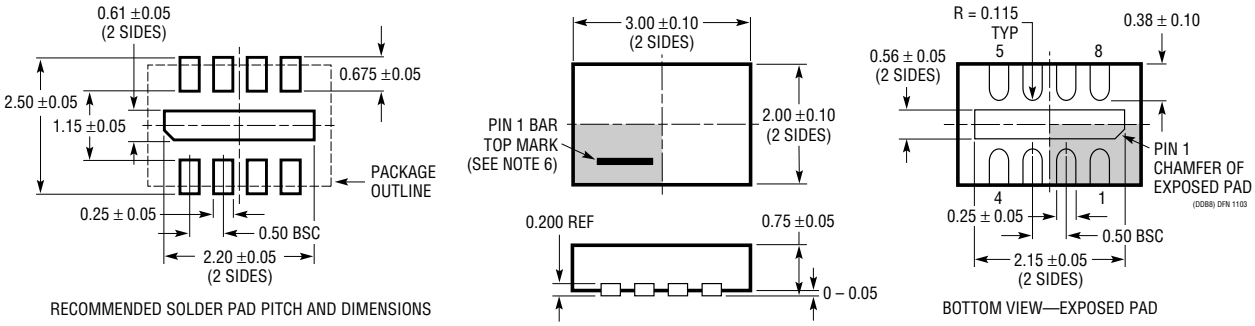


Figure 20. Layout Considerations

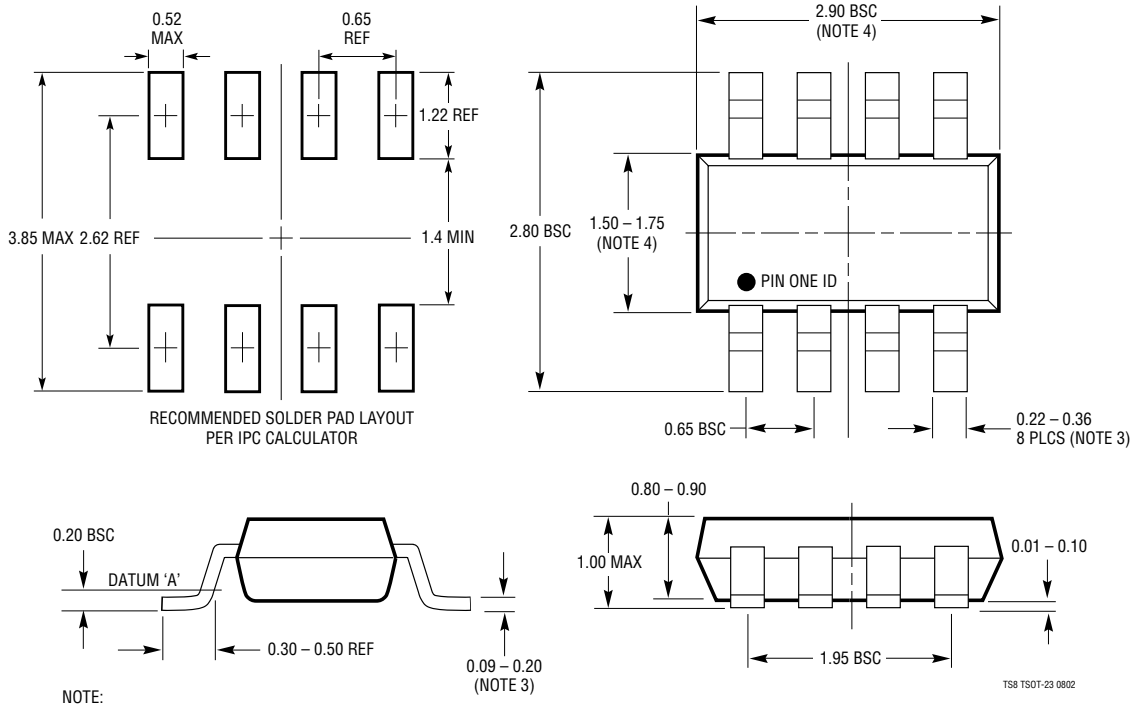
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193