Ultra-Low Power Supervisor with Power-Fail Output, Selectable Thresholds

FEATURES

- **500nA Quiescent Current**
- **±1.5% (Max) Accuracy over Temperature**
- **Integrated Precision Attenuators**
- **Eight Pin-Selectable Reset Thresholds**
- **Eight Pin-Selectable Power-Fail Thresholds**
- Early Warning Power-Fail Output
- 200ms Reset Timeout
- Manual Reset Input
- Compact 8-Lead, 2mm × 2mm DFN and TSOT-23 (ThinSOT™) Packages

APPLICATIONS

- Portable Equipment
- Battery-Powered Equipment
- Security Systems
- Point-of-Sale Devices
- Wireless Systems

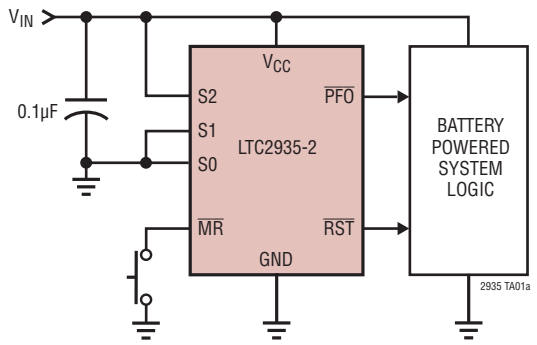
DESCRIPTION

The LTC®2935 ultra-low power voltage monitor provides system initialization, power-fail warning and reset generation functions. Low quiescent current (500nA typical) makes the LTC2935 an ideal choice for battery-operated applications.

Three binary threshold-select inputs configure one of eight integrated reset thresholds, ranging from 1.6V to 3.45V in pre-determined increments. Early warning of an impending low voltage condition is provided at the power-fail output ($\overline{PFO}$), whose threshold is above the configured reset threshold. Supervisory circuits monitor V_{CC} and pull $\overline{RST}$ low when V_{CC} drops below the configured reset threshold. When V_{CC} is rising from an under-threshold condition, an internal reset timer is started after exceeding the reset threshold by 5%. A 200ms reset timeout delays the return of the $\overline{RST}$ output to a high state. A pushbutton switch connected to the $\overline{MR}$ input is typically used to force a manual reset. Outputs $\overline{RST}$ and $\overline{PFO}$ are available with open-drain (LTC2935-1/LTC2935-3) or active pull-up (LTC2935-2/LTC2935-4) circuits. Operating temperature range is from –40°C to 85°C.

TYPICAL APPLICATION

Configurable Low Power Voltage Monitor



Falling Threshold Selection Table

LTC2935-1/LTC2935-2		LTC2935-3/LTC2935-4				
RESET THRESHOLD (V)	POWER-FAIL THRESHOLD (V)	RESET THRESHOLD (V)	POWER-FAIL THRESHOLD (V)	S2	S1	S0
3.30	3.45	2.44	2.56	Low	Low	Low
3.15	3.30	2.32	2.44	Low	Low	High
3.00	3.15	2.20	2.32	Low	High	High
2.85	3.00	2.08	2.20	Low	High	Low
2.70	2.85	1.96	2.08	High	High	Low
2.55	2.70	1.84	1.96	High	Low	Low
2.40	2.55	1.72	1.84	High	Low	High
2.25	2.40	1.60	1.72	High	High	High

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Input Voltages

V_{CC} ..... –0.3V to 6V

S2, S1, S0, $\overline{MR}$ ..... –0.3V to (V_{CC} + 0.3V)

Output Voltages ($\overline{PFO}$, $\overline{RST}$)

LTC2935-1/LTC2935-3 ..... –0.3V to 6V

LTC2935-2/LTC2935-4 ..... –0.3V to (V_{CC} + 0.3V)

RMS Currents

$\overline{PFO}$, $\overline{RST}$ ..... ±5mA

Operating Ambient Temperature Range

LTC2935C ..... 0°C to 70°C

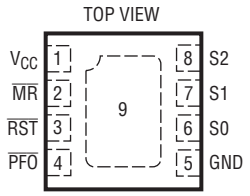
LTC2935I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

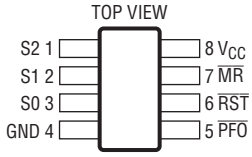
Lead Temperature (Soldering, 10 sec)

TSOT-23 Package ..... 300°C

PIN CONFIGURATION



DC PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 102°C/W
EXPOSED PAD (PIN 9), PCB GND CONNECTION OPTIONAL



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 125°C, θ_{JA} = 195°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2935CTS8-1#TRMPBF	LTC2935CTS8-1#TRPBF	LTDPW	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2935ITS8-1#TRMPBF	LTC2935ITS8-1#TRPBF	LTDPW	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2935CTS8-2#TRMPBF	LTC2935CTS8-2#TRPBF	LTDQB	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2935ITS8-2#TRMPBF	LTC2935ITS8-2#TRPBF	LTDQB	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2935CTS8-3#TRMPBF	LTC2935CTS8-3#TRPBF	LTFHV	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2935ITS8-3#TRMPBF	LTC2935ITS8-3#TRPBF	LTFHV	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2935CTS8-4#TRMPBF	LTC2935CTS8-4#TRPBF	LTFHX	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2935ITS8-4#TRMPBF	LTC2935ITS8-4#TRPBF	LTFHX	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2935CDC-1#TRMPBF	LTC2935CDC-1#TRPBF	LDPX	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2935IDC-1#TRMPBF	LTC2935IDC-1#TRPBF	LDPX	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2935CDC-2#TRMPBF	LTC2935CDC-2#TRPBF	LDQC	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2935IDC-2#TRMPBF	LTC2935IDC-2#TRPBF	LDQC	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2935CDC-3#TRMPBF	LTC2935CDC-3#TRPBF	LFHW	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2935IDC-3#TRMPBF	LTC2935IDC-3#TRPBF	LFHW	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2935CDC-4#TRMPBF	LTC2935CDC-4#TRPBF	LFHY	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2935IDC-4#TRMPBF	LTC2935IDC-4#TRPBF	LFHY	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.6V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Input Supply Voltage		●			5.5	V
I_{CC}	V_{CC} Input Supply Current		●	225	500	1000	nA
Reset Thresholds (LTC2935-1/LTC2935-2)							
V_{RTF1}	Reset Threshold 1 (V_{CC} Falling)	S2 = Low : S1 = Low : S0 = Low	●	3.251	3.300	3.349	V
V_{RTF2}	Reset Threshold 2 (V_{CC} Falling)	S2 = Low : S1 = Low : S0 = High	●	3.103	3.150	3.197	V
V_{RTF3}	Reset Threshold 3 (V_{CC} Falling)	S2 = Low : S1 = High : S0 = High	●	2.955	3.000	3.045	V
V_{RTF4}	Reset Threshold 4 (V_{CC} Falling)	S2 = Low : S1 = High : S0 = Low	●	2.808	2.850	2.892	V
V_{RTF5}	Reset Threshold 5 (V_{CC} Falling)	S2 = High : S1 = High : S0 = Low	●	2.660	2.700	2.740	V
V_{RTF6}	Reset Threshold 6 (V_{CC} Falling)	S2 = High : S1 = Low : S0 = Low	●	2.512	2.550	2.588	V
V_{RTF7}	Reset Threshold 7 (V_{CC} Falling)	S2 = High : S1 = Low : S0 = High	●	2.364	2.400	2.436	V
V_{RTF8}	Reset Threshold 8 (V_{CC} Falling)	S2 = High : S1 = High : S0 = High	●	2.217	2.250	2.283	V
ΔV_{RTF}	Reset Threshold Differential $V_{RTF(N+1)} - V_{RTF(N)}$	(Note 3)	●	142	150	158	mV
$V_{RT(HYST)}$	Reset Threshold Hysteresis (V_{CC} Rising)	Relative to Any Selected Reset Threshold	●	4.5	5	6	%
t_{UVR}	Undervoltage Detect to $\overline{RST}$ Falling	V_{CC} Below Threshold by 1% (Note 3)			1		ms
Reset Thresholds (LTC2935-3/LTC2935-4)							
V_{RTF1}	Reset Threshold 1 (V_{CC} Falling)	S2 = Low : S1 = Low : S0 = Low	●	2.404	2.440	2.476	V
V_{RTF2}	Reset Threshold 2 (V_{CC} Falling)	S2 = Low : S1 = Low : S0 = High	●	2.286	2.320	2.354	V
V_{RTF3}	Reset Threshold 3 (V_{CC} Falling)	S2 = Low : S1 = High : S0 = High	●	2.167	2.200	2.233	V
V_{RTF4}	Reset Threshold 4 (V_{CC} Falling)	S2 = Low : S1 = High : S0 = Low	●	2.049	2.080	2.111	V
V_{RTF5}	Reset Threshold 5 (V_{CC} Falling)	S2 = High : S1 = High : S0 = Low	●	1.931	1.960	1.989	V
V_{RTF6}	Reset Threshold 6 (V_{CC} Falling)	S2 = High : S1 = Low : S0 = Low	●	1.813	1.840	1.867	V
V_{RTF7}	Reset Threshold 7 (V_{CC} Falling)	S2 = High : S1 = Low : S0 = High	●	1.695	1.720	1.745	V
V_{RTF8}	Reset Threshold 8 (V_{CC} Falling)	S2 = High : S1 = High : S0 = High	●	1.576	1.600	1.624	V
ΔV_{RTF}	Reset Threshold Differential $V_{RTF(N+1)} - V_{RTF(N)}$	(Note 3)	●	112	120	128	mV
$V_{RT(HYST)}$	Reset Threshold Hysteresis (V_{CC} Rising)	Relative to Any Selected Reset Threshold	●	4.5	5	6	%
t_{UVR}	Undervoltage Detect to $\overline{RST}$ Falling	V_{CC} Below Threshold by 1% (Note 3)			1		ms
Power-Fail Thresholds (LTC2935-1/LTC2935-2)							
ΔV_{PFT}	Power-Fail Threshold Differential $V_{PFT(N)} - V_{RTF(N)}$	Any Selected Reset Threshold (V_{CC} Falling)	●	100	150	200	mV
$V_{PFT(HYST)}$	Power-Fail Threshold Hysteresis	Relative to Any Selected Power-Fail Threshold (V_{CC} Rising)	●	2	2.5	3.5	%
t_{UVP}	Undervoltage Detect to $\overline{PFO}$ Falling	V_{CC} Below Threshold by 1% (Note 3)			1		ms
Power-Fail Thresholds (LTC2935-3/LTC2935-4)							
ΔV_{PFT}	Power-Fail Threshold Differential $V_{PFT(N)} - V_{RTF(N)}$	Any Selected Reset Threshold (V_{CC} Falling)	●	70	120	170	mV
$V_{PFT(HYST)}$	Power-Fail Threshold Hysteresis	Relative to Any Selected Power-Fail Threshold (V_{CC} Rising)	●	2	2.5	3	%
t_{UVP}	Undervoltage Detect to $\overline{PFO}$ Falling	V_{CC} Below Threshold by 1% (Note 3)			1		ms
Control Inputs: $\overline{MR}$, S2, S1, S0							
$V_{IN(TH)}$	Control Input Threshold	S2, S1, S0 $\overline{MR}$	● ●	0.3 • V_{CC} 0.4		0.7 • V_{CC} 1.4	V V
t_{PW}	Input Pulse Width	$\overline{MR}$	●	20			µs
t_{PD}	Propagation Delay to $\overline{RST}$ Falling	Manual Reset Falling	●	2	5	20	µs
R_{PU}	Internal Pull-Up Resistance	$\overline{MR}$	●	600	900	1200	kΩ
I_{LK}	Input Leakage Current	S2, S1, S0 = V_{CC} or GND	●		±1	±10	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.6V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reset and Power-Fail Outputs: $\overline{RST}$, $\overline{PFO}$							
V_{OL}	Voltage Output Low	V_{CC} = 1V, 200µA Pull-Up Current V_{CC} = 3V, 3mA Pull-Up Current S2, S1, S0 = Low	● ●		25 50	100 150	mV mV
V_{OH}	Voltage Output High (LTC2935-2)	–200µA Pull-Down Current	●	0.7 • V_{CC}			V
I_{OH}	Current Output High, Leakage (LTC2935-1)	$V_{\overline{RST}}$, $V_{\overline{PFO}}$ = 3.6V	●		±1	±10	nA
t_{RST}	Reset Timeout Period		●	140	200	260	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

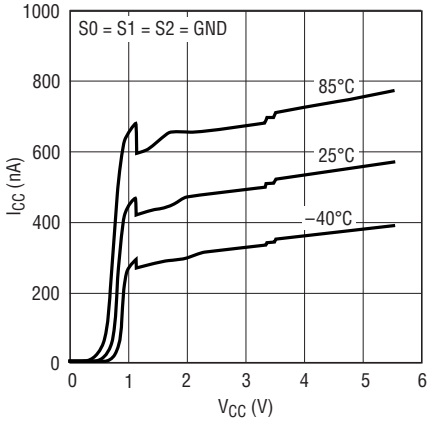
Note 2. All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

Note 3. Guaranteed by design. Characterized, but not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

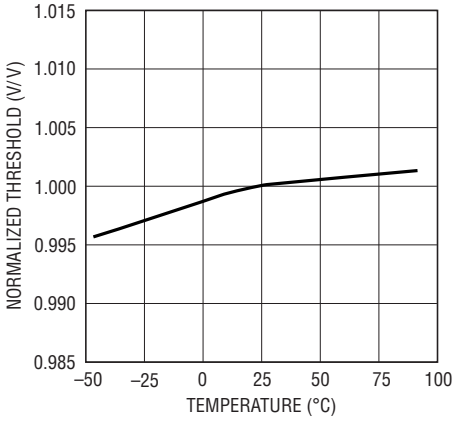
T_A = 25°C, unless otherwise noted.

Supply Current vs Supply Voltage



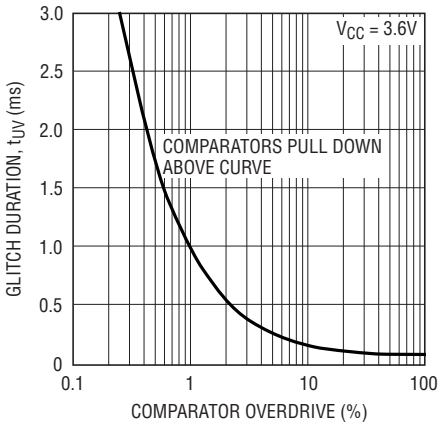
2935 G01

Normalized Reset and Power-Fail Thresholds vs Temperature



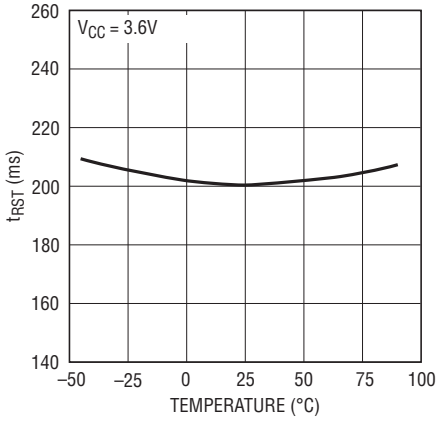
2935 G02

Comparator Undervoltage Glitch Immunity



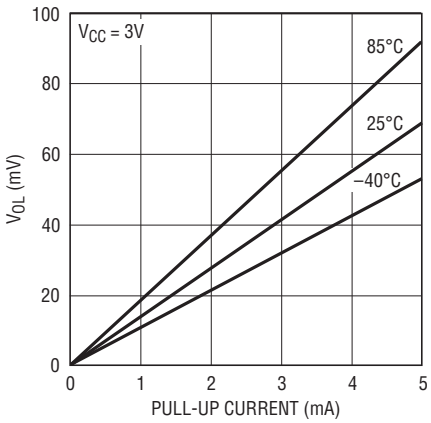
2935 G03

Reset Timeout Period vs Temperature



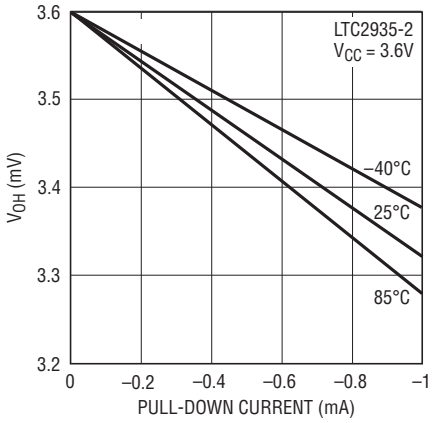
2935 G04

Voltage Output Low vs Pull-Up Current ($\overline{RST}$, $\overline{PFO}$)



2935 G05

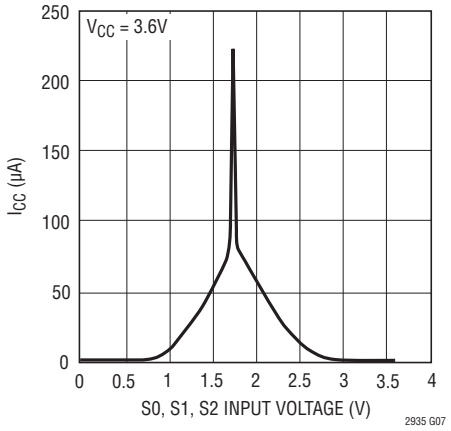
Voltage Output High vs Pull-Down Current ($\overline{RST}$, $\overline{PFO}$)



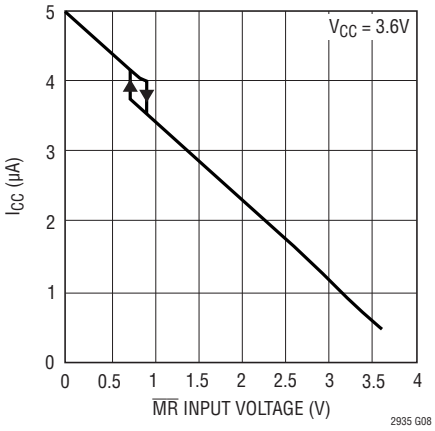
2935 G06

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Supply Current vs S0, S1, S2 Input Voltage



Supply Current vs $\overline{MR}$ Input Voltage



PIN FUNCTIONS

Exposed Pad (DFN Only): Exposed Pad may be left floating or connected to device ground.

GND: Device ground.

$\overline{MR}$: Manual Reset Input. Attach a pushbutton switch between this input and ground. A logic low on this input pulls $\overline{RST}$ low. When the $\overline{MR}$ input returns to logic high, $\overline{RST}$ returns high after 200ms. Tie to V_{CC} if unused.

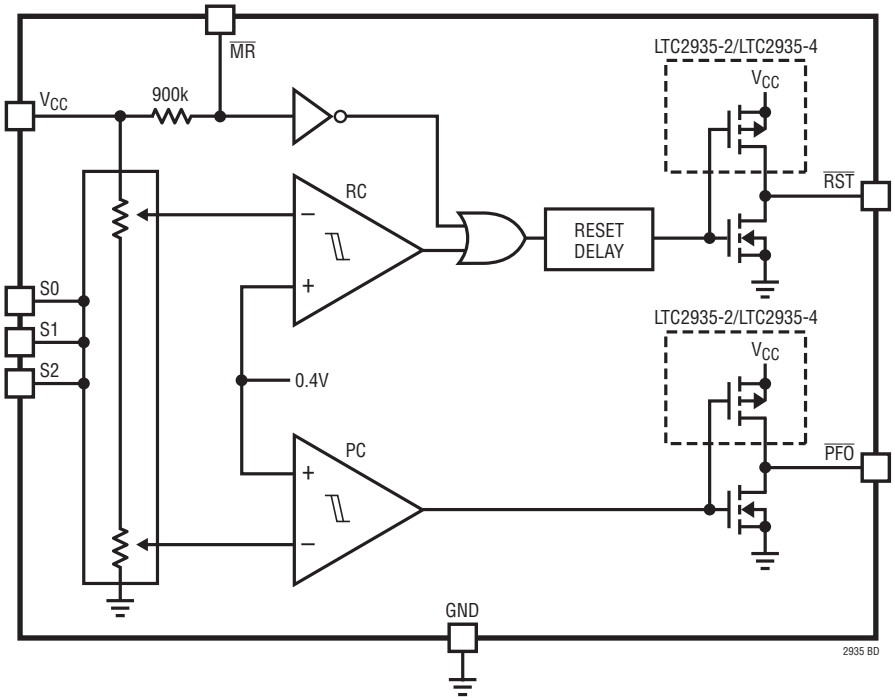
$\overline{PFO}$: Power-Fail Output. $\overline{PFO}$ pulls low when V_{CC} falls below the power-fail threshold. The power-fail threshold is above the configured falling reset threshold by a pre-determined margin. $\overline{PFO}$ is released when V_{CC} rises above the power-fail threshold by 2.5%. $\overline{PFO}$ is available with open-drain (LTC2935-1/LTC2935-3) or active pull-up (LTC2935-2/LTC2935-4) outputs. Leave open if unused.

$\overline{RST}$: Reset Output. $\overline{RST}$ pulls low when V_{CC} falls below the reset threshold. $\overline{RST}$ is released 200ms after V_{CC} exceeds the reset threshold plus 5% hysteresis. $\overline{RST}$ is available with open-drain (LTC2935-1/LTC2935-3) or active pull-up (LTC2935-2/LTC2935-4) outputs. Leave open if unused.

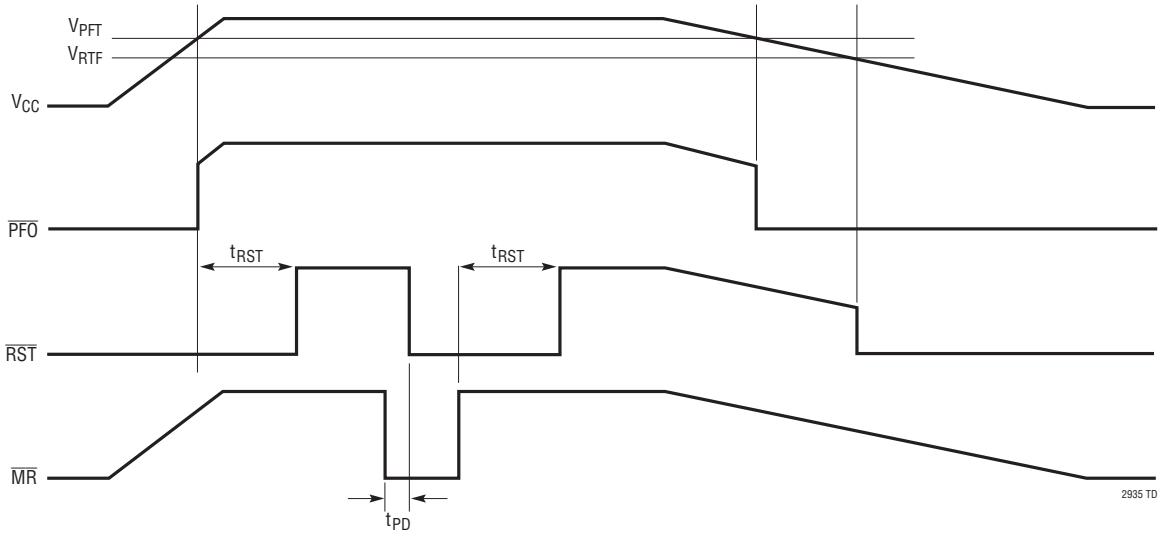
S2, S1, S0: Threshold Selection Inputs. Tie to GND or V_{CC} for required reset threshold. See the Falling Threshold Selection Table on page 1 for settings.

V_{CC}: Power Supply and Monitored Voltage Input. Bypass V_{CC} with a 0.1µF capacitor to GND.

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

VOLTAGE MONITORING

Unmanaged power can cause various system problems. At power-up, voltage fluctuation around critical thresholds can cause improper system or processor initialization. The LTC2935 provides power management capabilities for the system power-up phase. The supervisory device issues a system reset after the monitored voltage has stabilized. Built-in hysteresis and filtering ensures that fluctuations due to load transients or supply noise do not cause chattering of the status outputs. Comparator undervoltage glitch immunity is shown in the Typical Performance Characteristics section. The curve demonstrates the transient amplitude and width required to switch the comparators.

Because many batteries exhibit large series resistance, load currents can cause significant voltage drops. The low DC current draw of the LTC2935 (at any input voltage) does not add to the loading problem. When voltage is initially applied to V_{CC}, $\overline{RST}$ and $\overline{PFO}$ pull low once there is enough voltage to turn on the pull-down devices (1V maximum).

If the monitored supply voltage falls to the power-fail threshold, the built-in power-fail comparator pulls $\overline{PFO}$ low. At this point, there remains a voltage margin before the $\overline{RST}$ output pulls low. $\overline{PFO}$ remains low until V_{CC} rises above the power-fail threshold plus 2.5% hysteresis. $\overline{PFO}$ is typically used in signal preparation for controlled shutdown. For example, the $\overline{PFO}$ output may be connected to a processor nonmaskable interrupt. Upon interrupt, the processor may begin shutdown procedures. Shutdown events may include supply sequencing and/or storage/erasure of system state in nonvolatile memory.

If the monitored voltage drops below the reset threshold, $\overline{RST}$ pulls low until V_{CC} rises above the reset threshold plus 5% hysteresis. This may occur through battery charging or replacement. An internal reset timer delays the return of the $\overline{RST}$ output to a high state to provide settling and initialization time. The $\overline{RST}$ output is typically connected to a processor reset input.

Few, if any external components are necessary for reliable operation. However, a decoupling capacitor between V_{CC} and ground is recommended (0.01µF minimum).

Threshold Configuration

The LTC2935 monitors and compares the V_{CC} voltage against two internal thresholds during operation. The higher threshold (power-fail) is the level used for early warning of a low voltage condition, reported on the $\overline{PFO}$ output. The lower threshold (reset) is the level at which the $\overline{RST}$ output pulls low. Use system requirements to choose the appropriate reset threshold from Table 1.

Table 1. Falling Threshold Selection

LTC2935-1/LTC2935-2		LTC2935-3/LTC2935-4				
RESET THRESHOLD (V)	POWER-FAIL THRESHOLD (V)	RESET THRESHOLD (V)	POWER-FAIL THRESHOLD (V)	S2	S1	S0
3.30	3.45	2.44	2.56	Low	Low	Low
3.15	3.30	2.32	2.44	Low	Low	High
3.00	3.15	2.20	2.32	Low	High	High
2.85	3.00	2.08	2.20	Low	High	Low
2.70	2.85	1.96	2.08	High	High	Low
2.55	2.70	1.84	1.96	High	Low	Low
2.40	2.55	1.72	1.84	High	Low	High
2.25	2.40	1.60	1.72	High	High	High

In the LTC2935-1/LTC2935-2 the power-fail threshold is always 150mV higher than the configured reset threshold. In the LTC2935-3/LTC2935-4 the power-fail threshold is always 120mV higher than the configured reset threshold. Set the threshold selection inputs (S2, S1, S0) accordingly.

APPLICATIONS INFORMATION

Selecting Output Logic Style

The LTC2935 status outputs are available in two options: open-drain (LTC2935-1/LTC2935-3) or active pull-up (LTC2935-2/LTC2935-4). The open-drain options (LTC2935-1/LTC2935-3) allow the outputs to be pulled up to a user defined voltage with a resistor. The open-drain pull-up voltage may be greater than V_{CC} (5.5V maximum), which is not always possible with inferior battery supervisors, due to internal clamps. When the status outputs are low, power is dissipated in the pull-up resistors. Recommended resistor values lie in the range between 10k and 470k. Figure 1 demonstrates typical LTC2935-1/LTC2935-3 $\overline{RST}$ output behavior.

The active pull-up options (LTC2935-2/LTC2935-4) eliminate the need for external pull-up resistors on the status outputs. Integrated pull-up devices pull the outputs up to V_{CC}. Actively pulled up outputs may not be driven above V_{CC}.

Some applications require the $\overline{RST}$ and/or $\overline{PFO}$ outputs to be valid with V_{CC} down to ground. Active pull-up handles this requirement with the addition of an external resistor from the output to ground. The resistor provides a path for leakage currents, preventing the output from floating to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the pull-up circuitry. A 100k resistor from output to ground is satisfactory for most applications. When the status outputs are high, power is dissipated in the pull-down resistors. Figure 2 demonstrates typical LTC2935-2/LTC2935-4 $\overline{RST}$ output behavior.

Manual Reset Input

When V_{CC} is above its reset threshold, and the manual reset input ($\overline{MR}$) is pulled low, the $\overline{RST}$ output is forced low. $\overline{RST}$ remains low for 200ms after the manual reset input is released and pulled high. The manual reset input is pulled up internally through 900k to V_{CC}. If external leakage currents have the ability to pull down the manual reset input below its logic threshold, a lower value pull-up resistor, placed between V_{CC} and $\overline{MR}$ will fix the problem.

Input $\overline{MR}$ is often pulled down through a pushbutton switch requiring human contact. If extended ESD tolerance is required, series resistance between the switch and the input is recommended. For most applications, a 10k resistor provides sufficient current limiting.

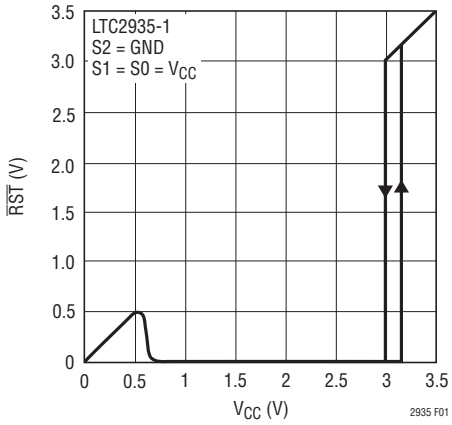


Figure 1. $\overline{RST}$ vs V_{CC} with 10k Pull-Up

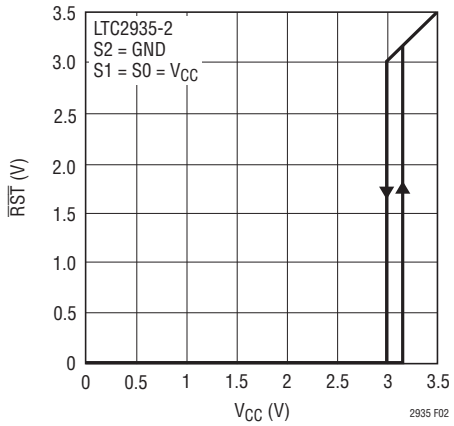
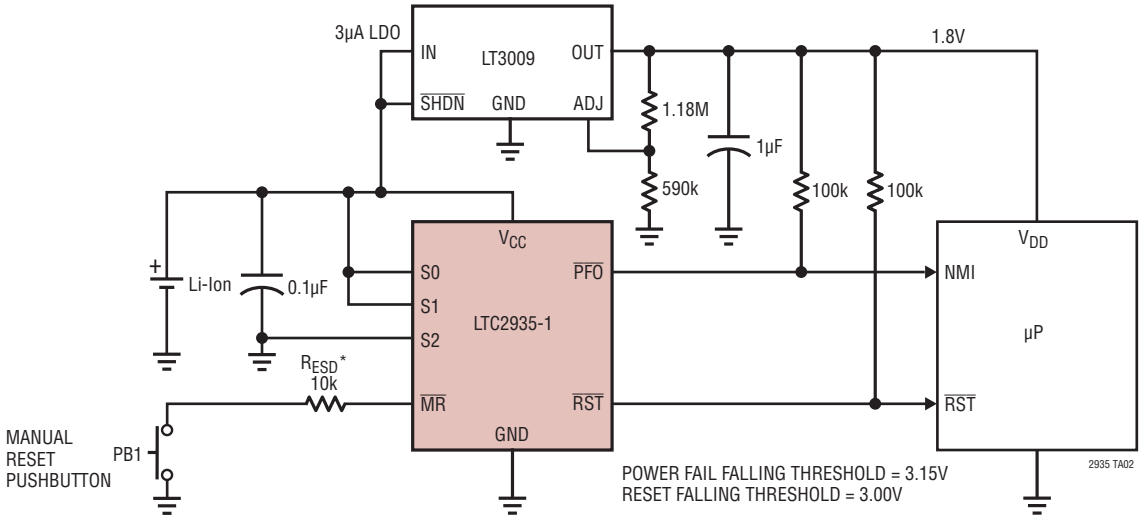


Figure 2. $\overline{RST}$ vs V_{CC}

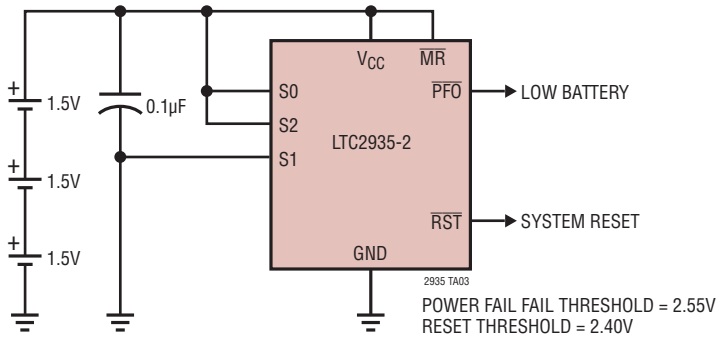
TYPICAL APPLICATIONS

Battery Monitor with Interface to Low Voltage Logic

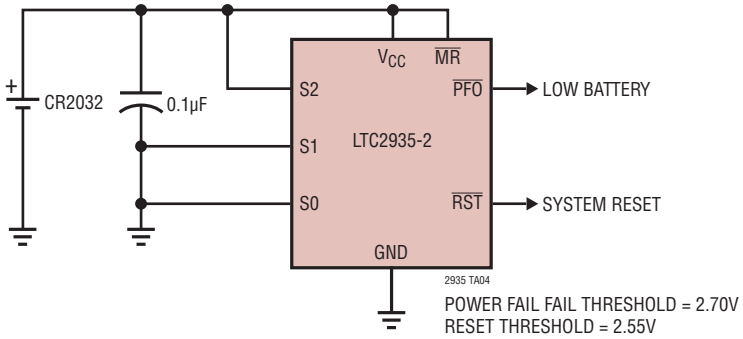


*OPTIONAL RESISTOR FOR ADDED ESD PROTECTION

Alkaline Cell Stack Voltage Monitor

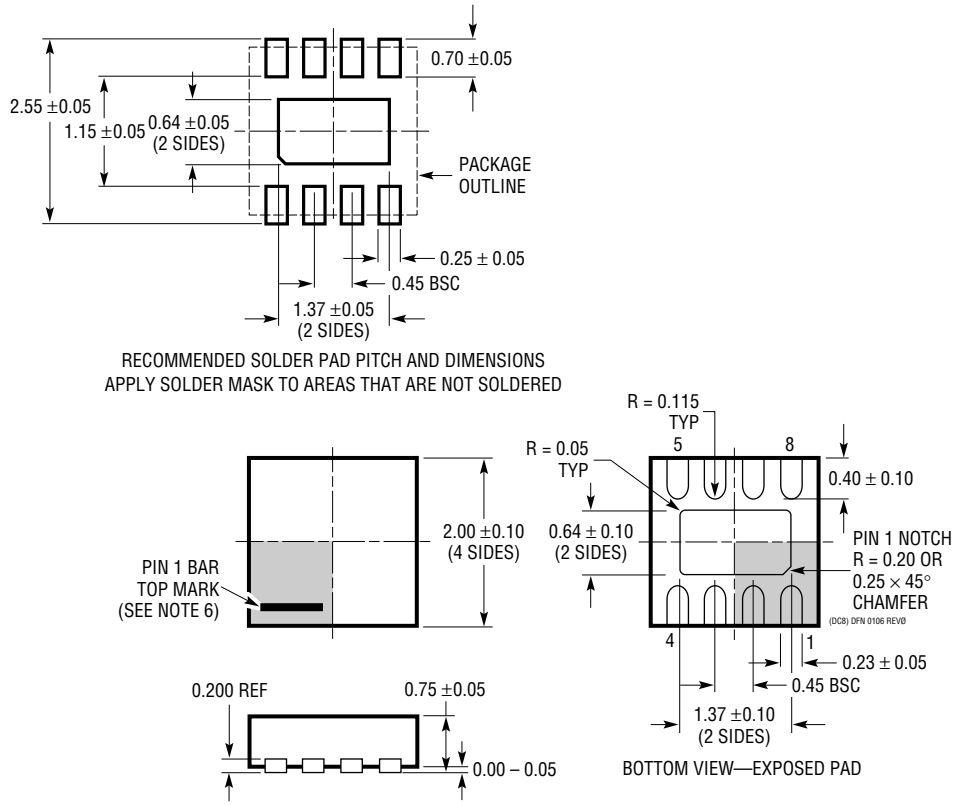


Coin Cell Voltage Monitor



PACKAGE DESCRIPTION

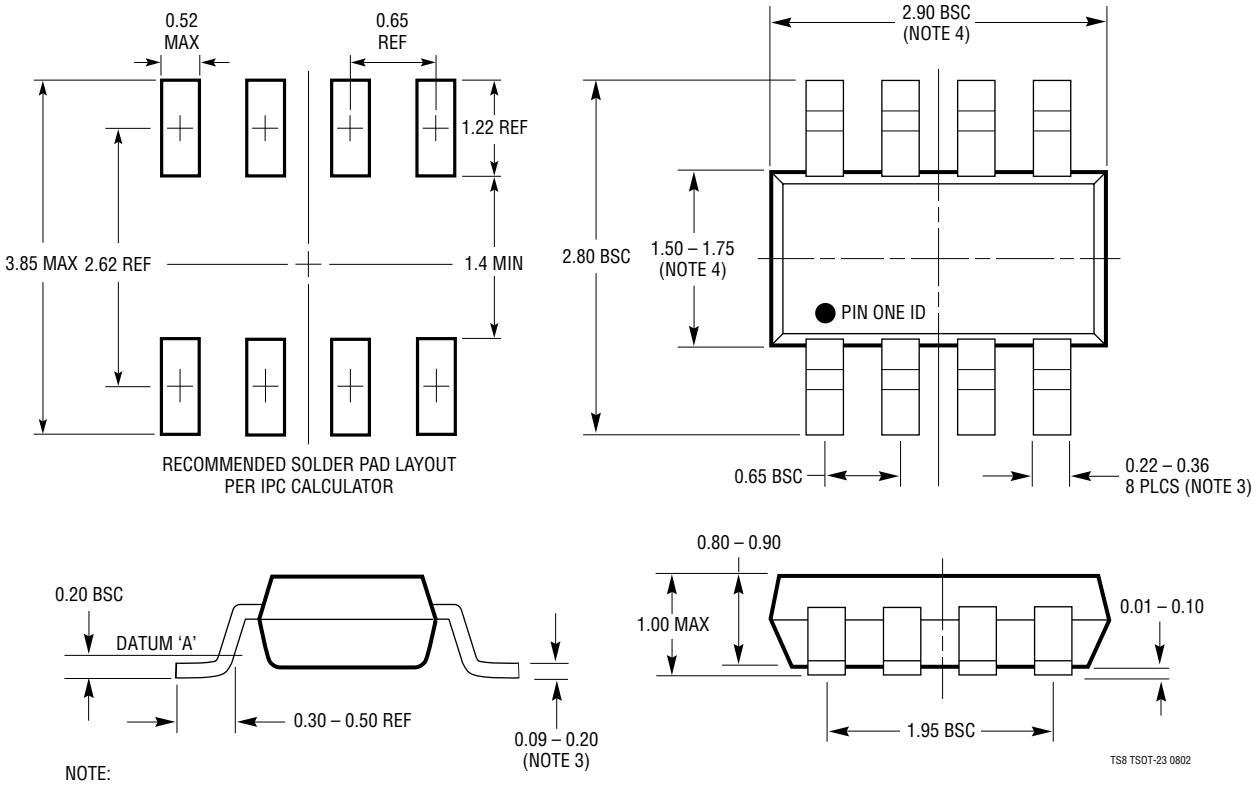
DC Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193