Battery Gas Gauge with I²C Interface

FEATURES

- **Indicates Accumulated Battery Charge and Discharge**
- **High Accuracy Analog Integration**
- **High Side Sense**
- **1% Charge Accuracy**
- ±50mV Sense Voltage Range
- SMBus/I²C Interface
- Configurable Alert Output/Charge Complete Input
- 2.7V to 5.5V Operating Range
- Quiescent Current Less Than 100µA
- Small 6-Pin 2mm × 3mm DFN and 8-Lead MSOP Packages

APPLICATIONS

- Low Power Handheld Products
- Cellular Phones
- MP3 Player
- Cameras
- GPS

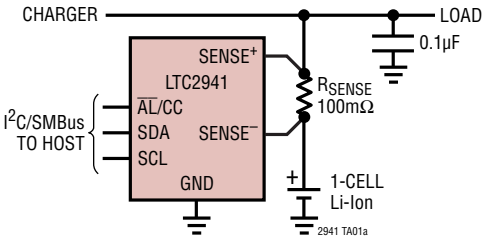
DESCRIPTION

The LTC®2941 measures battery charge state in battery-supplied handheld PC and portable product applications. Its operating range is perfectly suited for single-cell Li-Ion batteries. A precision coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. The measured charge is stored in internal registers. An SMBus/I²C interface accesses and configures the device.

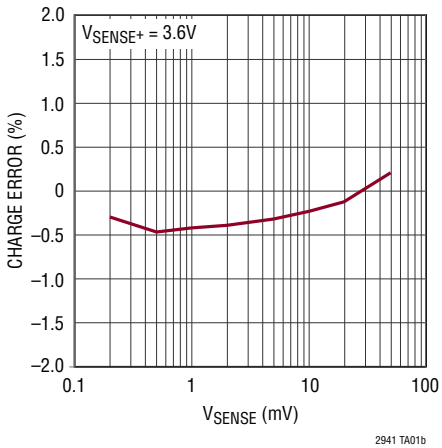
The LTC2941 features programmable high and low thresholds for accumulated charge. If a threshold is exceeded, the device communicates an alert using either the SMBus alert protocol or by setting a flag in the internal status register.

The LTC2941 requires only a single low value external sense resistor to set the current range.

TYPICAL APPLICATION



Total Charge Error vs Differential Sense Voltage



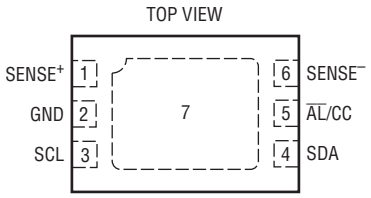
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ($SENSE^+$) ..... –0.3V to 6V
SCL, SDA, $\overline{AL}$/CC ..... –0.3V to 6V
$SENSE^-$ ..... –0.3V to (V_{SENSE+} + 0.3V)

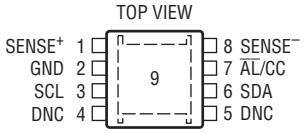
Operating Ambient Temperature Range
LTC2941C ..... 0°C to 70°C
LTC2941I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 120°C/W
EXPOSED PAD (PIN 7), DO NOT CONNECT



MSE PACKAGE
8-LEAD PLASTIC MSOP

PIN 4, PIN 5 AND EXPOSED PAD (PIN 9), DO NOT CONNECT

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2941CDCB#TRMPBF	LTC2941CDCB#TRPBF	LFKQ	6-Lead (2mm × 3mm) Plastic DFN	0°C to 70°C
LTC2941IDCB#TRMPBF	LTC2941IDCB#TRPBF	LFKQ	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
TUBE	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2941CMS8E#PBF	LTC2941CMS8E#TRPBF	LTGVY	8-Lead Plastic MSOP	0°C to 70°C
LTC2941IMS8E#PBF	LTC2941IMS8E#TRPBF	LTGVY	8-Lead Plastic MSOP	–40°C to 85°C

TRM = 500 pieces.

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
V_{SENSE+}	Supply Voltage			2.7		5.5	V
I_{SUPPLY}	Supply Current (Note 3)	Device On	●		70	100	µA
		Shutdown	●			2.5	µA
		Shutdown, $V_{SENSE+} \leq 4.2V$				1	µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{SENSE+} Falling, DCB Package V_{SENSE+} Falling, MSE Package	● ●	2.5 2.45	2.6 2.6	2.7 2.7	V V
Coulomb Counter							
V_{SENSE}	Sense Voltage Differential Input Range	$V_{SENSE+} - V_{SENSE-}$	●			±50	mV
	Differential Input Resistance, Across $SENSE^+$ and $SENSE^-$ (Note 7)				400		kΩ
q_{LSB}	Charge LSB (Note 4)	Prescaler M = 128 (Default), R_{SENSE} = 50mΩ			0.085		mAh
TCE	Total Charge Error (Note 5)	10mV ≤ $\|V_{SENSE}\|$ ≤ 50mV DC				±1	%
		10mV ≤ $\|V_{SENSE}\|$ ≤ 50mV, DC $V_{SENSE+} \leq 4.2V$	●			±1.5	%
		1mV ≤ $\|V_{SENSE}\|$ ≤ 50mV DC (Note 7)	●			±3.5	%
V_{BAT} Alert	V_{BAT} Alert Threshold	V_{SENSE+} Falling, B[7:6] = 01	●	2.75	2.8	2.85	V
		V_{SENSE+} Falling, B[7:6] = 10	●	2.85	2.9	2.95	V
		V_{SENSE+} Falling, B[7:6] = 11	●	2.95	3	3.05	V
Digital Inputs and Digital Outputs							
V_{ITH}	Logic Input Threshold, $\overline{AL}$/CC, SCL, SDA		●	0.3 • V_{SENSE+}		0.7 • V_{SENSE+}	V
V_{OL}	Low Level Output Voltage, $\overline{AL}$/CC, SDA	I = 3mA	●			0.4	V
I_{IN}	Input Leakage, $\overline{AL}$/CC, SCL, SDA	$V_{IN} = V_{SENSE+}/2$	●			1	µA
C_{IN}	Input Capacitance, $\overline{AL}$/CC, SCL, SDA	(Note 7)	●			10	pF
t_{PCC}	Minimum Charge Complete (CC) Pulse Width					1	µs
I^2C Timing Characteristics							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400	900		kHz
$t_{BUF(MIN)}$	Bus Free Time Between STOP/START		●			1.3	µs
$t_{SU,STA(MIN)}$	Minimum Repeated START Set-Up Time		●			600	ns
$t_{HD,STA(MIN)}$	Minimum Hold Time (Repeated) START Condition		●			600	ns
$t_{SU,STO(MIN)}$	Minimum Set-Up Time for STOP Condition		●			600	ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time Input		●			100	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input		●			0	µs
$t_{HD,DATO}$	Data Hold Time Output		●	0.3		0.9	µs
t_{Of}	Data Output Fall Time	(Notes 6, 7)	●	20 + 0.1 • C_B		300	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified

Note 3: $I_{SUPPLY} = I_{SENSE+} + I_{SENSE-}$

Note 4: The equivalent charge of an LSB in the accumulated charge registers (C, D) depends on the value of R_{SENSE} and the setting of the internal prescaling factor M. It is calculated by:

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{128}$$

See Choosing R_{SENSE} and Coulomb Counter Prescaler "M" B[5:3] section for more information.

1mAh = 3.6A • s = 3.6C (coulomb), 0.085mAh = 306mC.

Note 5: Deviation of q_{LSB} from its nominal value.

Note 6: C_B = capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 7: Guaranteed by design, not subject to test.

TIMING DIAGRAM

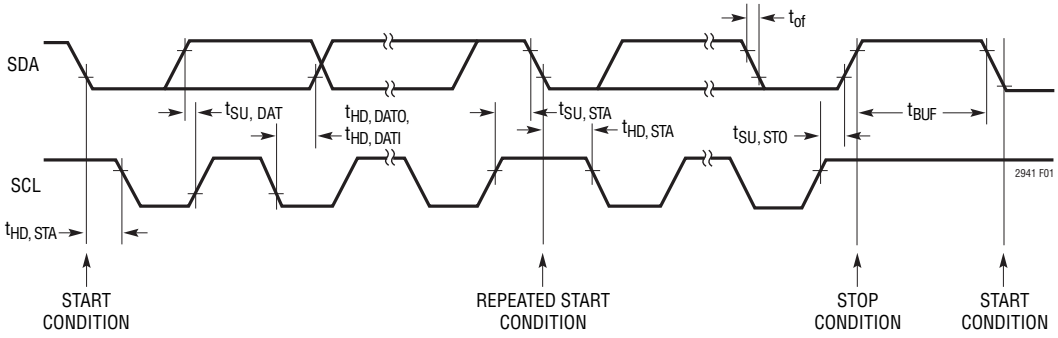
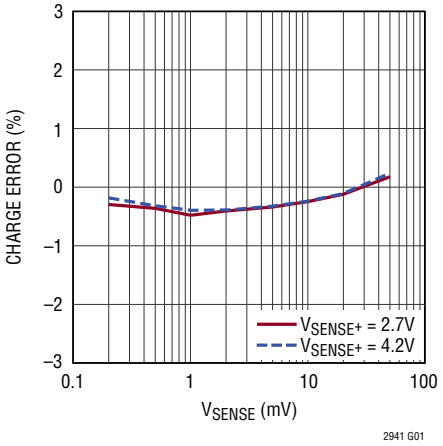


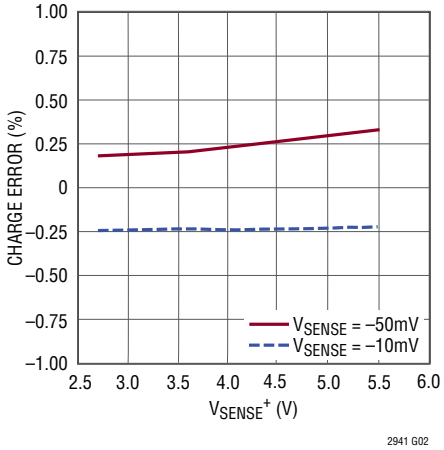
Figure 1. Definition of Timing on I^2C Bus

TYPICAL PERFORMANCE CHARACTERISTICS

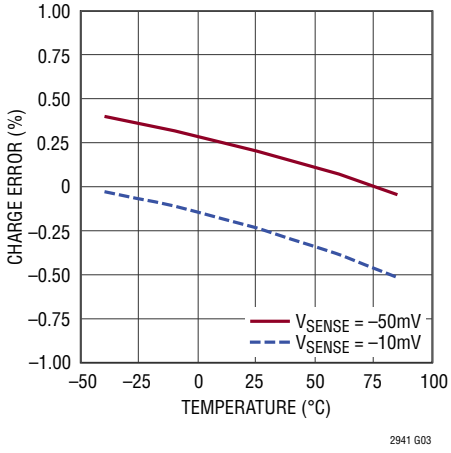
Total Charge Error vs Differential Sense Voltage



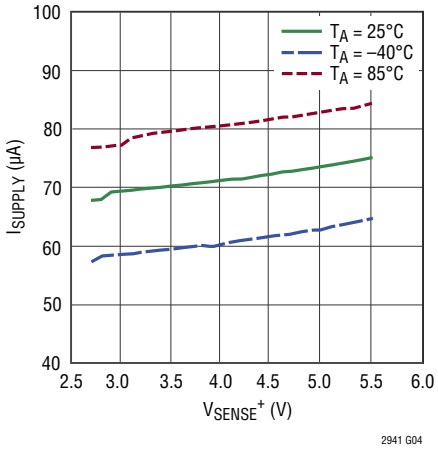
Total Charge Error vs Supply Voltage



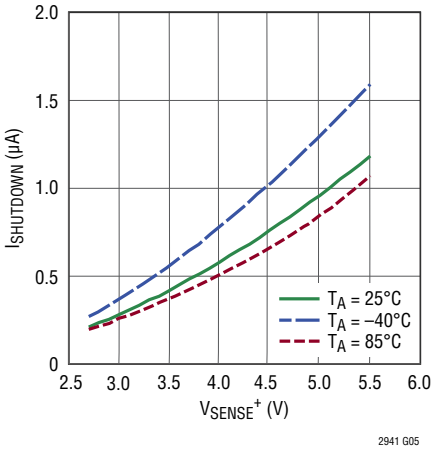
Total Charge Error vs Temperature



Supply Current vs Supply Voltage



Shutdown Supply Current vs Supply Voltage



PIN FUNCTIONS

SENSE+ (Pin 1): Positive Current Sense Input and Power Supply. Connect to the load/charger side of the sense resistor. V_{SENSE+} operating range is 2.7V to 5.5V.

GND (Pin 2): Device Ground. Connect directly to the negative battery terminal.

SCL (Pin 3): Serial Bus Clock Input.

SDA (Pin 4/Pin 6): Serial Bus Data Input and Output.

$\overline{AL}$/CC (Pin 5/Pin 7): Alert Output or Charge Complete Input. Configured either as an SMBus alert output or charge complete input by control register bits B[2:1]. At power-up, the pin defaults to alert mode conforming to the SMBus alert response protocol. It behaves as an open-drain logic output that pulls to GND when a value in the threshold registers is exceeded.

When configured as a charge complete input, connect to the charge complete output from the battery charger circuit. A high level at CC sets the value of the accumulated charge (registers C, D) to FFFFh.

SENSE– (Pin 6/Pin 8): Negative Current Sense Input. Connect SENSE– to the positive battery terminal side of the sense resistor. The voltage between SENSE– and SENSE+ must remain within ±50mV in normal operation.

Exposed Pad (Pin 7/Pin 9): Do not connect.

BLOCK DIAGRAM

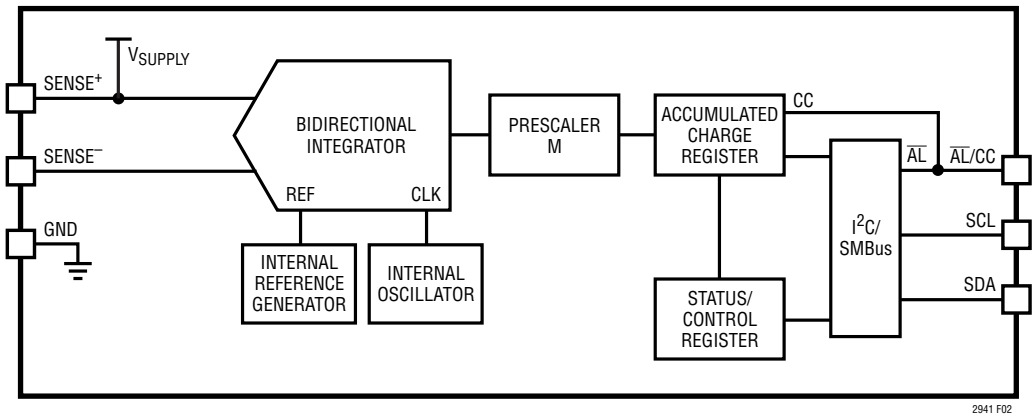


Figure 2. Block Diagram of the LTC2941

OPERATION

Overview

The LTC2941 is a battery gas gauge device designed for use with single Li-Ion cells and other battery types with a terminal voltage between 2.7V and 5.5V. A precision coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger.

Coulomb Counter

Charge is the time integral of current. The LTC2941 measures battery current by monitoring the voltage developed across a sense resistor and then integrates this information to infer charge. The differential voltage between $SENSE^+$ and $SENSE^-$ is applied to an auto-zeroed differential analog integrator to convert the measured current to charge.

When the integrator output ramps to REFHI or REFLO levels, switches S1, S2, S3 and S4 toggle to reverse the ramp direction. By observing the condition of the switches and the ramp direction, polarity is determined.

A programmable prescaler is incremented or decremented every time the integrator changes ramp direction. The prescaler effectively increases integration time by a factor M programmable from 1 to 128. At each under or overflow of the prescaler, the accumulated charge is incremented or decremented one count. The value of accumulated charge is read via the I^2C interface.

Power-Up Sequence

When V_{SENSE+} rises above a threshold of approximately 2.45V, the LTC2941 generates an internal power-on reset (POR) signal and sets all registers to their default state. In the default state, the coulomb counter is active. The accumulated charge is set to mid-scale (7FFFh), the low threshold registers are set to 0000h and all the high threshold registers are set to FFFFh. The alert mode is enabled and the coulomb counter prescaling factor M is set to 128.

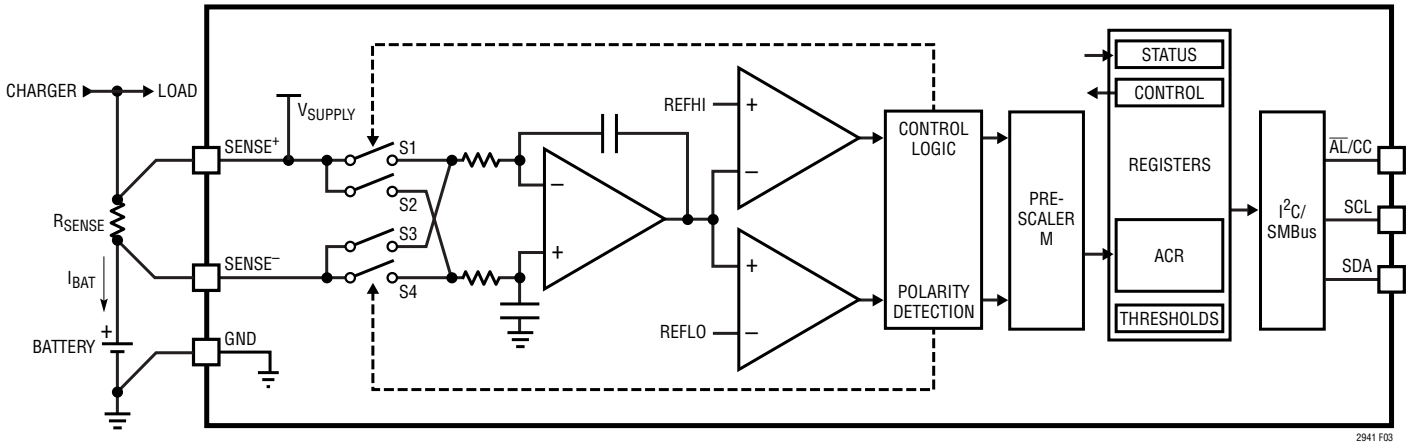


Figure 3. Coulomb Counter Section of the LTC2941

APPLICATIONS INFORMATION

I²C/SMBus Interface

The LTC2941 communicates with a bus master using a 2-wire interface compatible with I²C and SMBus. The 7-bit hard-coded **I²C address of LTC2941 is 1100100**.

The LTC2941 is a slave-only device. Therefore the serial clock line (SCL) is input only while the data line (SDA) is bidirectional. For more details refer to the I²C Protocol section.

Internal Registers

The LTC2941 integrates current through a sense resistor and stores a 16-bit result, accumulated charge, as two bytes in registers C and D. Two byte high and low limits programmed in registers E, F, G and H are continuously compared against the accumulated charge. If either limit is exceeded, a corresponding flag is set in the status register bits A[2] or A[3]. If the alert mode is enabled, the $\overline{AL}$/CC pin pulls low.

The internal eight registers are organized as shown in Table 1:

Table 1. Register Map

ADDRESS	NAME	REGISTER DESCRIPTION	R/W	DEFAULT
00h	A	Status	R	See Below
01h	B	Control	R/W	3Ch
02h	C	Accumulated Charge MSB	R/W	7Fh
03h	D	Accumulated Charge LSB	R/W	FFh
04h	E	Charge Threshold High MSB	R/W	FFh
05h	F	Charge Threshold High LSB	R/W	FFh
06h	G	Charge Threshold Low MSB	R/W	00h
07h	H	Charge Threshold Low LSB	R/W	00h

R = Read, W = Write

Status Register (A)

Table 2 shows the details of the status register (address 00h):

Table 2. Status Register A (Read Only)

BIT	NAME	OPERATION	DEFAULT
A[7]	Chip Identification	1: LTC2941 0: LTC2942	1
A[6]	Reserved	Not Used.	0
A[5]	Accumulated Charge Overflow/Underflow	Indicates that the value of the accumulated charge hit either top or bottom.	0
A[4]	Reserved	Not used.	0
A[3]	Charge Alert High	Indicates that the accumulated charge value exceeded the charge threshold high limit.	0
A[2]	Charge Alert Low	Indicates that the accumulated charge value dropped below the charge threshold low limit.	0
A[1]	V_{BAT} Alert	Indicates that the battery voltage (at $SENSE^-$) dropped below selected V_{BAT} threshold.	0
A[0]	Undervoltage Lockout Alert	Indicates recovery from undervoltage. If equal to 1, a UVLO has occurred and the content of registers is uncertain.	X

The $\overline{AL}$/CC pin can be configured to pull low whenever any status register bit is set (except for bit A[7] and A[0]), using control register bits B[2] and B[1]. All status register bits except A[7] are cleared after being read by the host if the conditions which set these bits have been removed.

As soon as one of the measured quantities exceeds the programmed limits, the corresponding bit A[3], A[2] or A[1] in the status register is set.

APPLICATIONS INFORMATION

Bit A[5] is set if the LTC2941's accumulated charge overflows or underflows the combined total in registers C and D. Note that the counting process does not roll over, but simply stops at FFFFh or 0000h until the direction is reversed.

The LTC2941 includes a battery undervoltage monitor, which sets bit A1 if the limit is exceeded. Limits are selected in the control register.

The undervoltage lockout (UVLO) bit A[0] is set if, during operation, the voltage on SENSE+ drops below 2.7V without reaching the POR level. The analog parts of the coulomb counter are switched off while the digital register values are retained. After recovery of the supply voltage the coulomb counter resumes integrating with the stored value in the accumulated charge registers (C, D) but it has missed any charge flowing while $V_{SENSE+} < 2.7V$.

The hard coded bit A[7] of the status register enables the host to distinguish the LTC2941 from the pin compatible LTC2942, allowing the same software to be used with both devices.

Control Register (B)

The operation of the LTC2941 can be controlled by programming the control register at address 01h. Table 3 shows the organization of the 8-bit control register B[7:0]

Table 3. Control Register B

BIT	NAME	OPERATION	DEFAULT
B[7:6]	V_{BAT} Alert	[11] Threshold Value = 3.0V. [10] Threshold Value = 2.9V. [01] Threshold Value = 2.8V. [00] V_{BAT} Alert Off.	[00]
B[5:3]	Prescaler M	Sets coulomb counter prescaling factor M between 1 and 128. Default is 128. $M = 2^{(4 \bullet B[5] + 2 \bullet B[4] + B[3])}$.	[111]
B[2:1]	$\overline{AL}$/CC Configure	Configures the $\overline{AL}$/CC pin. [10] Alert Mode. Alert functionality enabled. Pin becomes logic output. [01] Charge Complete Mode. Pin becomes logic input and accepts "charge complete" signal (e.g., from a charger) to set accumulated charge Register to FFFFh. [00] $\overline{AL}$/CC pin disabled. [11] Not allowed.	[10]
B[0]	Shutdown	Shut down analog section to reduce I_{SUPPLY}.	[0]

Power Down B[0]

Programming the last bit B[0] of the control register to 1 sets the analog parts of the LTC2941 in power down and the current consumption drops typically below 1µA. All analog circuits are disabled while the values in the registers are retained. Note that any charge flowing while B[0] is 1 is not measured and the charge information below 1 LSB of the accumulated charge register is lost.

Alert/Charge Complete Configuration B[2:1]

The $\overline{AL}$/CC pin is a dual function pin configured by the control register. By setting bits B[2:1] to [10] (default) the $\overline{AL}$/CC pin is configured as an alert pin following the SMBus protocol. In this alert mode the $\overline{AL}$/CC pin is a digital output and is pulled low if one of the measured quantities exceeds its high or low threshold or if the an overflow/underflow occurs in the accumulated charge registers C and D. An alert response procedure started by the master resets the alert at the $\overline{AL}$/CC pin. For further information see the Alert Response Protocol section.

Setting the control bits B[2:1] to [01] configures the $\overline{AL}$/CC pin as a digital input. In this mode, a high input on the $\overline{AL}$/CC pin communicates to the LTC2941 that the battery is full and the accumulated charge is set to its maximum value FFFFh. The $\overline{AL}$/CC pin would typically be connected to the "charge complete" output from the battery charger circuitry.

If neither the alert nor the charge complete functionality is desired, bits B[2:1] should be set to [00]. The $\overline{AL}$/CC pin is then disabled and should be tied to GND. Avoid setting B[2:1] to [11] as it enables the alert and the charge complete modes simultaneously.

Choosing R_{SENSE} and Coulomb Counter Prescaler "M" B[5:3]

To achieve the specified precision of the coulomb counter the differential voltage between SENSE+ and SENSE– must stay within ±50mV. For differential input signals up to ±300mV the LTC2941 will remain functional but the precision of the coulomb counter is not guaranteed.

APPLICATIONS INFORMATION

The value of the external sense resistor is determined by the maximum input range of V_{SENSE} and the maximum current of the application:

$$R_{SENSE} \leq \frac{50mV}{I_{MAX}}$$

The choice of the external sense resistor value influences the gain of the coulomb counter. A larger sense resistor gives a larger differential voltage between $SENSE^+$ and $SENSE^-$ for the same current which results in more precise coulomb counting. Thus the amount of charge represented by the least significant bit (q_{LSB}) of the accumulated charge (registers C, D) is given by:

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{128}$$

or

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}}$$

when the prescaler is set to its default value of M=128. Note that 1mAh = 3.6A • s = 3.6C (coulombs).

Choosing $R_{SENSE} = 50mV/I_{MAX}$ is not sufficient in applications where:

A. the battery capacity (Q_{BAT}) is very large compared to the maximum current (I_{MAX}):

$$Q_{BAT} > I_{MAX} \bullet 5.5 \text{ hours}$$

B. the battery capacity (Q_{BAT}) is very small compared to the maximum current (I_{MAX}):

$$Q_{BAT} < I_{MAX} \bullet 0.1 \text{ hours}$$

For case A: In low current applications using a large battery, choosing R_{SENSE} according to $R_{SENSE} = 50mV/I_{MAX}$ can lead to a q_{LSB} smaller than $Q_{BAT}/2^{16}$ and the 16-bit accumulated charge may underflow before the battery is exhausted or overflow during charge. Choose in this case a maximum R_{SENSE} of:

$$R_{SENSE} \leq \frac{0.085mAh \bullet 2^{16}}{Q_{BAT}} \bullet 50m\Omega$$

In an example application where the maximum current is I_{MAX} = 100mA, calculating $R_{SENSE} = 50mV/I_{MAX}$ would lead to a sense resistor of 500mΩ. This gives a q_{LSB} of 8.5µAh and the accumulated charge register can represent a maximum battery capacity of Q_{BAT} = 8.5µAh • 65535 = 557mAh. If the battery is larger, R_{SENSE} must be lowered. For example, R_{SENSE} must be reduced to 150mΩ if a battery with a capacity of 1800mAh is used.

For case B: In applications using a small battery but having a high maximum current, q_{LSB} can get quite large with respect to the battery capacity. For example, if the battery capacity is 100mAh and the maximum current is 1A, the standard equation leads to choose a sense resistor value of 50mΩ, resulting in:

$$q_{LSB} = 0.085mAh = 306mC$$

The battery capacity then corresponds to only 1176 q_{LSB}s and less than 2% of the accumulated charge register is utilized.

To preserve digital resolution in this case, the LTC2941 includes a programmable prescaler. Lowering the prescaler factor M allows reducing q_{LSB} to better match the accumulated charge registers C and D to the capacity of the battery. The prescaling factor M can be chosen between 1 and its default value 128. The charge LSB then becomes:

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{128}$$

APPLICATIONS INFORMATION

To use as much of the range of the accumulated charge registers C and D as possible the prescaler factor M should be chosen for a given battery capacity Q_{BAT} and a sense resistor R_{SENSE} as:

$$M \geq 128 \bullet \frac{Q_{BAT}}{2^{16} \bullet 0.085mAh} \bullet \frac{R_{SENSE}}{50m\Omega}$$

M can be set to 1, 2, 4, 8, …128 by programming B[5:3] of the control register as $M = 2^{(4 \bullet B[5] + 2 \bullet B[4] + B[3])}$. The default value after power up is $M = 128 = 2^7$ (B[5:3] = 111).

In the above example of a 100mAh battery and a R_{SENSE} of 50mΩ, the prescaler should be programmed to M = 4. The q_{LSB} then becomes 2.656µAh and the battery capacity corresponds to roughly 37650 q_{LSB}s.

Note that the internal digital resolution of the coulomb counter is higher than indicated by q_{LSB}. The digitized charge $q_{INTERNAL}$ is M • 8 smaller than q_{LSB}. $q_{INTERNAL}$ is typically 299µAs for a 50mΩ sense resistor.

V_{BAT} Alert B[7:6]

The V_{BAT} alert function allows the LTC2941 to monitor the voltage at SENSE⁻. If enabled, a drop of the voltage at the SENSE⁻ pin below a preset threshold is detected and bit A[1] in the status register is set. If the alert mode is enabled by setting B[2] to one, an alert is generated at the $\overline{AL}$/CC pin. The threshold for the V_{BAT} alert function is selectable according to Table 3.

Accumulated Charge Registers (C, D)

The coulomb counter of the LTC2941 integrates current through the sense resistor. The 16-bit result of this charge integration is stored in the accumulated charge registers C and D. As the LTC2941 does not know the actual battery status after initial power-up, the accumulated charge is set to mid-scale (7FFFh). If the host knows the status of the battery, the accumulated charge registers C[7:0] and D[7:0] can be either programmed to the correct value via I²C or it can be set after charging to FFFFh (full) by pulling the $\overline{AL}$/CC pin high (if charge complete mode is enabled via bits B[2:1]). Before writing the accumulated charge registers, the analog section should be shut down by setting B[0] to 1. In order to avoid a change in the accumulated charge registers between reading MSBs C[7:0] and LSBs D[7:0], it is recommended to read them sequentially, as shown in Figure 8.

Threshold Registers (E, F), (G, H)

For battery charge, the LTC2941 features a high and a low threshold register. At power-up the high threshold is set to FFFFh while the low threshold is set to 0000h. Both thresholds can be programmed to a desired value via I²C. As soon as the accumulated charge exceeds the high threshold or falls below the low threshold, the LTC2941 sets the corresponding flag in the status register and pulls the $\overline{AL}$/CC pin low if alert mode is enabled.

I²C Protocol

The LTC2941 uses an I²C/SMBus compatible 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the bus wires LOW and they never drive the bus HIGH. The bus wires should be externally connected to a positive supply voltage via a current source or pull-up resistor. When the bus is idle, both SDA and SCL are HIGH. Data on the I²C-bus can be transferred at rates of up to 100kbit/s in standard mode and up to 400kbit/s in fast mode.

Each device on the I²C/SMBus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be classified as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave. The LTC2941 always acts as a slave. Figure 4 shows an overview of the data transmission on the I²C bus.

APPLICATIONS INFORMATION

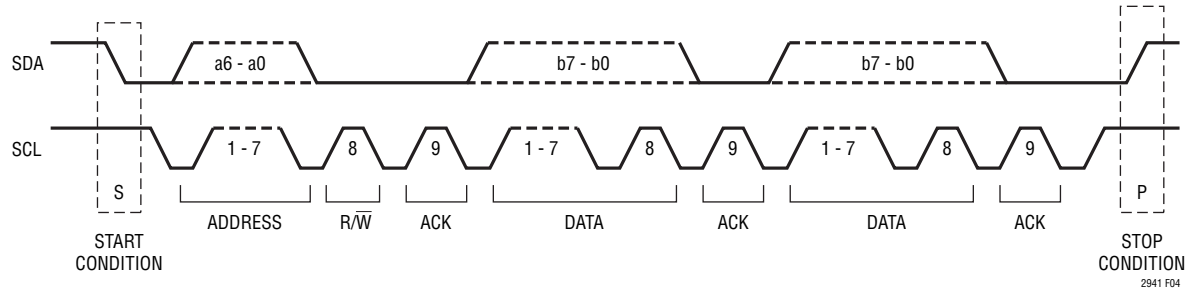


Figure 4. Data Transfer Over I²C or SMBus

START and STOP Conditions

When the bus is idle, both SCL and SDA must be HIGH. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from HIGH to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Data Transmission

After a START condition, the I²C bus is considered busy and data transfer begins between a master and a slave. As data is transferred over I²C in groups of nine bits (eight data bits followed by an acknowledge bit), each group takes nine SCL cycles. The transmitter releases the SDA line during the acknowledge clock pulse and the receiver issues an acknowledge (ACK) by pulling SDA LOW or leaves SDA HIGH to indicate a not-acknowledge (NACK) condition. Change of data state can only happen while SCL is LOW.

Write Protocol

The master begins communication with a START condition followed by the seven bit slave **address 1100100** and the R/$\overline{W}$ bit set to zero, as shown in Figure 5. The LTC2941 acknowledges this by pulling SDA LOW and then the master sends a command byte which indicates which internal register the master is to write. The LTC2941 acknowledges and then latches the command byte into its internal register address pointer. The master delivers the data byte, the LTC2941 acknowledges once more and latches the data into the desired register. The transmission is ended when the master sends a STOP condition. If the master continues by sending a second data byte instead of a STOP, the LTC2941 acknowledges again, increments its address pointer and latches the second data byte in the following register, as shown in Figure 6.

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave **address 1100100** and the R/$\overline{W}$ bit set to zero, as shown in Figure 7. The LTC2941 acknowledges and then the master sends a command byte which indicates which internal register the master is to read. The LTC2941 acknowledges and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/$\overline{W}$ bit now set to one. The LTC2941 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, the LTC2941 increments its address pointer and sends the contents of the following register, as shown in Figure 8.

APPLICATIONS INFORMATION

Alert Response Protocol

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt (Figure 9).

The master initiates the ARA procedure with a START condition and the special **7-bit ARA bus address (0001100)** followed by the read bit (R) = 1. If the LTC2941 is asserting the $\overline{AL}$/CC pin in alert mode, it acknowledges and responds by sending its **7-bit bus address (1100100)**

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	P
	1100100	0	0	01h	0	FCh	0	

2941 F05

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT-ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 5. Writing FCh to LTC2941 Control Register (B)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	DATA	A	P
	1100100	0	0	02h	0	F0h	0	01h	0	

2941 F06

Figure 6. Writing F001h to the LTC2941 Accumulated Charge Registers (C, D)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	S	ADDRESS	R	A	DATA	$\overline{A}$	P
	1100100	0	0	00h	0		1100100	1	0	81h	1	

2941 F07

Figure 7. Reading the LTC2941 Status Register (A)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	02h	0		1100100	1	0	80h	0	01h	1	

2941 F08

Figure 8. Reading the LTC2941 Accumulated Charge Registers (C, D)

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{A}$	P
	0001100	1	0	11001001	1	

2941 F09

Figure 9. LTC2941 Serial Bus SDA Alert Response Protocol

APPLICATIONS INFORMATION

and a 1. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LTC2941 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LTC2941 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LTC2941 will stop pulling down the $\overline{AL}$/CC pin and will not respond to further ARA requests until a new alert event occurs.

PC Board Layout Recommendations

Keep all traces as short as possible to minimize noise and inaccuracy. Use a 4-wire Kelvin sense connection for the sense resistor, locating the LTC2941 close to the resistor with short sense traces to $SENSE^+$ and $SENSE^-$. Use wider traces from the resistor to the battery, load and/or charger (see Figure 10). Put the bypass capacitor close to $SENSE^+$ and GND.

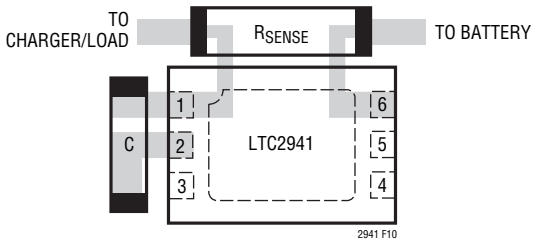
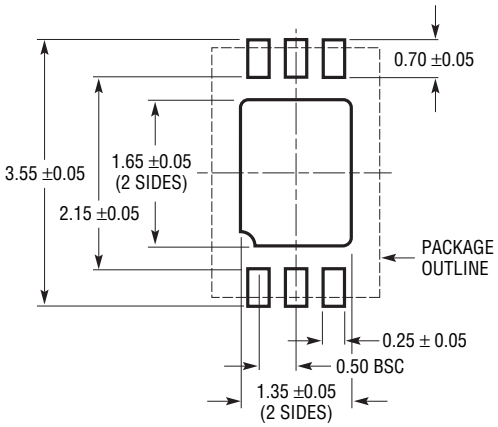


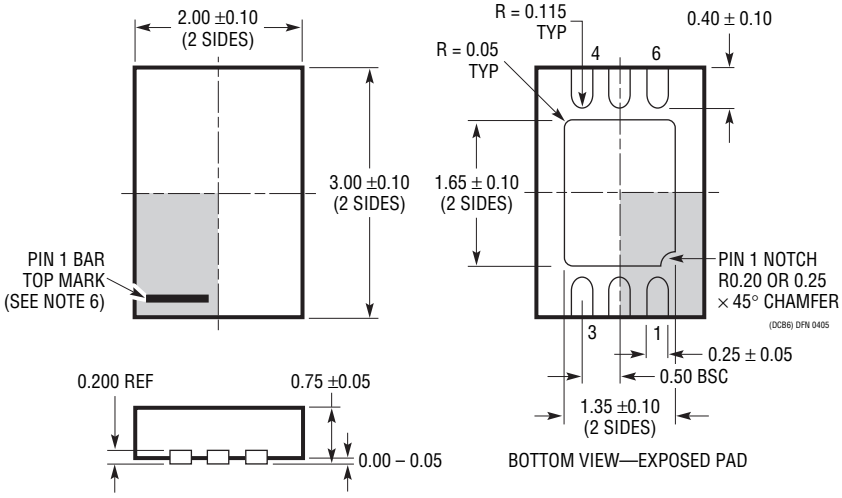
Figure 10. Kelvin Connection on Sense Resistor

PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

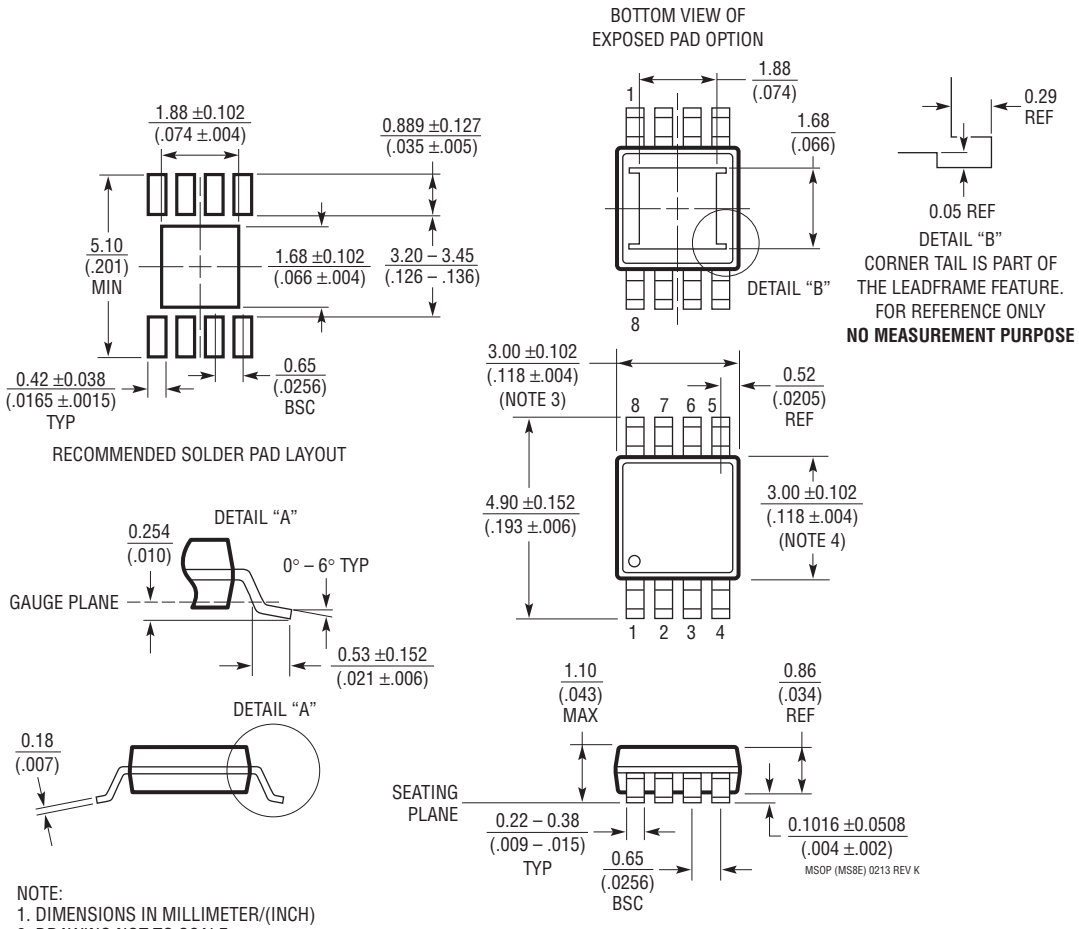


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	8/10	Revised Exposed Pad description in the Pin Configuration and Pin Functions sections	2, 5
B	02/16	Added MSOP Package option	1–18
C	11/18	Updated MSE Package description to include DNC (Do Not Connect) for MSE Package Corrected equation for external sense resistor calculation Note added to explain status output timing following internal self test operation	2 10 13