# Battery Gas Gauge with Temperature, Voltage Measurement

## FEATURES

- **Indicates Accumulated Battery Charge and Discharge**
- **High Accuracy Analog Integration**
- **ADC Measures Battery Voltage and Temperature**
- **Integrated Temperature Sensor**
- **High Side Sense**
- **1% Voltage and Charge Accuracy**
- ±50mV Sense Voltage Range
- SMBus/I²C Interface
- Configurable Alert Output/Charge Complete Input
- 2.7V to 5.5V Operating Range
- Quiescent Current Less than 100µA
- Small 6-Pin 2mm × 3mm DFN package

## APPLICATIONS

- Low Power Handheld Products
- Cellular Phones
- MP3 Players
- Cameras
- GPS

## DESCRIPTION

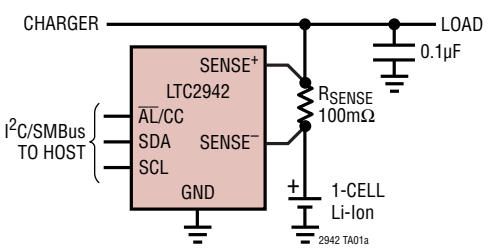
The LTC®2942 measures battery charge state, battery voltage and chip temperature in handheld PC and portable product applications. Its operating range is perfectly suited for single-cell Li-Ion batteries. A precision coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. Battery voltage and on-chip temperature are measured with an internal 14-bit No Latency ΔΣ™ ADC. The three measured quantities (charge, voltage and temperature) are stored in internal registers accessible via the onboard SMBus/I²C interface.

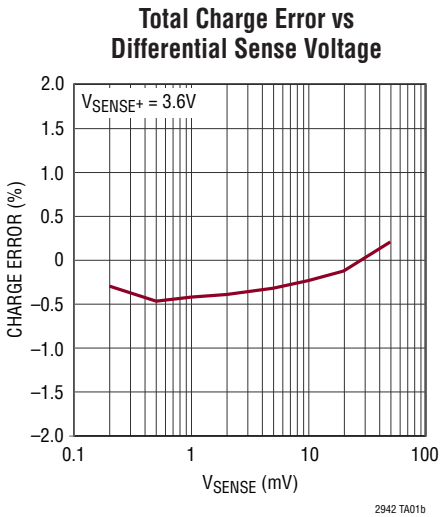
The LTC2942 features programmable high and low thresholds for all three measured quantities. If a programmed threshold is exceeded, the device communicates an alert using either the SMBus alert protocol or by setting a flag in the internal status register.

The LTC2942 requires only a single low value sense resistor to set the measured current range.



## TYPICAL APPLICATION



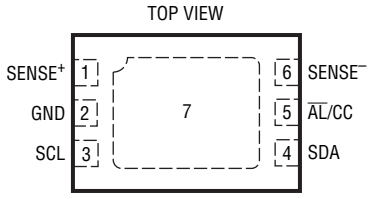



## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

Supply Voltage (SENSE+) ..... –0.3V to 6V
SCL, SDA, $\overline{AL}$/CC ..... –0.3V to 6V
SENSE– ..... –0.3V to ($V_{SENSE+}$ + 0.3V)
Operating Ambient Temperature Range
LTC2942C ..... 0°C to 70°C
LTC2942I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION




DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 120°C/W
EXPOSED PAD (PIN 7), DO NOT CONNECT

## ORDER INFORMATION

**Lead Free Finish**

| TAPE AND REEL (MINI) | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2942CDCB#TRMPBF | LTC2942CDCB#TRPBF | LDVN | 6-Lead (2mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC2942IDCB#TRMPBF | LTC2942IDCB#TRPBF | LDVN | 6-Lead (2mm × 3mm) Plastic DFN | –40°C to 85°C |

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Requirements** | | | | | | | |
| $V_{SENSE+}$ | Supply Voltage | | | 2.7 | | 5.5 | V |
| $I_{SUPPLY}$ | Supply Current (Note 3) | Battery Gas Gauge On, ADC Sleep | ● | | 70 | 100 | µA |
| | | Battery Gas Gauge On, ADC Converting Voltage | ● | | 300 | 350 | µA |
| | | Battery Gas Gauge On, ADC Converting Temperature | ● | | 350 | 420 | µA |
| | | Shutdown | ● | | | 2.5 | µA |
| | | Shutdown, $V_{SENSE+} \leq 4.2V$ | | | | 1 | µA |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | $V_{SENSE+}$ Falling | ● | 2.5 | 2.6 | 2.7 | V |
| **Coulomb Counter** | | | | | | | |
| $V_{SENSE}$ | Sense Voltage Differential Input Range | $V_{SENSE+} – V_{SENSE–}$ | ● | | | ±50 | mV |
| $R_{IDR}$ | Differential Input Resistance, Across SENSE+ and SENSE– (Note 8) | | | | 400 | | kΩ |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $q_{LSB}$ | Charge LSB (Note 4) | Prescaler M = 128 (Default), $R_{SENSE}$ = 50mΩ | | | 0.085 | | mAh |
| TCE | Total Charge Error (Note 5) | 10mV ≤ \|$V_{SENSE}$\| ≤ 50mV DC | | | | ±1 | % |
| | | 10mV ≤ \|$V_{SENSE}$\| ≤ 50mV DC, $V_{SENSE}$ + ≤ 4.2V | ● | | | ±1.5 | % |
| | | 1mV ≤ \|$V_{SENSE}$\| < 50mV DC (Note 8) | ● | | | ±3.5 | % |
| **Voltage Measurement ADC** | | | | | | | |
| | Resolution (No Missing Codes) | (Note 8) | ● | 14 | | | Bits |
| $V_{FS}$ | Full-Scale Voltage | | ● | | 6 | | V |
| $\Delta V_{LSB}$ | Quantization Step of 14-Bit Voltage ADC | (Note 6) | | | 366.2 | | µV |
| $TUE_V$ | Voltage Total Unadjusted Error | | <br>● | | | 1<br>1.3 | %<br>% |
| Gain | Gain Accuracy | | ● | | | 1.3 | % |
| $V_{OS}$ | Offset | Extrapolated from Measurements at 5.5V and 2.7V | | | ±1 | ±10 | LSB |
| INL | Integral Nonlinearity | | ● | | ±1 | ±4 | LSB |
| $t_{CONV}$ | Conversion Time | | ● | | | 15 | ms |
| **Temperature Measurement ADC** | | | | | | | |
| | Resolution (No Missing Code) | (Note 8) | | 10 | | | Bits |
| $T_{FS}$ | Full-Scale Temperature | | ● | | 600 | | K |
| $\Delta T_{LSB}$ | Quantization Step of 10-Bit Temperature ADC | (Note 6) | | | 0.586 | | K |
| $TUE_T$ | Temperature Total Unadjusted Error | $V_{SENSE+}$ ≥ 2.8V (Note 8) | <br>● | | | ±5<br>±3 | K<br>K |
| $t_{CONV}$ | Conversion Time | | ● | | | 15 | ms |
| **Digital Inputs and Digital Outputs** | | | | | | | |
| $V_{ITH}$ | Logic Input Threshold, $\overline{AL}$/CC, SCL, SDA | | ● | 0.3 • $V_{SENSE+}$ | | 0.7 • $V_{SENSE+}$ | V |
| $V_{OL}$ | Low Level Output Voltage, $\overline{AL}$/CC, SDA | I = 3mA | ● | | | 0.4 | V |
| $I_{IN}$ | Input Leakage, $\overline{AL}$/CC, SCL, SDA | $V_{IN}$ = $V_{SENSE+}$/2 | ● | | | 1 | µA |
| $C_{IN}$ | Input Capacitance, $\overline{AL}$/CC, SCL, SDA | (Note 8) | ● | | | 10 | pF |
| $t_{PCC}$ | Minimum Charge Complete (CC) Pulse Width | | | | | 1 | µs |
| **I²C Timing Characteristics** | | | | | | | |
| $f_{SCL(MAX)}$ | Maximum SCL Clock Frequency | | ● | 400 | 900 | | kHz |
| $t_{BUF(MIN)}$ | Bus Free Time Between STOP/START | | ● | | | 1.3 | µs |
| $t_{SU,STA(MIN)}$ | Minimum Repeated START Set-Up Time | | ● | | | 600 | ns |
| $t_{HD,STA(MIN)}$ | Minimum Hold Time (Repeated) START Condition | | ● | | | 600 | ns |
| $t_{SU,STO(MIN)}$ | Minimum Set-Up Time for STOP Condition | | ● | | | 600 | ns |
| $t_{SU,DAT(MIN)}$ | Minimum Data Set-Up Time Input | | ● | | | 100 | ns |
| $t_{HD,DATI(MIN)}$ | Minimum Data Hold Time Input | | ● | | | 0 | µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{HD,DATO}$ | Data Hold Time Output | | ● | 0.3 | | 0.9 | µs |
| $t_{OF}$ | Data Output Fall Time | (Notes 7, 8) | ● | 20 + 0.1 • $C_B$ | | 300 | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive, all voltages are referenced to GND unless otherwise specified

**Note 3:** $I_{SUPPLY} = I_{SENSE+} + I_{SENSE-}$

**Note 4:** The equivalent charge of an LSB in the accumulated charge register depends on the value of $R_{SENSE}$ and the setting of the internal prescaling factor M:

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{128}$$

See Choosing $R_{SENSE}$ and Choosing Coulomb Counter Prescaler M section for more information. 1mAh = 3.6C (coulombs).

**Note 5:** Deviation of $q_{LSB}$ from its nominal value.

**Note 6:** The quantization step of the 14-bit ADC in voltage mode and 10-bit ADC in temperature mode is not to be mistaken with the LSB of the combined 16-bit voltage registers (I, J) and 16-bit temperature registers (M, N).

**Note 7:** $C_B$ = Capacitance of one bus line in pF (10pF ≤ $C_B$ ≤ 400pF). See Voltage and Temperature Registers section for more information.

**Note 8:** Guaranteed by design, not subject to test.

## TIMING DIAGRAM

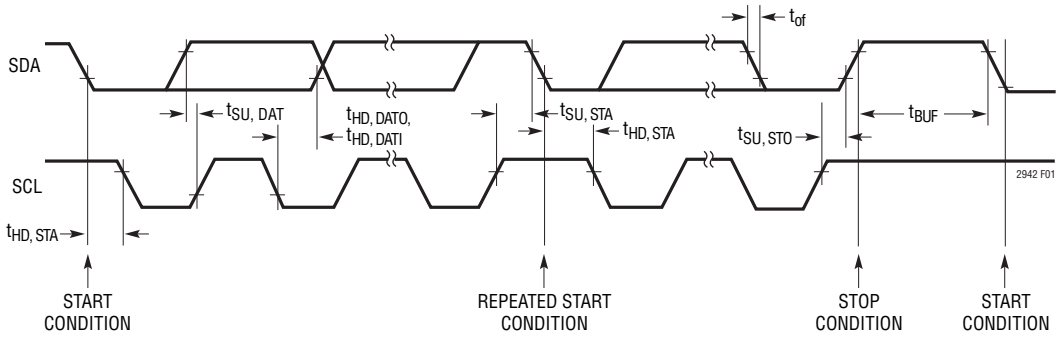
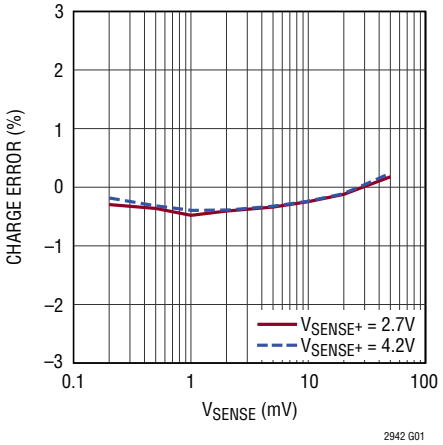


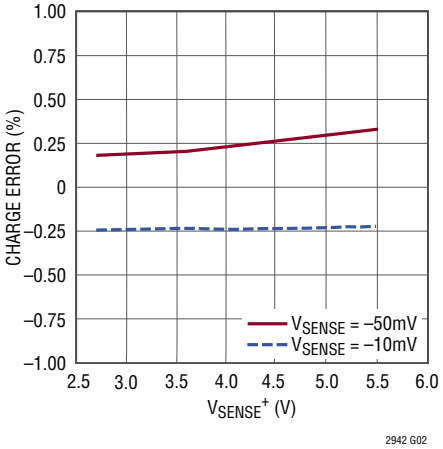

**Figure 1. Definition of Timing on $I^2C$ Bus**

# TYPICAL PERFORMANCE CHARACTERISTICS

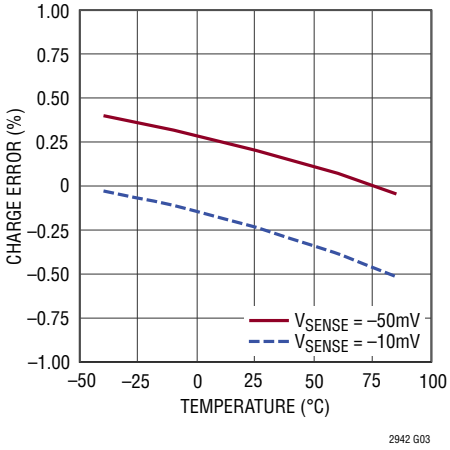
### Total Charge Error vs Differential Sense Voltage



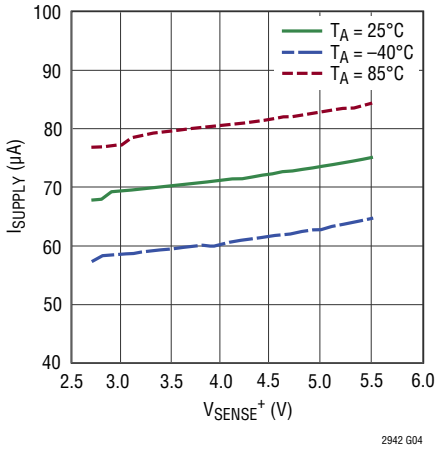

### Total Charge Error vs Supply Voltage



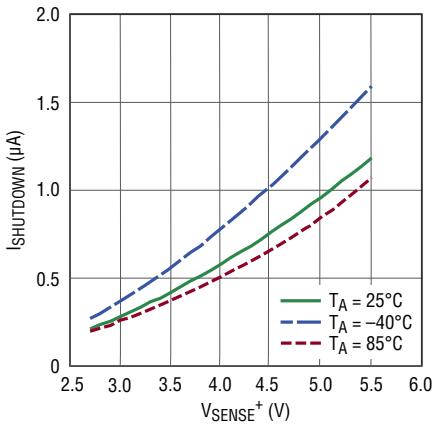

### Total Charge Error vs Temperature



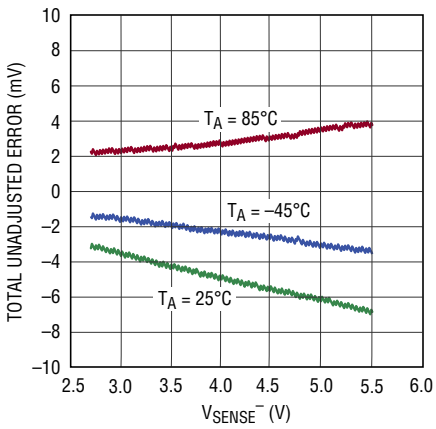

### Supply Current vs Supply Voltage



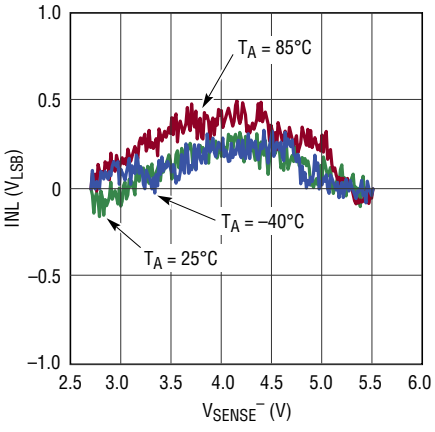

### Shutdown Supply Current vs Supply Voltage



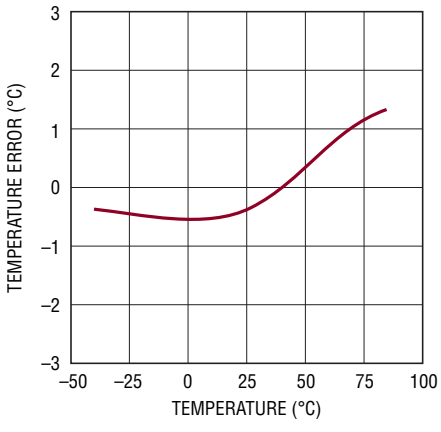

### Voltage Measurement ADC Total Unadjusted Error




### Voltage Measurement ADC Integral Nonlinearity




### Temperature Error vs Temperature



## PIN FUNCTIONS

**SENSE+ (Pin 1):** Positive Current Sense Input and Power Supply. Connect to the load/charger side of the sense resistor. $V_{SENSE^+}$ operating range is 2.7V to 5.5V.

**GND (Pin 2):** Device Ground. Connect directly to the negative battery terminal.

**SCL (Pin 3):** Serial Bus Clock Input.

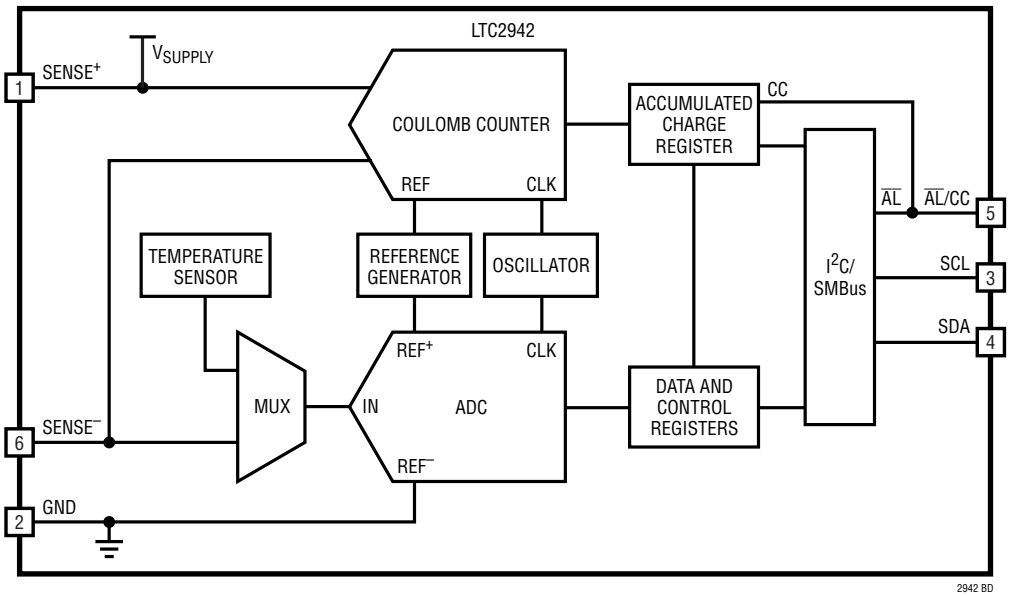
**SDA (Pin 4):** Serial Bus Data Input and Output.

**$\overline{AL}$/CC (Pin 5):** Alert Output or Charge Complete Input. Configured either as an SMBus alert output or charge complete input by control register bits B[2:1]. At power-up, the pin defaults to alert mode conforming to the SMBus alert response protocol. It behaves as an open-drain logic output that pulls to GND when any threshold register value is exceeded. When configured as a charge complete input, connect to the charge complete output from the battery charger circuit. A high level at CC sets the value of the accumulated charge (registers C, D) to FFFFh.

**SENSE– (Pin 6):** Negative Current Sense Input. Connect SENSE– to the positive battery terminal side of the sense resistor. The voltage between SENSE– and SENSE+ must remain within ±50mV in normal operation. SENSE– is also the input for the ADC in voltage measurement mode.

**Exposed Pad (Pin 7):** Do Not Connect.

## BLOCK DIAGRAM



# OPERATION

## Overview

The LTC2942 is a battery gas gauge device designed for use with single Li-Ion cells and other battery types with a terminal voltage at 2.7V to 5.5V. It measures battery charge and discharge, battery voltage and chip temperature.

A precision coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. Battery voltage and on-chip temperature are measured with an internal 14-bit/10-bit ADC.

## Coulomb Counter

Charge is the time integral of current. The LTC2942 measures battery current by monitoring the voltage developed across a sense resistor and then integrates this information to infer charge. The differential voltage between $SENSE^+$ and $SENSE^-$ is applied to an auto-zeroed differential analog integrator to convert the measured current to charge.

When the integrator output ramps to REFHI or REFLO levels, switches S1, S2, S3 and S4 toggle to reverse the ramp direction. By observing the condition of the switches and the ramp direction, polarity is determined.

A programmable prescaler effectively increases integration time by a factor M programmable from 1 to 128. At each underflow or overflow of the prescaler, the accumulated charge register (ACR) value is incremented or decremented one count. The value of accumulated charge is read via the $I^2C$ interface.

## Voltage and Temperature ADC

The LTC2942 includes a 14-bit No Latency ΔΣ analog-to-digital converter, with internal clock and voltage reference circuits.

The ADC can either be used to monitor the battery voltage at $SENSE^-$ or to convert the output of the on-chip temperature sensor. The sensor generates a voltage proportional to temperature with a slope of 2.5mV/K resulting in a voltage of 750mV at 27°C.

Conversion of either temperature or voltage is triggered by setting the control register via the $I^2C$ interface. The LTC2942 features an automatic mode where a voltage and a temperature conversion are executed every two seconds. At the end of each conversion the corresponding registers are updated and the converter goes to sleep to minimize quiescent current.

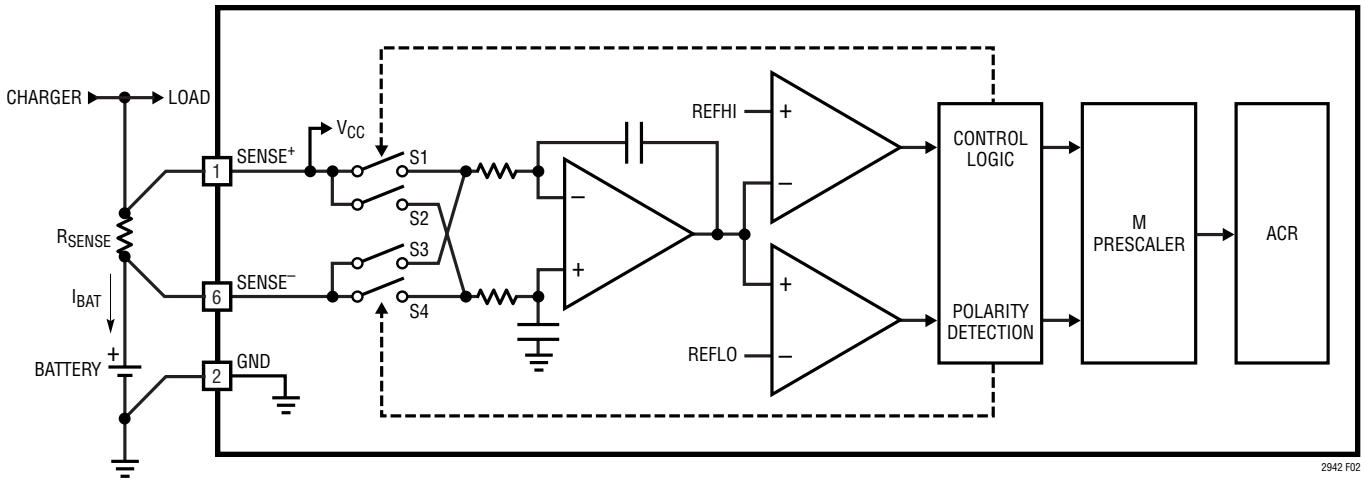



**Figure 2. Coulomb Counter Section of the LTC2942**

## OPERATION

### Power-Up Sequence

When SENSE+ rises above a threshold of approximately 2.5V, the LTC2942 generates an internal power-on reset (POR) signal and sets all registers to their default state. In the default state, the coulomb counter is active while the voltage and temperature ADC is switched off. The accumulated charge register is set to mid-scale (7FFFh), all low threshold registers are set to 0000h and all high threshold registers are set to FFFFh. The alert mode is enabled and the coulomb counter prescaling factor M is set to 128.

## APPLICATIONS INFORMATION

### I²C/SMBus Interface

The LTC2942 communicates with a bus master using a 2-wire interface compatible with I²C and SMBus. The 7-bit hard-coded **I²C address of the LTC2942 is 1100100**.

The LTC2942 is a slave-only device. Therefore the serial clock line (SCL) is an input only while the serial data line (SDA) is bidirectional. The device supports I²C standard and fast mode. For more details refer to the I²C Protocol section.

### Internal Registers

The LTC2942 integrates current through a sense resistor, measures battery voltage and temperature and stores the results in internal 16-bit registers accessible via I²C. High and low limits can be programmed for each measurement quantity. The LTC2942 continuously monitors these limits and sets a flag in the onboard status register when a limit is exceeded. If the alert mode is enabled, the $\overline{AL}$/CC pin pulls low.

The sixteen internal registers are organized as shown in Table 1.

**Table 1. Register Map**

| ADDRESS | NAME | REGISTER DESCRIPTION | R/W | DEFAULT |
|---|---|---|---|---|
| 00h | A | Status | R | See Below |
| 01h | B | Control | R/W | 3Ch |
| 02h | C | Accumulated Charge MSB | R/W | 7Fh |
| 03h | D | Accumulated Charge LSB | R/W | FFh |
| 04h | E | Charge Threshold High MSB | R/W | FFh |
| 05h | F | Charge Threshold High LSB | R/W | FFh |
| 06h | G | Charge Threshold Low MSB | R/W | 00h |
| 07h | H | Charge Threshold Low LSB | R/W | 00h |
| 08h | I | Voltage MSB | R | XXh |
| 09h | J | Voltage LSB | R | XXh |
| 0Ah | K | Voltage Threshold High | R/W | FFh |
| 0Bh | L | Voltage Threshold Low | R/W | 00h |
| 0Ch | M | Temperature MSB | R | XXh |
| 0Dh | N | Temperature LSB | R | XXh |
| 0Eh | O | Temperature Threshold High | R/W | FFh |
| 0Fh | P | Temperature Threshold Low | R/W | 00h |

R = Read, W = Write, XX = Unknown

## APPLICATIONS INFORMATION

### Status Register (A)

The status of the charge, voltage and temperature alerts is reported in the status register shown in Table 2.

**Table 2. Status Register A (Read only)**

| BIT | NAME | OPERATION | DEFAULT |
|---|---|---|---|
| A[7] | Chip Identification | 0: LTC2942<br>1: LTC2941 | 0 |
| A[6] | Reserved | | 0 |
| A[5] | Accumulated Charge Overflow/Underflow | Indicates that the value of the ACR hit either top or bottom. | 0 |
| A[4] | Temperature Alert | Indicates one of the temperature limits was exceeded. | 0 |
| A[3] | Charge Alert High | Indicates that the ACR value exceeded the charge threshold high limit. | 0 |
| A[2] | Charge Alert Low | Indicates that the ACR value dropped below the charge threshold low limit. | 0 |
| A[1] | Voltage Alert | Indicates one of the battery voltage limits was exceeded. | 0 |
| A[0] | Undervoltage Lockout Alert | Indicates recovery from undervoltage. If set to 1, a UVLO has occurred and the contents of the registers are uncertain. | X |

All status register bits except A[7] are cleared after being read by the host, if the conditions which set these bits have been removed.

As soon as one of the three measured quantities exceeds the programmed limits, the corresponding bit A[4], A[3], A[2] or A[1] in the status register is set.

Bit A[5] is set if the LTC2942's accumulated charge registers (ACR) overflows or underflows. In these cases, the ACR stays at FFFFh or 0000h and does not roll over.

The undervoltage lockout (UVLO) bit of the status register A[0] is set if, during operation, the voltage on $SENSE^+$ pin drops below 2.7V without reaching the POR level. The analog parts of the coulomb counter are switched off while the digital register values are retained. After recovery of the supply voltage the coulomb counter resumes integrating with the stored value in the accumulated charge registers but it has missed any charge flowing while $SENSE^+ < 2.7V$.

The hard-coded bit A[7] of the status register enables the host to distinguish the LTC2942 from the pin compatible LTC2941, allowing the same software to be used with both devices.

### Control Register (B)

The operation of the LTC2942 is controlled by programming the control register. Table 3 shows the organization of the 8-bit control register B[7:0].

**Table 3. Control Register B**

| BIT | NAME | OPERATION | Default |
|---|---|---|---|
| B[7:6] | ADC Mode | [11] Automatic Mode.<br>Performs voltage and temperature conversion every second.<br>[10] Manual Voltage Mode.<br>Performs single voltage conversion, then sleeps.<br>[01] Manual Temperature Mode.<br>Performs single temperature conversion, then sleeps.<br>[00] Sleep. | [00] |
| B[5:3] | Prescaler M | Sets coulomb counter prescaling factor M between 1 and 128.<br>Default is 128.<br>$M = 2^{(4 \bullet B[5] + 2 \bullet B[4] + B[3])}$ | [111] |
| B[2:1] | $\overline{AL}$/CC Configure | Configures the $\overline{AL}$/CC pin.<br>[10] Alert Mode.<br>Alert functionality enabled.<br>Pin becomes logic output.<br>[01] Charge Complete Mode.<br>Pin becomes logic input and accepts "charge complete" signal (e.g., from a charger) to set accumulated charge register (C, D) to FFFFh.<br>[00] $\overline{AL}$/CC pin disabled.<br>[11] Not allowed. | [10] |
| B[0] | Shutdown | Shut down analog section to reduce $I_{SUPPLY}$. | [0] |

### Power Down B[0]

Setting B[0] to 1 shuts down the analog parts of the LTC2942, reducing the current consumption to less than 1µA. All analog circuits are inoperative while the values in the registers are retained. Note that any charge flowing while B[0] is 1 is not measured and the charge information below 1LSB of the accumulated charge register is lost.

## APPLICATIONS INFORMATION

### Alert/Charge Complete Configuration B[2:1]

The $\overline{AL}$/CC pin is a dual function pin configured by the control register. By setting bits B[2:1] to [10] (default) the $\overline{AL}$/CC pin is configured as an alert pin following the SMBus protocol. In this configuration the $\overline{AL}$/CC pin is a digital output and is pulled low if one of the three measured quantities (charge, voltage, temperature) exceeds its high or low threshold or if the value of the accumulated charge register overflows or underflows. An alert response procedure started by the master resets the alert at the $\overline{AL}$/CC pin. For further information see the Alert Response Protocol section.

Setting the control bits B[2:1] to [01] configures the $\overline{AL}$/CC pin as a digital input. In this mode, a high input on the $\overline{AL}$/CC pin communicates to the LTC2942 that the battery is full and the accumulated charge register is set to its maximum value FFFFh. The $\overline{AL}$/CC pin would typically be connected to the "charge complete" output from the battery charger circuitry.

If neither the alert nor the charge complete functionality is desired, bits B[2:1] should be set to [00]. The $\overline{AL}$/CC pin is then disabled and should be tied to GND.

Avoid setting B[2:1] to [11] as it enables the alert and the charge complete modes simultaneously.

### Choosing $R_{SENSE}$

To achieve the specified precision of the coulomb counter, the differential voltage between $SENSE^+$ and $SENSE^-$ must stay within ±50mV. For differential input signals up to ±300mV the LTC2942 will remain functional but the precision of the coulomb counter is not guaranteed.

The required value of the external sense resistor, $R_{SENSE}$, is determined by the maximum input range of $V_{SENSE}$ and the maximum current of the application:

$$R_{SENSE} \leq \frac{50mV}{I_{MAX}}$$

The choice of the external sense resistor value influences the gain of the coulomb counter. A larger sense resistor gives a larger differential voltage between $SENSE^+$ and $SENSE^-$ for the same current which results in more precise coulomb counting. Thus the amount of charge represented by the least significant bit ($q_{LSB}$) of the accumulated charge (registers C, D) is equal to:

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{128}$$

or

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}}$$

when the prescaler is set to its default value of M = 128.

Note that 1mAh = 3.6C (coulomb).

Choosing $R_{SENSE}$ = 50mV/$I_{MAX}$ is not sufficient in applications where the battery capacity ($Q_{BAT}$) is very large compared to the maximum current ($I_{MAX}$):

$Q_{BAT} > I_{MAX} \bullet 5.5$ Hours

For such low current applications with a large battery, choosing $R_{SENSE}$ according to $R_{SENSE}$ = 50mV/$I_{MAX}$ can lead to a $q_{LSB}$ smaller than $Q_{BAT}/2^{16}$ and the 16-bit accumulated charge register may underflow before the battery is exhausted or overflow during charge. Choose, in this case, a maximum $R_{SENSE}$ of:

$$R_{SENSE} \leq \frac{0.085mAh \bullet 2^{16}}{Q_{BAT}} \bullet 50m\Omega$$

In an example application where the maximum current is $I_{MAX}$ = 100mA, calculating $R_{SENSE}$ = 50mV/$I_{MAX}$ would lead to a sense resistor of 500mΩ. This gives a $q_{LSB}$ of 8.5µAh and the accumulated charge register can represent a maximum battery capacity of $Q_{BAT}$ = 8.5µAh • 65535 = 557mAh. If the battery capacity is larger, $R_{SENSE}$ must be lowered. For example, $R_{SENSE}$ must be reduced to 150mΩ if a battery with a capacity of 1800mAh is used.

## APPLICATIONS INFORMATION

### Choosing Coulomb Counter Prescaler M B[5:3]

If the battery capacity ($Q_{BAT}$) is very small compared to the maximum current ($I_{MAX}$) ($Q_{BAT} < I_{MAX} \bullet 0.1$ Hours) the prescaler value M should be changed from its default value (128).

In these applications with a small battery but a high maximum current, $q_{LSB}$ can get quite large with respect to the battery capacity. For example, if the battery capacity is 100mAh and the maximum current is 1A, the standard equation leads to choosing a sense resistor value of 50mΩ, resulting in:

$q_{LSB} = 0.085mAh = 306mC$

The battery capacity then corresponds to only 1176 $q_{LSB}$s and less than 2% of the accumulated charge register is utilized.

To preserve digital resolution in this case, the LTC2942 includes a programmable prescaler. Lowering the prescaler factor M allows reducing $q_{LSB}$ to better match the accumulated charge register to the capacity of the battery. The prescaling factor M can be chosen between 1 and its default value 128. The charge LSB then becomes:

$$q_{LSB} = 0.085mAh \bullet \frac{50m\Omega}{R_{SENSE}} \bullet \frac{M}{128}$$

To use as much of the range of the accumulated charge register as possible the prescaler factor M should be chosen for a given battery capacity $Q_{BAT}$ and a sense resistor $R_{SENSE}$ as:

$$M \geq 128 \bullet \frac{Q_{BAT}}{2^{16} \bullet 0.085mAh} \bullet \frac{R_{SENSE}}{50m\Omega}$$

M can be set to 1, 2, 4, 8, … 128 by programming B[5:3] of the control register as $M = 2^{(4 \bullet B[5] + 2 \bullet B[4] + B[3])}$. The default value after power up is $M = 128 = 2^7$ (B[5:3] = 111).

In the above example of a 100mAh battery and an $R_{SENSE}$ of 50mΩ, the prescaler should be programmed to M = 4. The $q_{LSB}$ then becomes 2.656µAh and the battery capacity corresponds to roughly 37650 $q_{LSB}$s.

Note that the internal digital resolution of the coulomb counter is higher than indicated by $q_{LSB}$. The digitized charge $q_{INTERNAL}$ is M • 8 times smaller than $q_{LSB}$. $q_{INTERNAL}$ is typically 299µAs for a 50mΩ sense resistor.

### ADC Mode B[7:6]

The LTC2942 features an ADC which measures either voltage on SENSE⁻ (battery voltage) or temperature via an internal temperature sensor. The reference voltage and clock for the ADC are generated internally.

The ADC has four different modes of operation, as shown in Table 3. These modes are controlled by bits B[7:6] of the control register. At power-up, bits B[7:6] are set to [00] and the ADC is in sleep mode.

A single voltage conversion is initiated by setting the bits B[7:6] to [10]. A single temperature conversion is started by setting bits B[7:6] to [01]. After a single voltage or temperature conversion, the ADC resets B[7:6] to [00] and goes to sleep.

The LTC2942 also offers an automatic scan mode where the ADC converts voltage, then temperature, then sleeps for approximately two seconds before repeating the voltage and temperature conversions. The LTC2942 is set to this automatic mode by setting B[7:6] to [11] and stays in this mode until B[7:6] are reprogrammed by the host.

Programming B[7:6] to [00] puts the ADC to sleep. If control bits B[7:6] change within a conversion, the ADC will complete the current conversion before entering the newly selected mode.

A conversion of either voltage or temperature requires 10ms conversion time (typical). At the end of each conversion, the corresponding registers are updated. If the converted quantity exceeds the values programmed in the threshold registers, a flag is set in the status register and the $\overline{AL}$/CC pin is pulled low (if alert mode is enabled).

During a voltage conversion, the SENSE⁻ pin is connected through a small resistor to a sampling circuit with an equivalent resistance of 2MΩ, leading to a mean input current of $I = V_{SENSE^-}/2M\Omega$.

## APPLICATIONS INFORMATION

### Accumulated Charge Register (C, D)

The coulomb counter of the LTC2942 integrates current through the sense resistor. The result of this charge integration is stored in the 16-bit accumulated charge register (registers C, D). As the LTC2942 does not know the actual battery status at power-up, the accumulated charge register (ACR) is set to mid-scale (7FFFh). If the host knows the status of the battery, the accumulated charge (C[7:0]D[7:0]) can be either programmed to the correct value via I²C or it can be set after charging to FFFFh (full) by pulling the $\overline{AL}$/CC pin high if charge complete mode is enabled via bits B[2:1]. Before writing the accumulated charge registers, the analog section should be shut down by setting B[0] to 1. In order to avoid a change in the accumulated charge registers between reading MSBs C[7:0] and LSBs D[7:0], it is recommended to read them sequentially, as shown in Figure 10.

### Voltage and Temperature Registers (I, J), (M, N)

The result of the 14-bit ADC conversion of the voltage at SENSE⁻ is stored in the voltage registers (I, J), whereas the temperature measurement result is stored in the temperature registers (M, N). The voltage and temperature registers are read only.

As the ADC resolution is 14-bit in voltage mode and 10-bit in temperature mode, the lowest two bits of the combined voltage registers (I, J) and the lowest six bits of the combined temperature registers (M, N) are always zero. From the result of the 16-bit voltage registers I[7:0]J[7:0] the measured voltage can be calculated as:

$$V_{SENSE^-} = 6V \bullet \frac{RESULT_h}{FFFF_h} = 6V \bullet \frac{RESULT_{DEC}}{65535}$$

Example: a register value of I[7:0] = $B0_h$ and J[7:0] = $1C_h$ corresponds to a voltage on SENSE⁻ of:

$$V_{SENSE^-} = 6V \bullet \frac{B01C_h}{FFFF_h} = 6V \bullet \frac{45084_{DEC}}{65535} \approx 4.1276V$$

The actual temperature can be obtained from the two byte register C[7:0]D[7:0] by:

$$T = 600K \bullet \frac{RESULT_h}{FFFF_h} = 600K \bullet \frac{RESULT_{DEC}}{65535}$$

Example: a register value of C[7:0] = $80_h$ D[7:0] = $00_h$ corresponds to 300K or 27°C.

### Threshold Registers (E, F, G, H, K, L, O, P)

For each of the measured quantities (battery charge, voltage and temperature) the LTC2942 features a high and a low threshold registers. At power-up, the high thresholds are set to FFFFh while the low thresholds are set to 0000h. All thresholds can be programmed to a desired value via I²C. As soon as a measured quantity exceeds the high threshold or falls below the low threshold, the LTC2942 sets the corresponding flag in the status register and pulls the $\overline{AL}$/CC pin low if alert mode is enabled via bits B[2:1]. Note that the voltage and temperature threshold registers are single-byte registers and only the 8 MSBs of the corresponding quantity are checked. To set a low level threshold for the battery voltage of 3V, register L should be programmed to 80h; a high temperature limit of 60°C is programmed by setting register O to 8Eh.

### I²C Protocol

The LTC2942 uses an I²C/SMBus compatible 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the bus wires LOW and they never drive the bus HIGH. The bus wires must be externally connected to a positive supply voltage via a current source or pull-up resistor. When the bus is idle, both SDA and SCL are HIGH. Data on the I²C bus can be transferred at rates of up to 100kbit/s in standard mode and up to 400kbit/s in fast mode.

Each device on the I²C/SMBus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be classified as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device ad-

## APPLICATIONS INFORMATION

dressed is considered a slave. The LTC2942 always acts as a slave.

Figure 3 shows an overview of the data transmission for fast and standard mode on the I²C bus.

### START and STOP Conditions

When the bus is idle, both SCL and SDA must be HIGH. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from HIGH to LOW while SCL is HIGH. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

### Data Transmission

After a START condition, the I²C bus is considered busy and data transfer begins between a master and a slave. As data is transferred over I²C in groups of nine bits (eight data bits followed by an acknowledge bit), each group takes nine SCL cycles. The transmitter releases the SDA line during the acknowledge clock pulse and the receiver issues an acknowledge (ACK) by pulling SDA LOW or leaves SDA HIGH to indicate a not acknowledge (NACK) condition. Change of data state can only happen while SCL is LOW.

### Write Protocol

The master begins a write operation with a START condition followed by the seven bit slave **address 1100100** and the R/$\overline{W}$ bit set to zero, as shown in Figure 4. The LTC2942 acknowledges this by pulling SDA LOW and then the master sends a command byte which indicates which internal register the master is to write. The LTC2942 acknowledges and latches the command byte into its internal register address pointer. The master delivers the data byte, the LTC2942 acknowledges once more and latches the data into the desired register. The transmission is ended when the master sends a STOP condition. If the master continues by sending a second data byte instead of a STOP, the LTC2942 acknowledges again, increments its address pointer and latches the second data byte in the following register, as shown in Figure 5.

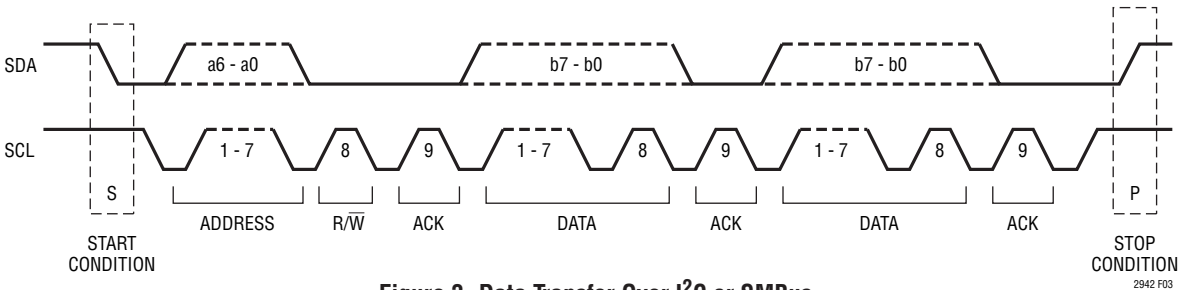



**Figure 3. Data Transfer Over I²C or SMBus**

| S | ADDRESS | $\overline{W}$ | A | REGISTER | A | DATA | A | P |
|---|---|---|---|---|---|---|---|---|
| | 1100100 | 0 | 0 | 01h | 0 | FCh | 0 | |

2942 F04

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
S: START CONDITION
P: STOP CONDITION
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)

**Figure 4. Writing FCh to the LTC2942 Control Register (B)**

| S | ADDRESS | $\overline{W}$ | A | REGISTER | A | DATA | A | DATA | A | P |
|---|---|---|---|---|---|---|---|---|---|---|
| | 1100100 | 0 | 0 | 02h | 0 | F0h | 0 | 01h | 0 | |

2942 F05

**Figure 5. Writing F001h to the LTC2942 Accumulated Charge Register (C, D)**

## APPLICATIONS INFORMATION

### Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave **address 1100100** and the R/$\overline{W}$ bit set to zero, as shown in Figure 6. The LTC2942 acknowledges and then the master sends a command byte which indicates which internal register the master is to read. The LTC2942 acknowledges and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/$\overline{W}$ bit now set to one. The LTC2942 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, the LTC2942 increments its address pointer and sends the contents of the following register as depicted in Figure 7.

### Alert Response Protocol

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt (Figure 8).

| S | ADDRESS | $\overline{W}$ | A | REGISTER | A | S | ADDRESS | R | A | DATA | $\overline{A}$ | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1100100 | 0 | 0 | 00h | 0 | | 1100100 | 1 | 0 | 01h | 1 | |

2942 F06

**Figure 6. Reading the LTC2942 Status Register (A)**

| S | ADDRESS | $\overline{W}$ | A | REGISTER | A | S | ADDRESS | R | A | DATA | A | DATA | $\overline{A}$ | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1100100 | 0 | 0 | 08h | 0 | | 1100100 | 1 | 0 | F1h | 0 | 24h | 1 | |

2942 F07

**Figure 7. Reading the LTC2942 Voltage Register (I, J)**

| S | ALERT RESPONSE ADDRESS | R | A | DEVICE ADDRESS | $\overline{A}$ | P |
|---|---|---|---|---|---|---|
| | 0001100 | 1 | 0 | 11001001 | 1 | |

2942 F08

**Figure 8. LTC2942 Serial Bus SDA Alert Response Protocol**

| S | ADDRESS | $\overline{W}$ | A | REGISTER | A | DATA | P | ←10ms→ | S | ADDRESS | $\overline{W}$ | A | REGISTER | A | S | ADDRESS | R | A | DATA | A | DATA | $\overline{A}$ | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1100100 | 0 | 0 | 01h | 0 | BC | | | | 1100100 | 0 | 0 | 08h | 0 | | 1100100 | 1 | 0 | F1h | 0 | 80h | 1 | |

2942 F09

**Figure 9. Voltage Conversion Sequence**

| S | ADDRESS | $\overline{W}$ | A | REGISTER | A | S | ADDRESS | R | A | DATA | A | DATA | $\overline{A}$ | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1100100 | 0 | 0 | 02h | 0 | | 1100100 | 1 | 0 | 80h | 0 | 01h | 1 | |

2942 F10

**Figure 10. Reading the LTC2942 Accumulated Charge Registers (C, D)**

## APPLICATIONS INFORMATION

The master initiates the ARA procedure with a START condition and the special **7-bit ARA bus address (0001100)** followed by the read bit (R) = 1. If the LTC2942 is asserting the $\overline{AL}$/CC pin in alert mode, it acknowledges and responds by sending its **7-bit bus address (1100100)** and a 1. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard $I^2C$ bus arbitration. If the LTC2942 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LTC2942 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LTC2942 will stop pulling down the $\overline{AL}$/CC pin and will not respond to further ARA requests until a new Alert event occurs.

### PC Board Layout Suggestions

Keep all traces as short as possible to minimize noise and inaccuracy. Use a 4-wire Kelvin sense connection for the sense resistor, locating the LTC2942 close to the resistor with short sense traces to the $SENSE^+$ and $SENSE^-$ pins. Use wider traces from the resistor to the battery, load and/or charger (see Figure 11). Put the bypass capacitor close to $SENSE^+$ and GND.

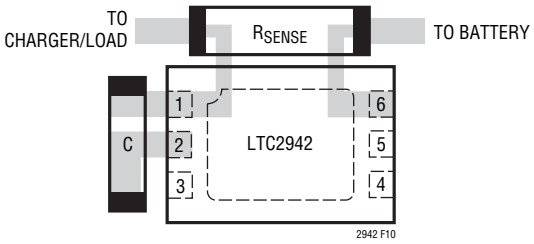
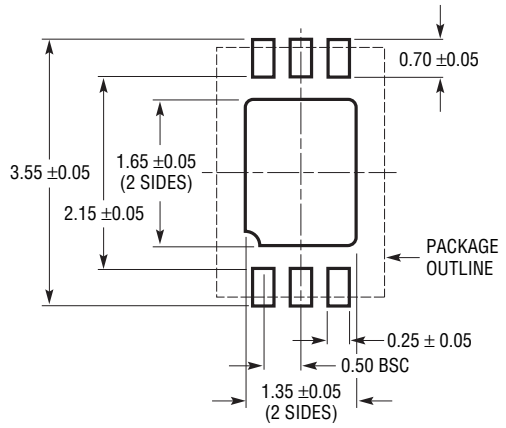



**Figure 11. Kelvin Connection on Sense Resistor**

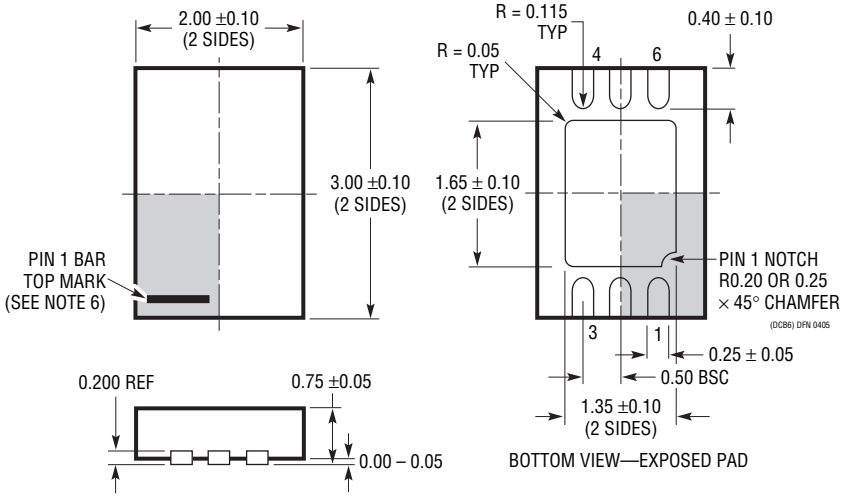
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**DCB Package**
**6-Lead Plastic DFN (2mm × 3mm)**
(Reference LTC DWG # 05-08-1715)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 8/10 | Revised Exposed Pad description in the Pin Configuration and Pin Functions sections. | 2, 6 |