Wide Range I²C Power Monitor

FEATURES

- **Rail-to-Rail Input Range: 0V to 80V**
- **Wide Input Supply Range: 2.7V to 80V**
- **Shunt Regulator for Supplies >80V**
- **ΔΣ ADC with less than ±0.75% Total Unadjusted Error**
- 12-Bit Resolution for Current and Voltages
- Internal Multiplier Calculates 24-Bit Power Value
- Stores Minimum and Maximum Values
- Alerts When Limits Exceeded
- Additional ADC Input Monitors an External Voltage
- Continuous Scan and Snapshot Modes
- Shutdown Mode with I_Q < 80µA
- Split SDA for Opto-Isolation
- Available in 12-Lead 3mm × 3mm QFN and MSOP Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Telecom Infrastructure
- Industrial
- Automotive
- Consumer

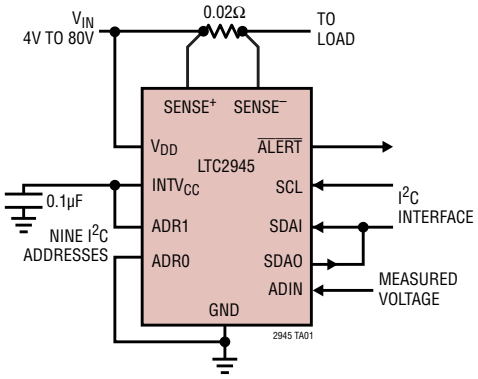
DESCRIPTION

The LTC®2945 is a rail-to-rail system monitor that measures current, voltage, and power. It features an operating range of 2.7V to 80V and includes a shunt regulator for supplies above 80V to allow flexibility in the selection of input supply. The current measurement range of 0V to 80V is independent of the input supply. An onboard 0.75% accurate 12-bit ADC measures load current, input voltage and an auxiliary external voltage. A 24-bit power value is generated by digitally multiplying the measured 12-bit load current and input voltage data. Minimum and maximum values are stored and an overrange alert with programmable thresholds minimizes the need for software polling. Data is reported via a standard I²C interface. Shutdown mode reduces power consumption to 20µA.

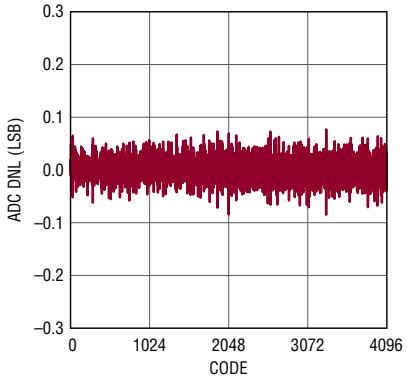
The LTC2945 I²C interface includes separate data input and output pins for use with standard or opto-isolated I²C connections. The LTC2945-1 has an inverted data output for use with inverting opto-isolator configurations.

TYPICAL APPLICATION

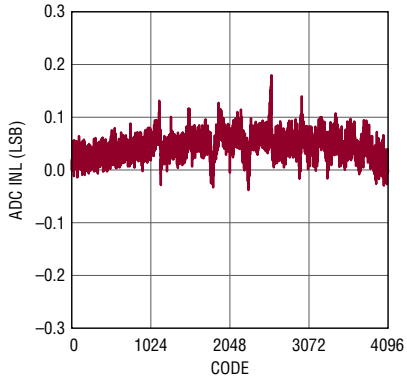
Wide Range Power Monitor with Onboard ADC and I²C



ADC Differential Nonlinearity (ADIN)



ADC Integral Nonlinearity (ADIN)



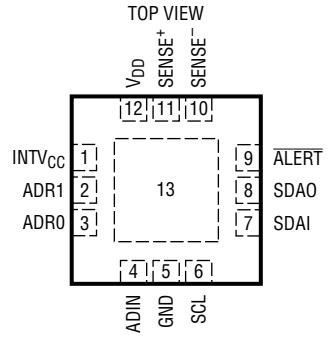
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

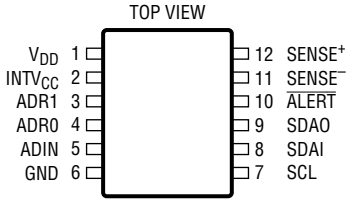
V_{DD} Voltage ..... –0.3V to 100V
$SENSE^+$ Voltage ..... –1V to 100V
$SENSE^-$ Voltage .....–1V or $SENSE^+$ – 1V to $SENSE^+$ + 1V
$INTV_{CC}$ Voltage (Note 3) ..... –0.3V to 5.9V
ADR1, ADR0, ADIN, $\overline{ALERT}$, SDAO, $\overline{SDAO}$ Voltage ..... –0.3V to 7V
$INTV_{CC}$ Clamp Current 35mA
SCL, SDAI Voltages (Note 4)..... –0.3V to 5.9V
SCL, SDAI Clamp Current 5mA
Operating Temperature Range
LTC2945C..... 0°C to 70°C
LTC2945I .....–40°C to 85°C
LTC2945H..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec)
MS Package Only.....300°C

PIN CONFIGURATION

LTC2945

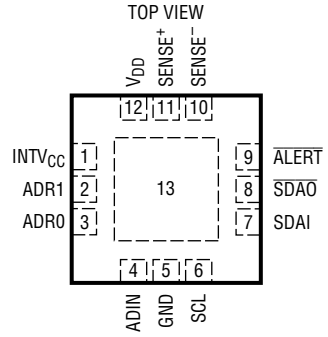


UD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 58.7°C/W
EXPOSED PAD (PIN 13) PCB GND CONNECTION OPTIONAL



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

LTC2945-1



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12-LEAD (3mm × 3mm) PLASTIC QFN
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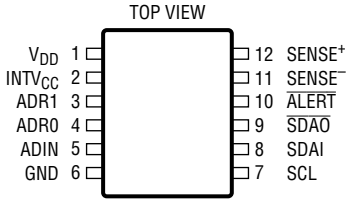
EXPOSED PAD (PIN 13) PCB GND CONNECTION OPTIONAL



MS PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2945CUD#PBF	LTC2945CUD#TRPBF	LFWK	12-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC2945IUD#PBF	LTC2945IUD#TRPBF	LFWK	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC2945HUD#PBF	LTC2945HUD#TRPBF	LFWK	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC2945CUD-1#PBF	LTC2945CUD-1#TRPBF	LFYX	12-Lead (3mm × 3mm) Plastic QFN	0°C to 70°C
LTC2945IUD-1#PBF	LTC2945IUD-1#TRPBF	LFYX	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C
LTC2945HUD-1#PBF	LTC2945HUD-1#TRPBF	LFYX	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC2945CMS#PBF	LTC2945CMS#TRPBF	2945	12-Lead Plastic MSOP	0°C to 70°C
LTC2945IMS#PBF	LTC2945IMS#TRPBF	2945	12-Lead Plastic MSOP	–40°C to 85°C
LTC2945HMS#PBF	LTC2945HMS#TRPBF	2945	12-Lead Plastic MSOP	–40°C to 125°C
LTC2945CMS-1#PBF	LTC2945CMS-1#TRPBF	29451	12-Lead Plastic MSOP	0°C to 70°C
LTC2945IMS-1#PBF	LTC2945IMS-1#TRPBF	29451	12-Lead Plastic MSOP	–40°C to 85°C
LTC2945HMS-1#PBF	LTC2945HMS-1#TRPBF	29451	12-Lead Plastic MSOP	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC2945HUD#WPBF	LTC2945HUD#WTRPBF	LFWK	12-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 4V to 80V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLIES							
V_{DD}	V_{DD} Supply Voltage Range		●	4		80	V
V_{INTVCC}	$INTV_{CC}$ Supply Voltage Range		●	2.7		5.9	V
I_{DD}	V_{DD} Supply Current	V_{DD} = 48V, $INTV_{CC}$ Open Shutdown	● ●		0.8 40	1.2 70	mA µA
I_{CC}	$INTV_{CC}$ Supply Current	$INTV_{CC}$ = V_{DD} = 5V Shutdown, $INTV_{CC}$ = V_{DD} = 5V	● ●		0.6 20	0.9 80	mA µA
I_{CCSRC}	$INTV_{CC}$ Linear Regulator Output Current	V_{DD} = 7V	●			–10	mA
V_{CC}	$INTV_{CC}$ Linear Regulator Voltage	7V < V_{DD} < 80V, I_{LOAD} = 1mA (C-, I-Grade) 7V < V_{DD} < 80V, I_{LOAD} = 1mA (H-Grade)	● ●	4.5 4.5	5 5	5.5 5.7	V V
ΔV_{CC}	$INTV_{CC}$ Linear Regulator Load Regulation	7V < V_{DD} < 80V, I_{LOAD} = 1mA to 10mA	●		100	200	mV
V_{CCZ}	$INTV_{CC}$ Shunt Regulator Voltage	V_{DD} = 48V, I_{CC} = 1mA	●	5.9	6.3	6.7	V
ΔV_{CCZ}	$INTV_{CC}$ Shunt Regulator Load Regulation	V_{DD} = 48V, I_{CC} = 1mA to 35mA	●			250	mV
$V_{CC(UVL)}$	$INTV_{CC}$ Supply Undervoltage Lockout	$INTV_{CC}$ Rising, V_{DD} = $INTV_{CC}$	●	2.2	2.6	2.69	V
$V_{DD(UVL)}$	V_{DD} Supply Undervoltage Lockout	V_{DD} Rising, $INTV_{CC}$ Open (C-, I-Grade) V_{DD} Rising, $INTV_{CC}$ Open (H-Grade)	● ●	2.9 2.6	3.2 3.2	3.5 3.5	V V
$V_{DDI2C(RST)}$	V_{DD} I^2C Logic Reset	V_{DD} Falling, $INTV_{CC}$ Open (C-, I-Grade) V_{DD} Falling, $INTV_{CC}$ Open (H-Grade)	● ●	2 1.7	2.5 2.5		V V
$V_{CCI2C(RST)}$	$INTV_{CC}$ I^2C Logic Reset	$INTV_{CC}$ Falling, V_{DD} = $INTV_{CC}$	●	1.5	1.8		V
SENSE INPUTS							
V_{CM}	$SENSE^+$, $SENSE^-$ Common Mode Voltage		●	0		80	V
$I_{SENSE^+(HI)}$	48V $SENSE^+$ Input Current	$SENSE^+$, $SENSE^-$, V_{DD} = 48V Shutdown	● ●		100	150 2	µA µA
$I_{SENSE^-(HI)}$	48V $SENSE^-$ Input Current	$SENSE^+$, $SENSE^-$, V_{DD} = 48V Shutdown	● ●			20 1	µA µA
$I_{SENSE^+(LO)}$	0V $SENSE^+$ Source Current	$SENSE^+$, $SENSE^-$ = 0V V_{DD} = 48V Shutdown	● ●			–10 –2	µA µA
$I_{SENSE^-(LO)}$	0V $SENSE^-$ Source Current	$SENSE^+$, $SENSE^-$ = 0V, V_{DD} = 48V Shutdown	● ●			–5 ±1	µA µA
ADC							
RES	Resolution (No missing codes)	(Note 5)	●	12			Bits
V_{FS}	Full-Scale Voltage	ΔSENSE (Note 7) V_{IN} ADIN	● ● ●	101.7 101.7 2.033	102.4 102.4 2.048	103.1 103.1 2.063	mV V V
LSB	LSB Step Size	ΔSENSE V_{IN} ADIN			25 25 0.5		µV mV mV
TUE	Total Unadjusted Error (Note 6)	ΔSENSE V_{IN} ADIN	● ● ●			±0.75 ±0.75 ±0.75	% % %
V_{OS}	Offset Error	ΔSENSE V_{IN} ADIN	● ● ●			±3.1 ±1.5 ±1.1	LSB LSB LSB
INL	Integral Nonlinearity	ΔSENSE V_{IN} ADIN	● ● ●			±3 ±2 ±2	LSB LSB LSB
σ_T	Transition Noise (Note 5)	ΔSENSE V_{IN} ADIN			1.2 0.3 10		μV_{RMS} mV_{RMS} μV_{RMS}

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 4V to 80V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{CONV}	Conversion Rate (Continuous Mode)		●	6	7.5	9	Hz
t_{CONV}	Conversion Time (Snapshot Mode)	ΔSENSE V_{IN}, ADIN	● ●	60 30	66 33	72 36	ms ms
R_{ADIN}	ADIN Pin Input Resistance	V_{DD} = 48V, ADIN = 3V	●	3	10		MΩ
I_{ADIN}	ADIN Pin Input Current	V_{DD} = 48V, ADIN = 3V	●			±1	µA
I²C INTERFACE (V_{DD} = 48V)							
$V_{ADR(H)}$	ADR0, ADR1 Input High Threshold		●	2.1	2.4	2.7	V
$V_{ADR(L)}$	ADR0, ADR1 Input Low Threshold		●	0.3	0.6	0.9	V
$I_{ADR(IN)}$	ADR0, ADR1 Input Current	ADR0, ADR1 = 0V, 3V	●			±13	µA
$I_{ADR(IN,Z)}$	Allowable Leakage When Open		●			±7	µA
$V_{OD(OL)}$	SDAO, $\overline{SDAO}$, $\overline{ALERT}$ Output Low Voltage	I_{SDAO}, $I_{\overline{SDAO}}$, $I_{\overline{ALERT}}$ = 8mA	●		0.15	0.4	V
$I_{SDA,SCL(IN)}$	SDAI, SDAO, $\overline{SDAO}$, SCL Input Current	SDAI, SDAO, $\overline{SDAO}$, SCL = 5V	●		0	±1	µA
$V_{SDA,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.5	1.9	2.2	V
$V_{SDA,SCL(CL)}$	SDAI, SCL Clamp Voltage	I_{SDAI}, I_{SCL} = 3mA	●	5.9	6.4	6.9	V
$I_{\overline{ALERT}(IN)}$	$\overline{ALERT}$ Input Current	$\overline{ALERT}$ = 5V	●		0	±1	µA
I²C INTERFACE TIMING							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency			400			kHz
t_{LOW}	Minimum SCL Low Period				0.65	1.3	µs
t_{HIGH}	Minimum SCL High Period				50	600	ns
$t_{BUF(MIN)}$	Minimum Bus Free Time Between Stop/Start Condition				0.12	1.3	µs
$t_{HD,STA(MIN)}$	Minimum Hold Time After (Repeated) Start Condition				140	600	ns
$t_{SU,STA(MIN)}$	Minimum Repeated Start Condition Set-Up Time				30	600	ns
$t_{SU,STO(MIN)}$	Minimum Stop Condition Set-Up Time				30	600	ns
$t_{HD,DATI(MIN)}$	Minimum Data Hold Time Input				–100	0	ns
$t_{HD,DATO(MIN)}$	Minimum Data Hold Time Output			300	600	900	ns
$t_{SU,DAT(MIN)}$	Minimum Data Set-Up Time				30	100	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width			50	110	250	ns
t_{RST}	Stuck Bus Reset Time	SCL or SDAI Held Low		25	33		ms
C_X	SCL, SDAI Input Capacitance (Note 5)				5	10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive. All voltages are referenced to ground, unless otherwise noted.

Note 3: An internal shunt regulator limits the $INTV_{CC}$ pin to a minimum of 5.9V. Driving this pin to voltages beyond 5.9V may damage the part. This pin can be safely tied to higher voltages through a resistor that limits the current below 35mA.

Note 4: Internal clamps limit the SCL and SDAI pins to a minimum of 5.9V. Driving these pins to voltages beyond the clamp may damage the part. The pins can be safely tied to higher voltages through resistors that limit the current below 5mA.

Note 5: Guaranteed by design and not subject to test.

Note 6:

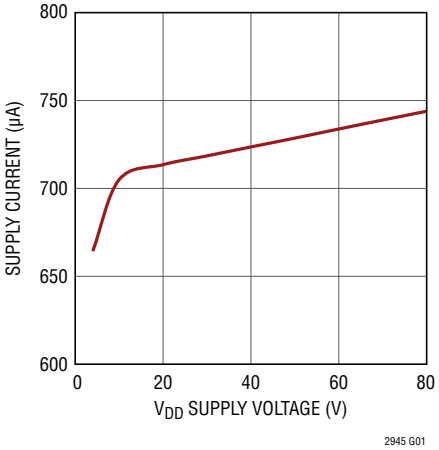
$$TUE = \frac{(ACTUAL\ CODE - IDEAL\ CODE)}{4096} \times 100\%$$

where IDEAL CODE is derived from a straight line passing through Code 0 at 0V and Theoretical Code of 4096 at V_{FS}.

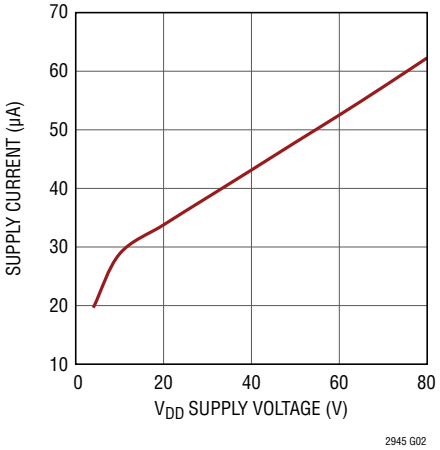
Note 7: ΔSENSE is defined as $V_{SENSE+} - V_{SENSE-}$

TYPICAL PERFORMANCE CHARACTERISTICS V_{DD} = 48V, T_A = 25°C, unless noted.

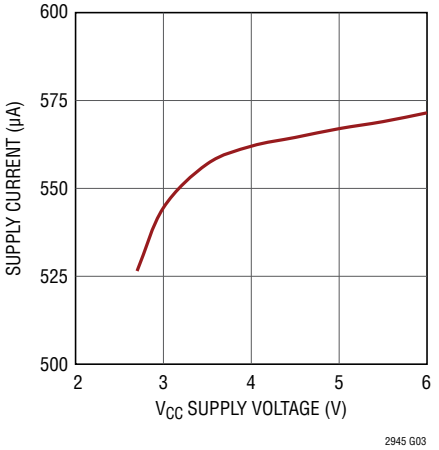
V_{DD} Supply Current



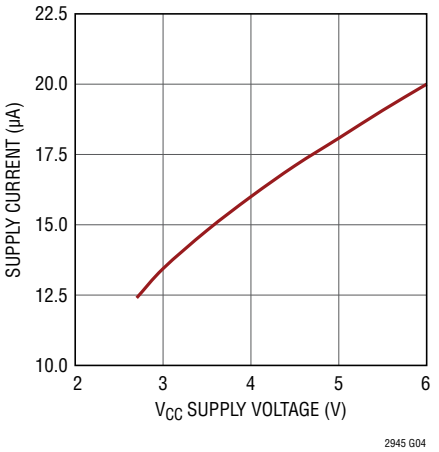
V_{DD} Supply Current in Shutdown



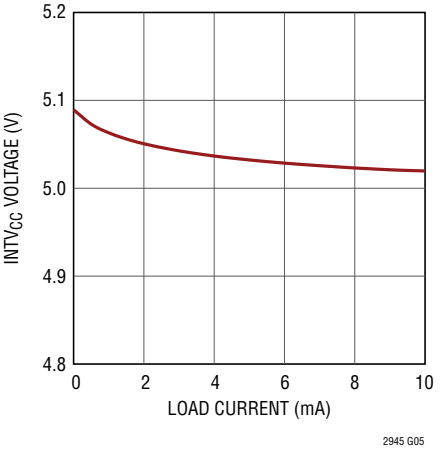
$INTV_{CC}$ Supply Current



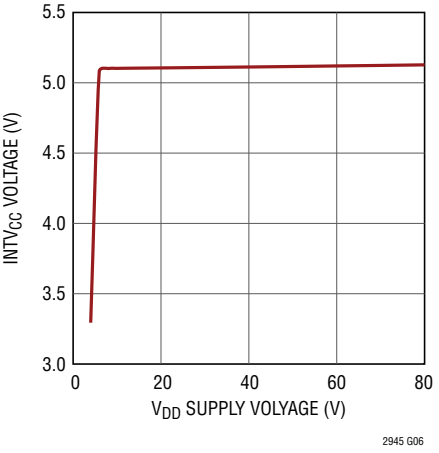
$INTV_{CC}$ Supply Current in Shutdown



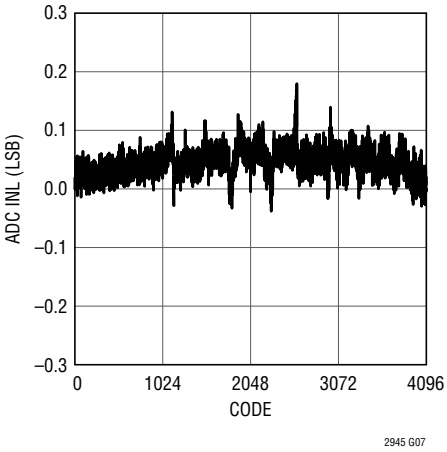
$INTV_{CC}$ Load Regulation



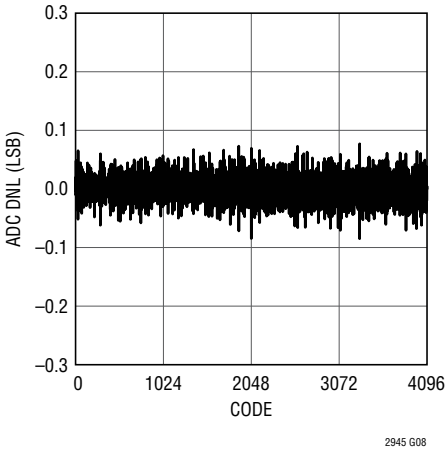
$INTV_{CC}$ Line Regulation



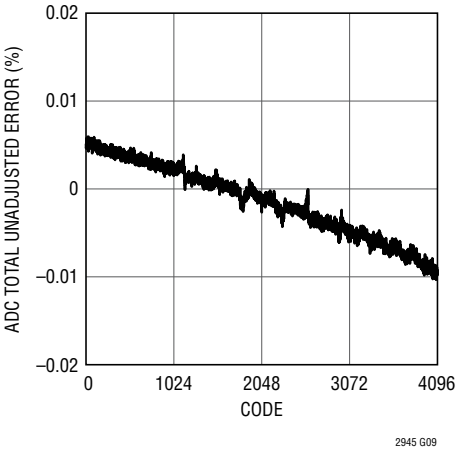
ADC Integral Nonlinearity (ADIN)



ADC Differential Nonlinearity (ADIN)

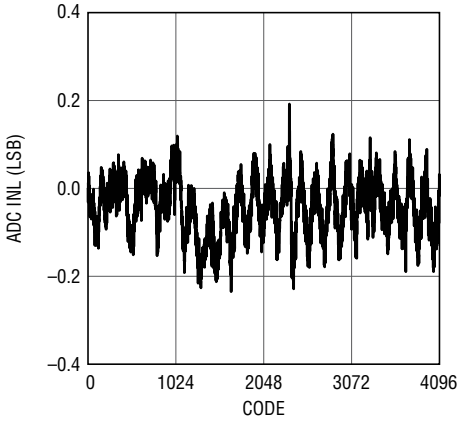


ADC Total Unadjusted Error (ADIN)

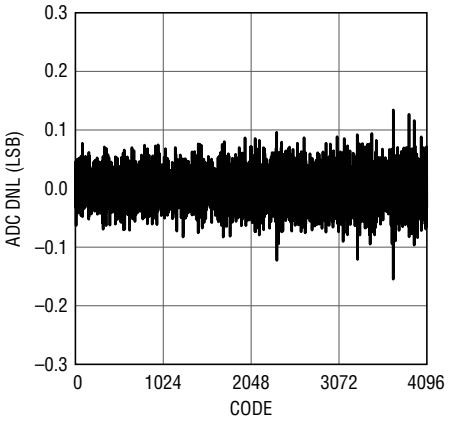


TYPICAL PERFORMANCE CHARACTERISTICS V_{DD} = 48V, T_A = 25°C, unless noted.

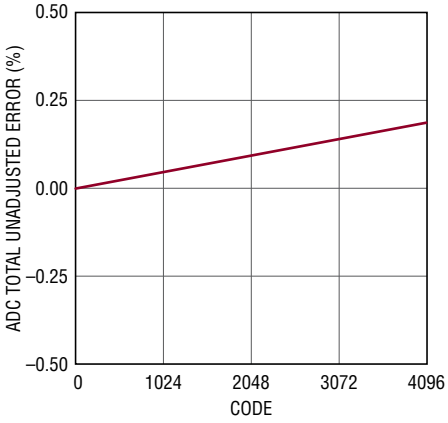
ADC Integral Nonlinearity (ΔSENSE)



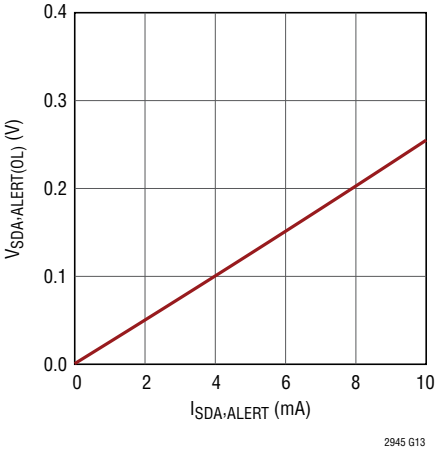
ADC Differential Nonlinearity (ΔSENSE)



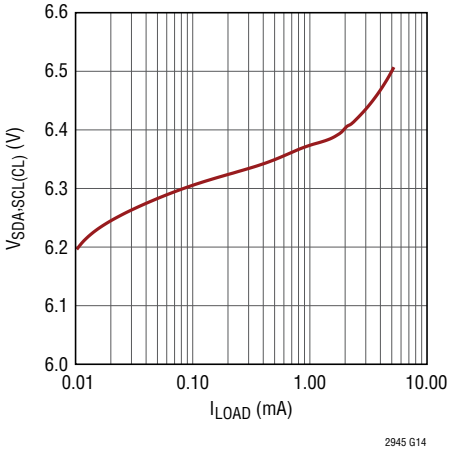
ADC Total Unadjusted Error (ΔSENSE)



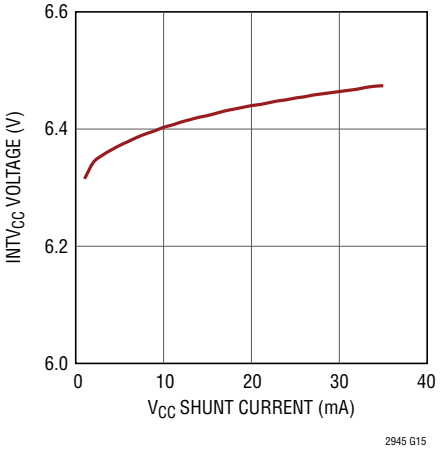
SDAO, $\overline{SDAO}$, $\overline{ALERT}$ Loaded Output Low Voltage



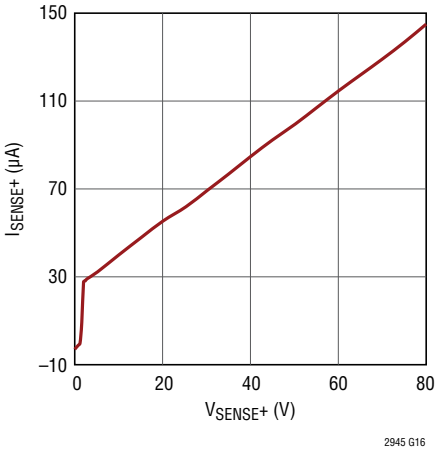
SCL, SDAI Loaded Clamp Voltage



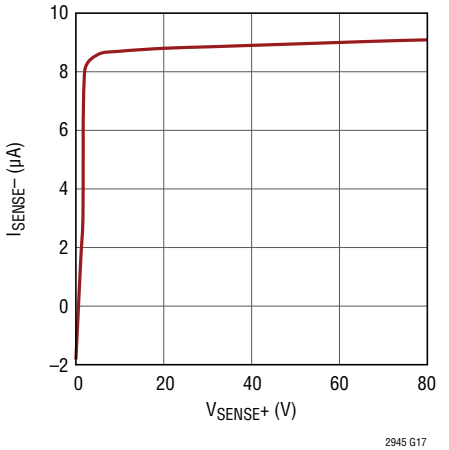
$INTV_{CC}$ Shunt Regulator Load Regulation



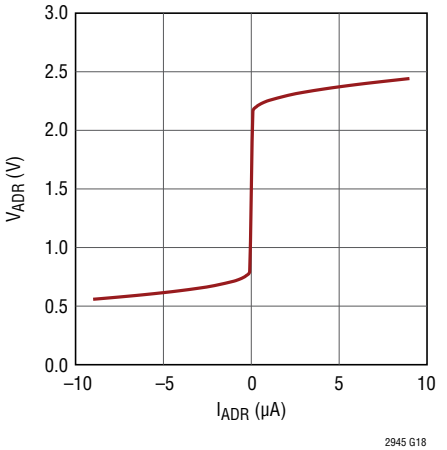
$SENSE^+$ Input Current



$SENSE^-$ Input Current



ADRO, ADR1 Voltage with Current Sink or Source



PIN FUNCTIONS (QFN/MSOP)

$INTV_{CC}$ (Pin 1/Pin 2): Internal Low Voltage Supply Input/Output. This pin is used to power internal circuitry. It can be configured as a direct input for a low voltage supply, as linear regulator from higher voltage supply connected to V_{DD}, or as a shunt regulator. Connect this pin directly to a 2.7V to 5.9V supply if available. When $INTV_{CC}$ is powered from an external supply, short the V_{DD} pin to $INTV_{CC}$. If V_{DD} is connected to a 4V to 80V supply, $INTV_{CC}$ becomes the 5V output of an internal series regulator that can supply up to 10mA to external circuitry. For even higher supply voltages or if a floating topology is desired, $INTV_{CC}$ can be used as a 6.3V shunt regulator. Connect the supply to $INTV_{CC}$ through a shunt resistor that limits the current to less than 35mA. An undervoltage lockout circuit disables the ADC when the voltage at this pin drops below 2.5V. Connect a bypass capacitor between 0.1µF and 1µF from this pin to ground.

ADR1, ADR0 (Pins 2, 3/Pins 3, 4): I^2C Device Address Inputs. Connecting these pins to $INTV_{CC}$, GND or leaving the pins open configures one of nine possible addresses. See Table 1 in Applications Information section for details.

ADIN (Pin 4/Pin 5): ADC Input. The onboard ADC measures voltages between 0V and 2.048V. Tie to ground if unused.

GND (Pin 5/Pin 6): Device Ground.

SCL (Pin 6/Pin 7): I^2C Bus Clock Input. Data at the SDAI pin is shifted in or out on rising edges of SCL. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SCL and V_{DD} or $INTV_{CC}$. The voltage at SCL is internally clamped to 6.4V (5.9V minimum)

SDAI (Pin 7/Pin 8): I^2C Bus Data Input. Used for shifting in address, command or data bits. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SDAI and V_{DD} or $INTV_{CC}$. The voltage at SDAI is internally clamped to 6.4V (5.9V minimum)

SDAO (Pin 8/Pin 9): I^2C Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required.

$\overline{SDAO}$ (Pin 8/Pin 9, LTC2945-1 Only): Inverted I^2C Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. Data is inverted for convenience of opto-isolation. An external pull-up resistor or current source is required.

$\overline{ALERT}$ (Pin 9/Pin 10): Fault Alert Output. Open drain logic output that is pulled to ground after an ADC conversion resulted in a fault to alert the host controller. A fault alert is enabled by setting the corresponding bit in the ALERT register as shown in Table 4. This device is compatible with the SMBus alert protocol. See Applications Information. Tie to ground if unused.

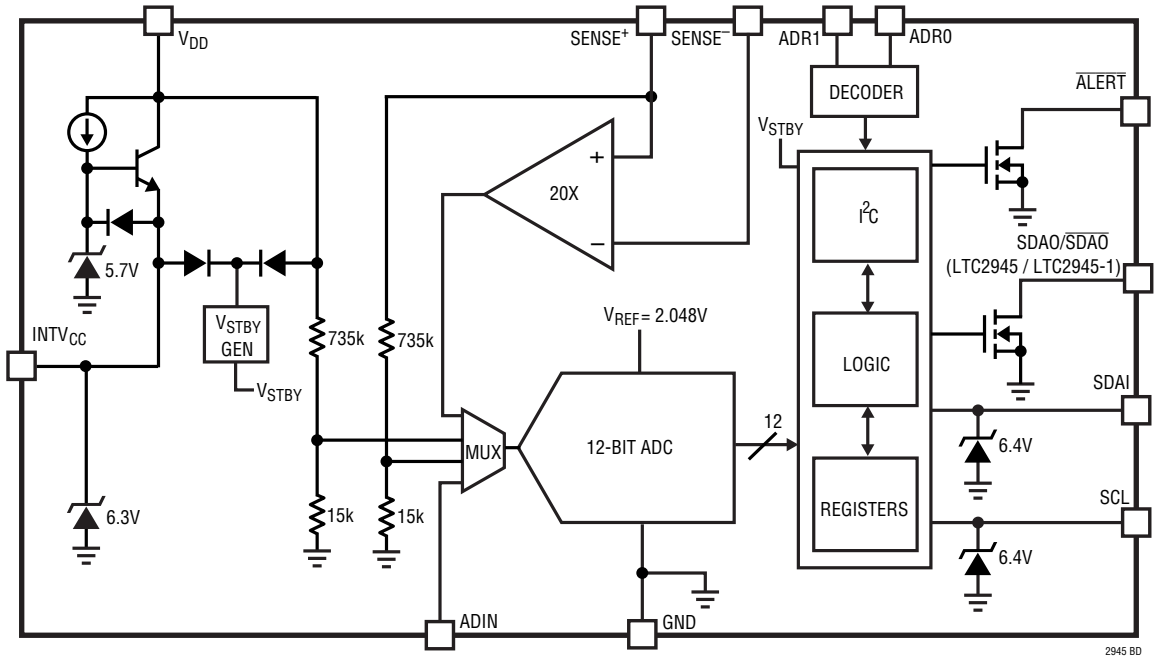
$SENSE^-$ (Pin 10/Pin 11): Current Sense Input. Connect an external sense resistor between $SENSE^+$ and $SENSE^-$. The differential voltage between $SENSE^+$ and $SENSE^-$ is monitored by the onboard ADC with a full-scale sense voltage of 102.4mV.

$SENSE^+$ (Pin 11/Pin 12): Supply Voltage and Current Sense Input. Used as a supply and current sense input for the internal current sense amplifier. The voltage at this pin is monitored by the onboard ADC with a full-scale input range of 102.4V. See Figure 17 for recommended Kelvin connection.

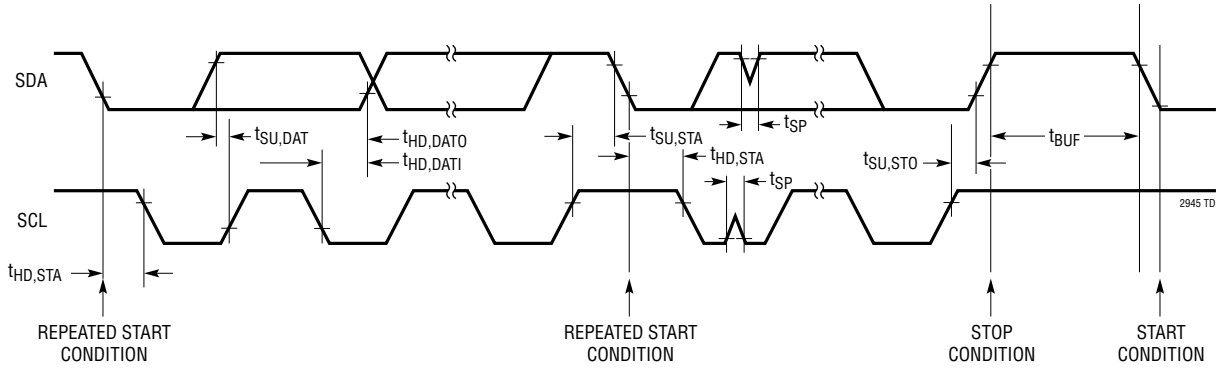
V_{DD} (Pin 12/Pin 1): High Voltage Supply Input. This pin powers an internal series regulator with input voltages ranging from 4V to 80V and produces 5V at $INTV_{CC}$ when the input voltage is above 7V. Connect a bypass capacitor between 0.1µF and 1µF from this pin to ground if external load is present on the $INTV_{CC}$ pin. The onboard 12-bit ADC can be configured to monitor the voltage at V_{DD} with a full-scale input range of 102.4V.

EXPOSED PAD (Pin 13, UD Package Only): Exposed pad may be left open or connected to device ground. For best thermal performance, connect to a large PCB area.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

The LTC2945 accurately monitors current, voltage, and power of any supply rail from 0V to 80V. An internal linear regulator allows the LTC2945 to operate directly from a 4V to 80V rail, or from an external supply voltage between 2.7V and 5.9V. Quiescent current is less than 0.9mA in normal operation. Enabling shutdown mode via the I^{2}C interface reduces the quiescent current to below 80µA. The LTC2945 includes a shunt regulator for operation from supply voltages above 80V.

The onboard 12-bit analog-to-digital converter (ADC) runs either continuously or on-demand using snapshot mode. In the default continuous scan mode, the ADC repeatedly measures the differential voltage between SENSE$^+$ and SENSE$^-$ (full-scale 102.4mV) the voltage at the SENSE$^+$ or V_{DD} pin (full-scale 102.4V), and the voltage at the ADIN pin (full-scale 2.048V). The conversion results are stored in onboard registers.

In snapshot mode, the LTC2945 performs a single measurement of one selected voltage or current. Snapshot mode is enabled by setting the snapshot mode enable bit in the CONTROL register via the I^{2}C interface. A status bit in the CONTROL register monitors the ADC's conversion; when complete, the conversion result is stored in the corresponding data registers.

Onboard logic tracks the minimum and maximum values for each ADC measurement, calculates power data by digitally multiplying the stored current and voltage data, and triggers a user-configurable alert by pulling the $\overline{\text{ALERT}}$ pin low when the ADC measured value falls outside the programmed window thresholds. All logic outputs are stored in onboard registers. The LTC2945 includes an I^{2}C interface to access the onboard data registers and to program the alert threshold and control registers. Two three-state pins, ADR1 and ADR0, are decoded to allow nine device addresses (see Table 1). The SDA pin is split into SDAI (input) and SDAO (output, LTC2945) or $\overline{\text{SDAO}}$ (output, LTC2945-1) to facilitate opto-isolation.

APPLICATIONS INFORMATION

The LTC2945 offers a compact and complete solution for high- and low-side power monitoring. With an input common mode range of 0V to 80V and a wide input supply operating voltage range from 2.7V to 80V, this device is ideal for a large variety of power management applications including automotive, industrial and telecom infrastructure. The basic application circuit shown in Figure 1 provides monitoring of high side current with a 0.02Ω resistor (5.12A full-scale), input voltage (102.4V full-scale) and an external voltage (2.048V full-scale), all using an internal 12-bit resolution ADC.

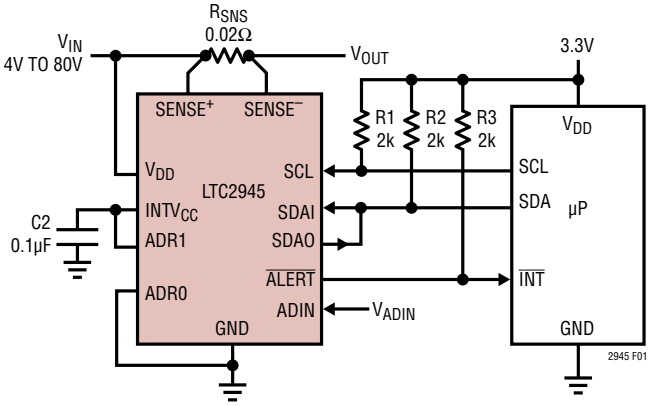


Figure 1. Monitoring High Side Current and Voltages Using the LTC2945

Data Converter

The LTC2945 features an onboard, 12-bit ΔΣ ADC that inherently averages input noise over the measurement window. The ADC continuously monitors three voltages in sequence: ΔSENSE first, V_{DD} or V_{SENSE}^+ second, and V_{ADIN} third. The differential voltage between SENSE$^+$ and SENSE$^-$ is monitored with 25µV resolution (102.4mV full-scale) to allow accurate measurement across very low value shunt resistors. The supply voltage at V_{DD} or SENSE$^+$ is directly measured with 25mV resolution (102.4V full-scale). The voltage at the uncommitted ADIN pin is measured with 0.5mV resolution (2.048V full-scale) to allow monitoring of an arbitrary external voltage. A 12-bit digital word corresponding to each measured voltage is stored in two adjacent registers out of the six total ADC data registers (ΔSENSE MSB/LSB, V_{IN} MSB/LSB, and ADIN MSB/LSB), with the

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eight MSBs in the first register and the four LSBs in the second (see Table 2). The lowest 4 bits in the LSB registers are set to 0. These data registers are updated immediately following the corresponding ADC conversion, giving an effective refresh rate of 7.5Hz in continuous scan mode.

The data converter also features a snapshot mode which makes a measurement of a single selected voltage (either ΔSENSE, V_{DD} or V_{SENSE}+, or V_{ADIN}). To make a snapshot measurement, set CONTROL register bit A7 and write the two-bit code of the desired ADC channel to A6 and A5 (Table 3) using a Write Byte command. When the Write Byte command is completed, the ADC converts the selected voltage and the Busy Bit (A3 in the CONTROL register) will be set to indicate that the conversion is in progress. After completing the conversion, the ADC will halt and the Busy Bit will reset to indicate that the data is ready. To make another snapshot measurement, rewrite the CONTROL register.

Flexible Power Supply to LTC2945

The LTC2945 can be externally configured to flexibly derive power from a wide range of supplies. The LTC2945 includes an onboard linear regulator to power the low-voltage internal circuitry connected to the $INTV_{CC}$ pin from high V_{DD} voltages. The regulator operates with V_{DD} voltages from 4V to 80V, and produces a 5V output capable of supplying 10mA at the $INTV_{CC}$ pin when V_{DD} is greater than 7V. The regulator is disabled when die temperature rises above 150°C, and the output is protected against accidental shorts. Bypass capacitors between 0.1µF and 1µF at both the V_{DD} and $INTV_{CC}$ pins are recommended for optimal transient performance. Note that operation with high V_{DD} voltages can cause significant power dissipation, and care is required to ensure the operating junction temperature stays below 125°C. For improved power dissipation, use the QFN package and solder the exposed pad to a large copper region for improved thermal resistance.

Figure 2a shows the LTC2945 being used to monitor an input supply that ranges from 4V to 80V. No secondary supply is needed since V_{DD} can be connected directly to the input supply. If the LTC2945 is used to monitor an input supply of 0V to 80V, it can derive power from a wide range secondary supply connected to the V_{DD} pin as shown in Figure 2b. The SENSE pins can be biased independent of the part's supply voltage. Alternatively, if a low voltage supply is present it can be connected to the $INTV_{CC}$ pin as shown in Figure 2c to minimize on-chip power dissipation. When $INTV_{CC}$ is powered from a secondary supply, connect V_{DD} to $INTV_{CC}$.

For supply voltages above 80V, the shunt regulator at $INTV_{CC}$ can be used in both high and low side configurations to provide power to the LTC2945 through an external shunt resistor, R_{SHUNT}. Figure 3a shows a high side power monitor with an input monitoring range beyond 80V in a high side shunt regulator configuration. The device ground is separated from ground through R_{SHUNT} and clamped at 6.3V below the input supply. Note that due to the different ground levels, the I^2C signals from the part need to be level shifted for communication with other ground referenced components. The bus voltage can be measured with the ADIN pin as shown in Figure 3a. To mitigate the effect of V_{BE} mismatch in the PNP mirror, select R1 (=R2) to drop 1V at the operating voltage. For details on the power calculation, refer to the Power Calculation and Configuration section. Figure 3b shows a high side rail-to-rail power monitor which derives power from a greater than 80V secondary supply. The voltage at $INTV_{CC}$ is clamped at 6.3V above ground in a low side shunt regulator configuration to power the part. In low side power monitors, the device ground and the current sense inputs are connected to the negative terminal of the input supply and the ADIN pin can be used to measure the bus voltage with an external resistive divider as shown in Figure 3c. The low side shunt regulator configuration allows operation with input supplies above 80V by clamping the voltage at $INTV_{CC}$. R_{SHUNT} should be sized according Equation 1.

$$\frac{V_{S(MAX)} - 5.9V}{35mA} \leq R_{SHUNT} \leq \frac{V_{S(MIN)} - 6.7V}{1mA + I_{LOAD(MAX)}} \qquad (1)$$

where $V_{S(MAX)}$ and $V_{S(MIN)}$ are the operating maximum and minimum of the supply. $I_{LOAD(MAX)}$ is the maximum external current load that is connected to the shunt regulator. The shunt resistor must also be rated to safely dissipate the worst-case power. As an example, consider the –48V Telecom System where the supply operates from –36V to –72V and the shunt regulator is used to supply an external load up to 4mA. R_{SHUNT} needs to be between

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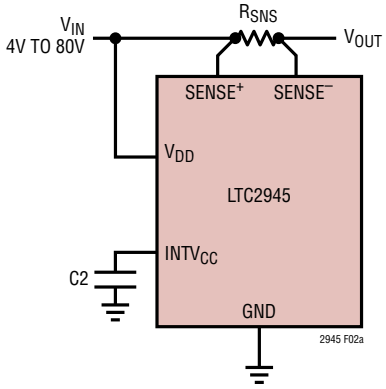
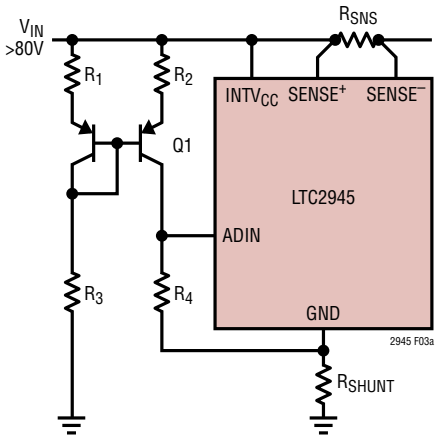
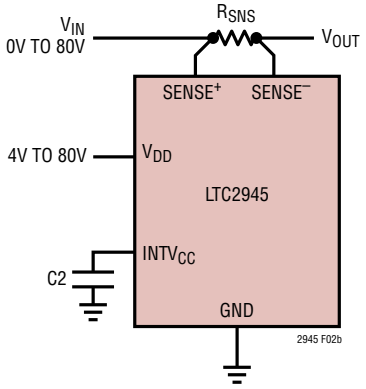


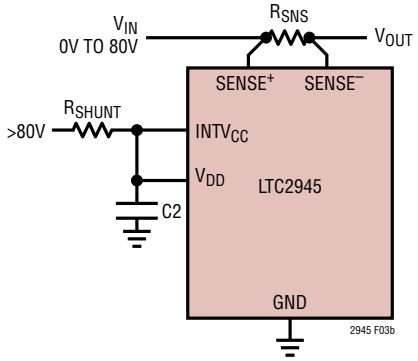
(a) Power from Supply Being Monitored



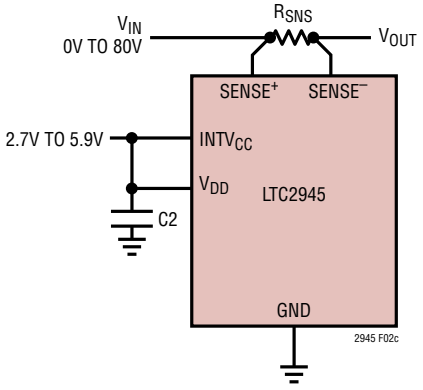
(a) Power Through High-Side Shunt Regulator



(b) Power from Wide Range Secondary Supply

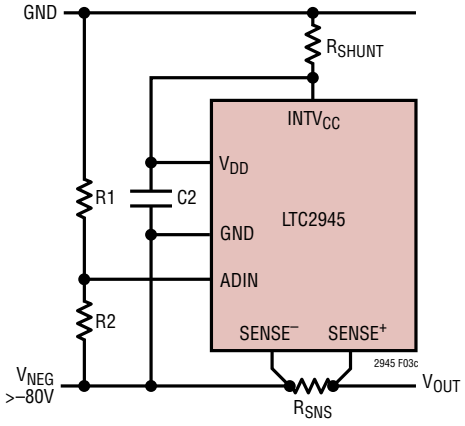


(b) Power Through Low-Side Shunt Regulator in High-Side Current Sense Topology



(c) Power from Low Voltage Secondary Supply

Figure 2. LTC2945 Derives Power



(c) Power Through Low-Side Shunt Regulator in Low-Side Current Sense Topology

Figure 3. LTC2945 Derives Power

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1.9k and 5.9k according to Equation 1, and for reduced power dissipation, a larger resistance is advantageous. The worst-case power dissipated in an R_{SHUNT} of 5.4k is calculated to be 0.8W. So, three 0.5W rated 1.8k resistors in series would suffice for this example.

If the supply input is nominally below 80V and transient is limited to below 100V, the shunt resistor is not required and V_{DD} can be connected to GND of the supply as shown in Figure 4.

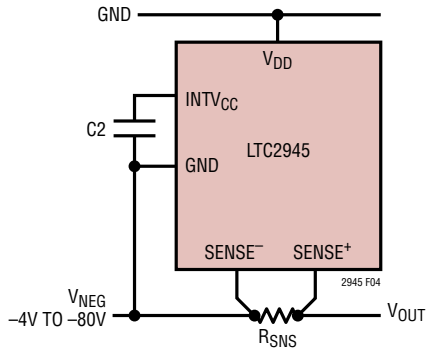

Figure 4. LTC2945 Derives Power from the Supply Being Monitored in Low-Side Current Sense Topology

Supply Undervoltage Lockout

During power-up, the internal I^2C logic and the ADC are enabled when either V_{DD} or $INTV_{CC}$ rises above its undervoltage lockout threshold. During power-down, the ADC is disabled when V_{DD} and $INTV_{CC}$ fall below their respective undervoltage lockout thresholds. The internal I^2C logic is reset when V_{DD} and $INTV_{CC}$ fall below their respective I^2C reset thresholds.

Shutdown Mode

The LTC2945 includes a low quiescent current shutdown mode, controlled by bit A1 in the CONTROL register (Table 3). Setting A1 puts the part in shutdown mode, powering down the ADC and internal reference. The internal I^2C bus remains active, and although the ADR1 and ADR0 pins are disabled, the device will retain the most recently programmed I^2C bus address. All on-board registers retain their contents and can be accessed through the I^2C interface. To re-enable ADC conversions, reset bit A1 in the CONTROL register. The analog circuitry will power up and all registers will retain their contents.

The onboard linear regulator is disabled in shutdown mode to conserve power. If low I_Q mode is not required and the regulator is used to power I^2C bus-related circuitry such as opto-couplers or pull-ups, ensure bit A1 in the CONTROL register is masked off during software development. In such applications, the user is advised that accidentally disabling the regulator would prevent I^2C communication from the master and cause the LTC2945 to disengage from the system. The LTC2945 would then have to be reset by cycling its power to come out of shutdown. It is recommended that external regulators be used in such applications if powering down the LTC2945 is desirable. Quiescent current drops below 80µA in shutdown mode with the internal regulator disabled.

Power Calculation and Configuration

The LTC2945 calculates power by multiplying the measured current with the measured voltage. In continuous mode, the differential voltage between $SENSE^+$ and $SENSE^–$ is measured to obtain load current data. The supply voltage data for multiplication can be selected between V_{DD}, $SENSE^+$, or ADIN. $SENSE^+$ is selected by default as it is normally connected to the supply voltage. In negative supply voltage systems such as shown in Figure 4, the device ground (GND pin of LTC2945) and $SENSE^–$ are connected to the supply and V_{DD} measures the supply voltage at GND with respect to the device ground. For negative supply voltages of more than 80V, use external resistors to divide down the voltage to suit the ADIN measurement range. In the CONTROL register,

- write bits A2=1, A0=1 to select $SENSE^+$ (Default)
- write bits A2=0, A0=1 to select V_{DD}
- write bits A2=1, A0=0 to select ADIN

More details on the CONTROL register can be found in Table 3.

Once the ADC conversions are complete, a 24-bit power value is generated by digitally multiplying the 12-bit load current data with the 12-bit supply voltage data. 1LSB of power is 1LSB of voltage multiplied by 1LSB of ΔSENSE (current). The result is held in the three adjacent POWER registers (Table 2). The POWER registers initialize with undefined data and subsequently refresh at a frequency of 7.5Hz in continuous scan mode. In snapshot mode, the POWER registers are not refreshed.

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Storing Minimum and Maximum Values

The LTC2945 compares each measurement including the calculated power with the stored values in the respective MIN and MAX registers for each parameter (Table 2). If the new conversion is beyond the stored minimum or maximum values, the MIN or MAX registers are updated with the new values. The MIN and MAX of the registers are refreshed at the end of their respective ADC conversions in both continuous scan mode and snapshot mode. They are also refreshed if the ADC registers are written via the I^2C bus with values beyond the stored values. To initiate a new peak hold cycle, write all 1's to the MIN registers and all 0's to the MAX registers via the I^2C bus. These registers will be updated when the next respective ADC conversion is done.

The LTC2945 also includes MIN and MAX THRESHOLD registers (Table 2) for the measured parameters including the calculated power. At power-up, the maximum thresholds are set to all 1's and minimum thresholds are set to all 0's, effectively disabling them. The thresholds can be reprogrammed to any desired value via the I^2C bus.

Fault Alert and Resetting Faults

As soon as a measured quantity falls below the minimum threshold or exceeds the maximum threshold, the LTC2945 sets the corresponding flag in the STATUS register and latches it into the FAULT register (see Figure 5). The $\overline{ALERT}$ pin is pulled low if the appropriate bit in the ALERT register is set. More details on the alert behavior can be found in the Alert Response Protocol section.

An active fault indication can be reset by writing zeros to the corresponding FAULT register bits or by reading the FAULT CoR register (Table 2), which clears all FAULT register bits. All FAULT register bits are also cleared if the V_{DD} and $INTV_{CC}$ fall below their respective I^2C logic reset threshold. Note that faults that are still present, as indicated in the STATUS registers, will immediately reappear.

I^2C Interface

The LTC2945 includes an I^2C/SMBus-compatible interface to provide access to the onboard registers. Figure 6 shows a general data transfer format using the I^2C bus.

The LTC2945 is a read-write slave device and supports the SMBus Read Byte, Write Byte, Read Word and Write Word protocols. The LTC2945 also supports extended Read and Write commands that allow reading or writing more than two bytes of data. When using the Read/Write Word or extended Read and Write commands, the bus master issues an initial register address and the internal register address pointer automatically increments by 1 after each byte of data is read or written. After the register address reaches 31h, it will roll over to 00h and continue incrementing. A Stop condition resets the register address pointer to 00h. The data formats for the above commands are shown in Figure 7 to Figure 12.

I^2C Device Addressing

Nine distinct I^2C bus addresses are configurable using the three-state pins ADR0 and ADR1, as shown in Table 1. ADR0 and ADR1 should be tied to $INTV_{CC}$, to GND, or left floating (NC) to configure the lower four address bits. During low power shutdown, the address select state is latched into memory powered from standby supply. Address bits a6, a5 and a4 are permanently set to (110) and the least significant bit is the R/$\overline{W}$ bit. In addition, all LTC2945 devices will respond to a common Mass Write address (1100 110)b; this allows the bus master to write to several LTC2945s simultaneously, regardless of their individual address settings. The LTC2945 will also respond to the standard ARA address (0001100)b if the Alert pin is asserted; see the Alert Response Protocol section for more details. The LTC2945 will not respond to the ARA address if no alerts are pending.

Start and Stop Conditions

When the I^2C bus is idle, both SCL and SDA are in the high state. A bus master signals the beginning of a transmission with a Start condition by transitioning SDA from high to low while SCL stays high. When the master has finished communicating with the slave, it issues a Stop condition by transitioning SDA from low to high while SCL stays high. The bus is then free for another transmission.

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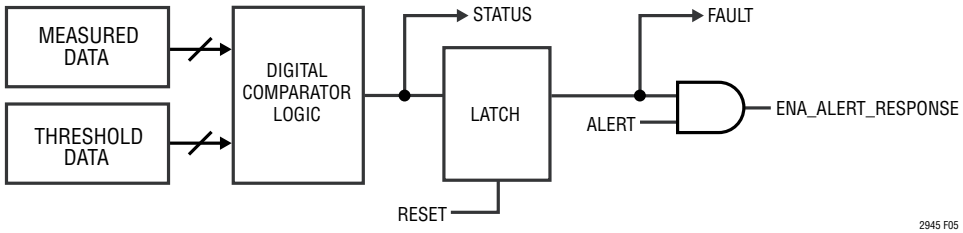


Figure 5. LTC2945 Fault Alert Generation Blocks

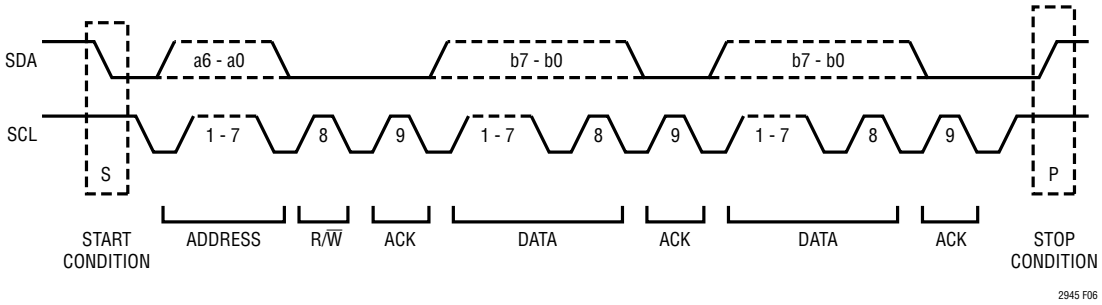


Figure 6. General Data Transfer Over I^2C

S	ADDRESS	W	A	COMMAND	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X b5:b0	0	b7:b0	0	

2945 F07

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 7. LTC2945 Serial Bus SDA Write Byte Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	P
	1 1 0 a3:a0	0	0	X X b5:b0	0	b7:b0	0	b7:b0	0	

2945 F08

Figure 8. LTC2945 Serial Bus SDA Write Word Protocol

S	ADDRESS	W	A	COMMAND	A	DATA	A	DATA	A	...	DATA	A	P
	1 1 0 a3:a0	0	0	X X b5:b0	0	b7:b0	0	b7:b0	0	...	b7:b0	0	

2945 F09

Figure 9. LTC2945 Serial Bus SDA Write Page Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	Ā	P
	1 1 0 a3:a0	0	0	X X b5:b0	0		1 1 0 a3:a0	1	0	b7:b0	1	

2945 F10

Figure 10. LTC2945 Serial Bus SDA Read Byte Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	Ā	P
	1 1 0 a3:a0	0	0	X X b5:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	1	

2945 F11

Figure 11. LTC2945 Serial Bus SDA Read Word Protocol

S	ADDRESS	W	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	...	DATA	Ā	P
	1 1 0 a3:a0	0	0	X X b5:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	...	b7:b0	1	

2945 F12

Figure 12. LTC2945 Serial Bus SDA Read Page Protocol

APPLICATIONS INFORMATION

Stuck-Bus Reset

The LTC2945 I²C interface features a stuck bus reset timer to prevent it from holding the bus lines low indefinitely if the SCL signal is interrupted during a transfer. The timer starts when either SCL or SDAI is low, and resets when both SCL and SDAI are pulled high. If either SCL or SDAI are low for over 33ms, the stuck-bus timer will expire and the internal I²C interface and the SDAO pin pulldown logic will be reset to release the bus. Normal communication will resume at the next Start command.

Acknowledge

The acknowledge signal is used for handshaking between the transmitter and the receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. The LTC2945 will pull the SDA line low on the 9th clock cycle to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master can abort the transmission by generating a Stop condition. When the master is receiving data from the slave, the master must acknowledge the slave by pulling down the SDA line during the 9th clock pulse to indicate receipt of a data byte. After the last byte has been received by the master, it will leave the SDA line high (not acknowledge) and issue a Stop condition to terminate the transmission.

Write Protocol

The master begins a write operation with a Start condition followed by the seven-bit slave address and the R/$\overline{W}$ bit set to zero. After the addressed LTC2945 acknowledges the address byte, the master then sends a command byte that indicates which internal register the master wishes to write. The LTC2945 acknowledges this and then latches the lower six bits of the command byte into its internal register address pointer. The master then delivers the data byte and the LTC2945 acknowledges once more and writes the data into the internal register pointed to by the register address pointer. If the master continues sending additional data bytes with a Write Word or extended Write command, the additional data bytes will be acknowledged by the LTC2945, the register address pointer will automatically increment by one, and data will be written as above. The write operation terminates and the register address pointer resets to 00h when the master sends a Stop condition.

Read Protocol

The master begins a read operation with a Start condition followed by the 7-bit slave address and the R/$\overline{W}$ bit set to zero. After the addressed LTC2945 acknowledges the address byte, the master then sends a command byte that indicates which internal register the master wishes to read. The LTC2945 acknowledges this and then latches the lower six bits of the command byte into its internal register address pointer. The master then sends a repeated Start condition followed by the same 7-bit address with the R/$\overline{W}$ bit now set to 1. The LTC2945 acknowledges and sends the contents of the requested register. The transmission terminates when the master sends a Stop condition. If the master acknowledges the transmitted data byte, as in a Read Word command, the LTC2945 will send the contents of the next register. If the master keeps acknowledging, the LTC2945 will keep incrementing the register address pointer and sending out data bytes. The read operation terminates and the register address pointer resets to 00h when the master sends a Stop condition.

Alert Response Protocol

When any of the fault bits in the FAULT register are set, a bus alert is generated if the appropriate bit in the ALERT register has been set. This allows the bus master to select which faults will generate alerts. At power-up, the ALERT register is cleared (no alerts enabled) and the $\overline{\text{ALERT}}$ pin is high. If an alert is enabled, the corresponding fault causes the $\overline{\text{ALERT}}$ pin to pull low. The bus master responds to the alert in accordance with the SMBus alert response protocol by broadcasting the Alert Response Address (0001100)b, and the LTC2945 replies with its own address and releases its $\overline{\text{ALERT}}$ pin as shown in Figure 13. The $\overline{\text{ALERT}}$ line is also released if the FAULT or FAULT CoR registers are read (see Table 2) since the faulting event can be identified by the content in these registers. The $\overline{\text{ALERT}}$ signal is not pulled low again until the Fault register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate additional alerts until the associated FAULT register bits have been cleared.

APPLICATIONS INFORMATION

If two or more LTC2945s on the same bus are generating alerts when the ARA is broadcasted, the bus master will repeat the alert response protocol until the $\overline{\text{ALERT}}$ line is released. The device with the highest priority (lowest address) will reply first and the device with the lowest priority (highest address) will reply last.

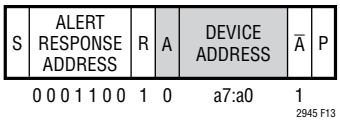


Figure 13. LTC2945 Serial Bus SDA Alert Response Protocol

Opto-Isolating the I²C Bus

Opto-isolating a standard I²C device is complicated by the bidirectional SDA pin. The LTC2945/LTC2945-1 minimize this problem by splitting the standard I²C SDA line into SDAI (input) and SDAO (output, LTC2945) or $\overline{\text{SDAO}}$ (inverted output, LTC2945-1). The SCL is an input only pin and does not require special circuitry to isolate. For conventional non-isolated I²C applications, use the LTC2945 and tie the SDAI and SDAO pins together to form a standard I²C SDA pin.

Low speed isolated interfaces that use standard open-drain opto-isolators typically use the LTC2945 with the SDAI and SDAO pins separated as shown in Figure 14. Connect SDAI to the output of the incoming opto-isolator with a pullup resistor to $INTV_{CC}$ or a local 5V supply; connect SDAO to the cathode of the outgoing opto-isolator with a current-limiting resistor in series with the anode. The input and output must be connected together on the isolated side of the bus to allow the LTC2945 to participate in I²C arbitration. Note that maximum I²C bus speed will generally be limited by the speed of the opto-couplers used in this application.

Both low and high side shunt regulators can supply up to 34mA of current to drive opto-isolator and pullup resistors as shown in Figure 15 and Figure 16. For identical SDAI/SCL pullup resistors the maximum load is given by Equation 2.

$$I_{LOAD(MAX)} = 6.7\left(\frac{2}{R1}+\frac{1}{R3}\right) \quad (2)$$

R_{SHUNT} can then be calculated using Equation 1. Note that both LTC2945 and LTC2945-1 can be used in the shunt regulator applications mentioned.

Figure 17 shows an alternate connection for use with low-speed opto-couplers and the LTC2945-1. This circuit uses a limited-current pullup on the internally clamped SDAI pin and clamps the $\overline{\text{SDAO}}$ pin with the input diode of the outgoing opto-isolator, removing the need to use $INTV_{CC}$ for biasing in the absence of an auxiliary low voltage supply. For proper clamping use Equation 3.

$$\frac{V_{S(MAX)} - 5.9V}{5mA} \le R4 \le \frac{V_{S(MIN)} - 6.9V}{0.5mA} \quad (3)$$

As an example, a supply that operates from 36V to 72V would require the value of R4 to be between 13k and 58k. The LTC2945-1 must be used in this application to ensure that the $\overline{\text{SDAO}}$ signal polarity is correct.

The LTC2945-1 can also be used with high-speed opto-couplers with push-pull outputs and inverted logic as shown in Figure 18. The incoming opto-isolator draws power from the $INTV_{CC}$, and the data output is connected directly to the SDAI pin with no pullup required. Ensure the current drawn does not exceed the 10mA maximum capability of the $INTV_{CC}$ pin. The $\overline{\text{SDAO}}$ pin is connected to the cathode of the outgoing optocoupler with a current limiting resistor connected back to $INTV_{CC}$. An additional discrete N-channel MOSFET is required at the output of the outgoing optocoupler to provide the open-drain pull-down that the I²C bus requires. Finally, the input of the incoming opto-isolator is connected back to the output as in the low-speed case.

Layout Considerations

A Kelvin connection between the sense resistor R_{SNS} and the LTC2945 is recommended to achieve accurate current sensing (Figure 19). The recommended minimum trace width for 1oz copper foil is 0.02" per amp to ensure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is preferred. Note that 1oz copper exhibits a sheet resistance of about 530µΩ per square.

APPLICATIONS INFORMATION

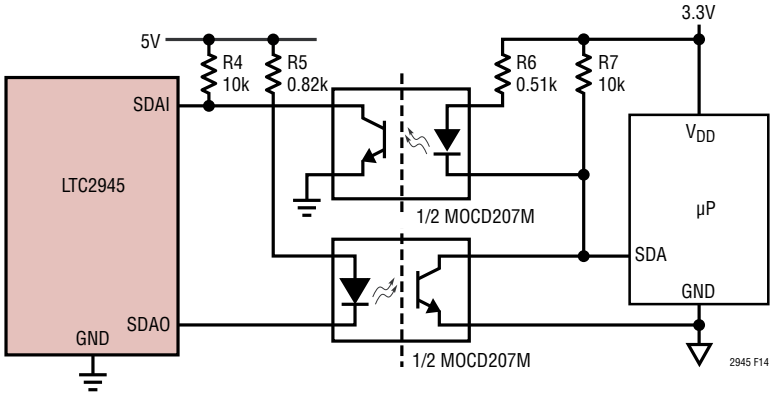


Figure 14. Opto-Isolation of a 10kHz I²C Interface Between LTC2945 and Microcontroller (SCL Omitted for Clarity)

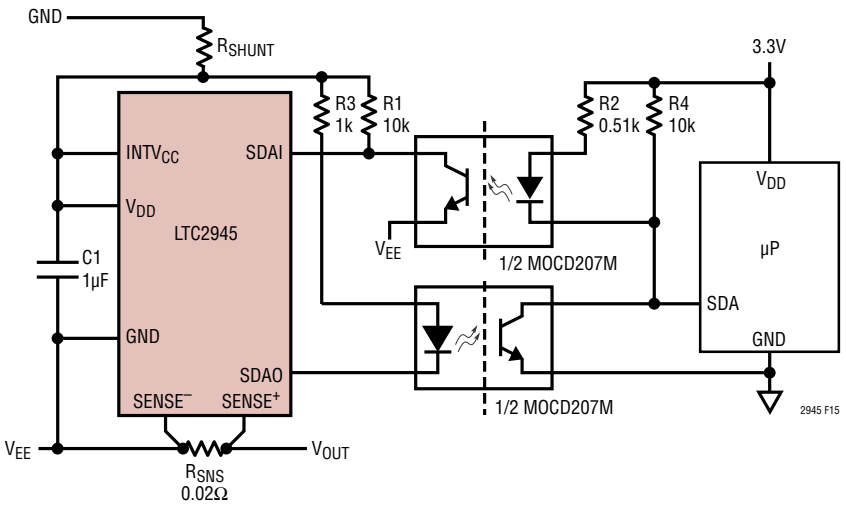


Figure 15. Low Speed 10kHz Opto-Isolators Powered from Low-Side Shunt Regulator

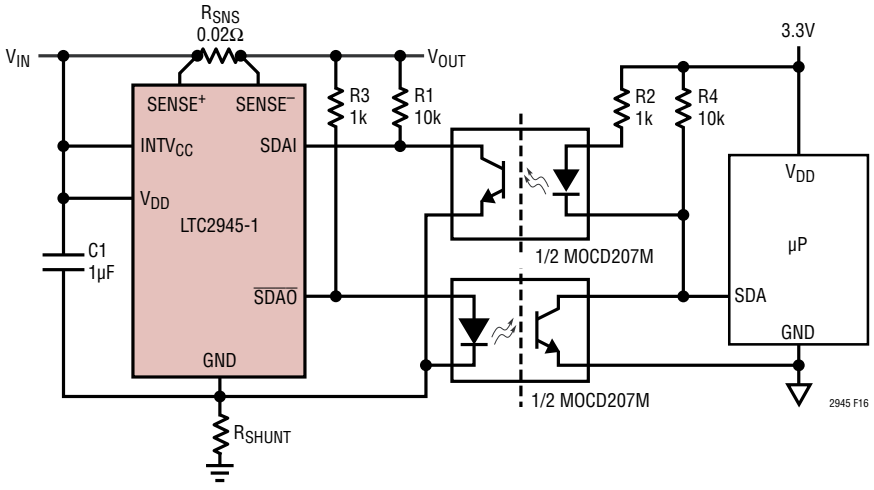


Figure 16. Low Speed 10kHz Opto-Isolators Powered from High-Side Shunt Regulator

APPLICATIONS INFORMATION

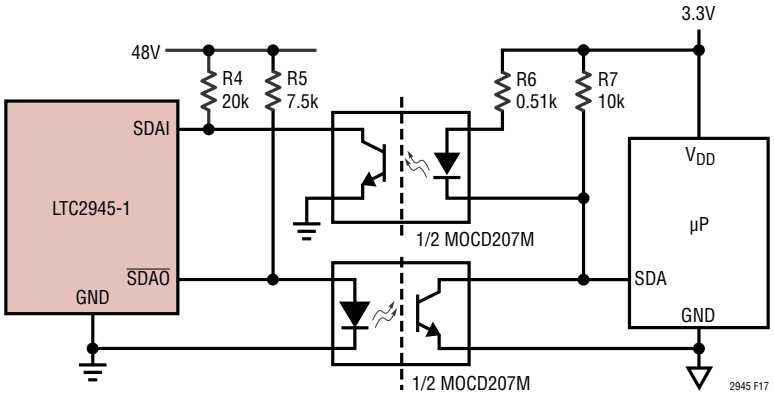


Figure 17. Opto-Isolation of a 1.5kHz I²C Interface Between LTC2945-1 and Microcontroller (SCL Omitted for Clarity)

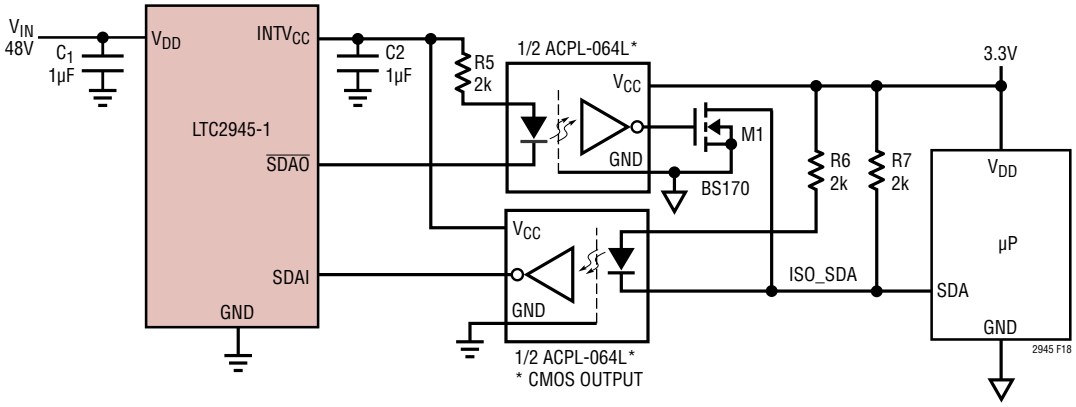


Figure 18. Opto-Isolation of I²C Interface with Low Power, High Speed Opto-Couplers (SCL Omitted for Clarity)

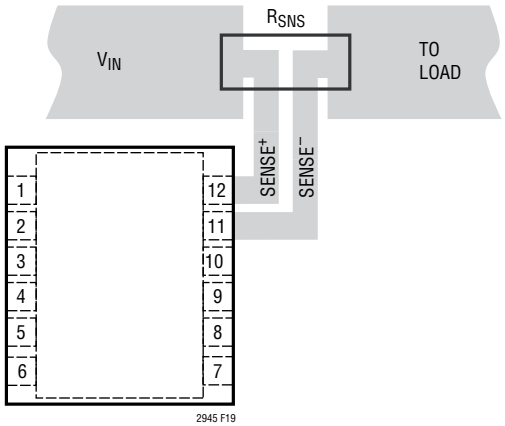


Figure 19. Recommended Layout for Kelvin Connection

APPLICATIONS INFORMATION

Table 1. LTC2945 Device Addressing

DESCRIPTION	HEX DEVICE ADDRESS	BINARY DEVICE ADDRESS								LTC2945 ADDRESS PINS	
	h	a6	a5	a4	a3	a2	a1	a0	R/$\overline{W}$	ADR1	ADR0
Mass Write	CC	1	1	0	0	1	1	0	0	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X
0	CE	1	1	0	0	1	1	1	X	H	L
1	D0	1	1	0	1	0	0	0	X	NC	H
2	D2	1	1	0	1	0	0	1	X	H	H
3	D4	1	1	0	1	0	1	0	X	NC	NC
4	D6	1	1	0	1	0	1	1	X	NC	L
5	D8	1	1	0	1	1	0	0	X	L	H
6	DA	1	1	0	1	1	0	1	X	H	NC
7	DC	1	1	0	1	1	1	0	X	L	NC
8	DE	1	1	0	1	1	1	1	X	L	L

Table 2. LTC2945 Register Addresses and Contents

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	DEFAULT
00h	CONTROL (A)	R/W	Controls ADC Operation Mode and Test Mode	05h
01h	ALERT (B)	R/W	Selects Which Faults Generate Alerts	00h
02h	STATUS (C)	R	System Status Information	00h
03h	FAULT (D)	R/W	Fault Log	00h
04h	FAULT CoR (E)	CoR	Same Data as Register D, D Content Cleared on Read	00h
05h	POWER MSB2	R/W**	Power MSB2 Data	XXh
06h	POWER MSB1	R/W**	Power MSB1 Data	XXh
07h	POWER LSB	R/W**	Power LSB Data	XXh
08h	MAX POWER MSB2	R/W**	Maximum Power MSB2 Data	00h
09h	MAX POWER MSB1	R/W**	Maximum Power MSB1 Data	00h
0Ah	MAX POWER LSB	R/W**	Maximum Power LSB Data	00h
0Bh	MIN POWER MSB2	R/W**	Minimum Power MSB2 Data	FFh
0Ch	MIN POWER MSB1	R/W**	Minimum Power MSB1 Data	FFh
0Dh	MIN POWER LSB	R/W**	Minimum Power LSB Data	FFh
0Eh	MAX POWER THRESHOLD MSB2	R/W	Maximum Power Threshold MSB2 to Generate Alert	FFh
0Fh	MAX POWER THRESHOLD MSB1	R/W	Maximum Power Threshold MSB1 to Generate Alert	FFh
10h	MAX POWER THRESHOLD LSB	R/W	Maximum Power Threshold LSB to Generate Alert	FFh
11h	MIN POWER THRESHOLD MSB2	R/W	Minimum Power Threshold MSB2 to Generate Alert	00h
12h	MIN POWER THRESHOLD MSB1	R/W	Minimum Power Threshold MSB1 to Generate Alert	00h
13h	MIN POWER THRESHOLD LSB	R/W	Minimum Power Threshold LSB to Generate Alert	00h
14h	ΔSENSE MSB	R/W**	ΔSENSE MSB Data	XXh
15h	ΔSENSE LSB	R/W**	ΔSENSE LSB Data	X0h
16h	MAX ΔSENSE MSB	R/W**	Maximum ΔSENSE MSB Data	00h

APPLICATIONS INFORMATION

Table 2. LTC2945 Register Addresses and Contents

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	DEFAULT
17h	MAX ΔSENSE LSB	R/W**	Maximum ΔSENSE LSB Data	00h
18h	MIN ΔSENSE MSB	R/W**	Minimum ΔSENSE MSB Data	FFh
19h	MIN ΔSENSE LSB	R/W**	Minimum ΔSENSE LSB Data	FOh
1Ah	MAX ΔSENSE THRESHOLD MSB	R/W	Maximum ΔSENSE Threshold MSB to Generate Alert	FFh
1Bh	MAX ΔSENSE THRESHOLD LSB	R/W	Maximum ΔSENSE Threshold LSB to Generate Alert	FOh
1Ch	MIN ΔSENSE THRESHOLD MSB	R/W	Minimum ΔSENSE Threshold MSB to Generate Alert	00h
1Dh	MIN ΔSENSE THRESHOLD LSB	R/W	Minimum ΔSENSE Threshold LSB to Generate Alert	00h
1Eh	V_{IN} MSB	R/W**	ADC V_{IN} MSB Data	XXh
1Fh	V_{IN} LSB	R/W**	ADC V_{IN} LSB Data	X0h
20h	MAX V_{IN} MSB	R/W**	Maximum V_{IN} MSB Data	00h
21h	MAX V_{IN} LSB	R/W**	Maximum V_{IN} LSB Data	00h
22h	MIN V_{IN} MSB	R/W**	Minimum V_{IN} MSB Data	FFh
23h	MIN V_{IN} LSB	R/W**	Minimum V_{IN} LSB Data	FOh
24h	MAX V_{IN} THRESHOLD MSB	R/W	Maximum V_{IN} Threshold MSB to Generate Alert	FFh
25h	MAX V_{IN} THRESHOLD LSB	R/W	Maximum V_{IN} Threshold LSB to Generate Alert	FOh
26h	MIN V_{IN} THRESHOLD MSB	R/W	Minimum V_{IN} Threshold MSB to Generate Alert	00h
27h	MIN V_{IN} THRESHOLD LSB	R/W	Minimum V_{IN} Threshold LSB to Generate Alert	00h
28h	ADIN MSB	R/W**	ADIN MSB Data	XXh
29h	ADIN LSB	R/W**	ADIN LSB Data	X0h
2Ah	MAX ADIN MSB	R/W**	Maximum ADIN MSB Data	00h
2Bh	MAX ADIN LSB	R/W**	Maximum ADIN LSB Data	00h
2Ch	MIN ADIN MSB	R/W**	Minimum ADIN MSB Data	FFh
2Dh	MIN ADIN LSB	R/W**	Minimum ADIN LSB Data	FOh
2Eh	MAX ADIN THRESHOLD MSB	R/W	Maximum ADIN Threshold MSB to Generate Alert	FFh
2Fh	MAX ADIN THRESHOLD LSB	R/W	Maximum ADIN Threshold LSB to Generate Alert	FOh
30h	MIN ADIN THRESHOLD MSB	R/W	Minimum ADIN Threshold MSB to Generate Alert	00h
31h	MIN ADIN THRESHOLD LSB	R/W	Minimum ADIN Threshold LSB to Generate Alert	00h

*Register address MSBs b7-b6 are ignored. ** Writable if bit A4 is set

APPLICATIONS INFORMATION

Table 3. CONTROL Register A (00h) – Read/Write

BIT	NAME	OPERATION
A7	ADC Snapshot Mode Enable	Enables ADC Snapshot Mode; 1 = Snapshot Mode Enabled. Only channel selected by A6 and A5 is measured by the ADC. After the conversion, the BUSY bit is reset and the ADC is halted. 0 = Snapshot Mode Disabled (Continuous Scan Mode. Default)
A6 A5	ADC Channel Label for Snapshot Mode	ADC Channel Label for Snapshot Mode A6 / A5 / ADC Channel 0 / 0 / ΔSENSE (Default) 0 / 1 / V_{IN} 1 / 0 / ADIN
A4	Test Mode Enable	Test Mode Halts ADC Operation and Enables Writes to Internal ADC/LOGIC Registers; 1 = Enable Test Mode, 0 = Disable Test Mode (Default)
A3	ADC Busy in Snapshot Mode	ADC Current Status; 1 = ADC Converting, 0 = ADC Conversion Completed (Default), Not Writable
A2	V_{IN} Monitor	Enables V_{DD} or $SENSE^+$ Voltage Monitoring; 1 = Monitor $SENSE^+$ Voltage (Default), 0 = Monitor V_{DD} Voltage
A1	Shutdown Enable	Enables Low-I_Q / Shutdown Mode; 1 = Enable Shutdown, 0 = Normal Operation (Default)
A0	Multiplier Select	Selects ADIN or $SENSE^+/V_{DD}$ (depends on A2) data for digital multiplication with SENSE data; 1 = Select $SENSE^+/V_{DD}$ (Default), 0 = Select ADIN

Table 4. ALERT Register B (01h) – Read/Write

BIT	NAME	OPERATION
B7	Maximum POWER Alert	Enables Alert When POWER Calculation Data is > Maximum Power Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B6	Minimum POWER Alert	Enables Alert When POWER Calculation Data is < Minimum Power Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B5	Maximum ΔSENSE Alert	Enables Alert When ADC ΔSENSE Measurement Data is > Maximum ΔSENSE Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B4	Minimum ΔSENSE Alert	Enables Alert When ADC ΔSENSE Measurement Data is < Minimum ΔSENSE Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B3	Maximum V_{IN} Alert	Enables Alert When ADC V_{IN} Measurement Data is > Maximum V_{IN} Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B2	Minimum V_{IN} Alert	Enables Alert When ADC V_{IN} Measurement Data is < Minimum V_{IN} Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B1	Maximum ADIN Alert	Enables Alert When ADC ADIN Measurement Data is > Maximum ADIN Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)
B0	Minimum ADIN Alert	Enables Alert When ADC ADIN Measurement Data is < Minimum ADIN Threshold; 1 = Enable Alert, 0 = Disable Alert (Default)

APPLICATIONS INFORMATION

Table 5. STATUS Register C (02h) – Read

BIT	NAME	OPERATION
C7	POWER Overvalue Present	Indicates POWER Overvalue When POWER is > Maximum Power Threshold; 1 = POWER Overvalue, 0 = POWER Not Overvalue
C6	POWER Undervalue Present	Indicates POWER Undervalue When POWER is < Minimum Power Threshold; 1 = POWER Undervalue, 0 = POWER Not Undervalue
C5	ΔSENSE Overvalue Present	Indicates ΔSENSE Overvalue When ΔSENSE is > Maximum ΔSENSE Threshold; 1 = ΔSENSE Overvalue, 0 = ΔSENSE Not Overvalue
C4	ΔSENSE Undervalue Present	Indicates ΔSENSE Undervalue When ΔSENSE is < Minimum ΔSENSE Threshold; 1 = ΔSENSE Undervalue, 0 = ΔSENSE Not Undervalue
C3	V_{IN} Overvalue Present	Indicates V_{IN} Overvalue When V_{IN} is > Maximum V_{IN} Threshold; 1 = V_{IN} Overvalue, 0 = V_{IN} Not Overvalue
C2	V_{IN} Undervalue Present	Indicates V_{IN} Undervalue When V_{IN} is < Minimum V_{IN} Threshold; 1 = V_{IN} Undervalue, 0 = V_{IN} Not Undervalue
C1	ADIN Overvalue Present	Indicates ADIN Overvalue When ADIN is > Maximum ADIN Threshold; 1 = ADIN Overvalue, 0 = ADIN Not Overvalue
C0	ADIN Undervalue Present	Indicates ADIN Undervalue When ADIN is < Minimum ADIN Threshold; 1 = ADIN Undervalue, 0 = ADIN Not Undervalue

Table 6. FAULT Register D (03h) – Read/Write

BIT	NAME	OPERATION
D7	POWER Overvalue Fault Occurred	Indicates POWER Overvalue Fault When POWER was > Maximum Power Threshold; 1 = POWER Overvalue Fault Occurred, 0 = No POWER Overvalue Faults
D6	POWER Undervalue Fault Occurred	Indicates POWER Undervalue Fault When POWER was < Minimum Power Threshold; 1 = POWER Undervalue Fault Occurred, 0 = No POWER Undervalue Faults
D5	ΔSENSE Overvalue Fault Occurred	Indicates ΔSENSE Overvalue Fault When ΔSENSE was > Maximum ΔSENSE Threshold; 1 = ΔSENSE Overvalue Fault Occurred, 0 = No ΔSENSE Overvalue Faults
D4	ΔSENSE Undervalue Fault Occurred	Indicates ΔSENSE Undervalue Fault When ΔSENSE was < Minimum ΔSENSE Threshold; 1 = ΔSENSE Undervalue Fault Occurred, 0 = No ΔSENSE Undervalue Faults
D3	V_{IN} Overvalue Fault Occurred	Indicates V_{IN} Overvalue Fault When V_{IN} was > Maximum V_{IN} Threshold; 1 = V_{IN} Overvalue Fault Occurred, 0 = No V_{IN} Overvalue Faults
D2	V_{IN} Undervalue Fault Occurred	Indicates V_{IN} Undervalue Fault When V_{IN} was < Minimum V_{IN} Threshold; 1 = V_{IN} Undervalue Fault Occurred, 0 = No V_{IN} Undervalue Faults
D1	ADIN Overvalue Fault Occurred	Indicates ADIN Overvalue Fault When ADIN was > Maximum ADIN Threshold; 1 = ADIN Overvalue Fault Occurred, 0 = No ADIN Overvalue Faults
D0	ADIN Undervalue Fault Occurred	Indicates ADIN Undervalue Fault When ADIN was < Minimum ADIN Threshold; 1 = ADIN Undervalue Fault Occurred, 0 = No ADIN Undervalue Faults

APPLICATIONS INFORMATION

Table 7. ADC, ADC MIN/MAX, MIN/MAX ADC THRESHOLD Register Data Format: MSB Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (11)	Data (10)	Data (9)	Data (8)	Data (7)	Data (6)	Data (5)	Data (4)

*Set Bit A4 before writing to ADC and MIN/MAX ADC Registers

Table 8. ADC, ADC MIN/MAX, MIN/MAX THRESHOLD Register Data Format: LSB Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (3)	Data (2)	Data (1)	Data (0)	Reserved**	Reserved**	Reserved**	Reserved**

* Set Bit A4 before writing to ADC and MIN/MAX ADC Registers

** Read as '0'

Table 8. POWER, MIN/MAX POWER, MIN/MAX POWER THRESHOLD Register Data Format: MSB2 Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (23)	Data (22)	Data (21)	Data (20)	Data (19)	Data (18)	Data (17)	Data (16)

* Set Bit A4 before writing to POWER and MIN/MAX POWER Registers

Table 9. POWER, MIN/MAX POWER, MIN/MAX POWER THRESHOLD Register Data Format: MSB1 Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (15)	Data (14)	Data (13)	Data (12)	Data (11)	Data (10)	Data (9)	Data (8)

* Set Bit A4 before writing to POWER and MIN/MAX POWER Registers

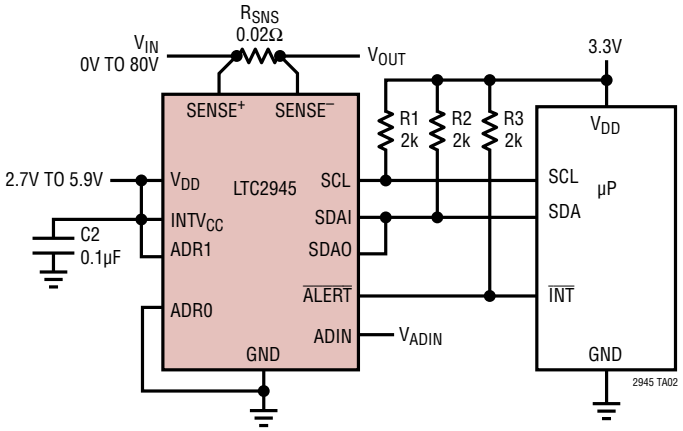
Table 10. POWER, MIN/MAX POWER, MIN/MAX POWER THRESHOLD Register Data Format: LSB Bytes – Read/Write*

BIT (7)	BIT (6)	BIT (5)	BIT (4)	BIT (3)	BIT (2)	BIT (1)	BIT (0)
Data (7)	Data (6)	Data (5)	Data (4)	Data (3)	Data (2)	Data (1)	Data (0)

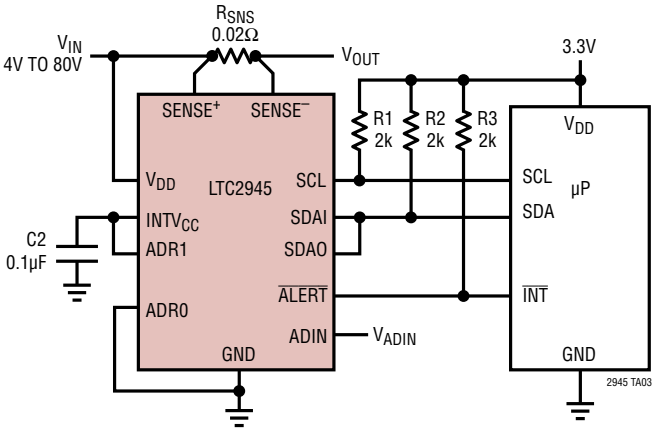
* Set Bit A4 before writing to POWER and MIN/MAX POWER Registers

TYPICAL APPLICATIONS

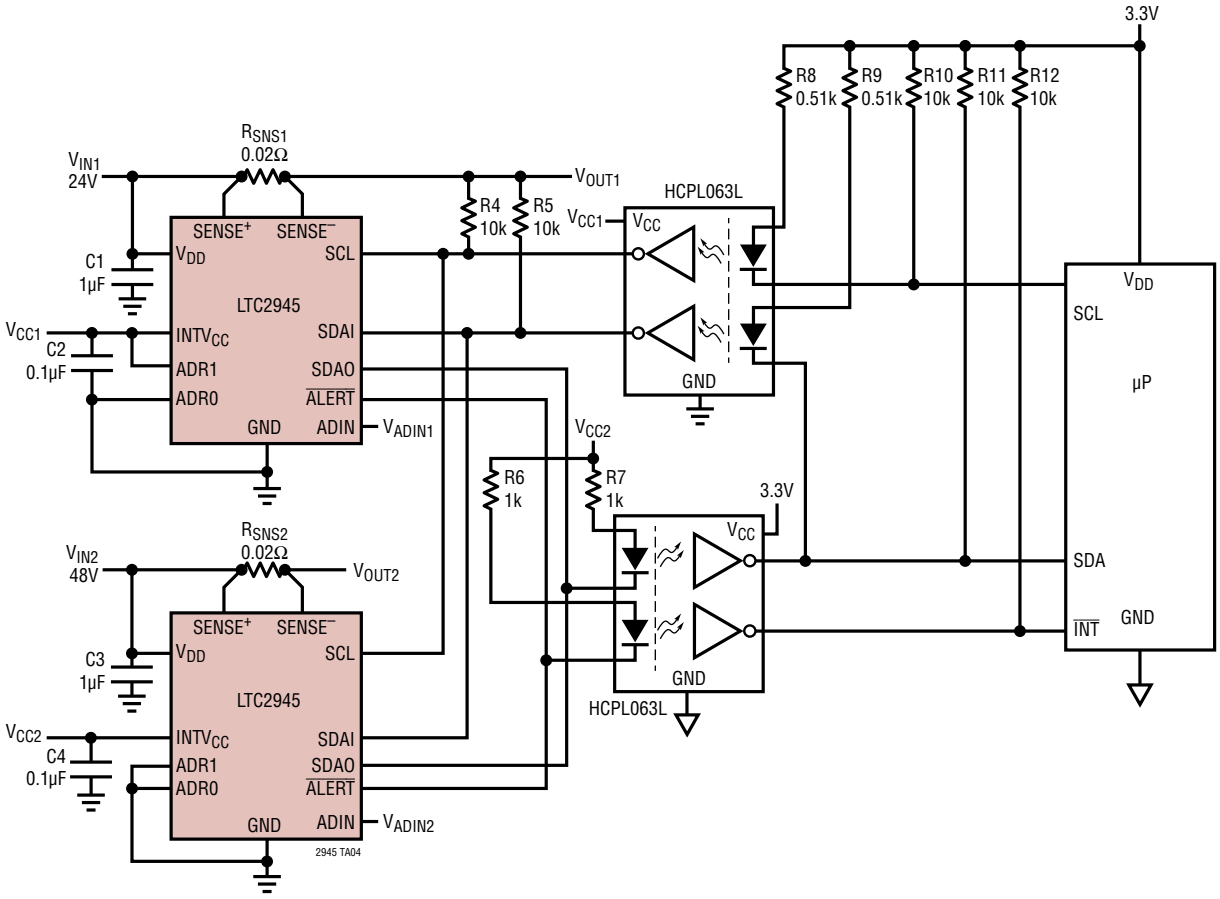
A Wide Range Supply Monitor



Wide Range Supply Monitor with Wide Range V_{DD} Input

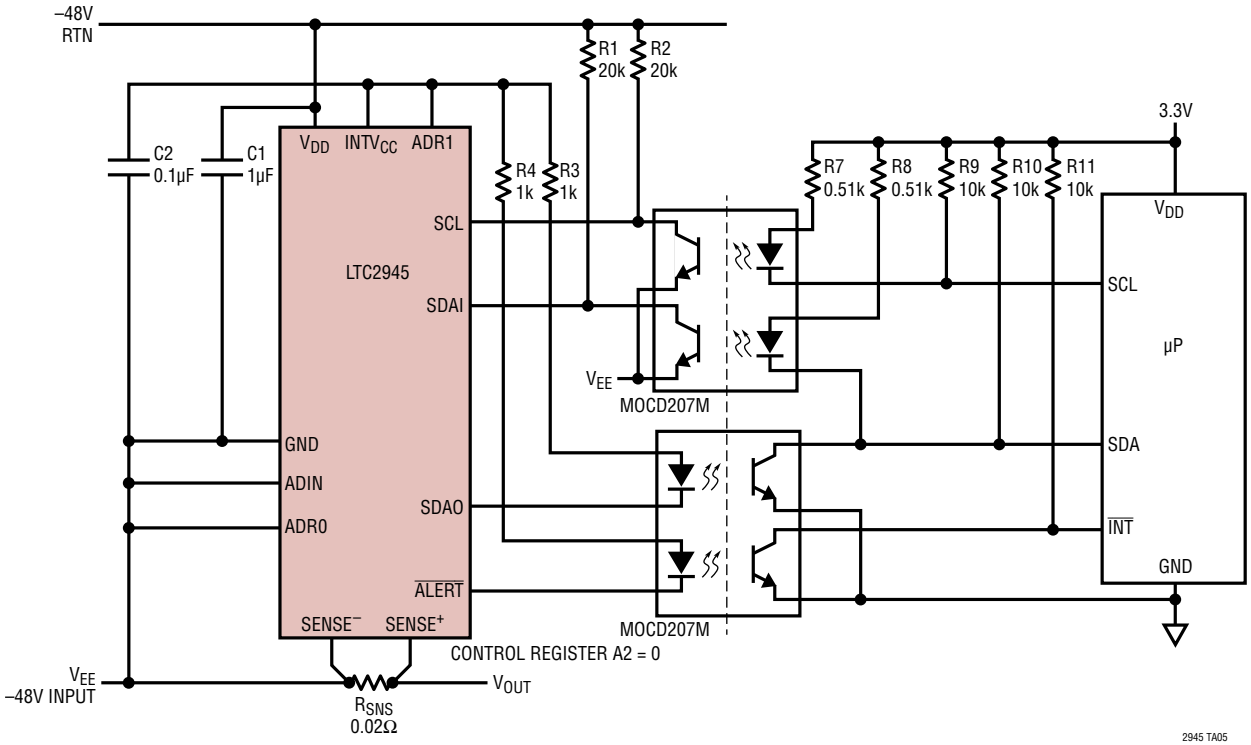


Dual Supply Monitor with Common Opto-Coupler for Galvanic Isolation

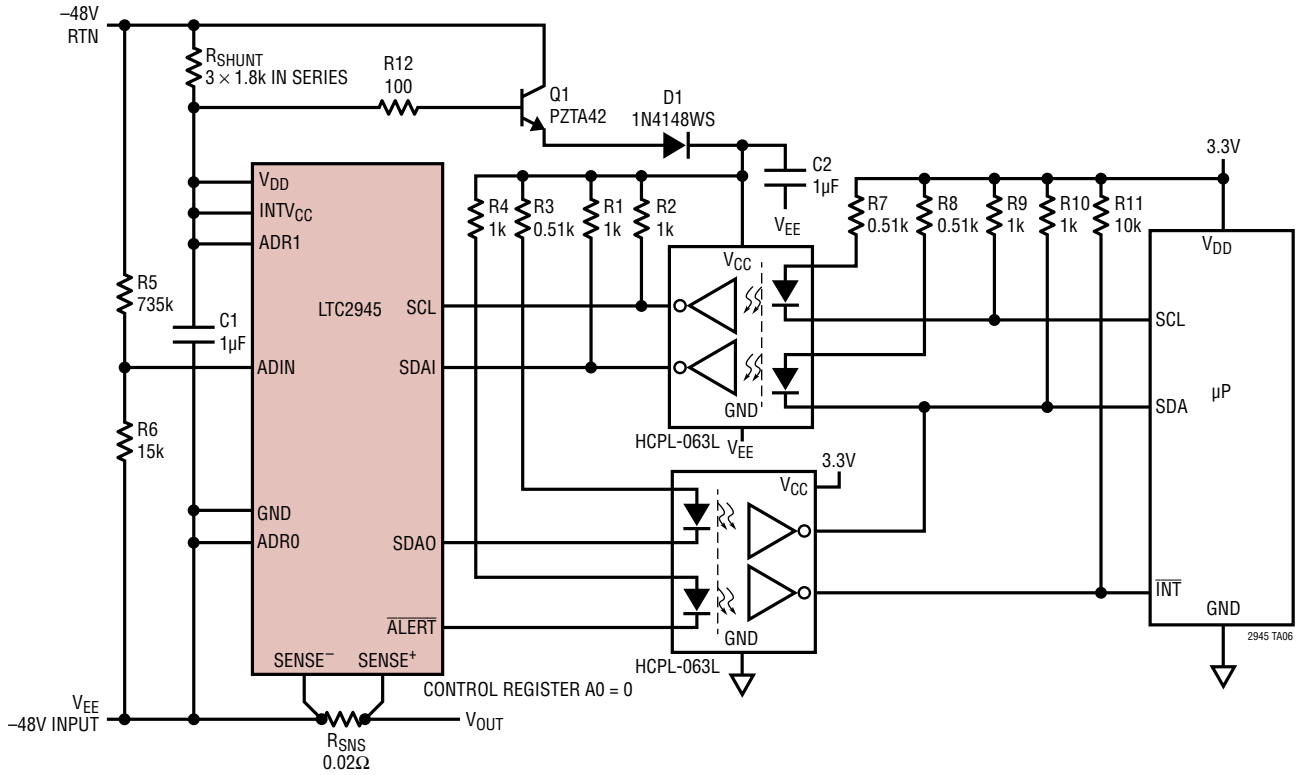


TYPICAL APPLICATIONS

Power Monitoring in –48V System Using Low Side Sensing (1.5kHz I²C Interface)



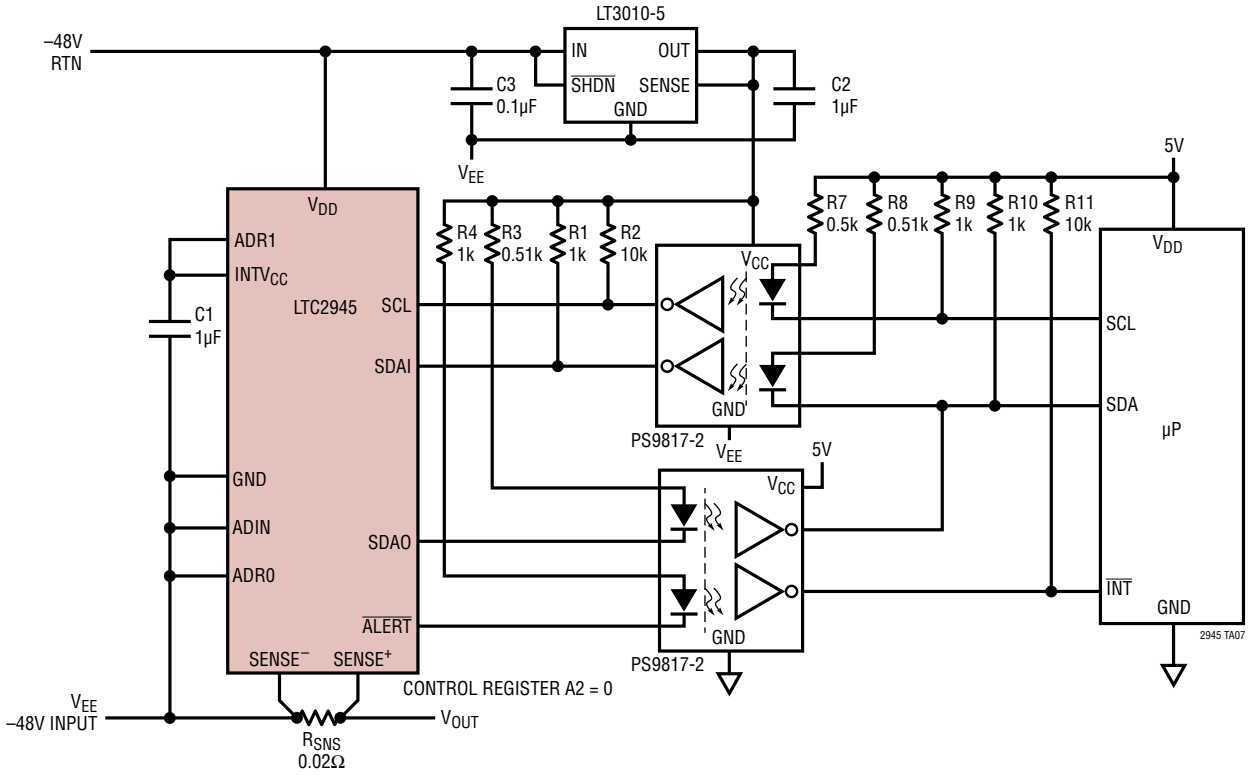
Power Monitoring in –48V Harsh Environment Using $INTV_{CC}$ Shunt Regulator to Tolerate 200V Transients



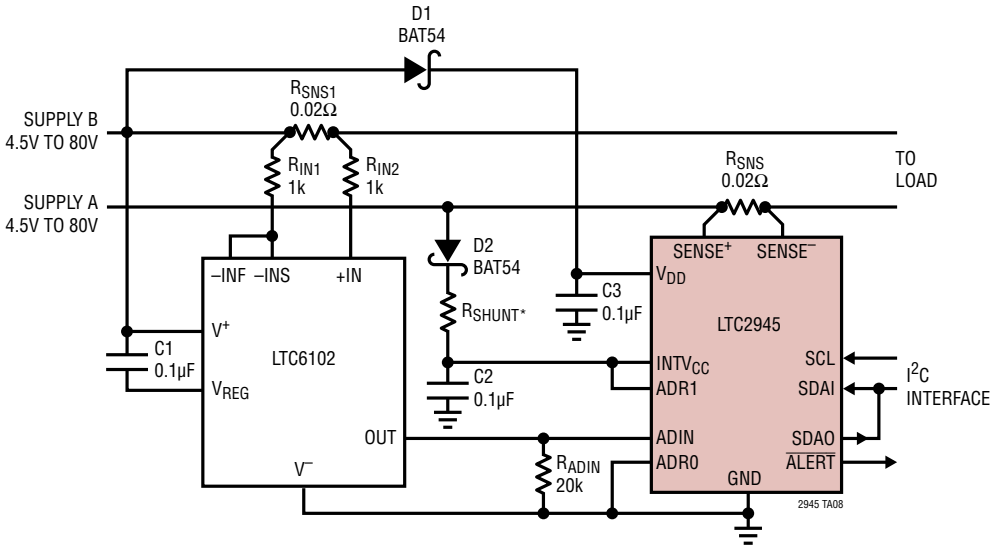
Rev. C

TYPICAL APPLICATIONS

Power Monitoring in –48V System Using External Linear Regulator to Supply Opto-Couplers and SCL/SDA Resistive Pull-Ups



Wide Range Dual Supply Monitor with Single LTC2945

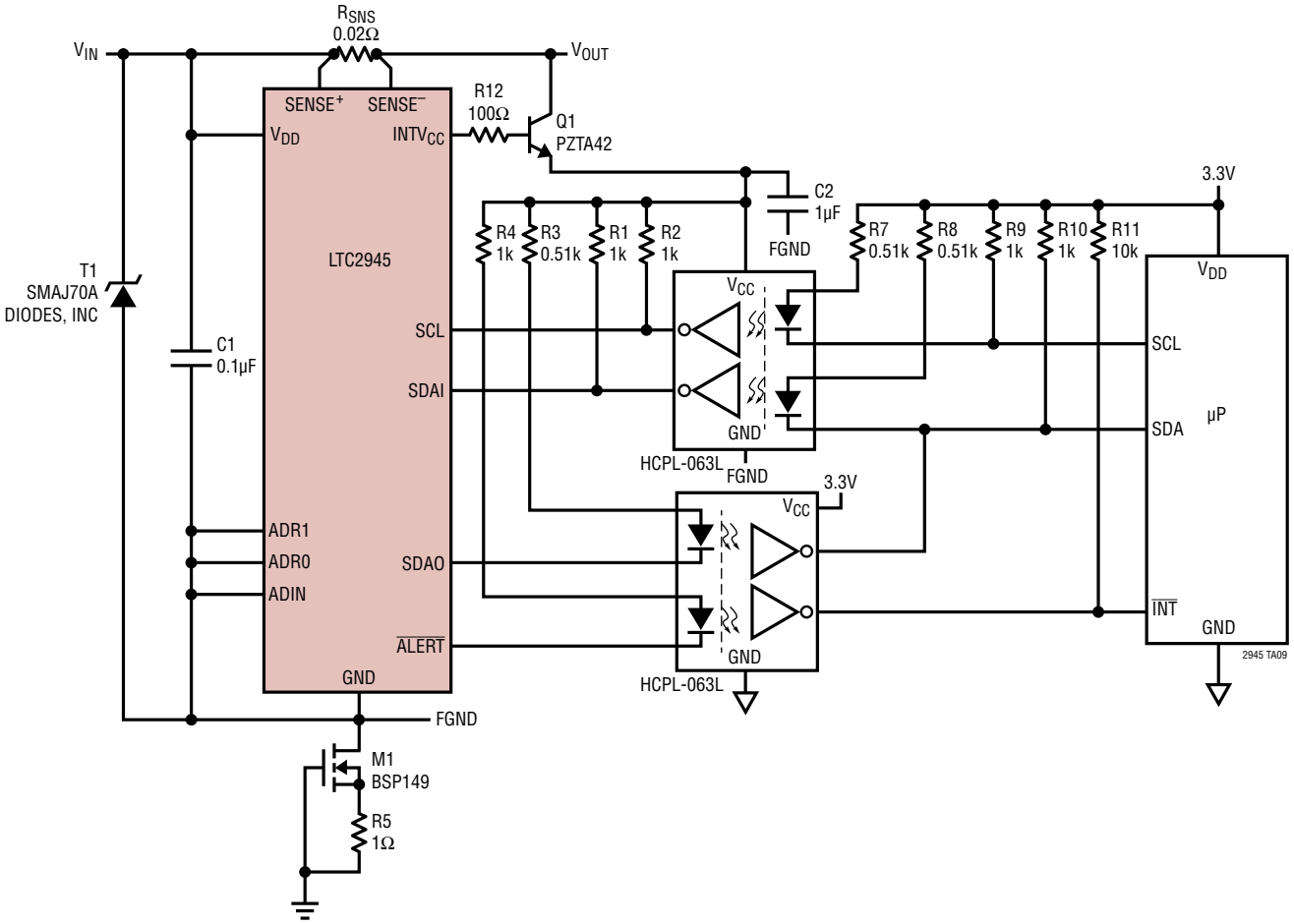


	CONTROL REG A2	VOLTAGE DATA	CURRENT DATA	POWER DATA
SUPPLY A	1	SENSE+	ΔSENSE	INTERNALLY GENERATED
SUPPLY B	0	V_{DD}**	ADIN	USE EXTERNAL µP TO MULTIPLY VOLTAGE (V_{DD}) AND CURRENT (ADIN) DATA

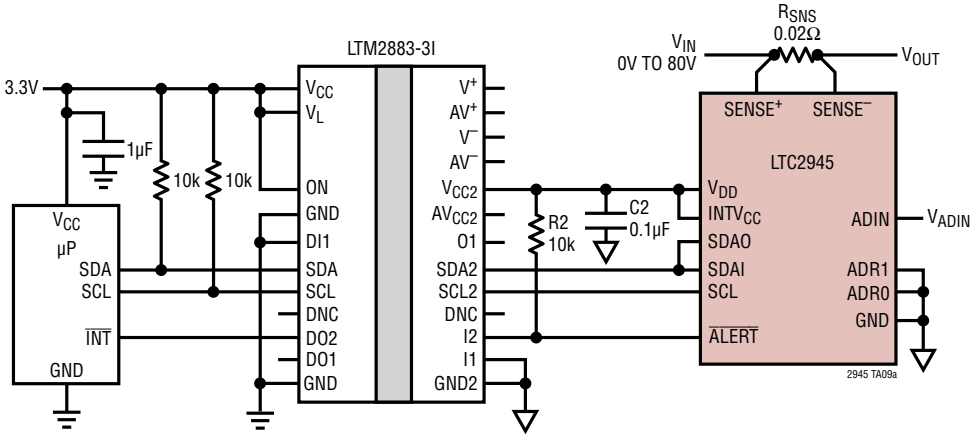
* SELECT RSHUNT ACCORDING TO THE EQUATION IN THE "FLEXIBLE POWER SUPPLY TO LTC2945" SECTION.
** VOLTAGE DATA HAS AN OFFSET VALUE DUE TO D1'S DROP, IF DESIRABLE THIS CAN BE COMPENSATED THROUGH SOFTWARE.

TYPICAL APPLICATIONS

Ruggedized 4V to 70V High Side Power Monitor with Surge Protection Up to 200V

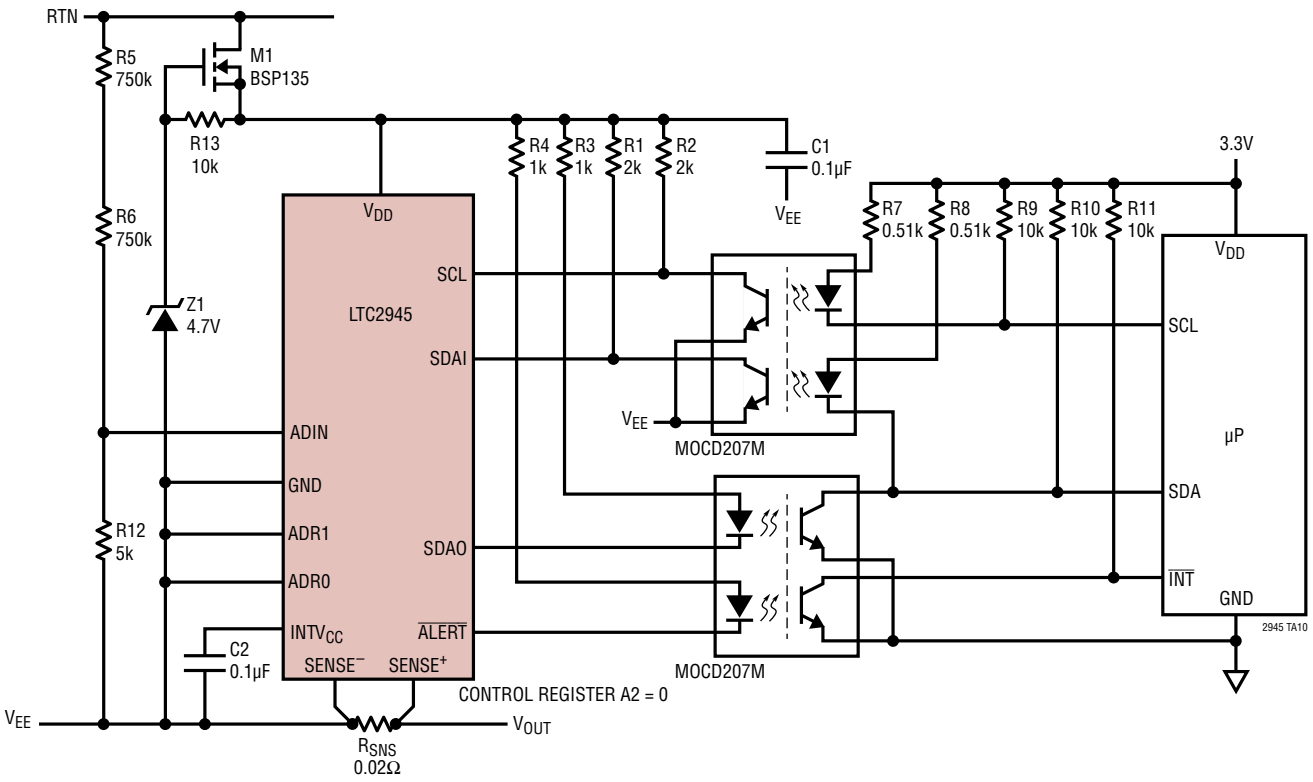


Isolated Wide Range I²C Power Monitor



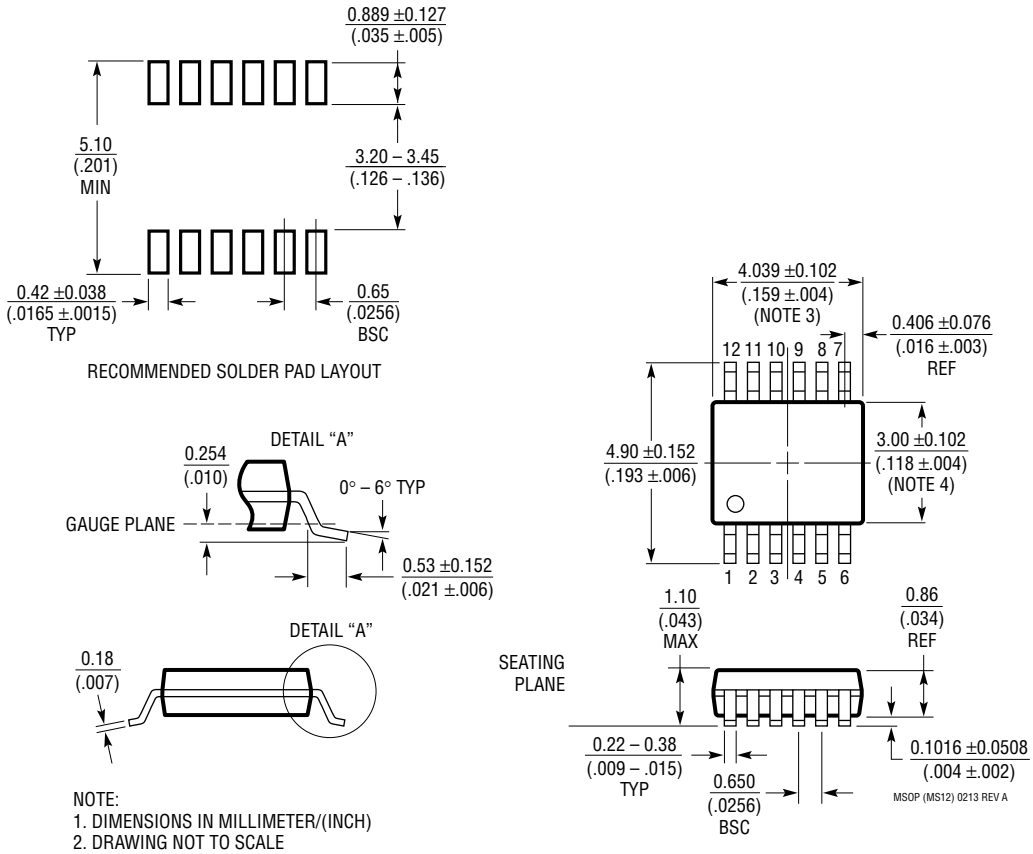
TYPICAL APPLICATIONS

Wide Range –4V to –500V Negative Power Monitor (10kHz I²C Interface)



PACKAGE DESCRIPTION

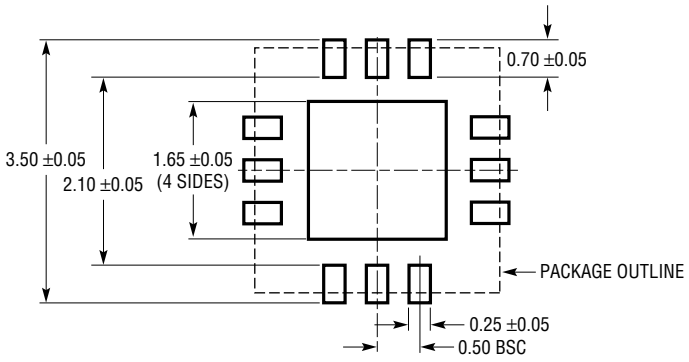
MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)



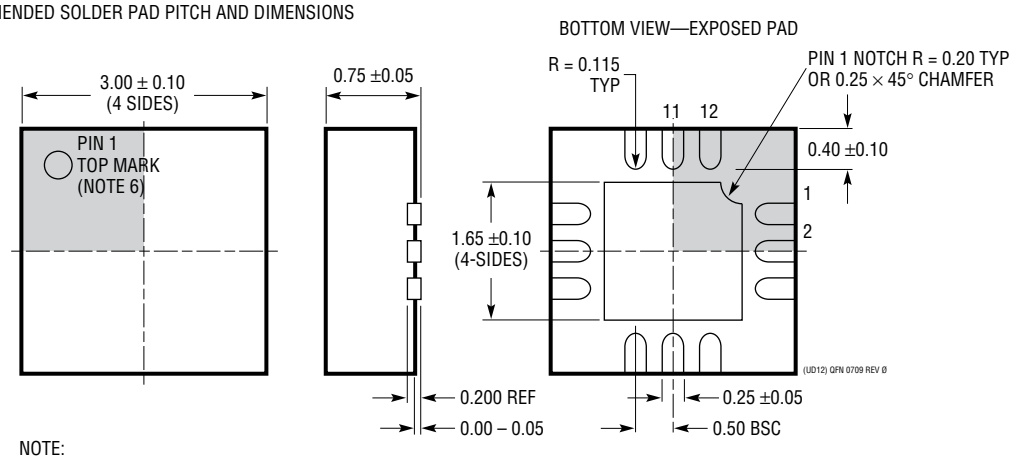
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

UD Package
12-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1855 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/13	Added Limits to Full-Scale Voltage.	4
		Removed Note 5 from I^2C Interface Timing.	5
		Added Note 5 to SCL, SDAI Input Capacitance.	5
		Added ADIN and Resistive Divider Information with Regards to Figure 3a and Figure 3c.	12
		Revised Figure 3a and Figure 3c.	13
		Revised Figure 14 and Figure 19.	19, 20
		Revised Bottom Figure.	26
		Top Figure: Replaced SMAJ78A with SMAJ70A and Changed C2 Connection from VEE to FGND.	29
		Added “Isolated Wide Range I^2C Power Monitor” Figure.	29
B	9/15	Added H-Grade.	2, 3
C	02/22	Added Automotive “W” Part Numbers.	2
		Added Pin Numbers to Pin Functions.	8
		Renumbered Figure 4 through Figure 19.	14, 16, 18-20