Current, Voltage, and Charge Monitor for High Voltage Battery Packs

FEATURES

- **Measures Battery Stack Voltage, Current and Power**
- **Indicates Accumulated Battery Charge and Energy**
- **20-Bit Current Measurement with <1µV Offset**
- **Built-In Isolated isoSPI™ or SPI Interface**
- **LTC68xx/ADBMS68xx Compatible, Supports Synchronous Measurements with Cell Monitors**
- Up to 12 Buffered Voltage Measurement Inputs
- Up to 5 GPIOs, Configurable to Drive Ground, Supply or Toggling at 400kHz
- High or Low Side Current Sense
- 0.3% Current and Voltage Accuracy
- 1% Energy and Charge Accuracy
- True Average ADCs
- I^2C EEPROM Interface to Store Board Calibration Factors
- Threshold Registers for all Measured Quantities
- Engineered for ISO26262 Compliant Systems
- Open Wire Detection on Input Pins
- Available in 48-Lead LQFP Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Electric and Hybrid Vehicles
- Isolated Current Sensing
- Backup Battery Systems
- High Power Portable Equipment

DESCRIPTION

The LTC®2949 is a high precision current, voltage, temperature, charge and energy meter for electrical and hybrid vehicles and other isolated current sense applications. It infers charge and energy flowing in and out of the battery pack by monitoring simultaneously the voltage drop over up to two sense resistors and the battery pack voltage.

Low offset ΔΣ ADCs ensure accurate measurement of voltage and current with insignificant power loss. Continuous integration of current and power ensures lossless tracking of charge and energy delivered or received by the battery pack.

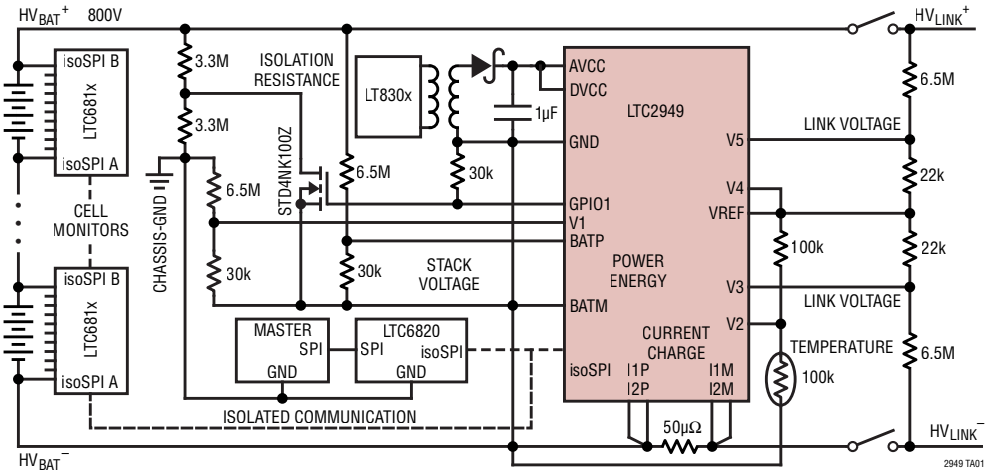
The built-in serial interface can be configured to support isolated isoSPI communication to the host or as SPI interface.

The LTC2949 features 12 internally buffered high impedance inputs (V1 to V12) for measuring voltages from external sensors or resistor dividers allowing to measure temperatures, HV-Link voltages, chassis isolation and supervise contactor states. LTC2949 has up to five programmable digital outputs which can be set to ground, supply or toggling at 400kHz.

Programmable threshold and tracking registers reduce digital traffic to the host.

TYPICAL APPLICATION

Electric Vehicle Battery Meter



Rev A

TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Pins

AVCC to AGND ..... –0.3V to 14.5V
DVCC to DGND..... –0.3V to 14.5V
AVCC to DVCC..... –0.1V to 0.1V
DGND to AGND. ..... –0.1V to 0.1V

Analog Pins

I1P, I1M, I2P, I2M ..... –0.3V to V_{AVCC} + 0.3V
I1P to I1M, I2P to I2M .....±1V
VBATP, VBATM ..... –0.3V to V_{AVCC} + 0.3V
V1-V12..... –0.3V to V_{AVCC} + 0.3V
CLKO, DNC.....(Note 3)

Digital Input/Output Pins

IOVCC, CLKI, CSB(IM), SCK(IP)..... –0.3V to 5V
SDI (ICMP), SDO (IBIAS)..... –0.3V to 5V
SDA, SCL ..... –0.3V to 2.75V

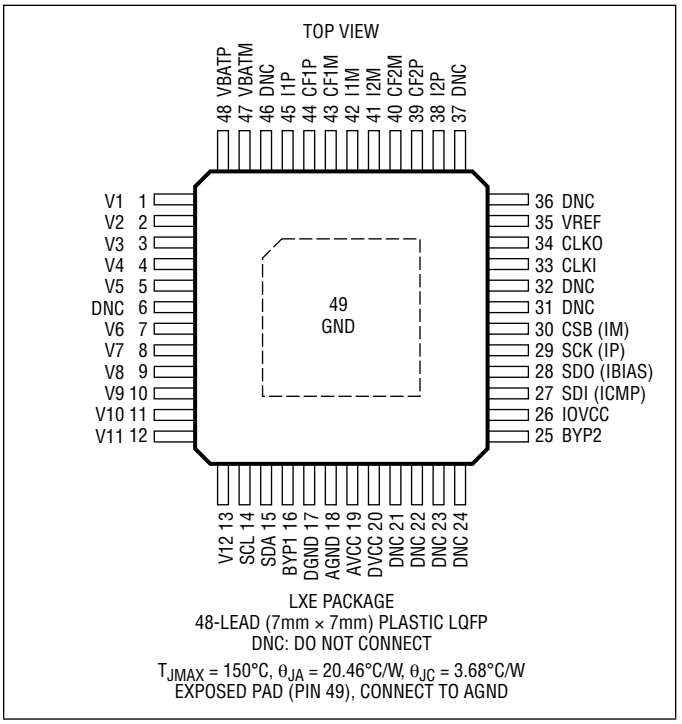
Current In/Out of Pins

IP, IM.....±30mA
SDO (IBIAS) ..... –1mA to 9mA
V8-V12 .....±2mA
VREF (Note 4) .....±2mA
BYP1 (Note 4)..... –10mA to 0mA
BYP2 (Note 4)..... –10mA to 0mA

Operating Ambient Temperature Range

LTC2949I .....–40°C to 85°C
LTC2949H.....–40°C to 125°C
Storage Temperature Range…..... .....–65°C to 150°C

PIN CONFIGURATION



LXE PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP
DNC: DO NOT CONNECT

T_{JMAX} = 150°C, θ_{JA} = 20.46°C/W, θ_{JC} = 3.68°C/W
EXPOSED PAD (PIN 49), CONNECT TO AGND

ORDER INFORMATION

AUTOMOTIVE PRODUCTS**

TRAY (250PC)	TAPE AND REEL (2000PC)	PART MARKING*	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE
LTC2949ILXE#3ZZPBF	LTC2949ILXE#3ZZTRPBF	LTC2949LXE	48-LEAD PLASTIC eLQFP	3	–40°C to 85°C
LTC2949HLXE#3ZZPBF	LTC2949HLXE#3ZZTRPBF	LTC2949LXE	48-LEAD PLASTIC eLQFP	3	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #3ZZ suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply								
V_{AVCC}	Analog Supply Voltage			●	4.5		14	V
V_{DVCC}	Digital Supply Voltage			●	4.5		14	V
V_{UVLO}	Supply Undervoltage Lockout Threshold	V_{AVCC}, V_{DVCC} Falling		●			4.5	V
I_{CC}	Average Supply Current into AVCC and DVCC	Core State: STANDBY or MEASURE		●		16	20	mA
		Core State: SLEEP				9	15	µA
		Core State: SLEEP		●			150	µA
	Additional DVCC Supply Current if isoSPI in READY/ACTIVE States Note: ACTIVE State Current Assumes t_{CLK} = 1µs, (Note 5)	R_{B1} + R_{B2} = 2k	READY	●		4.8	5.8	mA
			ACTIVE	●		6.1	7.8	mA
		R_{B1} + R_{B2} = 20k	READY	●		2.1	3	mA
			ACTIVE	●		2.5	3.5	mA
V_{BYP1}	BYP1 Regulated Output Voltage			●	2.25	2.5	2.75	V
	BYP1 Load Current			●	–10		0	mA
	BYP1 Load Regulation Error	I_{LOAD} = –10mA		●	–15		0	mV
	BYP1 Undervoltage Lockout Threshold			●			2.25	V
V_{BYP2}	BYP2 Regulation Output Voltage			●	3	3.25	3.6	V
	BYP2 Load Current			●	–10		0	mA
	BYP2 Load Regulation Error	I_{LOAD} = –10mA		●	–60			mV
	Thermal Shutdown Temperature					170		°C
Current Sense ADC								
	Resolution (No Missing Codes)	Slow Mode Filtered (Note 7)		●	20			Bit
		Slow Mode (Note 7)		●	18			Bit
		Fast Mode (Note 7)		●	15			Bit
	Full-Scale Differential Input Voltage	V_{I1P}-V_{I1M}, V_{I2P}-V_{I2M}				±124		mV
$VDIF_I$	Differential Input Voltage Range	V_{I1P}-V_{I1M}, V_{I2P}-V_{I2M}		●			±110	mV
	Pin Voltage of I1P, I1M, I2P, I2M			●	–0.11		V_{AVCC}+0.11	V
	Current Sense Quantization Step	Slow Mode Filtered				237.5		nV
		Slow Mode				950		nV
		Fast Mode				7.60371		µV
CFPx	Input Leakage Current at CF1P, CF1M, I1P, I1M, CF2P, CF2M, I2P, I2M	Core State = SLEEP/STANDBY		●			60	nA
	Differential Input Current from CF1P to CF1M, CF2P to CF2M	Core State: MEASURE; Pin Voltages: 0V ≤ V_{CF1P}, V_{CF1M}, V_{I1P}, V_{I1M}, V_{CF2P}, V_{CF2M}, V_{I2P}, V_{I2M} ≤ V_{AVCC}				$VDIF_I$/100kΩ		µA
	Noise	Slow Mode Filtered				160		nV_{RMS}
		Slow Mode				320		nV_{RMS}
		Fast Mode				3		$µV_{RMS}$
	Gain Error	$\|VDIF_I\|$ ≤ 110mV					0.15	%
				●			0.3	%
	Offset Voltage	IADCx, IxP, IxM = 0V	Slow Mode	●		0	±1	µV
		V_{AVCC} = V_{DVCC} = 5V	Fast Mode	●		0	±2	µV
	Total Unadjusted Error	$\|VDIF_I\|$ ≥ 25mV		●			0.3	%

Rev A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Voltage Common Mode Rejection at DC		●	100			dB
	Input Sampling Frequency				10.48		MHz
	Conversion Time	Slow Mode Filtered			400		ms
		Slow Mode			100		ms
		Fast Mode	●		0.782	0.8211	ms
Voltage Measurement by Power ADC							
	Resolution (No Missing Codes)	Slow Mode (Note 7)	●	18			Bit
		Fast Mode (Note 7)	●	15			Bit
VFS_V	Full-Scale Differential Input Voltage	$V_{VBATP} – V_{VBATM}$			±6.14		V
$VDIF_V$	Differential Input Voltage Range	$V_{VBATP} – V_{VBATM}$	●			±4.8	V
	Pin Voltage of VBATP, VBATM	$V_{AVCC} \geq 5V$	●	–0.1		V_{AVCC}+0.1	V
		$V_{AVCC} < 5V$	●	–0.1		V_{AVCC}-1.5	V
LSB_V	Differential Input Voltage Quantization Step	Slow Mode			46.875		µV
		Fast Mode			375.183		µV
	Input Leakage Current	Core State: SLEEP/STANDBY	●			60	nA
	Differential Input Resistance	Core State: MEASURE; Pin Voltages 0V ≤ V_{BATP}, $V_{BATM} \leq V_{AVCC}$		50			MΩ
			●	20			MΩ
	Gain Error		●			0.3	%
	Offset	$V_{BATP} = V_{BATM}$ = 0V	●		0	±3	LSB_V
	Voltage Total Unadjusted Error	$1V \leq \lvert VDIF_V \rvert \leq 4.8V$	●			0.4	%
	Input Voltage Common Mode Rejection at DC		●	80			dB
	Noise	Slow Mode (Note 7)			3		$µV_{RMS}$
		Fast Mode (Note 7)			30		$µV_{RMS}$
	Input Sampling Rate				5.24		MHz
	Conversion Time	Slow Mode			100		ms
		Fast Mode	●		0.782	0.8211	ms
Power Measurement by Power ADC							
	Resolution (No Missing Codes)	Slow Mode (Note 7)	●	18			Bit
		Fast Mode (Note 7)	●	11			Bit
FS_P	Full-Scale Power	$FS_P = VFS_V \bullet VFS_I/R_{ISENSE}/VDIV_V$			±0.76504		$[V^2/Ω]$
LSB_P	Power Quantization Step	$LSB_P = FS_P/2^{17}$			5.8368		$µ[V^2/Ω]$
POS	Power Offset	$VDIF_1 = 0$			1		LSB_P
TUE_P	Power Total Unadjusted Error	$1V \leq \lvert VDIF_V \rvert \leq 4.8V$, $25mV \leq \lvert VDIF_I \rvert \leq 110mV$	●			0.9	%
	RMS Noise	Slow Mode; VBATP – VBATM = 4.8V (Note 7)			0.3		LSB_P
		Slow Mode; VBATP – VBATM = 0V (Note 7)			0.03		LSB_P
	Input Sampling Frequency				5.24		MHz
	Power Modulation Frequency				5.24		MHz
	Conversion Time	Slow Mode			100		ms
		Fast Mode	●		0.782	0.8211	ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Energy Measurement							
TUE_E	Energy Total Unadjusted Error	1V ≤ |VDIF$_V$| ≤ 4.8V, 25mV ≤ |VDIF$_I$| ≤ 110mV, Ideal External Clock or 4MHz Crystal	●			0.9	%
		1V ≤ |VDIF$_V$| ≤ 4.8V, 25mV ≤ |VDIF$_I$| ≤ 110mV, Internal Clock	●			1.9	%
Charge Measurement							
TUE_C	Charge Total Unadjusted Error	1V ≤ |VDIF$_V$| ≤ 4.8V, 25mV ≤ |VDIF$_I$| ≤ 110mV, Ideal External Clock or 4MHz Crystal	●			0.4	%
		1V ≤ |VDIF$_V$| ≤ 4.8V, 25mV ≤ |VDIF$_I$| ≤ 110mV, Internal Clock	●			1.4	%
Voltage Measurement by AUXILIARY ADC							
	Resolution (No Missing Codes)	(Note 7)	●	15			Bit
VFS_{AUX}	Full-Scale Differential Input Voltage	$V_{VBATP} – V_{VBATM}$, $V_{MUXP} – V_{MUXN}$			±6.14		V
$VDIF_{AUX}$	Differential Input Voltage Range	$V_{VBATP} – V_{VBATM}$, $V_{MUXP} – V_{MUXN}$	●			±4.8	V
	Pin Voltage of VBATP, VBATM, V1 – V12, CF1P, CF1M, CF2P, CF2M	V_{AVCC} ≥ 5V	●	–0.1		V_{AVCC}+0.1	V
		V_{AVCC} < 5V	●	–0.1		V_{AVCC}–1.5	V
LSB_{AUX}	Differential Voltage Quantization Step	Slow Mode			375		µV
		Fast Mode			375.183		µV
	Input Leakage Current		●		1	60	nA
	Differential Input Resistance		●	40			MΩ
	Gain Error	|$VDIF_{AUX}$| ≤ 4.8V	●			0.3	%
	Offset	$V_{BATP} = V_{BATM}$ = 0V	●		0	±1	LSB_V
	Total Unadjusted Error	1V ≤ |VDIF$_V$| ≤ 4.8V	●			0.4	%
	Input Voltage Common Mode Rejection at DC		●	80			dB
	Sampling Rate				5.24		MHz
	Conversion Time		●		0.782	0.8211	ms
On-Die Temperature Measurement by AUXILIARY ADC							
	Resolution (No Missing Codes)	(Note 7)	●	13			Bit
	Full-Scale Temperature				819.2		K
ΔT_{LSB}	Temperature Quantization Step				0.2		K
	Total Unadjusted Error				±3		K
	Conversion Time				13.1		ms
	Self-Heating				20		K/W
Supply Voltage Measurement by AUXILIARY ADC							
	Resolution (No Missing Codes)	(Note 7)	●	14			Bit
	Full-Scale Differential Input Voltage				18.43		V
	A/DVCC Measurement Quantization Step				2.2583		mV
	Total Unadjusted Error		●		2	±5	%
	Conversion Time				6.55		ms
AUX MUX							
	Signal Range		●	–0.1		V_{AVCC}+0.1	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Pull-Up Current Source	Pin Voltage < V_{AVCC} – 3.0V	●		–250	–150	µA
	Pull-Down Current Source	Pin Voltage > 2.5V	●	200	250		µA
Reference Voltages							
VREF	Reference Pin Voltage				3		V
	VREF Error		●			±1	%
	VREF Temperature Coefficient				7		ppm/K
	VREF Long Term Drift				80		ppm/$\sqrt{kHr}$
	VREF Load Regulation Error	–0.5mA ≤ I_{LOAD} ≤ 0.5mA	●	–5		0	mV
VREF2	Internal Redundant Reference Voltage				2.39		V
	VREF2 Error		●			±0.85	%
	VREF2 Temperature Coefficient				10		ppm/K
	VREF2 Long Term Drift				80		ppm/$\sqrt{kHr}$
Overcurrent Comparator							
	Pin Voltages I1P, I1M I2P, I2M		●	–0.11		V_{AVCC}+0.11	V
	Total Unadjusted Error	|Vthr| ≤ 103mV	●			±5	mV
		|Vthr| > 103mV	●			±10	mV
		|Vthr| = 310mV	●			±20	mV
	Programmable Deglitch Time Delay	T_{degl} 20, 80, 320µs	●	T_{degl} –10		T_{degl} +37	µs
		T_{degl} 1280µs	●	T_{degl} –26		T_{degl} +56	µs
Digital Input CLKI							
	Logic Input Threshold		●	0.4		2	V
	Input Current DC Current		●			±1	µA
	Input Capacitance	(Note 7)	●			10	pF
	External Clock Frequency		●	0.1		25	MHz
General Purpose Outputs GPIOx							
	Low Level Output Voltage at GPIOx	I_{GPIOx} = 0.5mA	●			0.4	V
	High Level Output Voltage at GPIOx	I_{GPIOx} = –0.25mA	●	V_{DVCC} –0.5			V
	GPIOx Toggling Frequency		●	370	400	430	kHz
SPI Interface DC Specification IOVCC, CSB, SCK, SDI, SDO							
V_{IOVCC}	SPI Mode IOVCC Operating Voltage		●	1.8		4.5	V
	Pin Voltages CSB, SCK, SDI, SDO		●			V_{IOVCC}	V
	Logic Input Threshold (CSB, SCK, SDI)		●	0.3 • V_{IOVCC}		0.7 • V_{IOVCC}	V
	DC Input Current (CSB, SCK, SDI)		●			±1	µA
	Input Capacitance (CSB, SCK, SDI)	(Note 7)	●			10	pF
	Low Level Output Voltage at SDO	V_{IOVCC} ≥ 3.3V, I_{SDO} = 3mA, 1.8V ≤ V_{IOVCC} ≤ 3.3V, I_{SDO} = 1mA	●			0.4	V
SPI Timing Requirements (See Figure 7)							
t_{CLK}	SCK Period	(Note 6)	●	1			µs
t_1	SDI Setup Time Before SCK Rising Edge		●	25			ns
t_2	SDI Hold Time After SCK Rising Edge		●	25			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_3	SCK Low	$t_{CLK} = t_3 + t_4 \geq 1\mu s$	●	200			ns
t_4	SCK High	$t_{CLK} = t_3 + t_4 \geq 1\mu s$	●	200			ns
t_5	CSB Rising Edge to CSB Falling Edge		●	0.65			µs
t_6	SCK Rising Edge to CSB Rising Edge	(Note 6)	●	0.8			µs
t_7	CSB Falling Edge to SCK Rising Edge	(Note 6)	●	1			µs
t_8	SCK Falling Edge to SDO Valid	(Note 9), VIOVCC ≥ 3.3V	●			60	ns
		(Note 9), VIOVCC < 3.3V	●			150	ns
isoSPI DC Specifications (See Figure 10)							
	Voltage at IOVCC to Select isoSPI		●			0.5	V
V_{IBIAS}	Voltage on IBIAS Pin	READY/ACTIVE State	●	1.9	2	2.1	V
		IDLE			0		V
I_B	Isolated Interface Bias Current	R_{BIAS} = 2kΩ to 20kΩ	●	0.1		1	mA
A_{IB}	Isolated Interface Current Gain	$V_A \leq 1V$, I_B = 1mA	●	18	20	22	mA/mA
		I_B = 0.1mA	●	17	20	24.5	mA/mA
V_A	Transmitter Pulse Amplitude	$V_A = \lvert V_{IP} - V_{IM} \rvert$	●			1.4	V
V_{ICMP}	Threshold-Setting Voltage on ICMP Pin	$V_{TCMP} = A_{TCMP} \bullet V_{ICMP}$	●	0.2		1.5	V
	Input Leakage Current on ICMP Pin	V_{ICMP} = 0V to V_{BYP2}	●			±1	µA
	Leakage Current on IP and IM Pins	IDLE State, V_{IP} or V_{IM} = 0V to V_{BYP2}	●			±1	µA
A_{TCMP}	Receiver Comparator Threshold Voltage Gain	V_{CM} = V_{BYP2}/2 to V_{BYP2} – 0.2V, V_{ICMP} = 0.2V to 1.5V	●	0.4	0.5	0.6	V/V
V_{CM}	Receiver Common Mode Bias	IP, IM Not Driving			V_{BYP2} – V_{ICMP}/3 – 167mV		V
	Receiver Input Resistance	Single-Ended to IP, IM	●	27	35	43	kΩ
isoSPI IDLE/WAKE-UP Specifications (See Figure 3)							
V_{WAKE}	Differential Wake-Up Voltage	t_{DWELL} = 240ns	●	200			mV
t_{DWELL}	Dwell Time at V_{WAKE} Before Wake Detection	V_{WAKE} = 200mV	●	240			ns
t_{READY}	Start-Up Time After Wake Detection		●			10	µs
t_{IDLE}	Idle Timeout Duration		●	4.3	6.4	8	ms
isoSPI Pulse Timing Specifications (See Figures 10,11)							
$t_{FILT(CS)}$	Chip-Select Signal Filter	Receiver	●	70	90	115	ns
$t_{WNDW(CS)}$	Chip-Select Valid Pulse Window	Receiver	●	220	270	330	ns
$t_{1/2PW(D)}$	Data Half-Pulse Width	Transmitter	●	40	50	60	ns
$t_{FILT(D)}$	Data Signal Filter	Receiver	●	10	25	35	ns
$t_{INV(D)}$	Data Pulse Inversion Delay	Transmitter	●	40	55	69	ns
$t_{WNDW(D)}$	Data Valid Pulses Window	Receiver	●	70	90	110	ns
t_{RTN}	Data Return Delay		●		485	625	ns
I^2C Interface DC Specification (SCL, SDA)							
	Logic Input Threshold (SDA)		●	0.9		1.6	V
	DC Input Current (SDA)		●			±1	µA
	Input Capacitance (SDA)	(Note 7)	●			10	pF
	Low Level Output Voltage at SDA, SCL	I = 0.5mA	●			0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Interface Timing Specification (SCL, SDA)							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●		8	10	kHz
t_{SCLLO}	SCL Low Period		●	80			µs
t_{SDALO}	SDA Low Period		●	80			µs
$t_{BUF(MIN)}$	Bus Free Time Between STOP/START		●	30			µs
$t_{SU,STA(MIN)}$	Minimum Repeated START Setup Time		●	30			µs
$t_{HD,STA(MIN)}$	Minimum Hold Time (Repeated) START Condition		●	30			µs
$t_{SU,STO(MIN)}$	Minimum Setup Time for STOP Condition		●	30			µs
$t_{SU,DAT(MIN)}$	Minimum Data Setup Time Input		●	30			µs
$t_{HD,DAT(MIN)}$	Minimum Data Hold Time Input		●			0	ns
$t_{HD,DATO}$	Minimum Data Hold Time Output		●	30			µs
t_{OF}	Data Output Fall Time	(Notes 7, 8)	●	20 + 0.1 • C_B			ns
Digital Core Timings (See Figure 3)							
t_{BOOT}	Core Boot-Up Time from SLEEP or POWER-OFF to STANDBY	AVCC/DVCC Pins at Minimum Operating Voltage	●			100	ms
t_{IDLE_CORE}	Core STANDBY Cycle Time	(Note 10)	●		17	20	ms
t_{CONT}	Core MEASURE Cycle Time	(Note 11)	●	90	100	110	ms
$t_{MLCK,M}$	Memory Lock Request to Acknowledge Time	Core Status MEASURE	●			130	ms
$t_{MLCK,S}$	Memory Lock Request to Acknowledge Time	Core Status STANDBY	●			40	ms
t_{ACKN}	Time from Core Entering STANDBY to Return to SLEEP, When Wake-Up is not Confirmed	No Write of 0x0 to Reg. WKUPACK, No Write of 0x8 to Reg. OPCTRL	●	0.6		1.5	s
Time Base							
TUE_{TB}	TUE Time Base	Internal Clock				0.5	%
			●			1	%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect the device reliability and lifetime.

Note 2: Positive currents flow into pins, negative currents flow out of pins. Minimum and maximum values refer to absolute values.

Note 3: Do not apply a voltage or current source to these pins. They must be unconnected, connected to capacitive loads or connected to a crystal according to their pin description. Otherwise permanent damage may occur.

Note 4: Do not apply a voltage source to these pins. Overloading these pins might disrupt operation.

Note 5: Active supply current (I_{CC}) is dependent on the amount of time that the output drivers are active on IP and IM. During those times I_{CC} will increase by the 20 • I_B drive current. For the maximum data rate 1MHz, the drivers are active approximately 5% of the time.

Note 6: These timing specifications are dependent on the delay through the cable, and include allowances for 50ns of delay each direction. 50ns corresponds to 10m of CAT-5 cable (which has a velocity of propagation of 66% the speed of light). Use of longer cables would require derating these specs by the amount of additional delay.

Note 7: Guaranteed by design and characterization, not subject to production test.

Note 8: C_B = capacitance of one bus line in pf (10pF < C_B < 400pF)

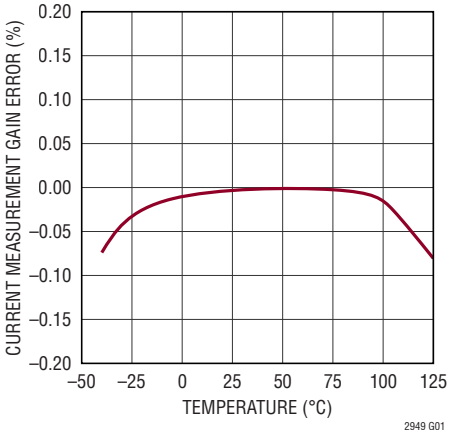
Note 9: These specifications do not include rise time of SDO due to pull up resistance and load capacitance on SDO pin.

Note 10: Cycle time at which STATUS/FAULTS and V_{REF} registers are updated.

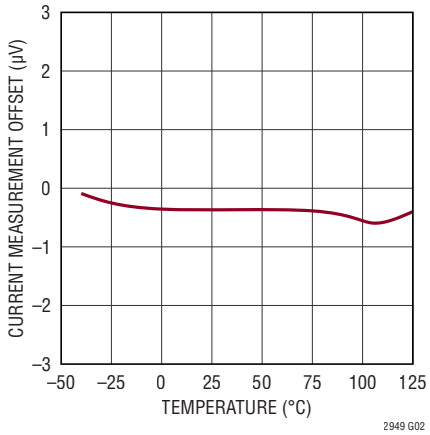
Note 11: Cycle time at which STATUS/ALERT/FAULTS registers and all slow channel measurement results are updated after the first update. The first update after enabling any measurement is typically 50ms delayed.

TYPICAL PERFORMANCE CHARACTERISTICS

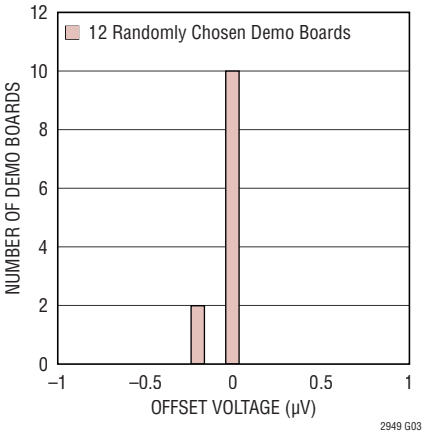
Current Measurement Gain Error vs Temperature



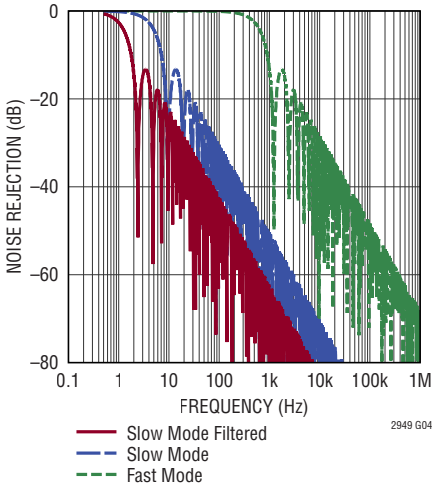
Current Measurement Offset vs Temperature



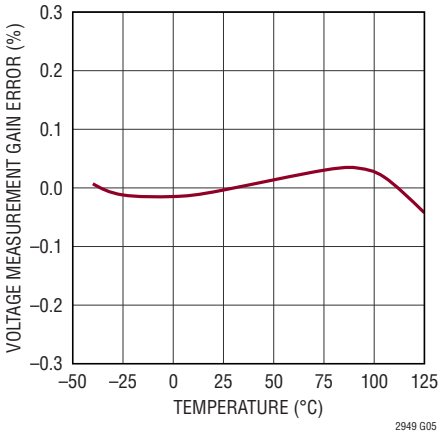
Current Measurement Offset Distribution



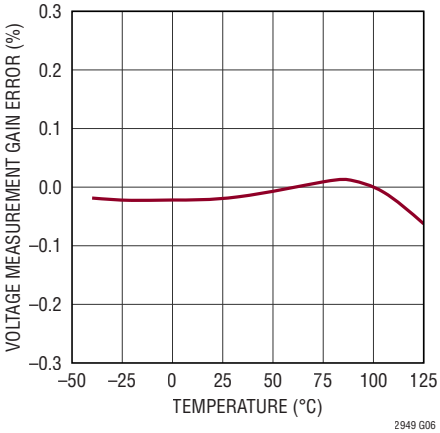
Current Measurement Noise Filter Response



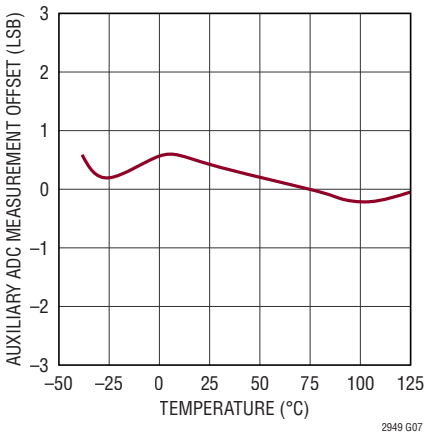
Power as Voltage Gain Error vs Temperature



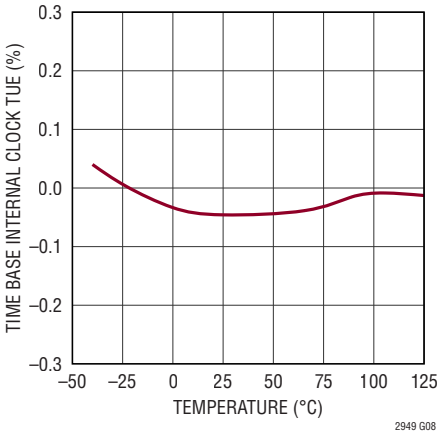
AUXADC Gain Error vs Temperature



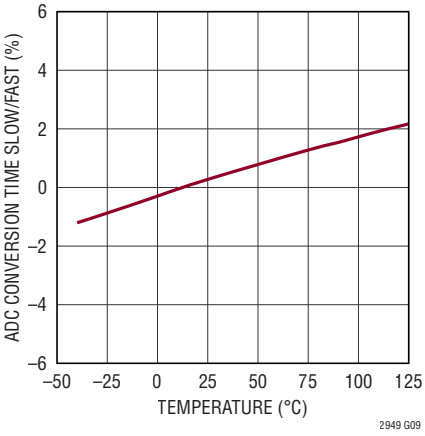
Auxiliary ADC Measurement Offset vs Temperature



Time Base Internal Clock TUE vs Temperature



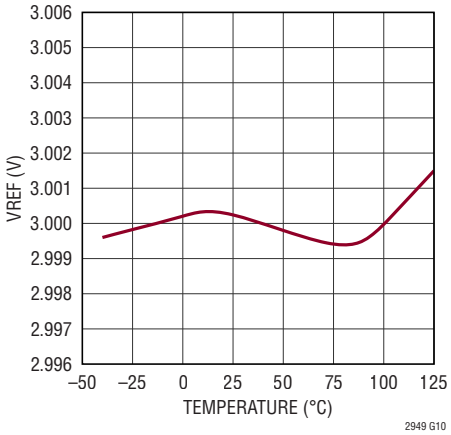
ADC Conversion Time Error Slow/ Fast vs Temperature



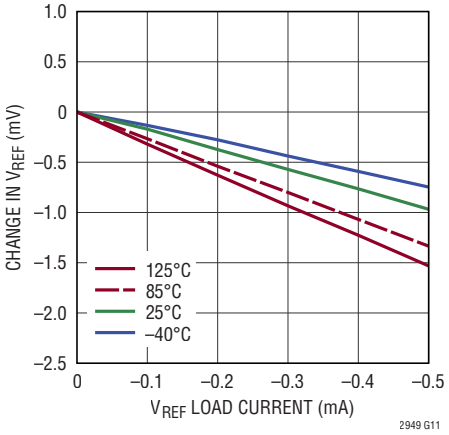
Rev A

TYPICAL PERFORMANCE CHARACTERISTICS

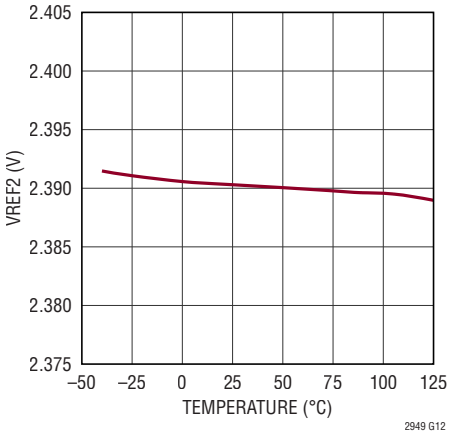
VREF vs Temperature



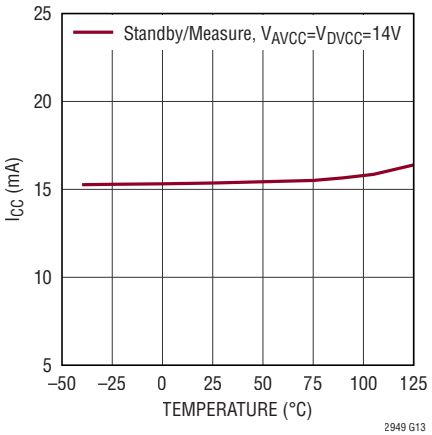
VREF Load Regulation



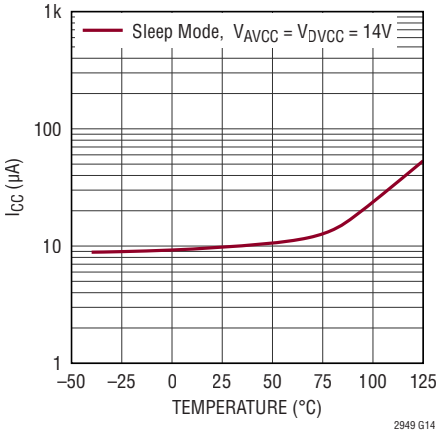
VREF2 vs Temperature



AVCC/DVCC Supply Current Standby/Measure vs Temperature



AVCC/DVCC Supply Current vs Temperature



PIN FUNCTIONS

AVCC (Pin 19): Analog Supply Voltage. Bypass this pin to AGND with a 0.1µF (or greater) capacitor. AVCC operating range is 4.5V to 14V.

AGND (Pin 18): Analog Ground. Bypass this pin to AVCC with a 0.1µF (or greater) capacitor.

BYP1 (Pin 16): Internal Supply Voltage. Bypass BYP1 to DGND with a 1µF capacitor. BYP1 is regulated to 2.5V. Can supply external circuitry (example EEPROM) with up to 10mA. Overloading might disrupt LTC2949 functionality.

BYP2 (Pin 25): Internal 3.25V Supply Voltage. Bypass BYP2 to DGND with a 1µF capacitor. Can supply external circuitry (example SPI isolator ADuM141E or ADuM4154) with up to 10mA. Overloading might disrupt LTC2949 functionality.

CF1P, CF1M (Pins 44, 43): Filter Capacitor Inputs for the first current channel. Connect a 1µF capacitor between CF1P and CF1M for filtering differential noise and fast current variations. Connect 0.1µF capacitors between AGND and the filter pins for damping high frequency common mode variations.

PIN FUNCTIONS

CF2P, CF2M (Pins 39, 40): Filter Capacitor Inputs for the second current channel. Connect a 1µF capacitor between CFI2P and CFI2M for filtering differential noise and fast current variations. Connect 0.1µF capacitors between AGND and the filter pins for damping high frequency common mode variations.

CLKI (Pin 33): Clock Input. Connect to ground if internal clock is used. For improved measurement accuracy, connect a 4MHz crystal between CLKI and CLKO and matching capacitors to ground, or drive with an external clock. See the Timebase Control section.

CLKO (Pin 34): Clock Output. Connect a 4MHz crystal between CLKO and CLKI if used; leave pin unconnected otherwise.

CSB/IM (Pin 30): Active Low Chip Select in SPI mode or Isolated Interface Negative Input/Output in isoSPI mode.

DGND (Pin 17): Digital Ground. Connect to AGND.

DNC (Pins 6, 21, 22, 23, 24, 31, 32, 36, 37, 46): Do not connect.

DVCC (Pin 20): Supply Voltage. Bypass this pin to DGND with a 1µF capacitor. Operating range is 4.5V to 14V.

I1P, I1M (Pins 45, 42): Differential Input of I1ADC and overcurrent comparator 1. Tie to AGND if unused.

I2P, I2M (Pins 38, 41): Differential Input of I2ADC and overcurrent comparator 2. Tie to AGND if unused.

IOVCC (Pin 26): Serial Interface Configuration and Supply Pin. Tie pin to DGND for isoSPI communication. Tie pin to a voltage ≥1.8V and ≤ 4.5V and bypass with 1µF to DGND for standard SPI communication. In SPI mode IOVCC supplies the digital input and output circuits of the serial interface.

SCK/IP (Pin 29): Serial Clock Input in SPI mode or Isolated Interface Positive Input/Output in isoSPI mode.

SCL (Pin 14): I^2C Master Clock Open Drain Output. Connect to clock input of EEPROM.

SDA (Pin 15): I^2C Data Input And Open Drain Output. Connect to data line of EEPROM. SDA driven low at power up prevents LTC2949 to go automatically into SLEEP state and to execute HW memory BIST. Connect a 4.7k-10k pull-up resistor from SDA to BYP1 to ensure correct operation of auto-sleep and memory BIST.

SDI/ICMP (Pin 27): Serial Data Input in SPI mode or Isolated Interface Comparator Voltage Threshold in isoSPI mode. Tie ICMP to the resistor divider between IBIAS and DGND to set the voltage threshold of the isoSPI receiver comparators. The comparator thresholds are set to 1/2 the voltage on the ICMP pin.

SDO/I_{BIAS} (Pin 28): Open Drain Serial Data Output in SPI mode or Isolated Interface Current Bias in isoSPI mode. In SPI mode tie with a pullup resistor to IOVCC. In isoSPI mode tie IBIAS to DGND through a resistor divider to set the interface output current level. When the isoSPI interface is enabled, the IBIAS pin voltage is regulated to 2V. The IP/IM output current drive is set to 20 times the current IB, sourced from the IBIAS pin.

V1, V2, V3, V4, V5, V6, V7 (Pins 1, 2, 3, 4, 5, 7, 8): Voltage Measurement Inputs. Pins are internally buffered before being applied to the AUXADC for ensuring high input impedance (50MΩ) and low leakage. Can be left floating if unused.

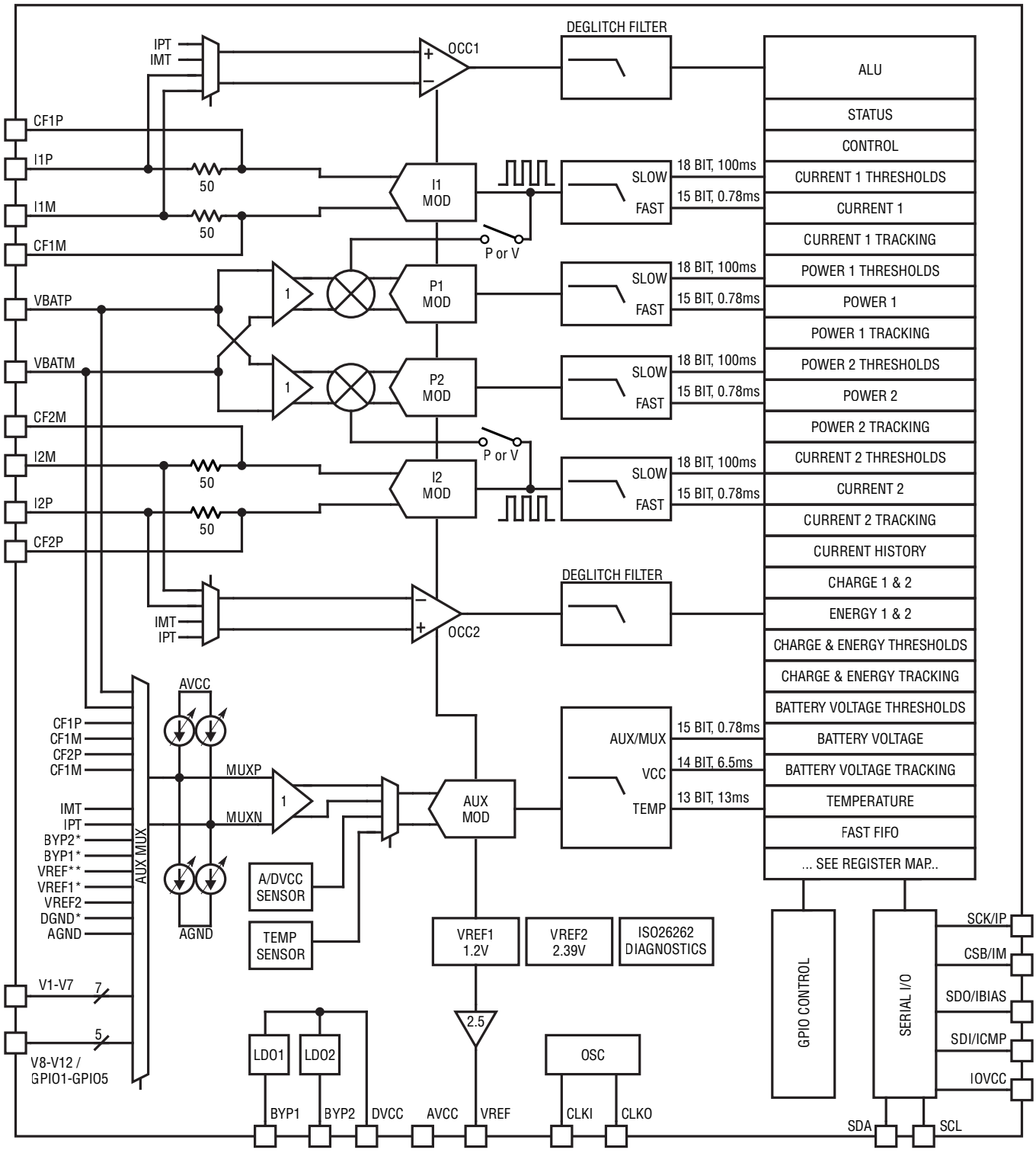
V8-V12/GPIO1-GPIO5 (Pins 9, 10, 11, 12, 13): General Purpose Voltage In– and Digital Outputs. Pins are internally buffered before being applied to the AUXADC for ensuring high input impedance (50MΩ) and low leakage (<10nA). Each pin can be switched to DVCC, switched to DGND or to toggle at 400kHz (typ.) between DVCC and DGND. Pins are tri-state in sleep mode. Can be left floating if unused.

VBATP, VBATM (Pins 48, 47): Battery Voltage Measurement. The differential voltage between VBATP and VBATM is internally buffered for ensuring high input impedance (50MΩ) and low leakage (<10nA).

VREF (Pin 35): Reference Voltage Output. VREF provides a buffered 3V reference voltage for temperature measurements with NTCs. Current load is limited to 0.5mA. Bypass this pin to AGND with a 1µF capacitor.

EXPOSED PAD (Pin 49): Connect to AGND.

BLOCK DIAGRAM



* Measured value not accessible by user. Only used for internal diagnostics.
** VREF measurement value is only accessible by user from the AUX slow channel.
See also section 'Unused Input Pins V1-V12' for recommendation to allow VREF measurement from AUX fast channel.

See also 'Table 57. MUX Settings' for more details on AUX MUX configuration.

OPERATION

OVERVIEW

The LTC2949 is a high precision current, voltage, charge and energy meter for electrical and hybrid vehicles or other applications requiring isolated data acquisition. Operating from supply voltages from 4.5 to 14V, it infers charge and energy flowing in and out of the battery pack by monitoring simultaneously the current through up to two sense resistors and the battery pack voltage. Five rail-to-rail low-offset ΔΣ ADCs ensure accurate measurement of currents, voltage and power with insignificant power loss. The LTC2949 uses instantaneous multiplication of voltage and current at a high sampling rate to infer accurately power even in presence of fast load variations. Additionally to the inputs for measuring currents and battery voltage, the LTC2949 features 12 analog input pins (V1 to V12) for measuring external voltages. Using its built-in multiplexer, the LTC2949 performs differential high input impedance rail-to-rail voltage measurements between any pair of input pins. Pins V8 to V12 can be configured as high voltage digital outputs, swinging from ground to digital supply voltage (DVCC) for controlling external components such as high voltage transistors. One automatic measurement cycle of current, voltage, power, temperature, supply voltage and two programmable multiplexer settings takes 100ms in slow mode. The LTC2949 repeatedly performs such measurements and recalculates energy, charge, time and updates the minimum/maximum tracking and threshold registers, resulting in continuous integration of current and power with lossless tracking of charge and energy delivered or received by the battery pack. An on-chip oscillator provides a 1% precise time base for calculating total charge, energy and time. If higher accuracy is required, a 4MHz crystal connected between pin CLKI and CLKO or an external clock can be used.

For time critical applications, a fast mode is available which reduces conversion times to 782µs. Data acquired during fast operation is stored in four FIFOs which contain each up to 1000 fast ADC readings from 4 synchronously measured parameters. Reading data from the FIFO yields simultaneously converted conversion results, enabling battery impedance tracking, current profiling or monitoring of other fast events, such as the pre-charging voltage before closing contactors. Thresholds can be set for parameters measured in slow mode, and the LTC2949 will set the corresponding bit in the Alert Register if a threshold is exceeded. Programmable heartbeat functions on up to two GPIOs allow to signal any enabled alert over an isolation barrier, independent of the serial interface. Those pins toggle at 400kHz and stop toggling in case of an alert.

The LTC2949 features a programmable analog overcurrent comparator for each current channel for applications which require fast detection of overcurrent conditions. A programmable deglitch filter allows to discard overcurrent conditions shorter than a predefined time duration*.

A 3V reference voltage output (VREF) is provided for connecting external NTCs or voltage dividers allowing to measure signals below ground. In slow mode, the LTC2949 provides means for linearizing temperature readings of up to two external NTCs by solving Steinhart-Hart equations with programmable coefficients. The LTC2949 can be configured to automatically compensate user-programmed temperature coefficients of low-cost shunt resistors by using linearized NTC temperature readings.

The LTC2949 features programmable gain correction factors to compensate for tolerances of external shunt resistors and resistor dividers. A master I^2C interface and dedicated commands allow to read from and write to an external EEPROM which can be used for storing calibration factors and the entire register content of the LTC2949 to guarantee data retention without supply. Storing correction factors in an EEPROM enables a modular approach to factory-calibration of application boards.

A thermal shutdown circuit trips at die temperatures above 150°C and resets the IC to default state, only the thermal shutdown bit itself is not reset.

Measured quantities are stored in internal registers accessible via the onboard SPI or LTC-proprietary isoSPI interface which allows fully isolated operation of the LTC2949. The LTC2949 was developed for compatibility with Linear's Multicell Battery Monitors (LTC68XX). Various bus structures in either SPI or isoSPI, multi-drop and/or daisy chaining are possible. The LTC2949 supports a limited set of Linear's Battery Cell Monitor compatible commands for triggering synchronous ADC conversions and reading back data.

*An overcurrent condition is signaled by a dedicated heartbeat pin for fastest response times.

OPERATION

Digital data acquired in isolated operation is transferred over external capacitors or transformers across an isolation barrier. Bridging potential differences of several kV is achieved by choosing appropriate external components.

All those features enable a wide variety of applications beyond current and charge measurement, like measuring isolation resistance, controlling pre-charge switches, signaling alarm conditions, monitoring state of contactors, etc. The LTC2949 offers various diagnosis functions to support functional safety critical systems, see the Safety Manual for more information.

MODES OF OPERATION

Core State Description

When all power supply voltages have risen above their UVLO thresholds, the LTC2949 boots up, sets all registers to their default state and enters after 1s its default SLEEP state with a current consumption of 9µA (typ), preventing rapid discharge after insertion when being supplied by a battery.

In SLEEP state, all GPIOs are tri-state and the LTC2949 monitors the serial interface and initiates the boot sequence on a falling edge of CSB in SPI mode. In isoSPI mode the isoSPI interface must first be woken up by a wake-up pulse before a pulse generating a negative edge on the internal CSB can be sent. During the boot sequence, the host can poll the SLEEP bit in the Operation Control Register to check that the LTC2949 is awake and in STANDBY mode (see also Figure 20 about Wake-Up and Boot procedure). LTC2949 enters STANDBY state maximum 100ms (t_{BOOT}) after the first falling edge of CSB. In STANDBY state all reference voltages are powered up and a clock is provided to digital circuits. The LTC2949 automatically returns to SLEEP state if no wake up confirmation command is received within 1 second (t_{ACKN}) after entering STANDBY state. Wake up is confirmed by writing 0x00 to register WKUPACK.

The LTC2949 enters SLEEP state ~200ms (t_{SLEEP}) after receiving a sleep command. A negative edge on CSB during

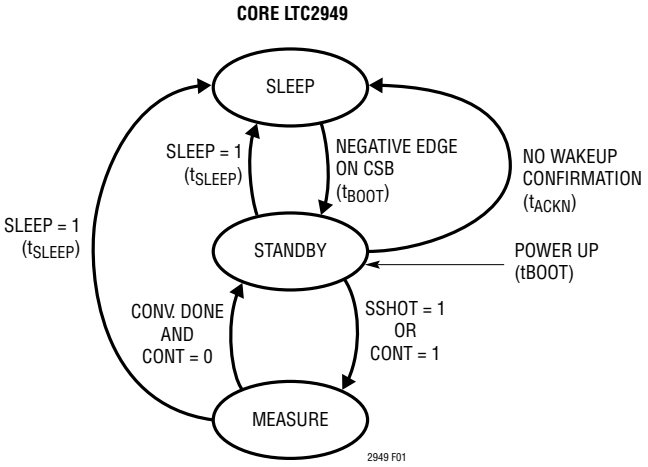


Figure 1. LTC2949 Operation State Diagram

t_{SLEEP} will prevent the LTC2949 from entering SLEEP state. In SLEEP, internal analog supplies and BYP1 are switched off, causing the UVLOA and UVLOD bits to be set when the LTC2949 resumes from SLEEP. An internal always-on regulated voltage supplies the memory and guarantees data retention during SLEEP. If AVCC or DVCC drop below the UVLO threshold, the UVLO bit of the internal always-on supply UVLOSTBY is set and a power-on-reset occurs, resetting all registers to their default value. In STANDBY state, all internal circuitry is active but no measurements except the reference voltage (VREF) are being made. From STANDBY, the LTC2949 can be instructed to go into MEASURE state by setting the single shot (SSHOT) or continuous (CONT) bit in the Operations Control Register OPCTRL.

isoSPI State Description

If the IOVCC pin is tied to a supply voltage ≥1.8V, the LTC2949 operates in normal SPI mode and IOVCC supplies the receiving circuit and output driving circuit for all SPI signals.

Tying IOVCC to DGND enables the isoSPI port. The isoSPI port has three different states: IDLE, READY and ACTIVE. In IDLE state, the isoSPI port is powered down. Only

OPERATION

differential activity on IP-IM generates a wake-up signal and the isoSPI port will enter READY state after t_{READY} (10µs) and be ready to send or receive data. The current consumption increases by several mA in READY. When communication takes place the isoSPI port is in ACTIVE state and supply current rises further depending on clock frequency. In order to save power the isoSPI port enters IDLE state when there has been no differential activity on IP-IM for more than t_{IDLE} (6.4ms typ.). Communication to the LTC2949 core is only possible if the isoSPI port is not in IDLE state. This means that even when the LTC2949 core is in STANDBY or MEASURE state and the isoSPI port is in IDLE state, communication can only take place 10µs (t_{READY}) after differential activity on IP-IM.

Figure 2 displays the sequence of states which the isoSPI interface and the LTC2949 core go through from waking up the interface until effectuating ADC measurements. See also Figure 20 for recommended wake-up sequence implementations.

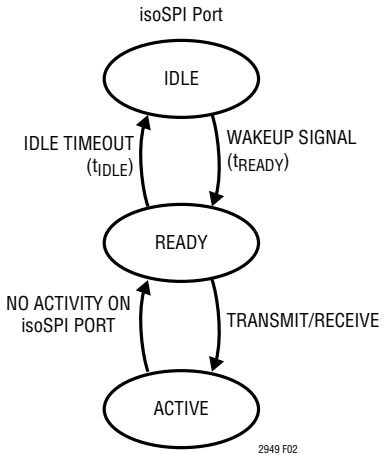


Figure 2. isoSPI State Diagram

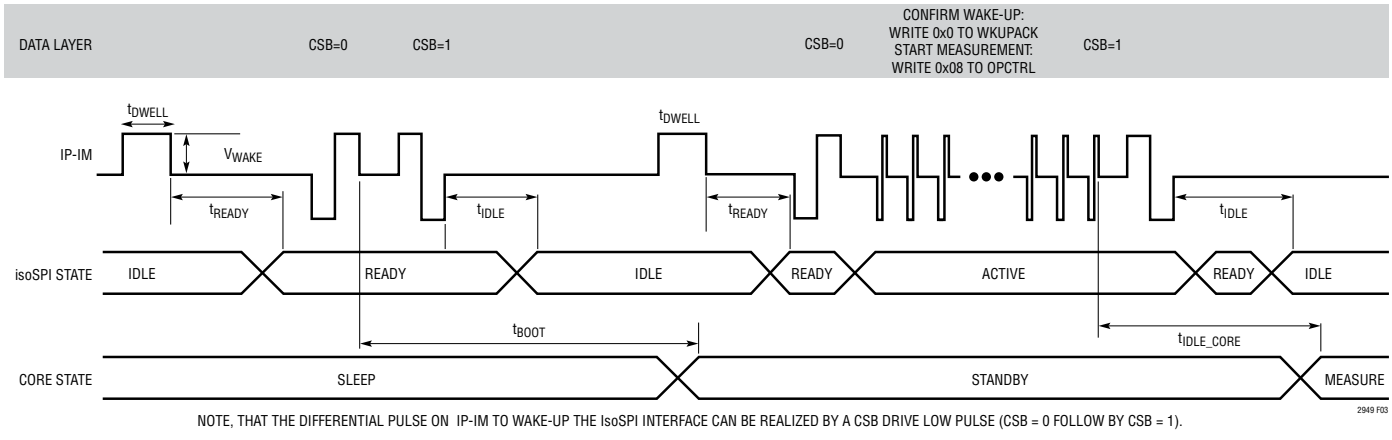
DATA ACQUISITION CHANNELS

The LT2949 has two current ADCs (I1ADC, I2ADC), two power ADCs (P1ADC, P2ADC) and one Auxiliary ADC (AUXADC). I1ADC and P1ADC are grouped together and form data acquisition channel 1 (CH1), I2ADC and P2ADC form channel 2 (CH2) and the AUXADC together with auxiliary multiplexer (AUXMUX), die-temperature sensor and supply voltage sensor form channel AUX (CHAUX).

CH1 and CH2 can be individually set to an 18-bit high precision mode (slow mode, default) or a 15-bit fast mode. Activating fast mode reduces conversion times from 100ms to 782µs on the selected channel. The power ADCs can be individually configured as voltage ADCs by disabling the power multiplication after the input buffers by setting the corresponding Power as Voltage (PasV) bit in ADC Configuration Register (ADCCONF).

Slow, High Precision Mode

By default, LTC2949's acquisition channels are in slow high precision mode where conversions of CH1 or CH2 take 100ms and yield 18-bit conversion results of current and power or current and voltage, if PasV set. During these 100ms the auxiliary channel (CHAUX) measures



NOTE, THAT THE DIFFERENTIAL PULSE ON IP-IM TO WAKE-UP THE IsoSPI INTERFACE CAN BE REALIZED BY A CSB DRIVE LOW PULSE (CSB = 0 FOLLOW BY CSB = 1).

Figure 3. Timing of IsoSPI and Core States

OPERATION

sequentially six different quantities using its Round Robin (RR) mode starting with VBATP – VBATM (BAT) then die-temperature (TEMP), AVCC supply voltage (VCC), two AUXMUX inputs (SLOT1 and SLOT2), selectable by the Multiplexer Setting Registers and finally the Reference Voltage (VREF). Furthermore, a moving average of the last four measurements of IADC1 and IADC2 in slow mode is provided, yielding a 20-bit result. In slow, high precision mode a single conversion or continuous conversions can be triggered. The continuous slow mode (CONT) is the most typical operation and also the prerequisite to make fast conversions.

Single Shot Measurement Mode (SSHOT)

When bit SSHOT in the Operation Control Register is set, the LTC2949 takes measurements of CH1 and CH2 as well as the six auxiliary channel measurements described above, updates the corresponding minimum, maximum and threshold registers, resets bit SSHOT, sets the bit UPDATE in Status Register and returns to the STANDBY state. No time measurements are made and the charge and energy registers are not updated and therefore not compared against minimum/maximum thresholds. The host can poll the UPDATE bit in the STATUS Register to detect the completion of the measurement cycle. A measurement starts within 20ms (t_{IDLE_CORE}) after setting bit SSHOT.

Continuous Measurement Mode (CONT)

When the bit CONT in the Operation Control is set, the LTC2949 repeatedly takes measurements of CH1 and CH2 as well as the six auxiliary channel measurements, recalculates energy, charge, time and updates the minimum/maximum tracking and status registers every 100ms. The start of continuous high precision measurements can take up to 20ms (t_{IDLE_CORE}) after setting bit CONT. The current and power ADCs run continuously in this mode, ensuring that no charge or energy is missed. If a power ADC is configured to measure voltage (PasV), the energy of the corresponding channel is not accumulated. The LTC2949 remains in continuous mode until bit CONT of the Operation Control Register is reset by the user. If the SSHOT bit is set while in continuous mode, the LTC2949 completes the current measurement cycle and then enters single shot mode, clearing the CONT bit in the Operation Control Register.

In continuous measurement mode, the host can poll for the end of a measurement cycle by periodically checking the corresponding time registers (TB1, TB2, TB3 or TB4) for incrementation.

Accessing High Precision Results

At the end of each measurement cycle of 100ms, all result register for the measured quantities are updated; in continuous mode, accumulated quantities are updated also. Furthermore, the four preceding measurements of each current channel are stored in Current History Registers and their average in Current Average Registers, see the Register Map section for more details. The completion of register updates of the measurement results can be detected by reading one of the time registers (TB1-TB4) and looking for a changed value.

Fast Mode

The LTC2949 provides a fast mode with a reduced conversion time of 782µs and a resolution of 15-bit. Fast mode allows to start measurements at a precise point in time and thereby perform measurements synchronized with the voltage measurements of LTC's Battery Stack Monitors, for example to deduce cell impedance of individual cells.

Fast Mode Configurations

The LTC2949 allows to set data acquisition channel 2 in fast mode while data acquisition channel 1 stays in slow high precision mode or to set both data acquisition channels 1 and 2 in fast mode by setting the corresponding bit FACH1 or FACH2 in the Fast Control Register (FACTRL). The auxiliary channel can be set to fast mode independently of CH1 and CH2, converting only a single quantity (selected by the Fast MUX Control Registers) instead of Round-Robin (RR).

To enable short startup delays, the LTC2949 must be in continuous mode (CONT=1) before triggering fast conversions. Fast measurements are triggered either by an ADCV command (fast single shot) or by setting bit FACONV in the Fast Control Register (FACTRL). The ADCV command triggers a single fast conversion of the selected channels right after the correct PEC is received, synchronous to

OPERATION

LTC's Battery Stack Monitors. If fast measurements are triggered by setting FACONV=1, LTC2949 executes a sequence of fast conversions until FACONV or CONT is reset. Samples acquired during fast continuous mode are stored in individual FIFOs for up to four fast input channels (I1, I2, BAT via P1 or P2 and AUX).

CH1 and CH2 automatically restart in slow high precision mode after completion of joint fast mode conversions. If CH2 was in fast mode while CH1 continued in slow high precision mode, CH2 will stop converting after completion of fast mode acquisitions ready to perform further fast mode conversions when requested either by an ADCV command or by setting FACONV again. The auxiliary channel slow mode Round-Robin (BAT, TEMP, VCC, SLOT1, SLOT2, VREF) is automatically restarted after all fast measurements were stopped for 300 ms. In applications were continuous high AUX measurement rates (faster than every 100ms) are required, it is recommended to measure also VREF and optionally VCC via external connections to V1-V12 and implement a manual Round-Robin by fast single shot measurements in software.

Accessing Fast Mode Results

The last results of fast conversions can be read out by the RDCV command providing sequentially the results of I1, I2, BAT via P1 or P2 and AUX followed by an indicator if the data is new (0xF) or old (0x0). BAT is the result of the power ADC, if the ADC is set in voltage mode (bit PasV=1), otherwise, the power ADC result is 0. If both channels are in fast mode with their power ADCs in voltage mode, BAT is obtained from PADC1. Please note that to be compliant with LTCs Battery Stack Monitors, RDCV reports LSByte first.

Furthermore, the last 1000 fast conversion results of I1, I2, BAT via P1 or P2 and AUX are stored in First-In-First-Out Registers accessible by FIFOI1, FIFOI2, FIFOBAT and FIFOAUX. Reading continuously from FIFOI1 provides successively 3 bytes for each sample of the first current ADC: I1 MSB, I1 LSB and a qualifier (TAG) whether the corresponding FIFO data is fine (0x00), has been already read because no new data has been added to the FIFO since the whole FIFO was read (0x55, default), or has been overwritten because the FIFO was filled without being read (0xAA). The other FIFOs present the respective quantities accordingly. All tags are initialized to their default value (0x55), if fast conversions are triggered by an ADCV command (while FACONV = 0) or by setting FACONV. Also leaving the continuous mode by resetting CONT will clear the FIFOs.

The LSB sizes of the fast conversion results are the same for the RDCV and FIFO readings and are listed in Table 28.

When CH1 and CH2 are both in fast mode, 128 conversion results of IADC1 and IADC2 are averaged and stored in their respective non-accumulated results registers Current1 and Current2 and are added to the Charge1 and Charge2 registers ensuring that battery charge and discharge is monitored also in fast mode.

Similarly 128 conversion results of PADC1 and PADC2 with 11 bit resolution are averaged and stored in their respective non-accumulated results registers Power1 at and Power2 and are added to the Energy1 and Energy2 registers if the PADCs are in Power Mode (PasV=0). If CH1 is in slow mode and CH2 in fast mode, only CH1 results are reported in the Current and Power results registers, CH2 results can be accessed via RDCV or the respective FIFOs.

Recommended Configurations of Data Acquisition Channels

In a typical application case, both data acquisition channels offered by LTC2949 could monitor the current over a single shunt resistor, where CH1 is used to do high precision current and power measurements and charge and energy integration, while channel two takes fast snapshots of current and voltage for example for impedance measurement.

Alternatively, the two data acquisition channels offered by LTC2949 might be used to monitor currents over two different shunt resistors. In this application case, both channels might be used in either fast or slow mode. CHAUX can be configured fully independently from CH1 and CH2. The default mode of AUXADC is RR, which is deactivated by enabling fast mode on CHAUX.

OPERATION

Table 1. Acquisition Channels Configurations

	SINGLE SHUNT	DUAL SHUNT	
CH1	Slow	Slow	Fast
CH2	Fast	Slow	Fast
CHAUX	RR/Fast	RR/Fast	RR/Fast

Single Shunt Configuration

If only one external shunt is used, CH1 can be used to perform continuous high precision integrated charge and energy measurements, while CH2 is used to perform fast measurements synchronized with LTC's Battery Stack Monitors. By setting bit CONT in the Operation Control Register (OPCTRL) and bit FACH2 in the Fast Control Register (FACTRL), CH1 will effectuate consecutive slow measurements, while CH2 is available for fast measurements triggered by an ADCV command. Measurements of CH1 and its integrated quantities are updated every 100ms while CH2 results can be read out with an RDCV command or obtained from the FIFO registers, in case of fast continuous (FACONV) operation.

Dual Shunt High Precision Configuration

For dual shunt applications that require continuous uninterrupted high precision coulomb counting and energy measurement CH1 and CH2 should be both configured to slow high precision mode by setting bit CONT in OPCTRL. Conversions on CH1 and CH2 take 100ms and a new RR cycle of CHAUX is started at every start of conversion of CH1.

If fast voltage data is required, the AUXADC can be configured for fast mode without interrupting charge and energy accumulation on CH1 and CH2. After setting bits FACONV and FACHA the AUXADC immediately stops RR mode and continuously measures a single quantity selected by the Fast MUX Control Registers. Data is written to the FIFOAUX. After clearing bit FACHA the AUXADC automatically returns to RR operation (after 300ms). Measurements of VREF, internal die temperature and VCC are only available if RR is enabled. Alternatively, external connections to V1-V12 can be applied to measure VREF and VCC (via an external resistive divider) also in fast mode.

Dual Shunt Fast Measurement Configuration

CH1 and CH2 are both set to fast mode by setting bits FACONV, FACH1 and FACH2. Charge is accumulated by summing up 15-bit current results, energy by summing up 11 bit power results.

One conversion takes 782µs and a new RR cycle is started after every 100ms. This configuration fits to an application where two shunt resistors are used and fast current, voltage and power is required. E.g.: Fast impedance tracking or measuring pre-charge voltage and current.

POWER MEASUREMENT

The LTC2949 measures power with additional ADCs that multiply voltage (VBATP – VBATM) and current at the full 5.24MHz sampling frequency, prior to any averaging due to the analog-to-digital conversion. This maintains accuracy even if current and voltage change in phase during the 100ms conversion time, which can happen if the power is drawn from a battery with significant impedance. Figure 4 shows an example of the BAT voltage dropping from 4V to 3V due to battery impedance when an AC current is drawn by the load. In this example, the multiplication of average current with average voltage would lead to a +8% error in the calculated power as the voltage is significantly lower than the average voltage at the moments where the peak current is drawn. The scheme used by the LTC2949 avoids this error, maintaining specified accuracy with signals up to 50kHz.

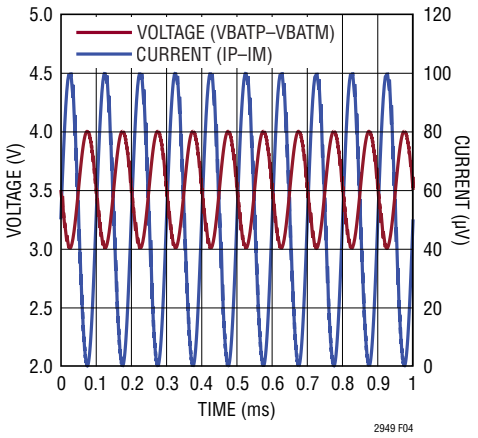


Figure 4. Power Measurement of Transient Signals

OPERATION

CHARGE, ENERGY AND TIME

The LTC2949 integrates the current and power measurements over time to calculate charge and energy flowing to the load. It also keeps track of total accumulated time used for the integration.

For the quantities charge and energy the LTC2949 provides three sets of registers each, for the quantity "time" four register sets.

Charge1, Energy1 and Time1 contain accumulated quantities of Channel1. Charge2, Energy2 and Time2 contain accumulated quantities of Channel2. Charge3 and Time3 contain the sum of charges monitored by Channel1 and Channel2 and the corresponding time. Similarly Energy4 and Time4 contain the sum of energies monitored by Channel1 and Channel2 and the corresponding time. See the Accumulated Result Registers section in the Register Map description for more details.

Each register set can be separately configured to accumulate current and power based on the sign of the measured current. A minimum current threshold can also be set below which integration is stopped. See the Control Registers section in the Register Map description for more details.

Time Base

Accurately measuring charge and energy by integrating current and power requires a precise integration period. The LTC2949 uses either a trimmed internal oscillator or an external clock as the time base for determining the integration period. It can use either an external square wave clock in a frequency range between 100kHz and 25MHz or a 4MHz crystal as external clock input. If an external square wave is used, it should be connected to the CLKI pin and the CLKO pin should be left unconnected.

Figure 5 shows the recommended circuit if a crystal is used to generate the reference clock. In case the internal clock is used, tie CLKI to ground and leave CLKO unconnected.

Timebase Control

The LTC2949 uses the internal oscillator by default. If an external clock or a crystal is used, the PRE and DIV parameters in the Timebase Control Register need to be set appropriately. The LTC2949 then compares its internal clock to the external frequency and represents Time, Charge, and Energy as multiples of the external clock period. To accommodate the large range of allowed external frequencies, an internal prescaler must be configured via the Timebase Control Register.

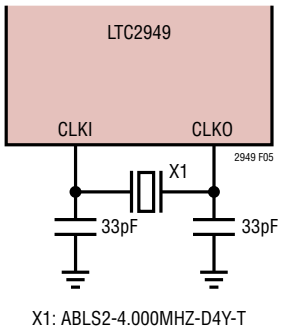


Figure 5. Reference Clock with a 4MHz Crystal

The prescaler consists of 2 stages, with the first dividing the external frequency f_{REF} by a factor 2^{PRE}, and the second by a factor DIV. PRE is set between 0 and 5 with bits [2:0] of the Timebase Control Register. PRE should be configured such that the external frequency divided by 2^{PRE} is less than 1MHz as shown in Table 2:

Table 2. Parameter PRE with External Clock

f_{REF}	PRE	2^{PRE}	PRE[2:0]
$0.1MHz \le f_{REF} \le 1MHz$	0	1	000
$1MHz \le f_{REF} \le 2MHz$	1	2	001
$2MHz \le f_{REF} \le 4MHz$	2	4	010
$4MHz \le f_{REF} \le 8MHz$	3	8	011
$8MHz \le f_{REF} \le 16MHz$	4	16	100
$16MHz \le f_{REF} \le 25MHz$	5	32	101
Internal	7		111

The second stage of the prescaler then divides the result by a factor DIV. DIV is set between 0 and 31 by bits [7:3] of the Time Base Control Register. DIV should be set to the next lower integer value of the ratio between the output of the first stage of the prescaler ($f_{REF\_}1 = f_{REF}/2^{PRE}$) and 32768Hz or, in other terms:

$$DIV = \text{floor}\left(\frac{f_{REF}}{2^{PRE} \bullet 32768Hz}\right)$$

If a crystal is used, the values are: PRE = 2, DIV = 30. The Quick Eval™ Software for the LTC2949 contains an easy to use calculator for these parameters. Table 3 gives a few examples for common frequencies.

Rev A

OPERATION

Table 3. Timebase Settings for Common Frequencies

f_{REF} [MHz]	PRE	2^{PRE}	$f_{REF\_}1$[MHz]	DIV	TIME BASE CONTROL [7:0]
1	0	1	1	30	1111 0000
1.5	1	2	0.75	22	1011 0001
4	2	4	1	30	1111 0010
10	4	16	0.625	19	1001 1100
20	5	32	0.625	19	1001 1101
25	5	32	0.781	23	1011 1101
Int.	7			X	XXXX X111

OVERCURRENT COMPARATORS

The LTC2949 features two fast differential over-current comparators with rail to rail input common mode and programmable threshold followed by configurable filters to suppress input glitches. Overcurrent comparator 1 (OCC1) is connected to pins I1P and I1M while overcurrent comparator 2 (OCC2) supervises the differential voltage between I2P and I2M. Both overcurrent comparators can individually be configured to detect either only positive or only negative overcurrents or overcurrents independent of their polarity. When at least one of the overcurrent comparators is enabled, GPIO5 turns into a heartbeat signal toggling at 400kHz while currents are within the desired range and staying low if any current exceeds its programmed limit.

The overcurrent comparator 1 (OCC1) between I1P and I1M is controlled by the control register OCC1CTRL while overcurrent comparator 2 (OCC2) is controlled by its control register at OCC2CTRL, both on page 0 of the register map. Both OCC Control Registers are organized as shown in Table 4.

Table 4. Overcurrent Comparator Control Registers

BIT #	NAME	FUNCTION
0	OCCxEN	Enable OCC
1	OCCxDAC0	Threshold DAC[0]
2	OCCxDAC1	Threshold DAC[1]
3	OCCxDAC2	Threshold DAC[2]
4	OCCxDGLT0	Deglitch [0]
5	OCCxDGLT1	Deglitch [1]
6	OCCxPOL0	Polarity [0]
7	OCCxPOL1	Polarity [1]

The overcurrent comparators are enabled by setting the respective OCCxEN to 1.

Bits OCCxPOLx control the polarity sensitivity of the comparator as in Table 5.

Table 5. OCC Polarity Configuration

OCCxPOL1	OCCxPOL0	POLARITY
0	0	Both Polarities
0	1	Positive Currents
1	0	Negative Currents

The thresholds of the overcurrent comparators can be programmed individually by means of the OCCxDACx bits between 0 and 310mV.

Table 6. OCC Thresholds

OCCxDAC2	OCCxDAC1	OCCxDAC0	Threshold [mV]
0	0	0	0
0	0	1	26
0	1	0	52
0	1	1	78
1	0	0	103
1	0	1	155
1	1	0	207
1	1	1	310

Similarly, the duration of a threshold exceeding not reported by the comparator (Deglitch Time) can be programmed by the bits OCCxDGLTx between 20µs to 1.28ms.

Table 7. OCC Deglitch Time

OCCxDGLT1	OCCxDGLT0	DEGLITCH TIME [µs]
0	0	20
0	1	80
1	0	320
1	1	1280

Overcurrents are reported by setting OCC1 and OCC2 of VCC and OCC Status Register (STATVCC) and by stopping the heartbeat signal on GPIO5. While the update of the output register can take up to 100ms, the heartbeat is stopped within 15µs after an overcurrent exceeded the programmed deglitch time. Once an overcurrent occurred, the result bits in the register remain set until they are read by the host and subsequently cleared.

For diagnostic purposes, the overcurrent comparators have a self-test built in using test input signals IPT and IMT, see the Safety Manual for more information.

SERIAL INTERFACES

SERIAL INTERFACES OVERVIEW

LTC2949 has two serial interfaces, one for communication with the host and a second to address an external EEPROM. The interface for host communication is composed by pins 27 through 30 and can be configured to be either a standard 4-wire serial peripheral interface (SPI) or a 2-wire isolated interface (isoSPI) based on the voltage of the IOVCC pin. Regardless of which configuration is selected, the LTC2949 acts as an SPI slave. The LTC2949 can be operated in addressable mode (SPI & isoSPI) or as last element of a daisy chain of LTC68xx Cell Monitors (isoSPI only).

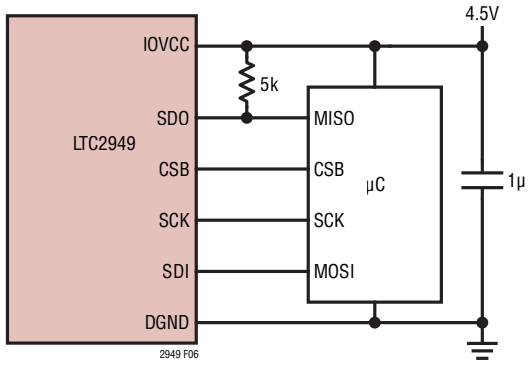


Figure 6. 4-Wire SPI External Connections

A second interface composed by pins 14 and 15 is a master I^2C interface, allowing to save and restore LTC2949's register content to and from an external EEPROM see the External EEPROM Control Register section for more information.

4-WIRE SERIAL PERIPHERAL INTERFACE (SPI) PHYSICAL LAYER

Connecting pin IOVCC to a supply voltage ≥1.8V configures the serial port for 4-wire SPI. Logic input thresholds and output swings are set by the voltage at the IOVCC pin, which should be connected to the same supply as the SPI master device. A 1µF bypass capacitor is recommended from IOVCC to DGND. The pin SDI is often referred to as MOSI, the pin SDO as MISO. The 4-wire serial port is configured to operate in a SPI system using CPHA = 1 and CPOL = 1. Consequently, data on SDI must be stable during the rising edge of SCK and data on SDO will be updated on the falling edge of SCK. The timing is depicted in Figure 7. The maximum data rate is 1Mbps. See Electrical Characteristics. SDO is open drain and requires a pull-up.

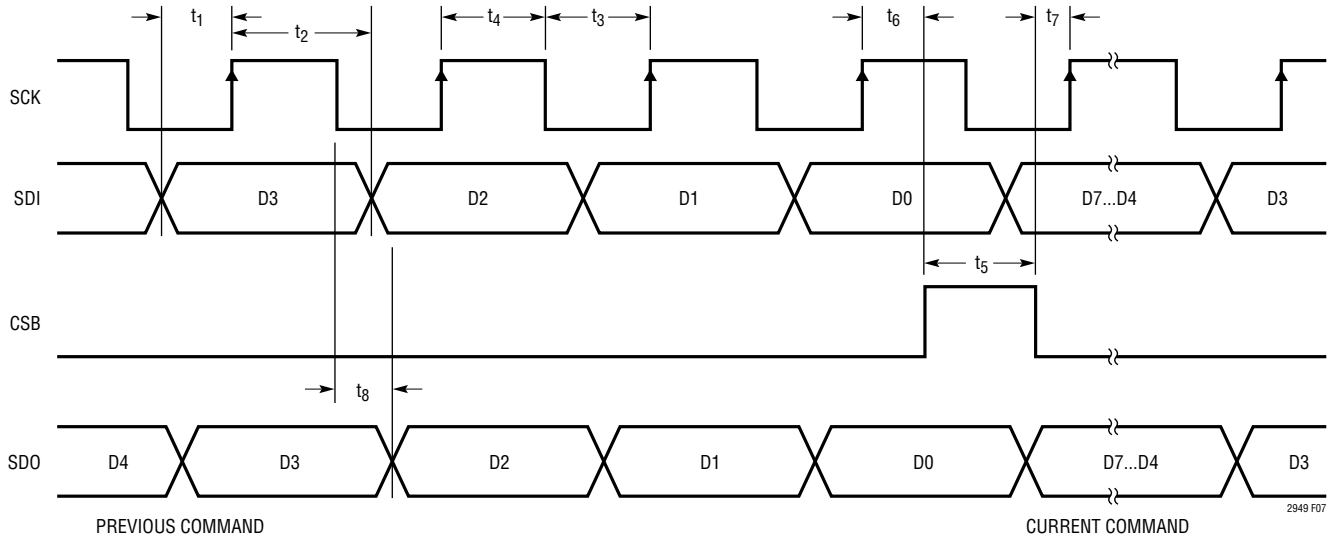


Figure 7. Timing Diagram of 4-Wire Serial Peripheral Interface

SERIAL INTERFACES

2-WIRE ISOLATED INTERFACE (ISOSPI) PHYSICAL LAYER

Tying IOVCC to local chip ground enables the isoSPI 2-wire interface which allows fully isolated operation of the LTC2949. The 2-wire interface provides means to communicate to LTC2949 using simple twisted pair cabling. An LTC6820 should be used for translating standard SPI signals from the SPI master into pulses that are sent over an isolation barrier to the LTC2949.

The interface is designed for low packet error rates when the cabling is subjected to high RF fields. Isolation is achieved through an external transformer. Capacitive coupling with 10nF capacitors could also be used, but has a very limited common mode noise rejection (only for low frequencies) and is only recommended for short single PCB interconnections with limited voltage transients at the isolation barrier. Additional clamping Schottky diodes might be necessary from IP and IM to VCC and GND. Standard SPI signals are encoded into differential pulses. The strength of the transmission pulse and the threshold level of the receiver are set by two external resistors. The values of the resistors allow the user to trade off power dissipation for noise immunity. Figure 9 illustrates how the isoSPI

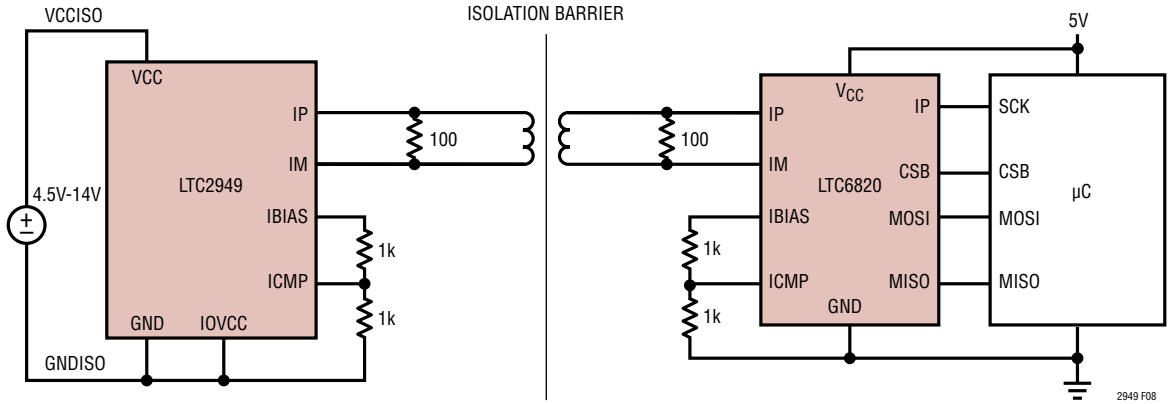


Figure 8. isoSPI Physical Layer

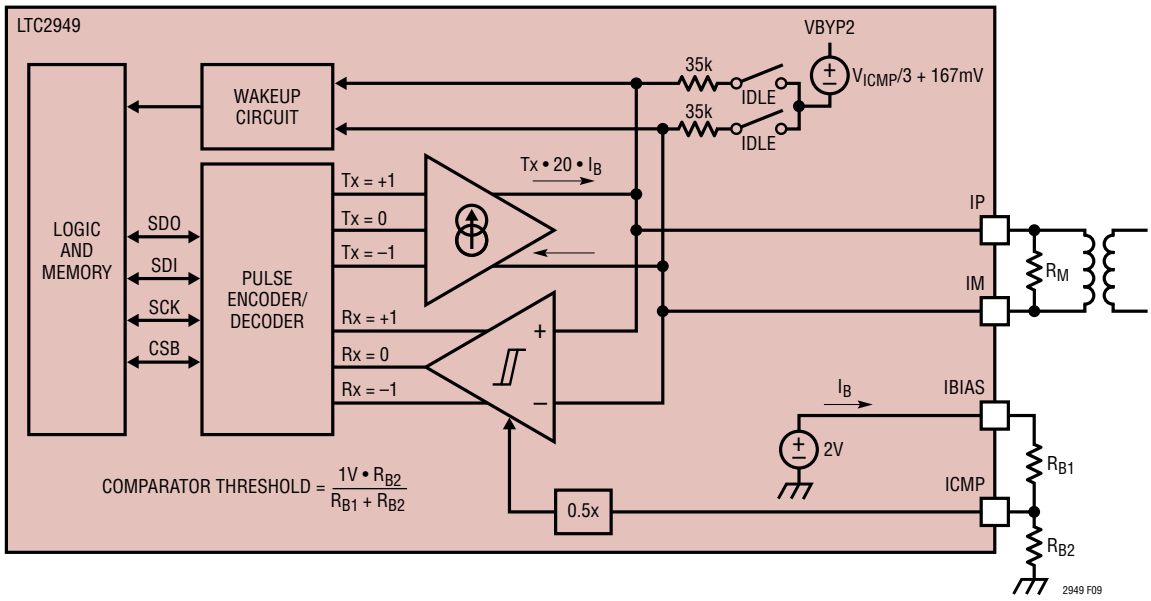


Figure 9. isoSPI Interface

SERIAL INTERFACES

circuit operates. A 2V reference drives the IBIAS pin. External resistors R_{B1} and R_{B2} create the reference current I_B. This current sets the drive strength of the transmitter. R_{B1} and R_{B2} also form a voltage divider of the 2V reference at the ICMP pin. This sets the threshold voltage of the receiver circuit.

Waking Up the isoSPI Port

The isoSPI port has 3 modes of operation, IDLE, READY and ACTIVE as described in the section isoSPI State Description. In IDLE, the WAKEUP circuit monitors activity on pins IP and IM. Differential activity on IP-IM wakes up the isoSPI interface. The isoSPI port will return to the low power IDLE state if there is no activity on IP/IM for a time of t_{IDLE}. The LTC2949 will be ready to communicate when the core is not in SLEEP and the isoSPI state changes to READY (within t_{READY} after wakeup) as illustrated in Figure 3. Common mode signals will not wake up the serial interface. The interface is designed to wake up after receiving a large signal single-ended pulse, or a low-amplitude symmetric pulse. The differential signal |IP – IM|, must be at least V_{WAKE} = 200mV for a minimum duration of t_{DWELL} = 240ns to qualify as a wake up signal that powers up the serial interface.

"Long -1" or "Long +1" pulses (= drive CSB low, high) generated by LTC6820 and compatible isoSPI devices (e.g. LTC68xx Cell Monitors) will always meet this requirement. See following chapters for isoSPI pulse details.

Selecting Bias Resistors

The adjustable signal amplitude allows the system to trade power consumption for communication robustness, and the adjustable comparator threshold allows the system to account for signal losses. The isoSPI transmitter drive current and comparator voltage threshold are set by a resistor divider ($R_{BIAS} = R_{B1} + R_{B2}$) between the IBIAS and DGND. The divided voltage (V_{ICMP}) is connected to the ICMP pin which sets the comparator threshold (V_{ICMP}) to 1/2 of this voltage. When the isoSPI interface is enabled (not IDLE) IBIAS is held at 2V, causing a current I_B to flow out of the IBIAS pin. The IP and IM pin drive currents are 20 • I_B.

As an example, if divider resistor R_{B1} is 2.8k and resistor R_{B2} is 1.21k (so that R_{BIAS} = 4k), then:

$$I_B = \frac{2V}{R_{B1}+R_{B2}} = 0.5mA$$

$$I_{DRV} = I_{IP} = I_{IM} = 20 \bullet I_B = 10mA$$

$$V_{ICMP} = 2V \bullet \frac{R_{B2}}{R_{B1}+R_{B2}} = I_B \bullet R_{B2} = 603mV$$

$$V_{TCMP} = 0.5 \bullet V_{ICMP} = 302mV$$

In this example, the pulse drive current IDRV will be 10mA, and the receiver comparators will detect pulses with IP-IM amplitudes greater than ±302mV. If the isolation barrier uses 1:1 transformers connected by a twisted pair and terminated with 100Ω resistors on each end, then the transmitted differential signal amplitude (±) will be:

$$V_A = I_{DRV} \bullet \frac{R_M}{2} = 0.5V$$

(This result ignores transformer and cable losses, which may reduce the amplitude).

isoSPI Pulse Detail

The transmitter can output three voltage levels: $+V_A$, 0V, and $–V_A$. A positive output results from IP sourcing current and IM sinking current across load resistor R_M. A negative voltage is developed by IP sinking and IM sourcing. When both outputs are off, the load resistance forces the differential output to 0V. To eliminate the DC signal component and enhance reliability, the isoSPI uses bipolar pulses of two different pulse length. This allows for four types of pulses to be transmitted, as shown in Table 8. A +1 pulse will be transmitted as a positive pulse followed by a negative pulse. A –1 pulse will be transmitted as a negative pulse followed by a positive pulse. The duration of each pulse is defined as $t_{1/2PW}$, since each is half of the required symmetric pair. (The total isoSPI pulse duration is 2 • $t_{1/2PW}$).

SERIAL INTERFACES

Table 8. isoSPI Pulse Types

PULSE TYPE	FIRST LEVEL ($t_{1/2PW}$)	SECOND LEVEL ($t_{1/2PW}$)	ENDING LEVEL
Long +1	$+V_A$ (150ns)	$-V_A$ (150ns)	0V
Long –1	$-V_A$ (150ns)	$+V_A$ (150ns)	0V
Short +1	$+V_A$ (50ns)	$-V_A$ (50ns)	0V
Short –1	$-V_A$ (50ns)	$+V_A$ (50ns)	0V

An LTC6820 should be used to translate the SPI signals of a micro controller into isoSPI pulses. On the other side of the isolation barrier (i.e. at the other end of the cable), the LTC2949 will have IOVCC tied to its local GND. It receives transmitted pulses and reconstructs the SPI signals internally, as shown in Table 9. In addition, during a READ command this port may transmit return data pulses which are transmitted t_{RTN} after the received pulse. The LTC2949 isoSPI port is a slave port and only transmits short –1 pulses, never long CSB pulses nor short +1 pulses. The master port recognizes a null response as a logic 1 (for this reason a no reply to a read command is equivalent to read only 0xFF.. on the MISO line, which will also cause a PEC error, see chapters DATA LINK LAYER and following). This allows for multiple slave devices on a single cable without risk of collisions (Multidrop). Figure 11 shows the isoSPI timing diagram for a READ command.

Table 9. LTC2949 isoSPI Port Function

RECEIVED PULSE	INTERNAL SPI PORT ACTION	RETURN PULSE
Long +1	Drive CSB High	None
Long –1	Drive CSB Low	
Short +1	1. Set SDI = 1 2. Pulse SCK	Short –1 Pulse if Reading a 0-bit
Short –1	1. Set SDI = 0 2. Pulse SCK	(No Return Pulse if Not in READ Mode or if Reading a 1-bit)

Supported Bus Structures

The addressing feature of the LTC2949 and LTC68xx-2 Cell Monitors allows multiple devices with different addresses to be connected on a single bus by multi-dropping them. Multi-dropping can be used in either SPI or isoSPI (See Figure 12 (A)). The LTC2949 also operates in parallel to or as last element of a daisy chain of LTC68xx Cell Monitors (See Figure 12 (B&C)).

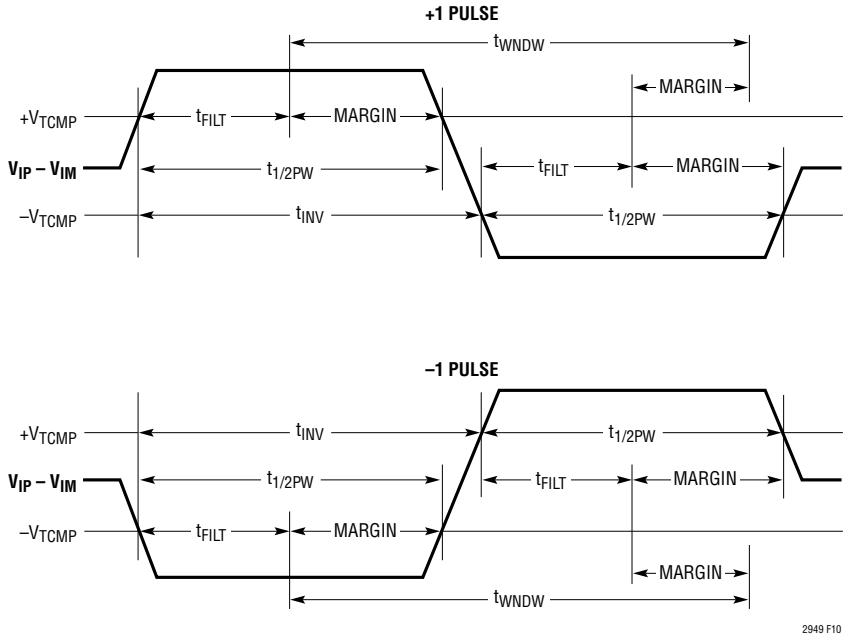


Figure 10. isoSPI Pulse Detail

SERIAL INTERFACES

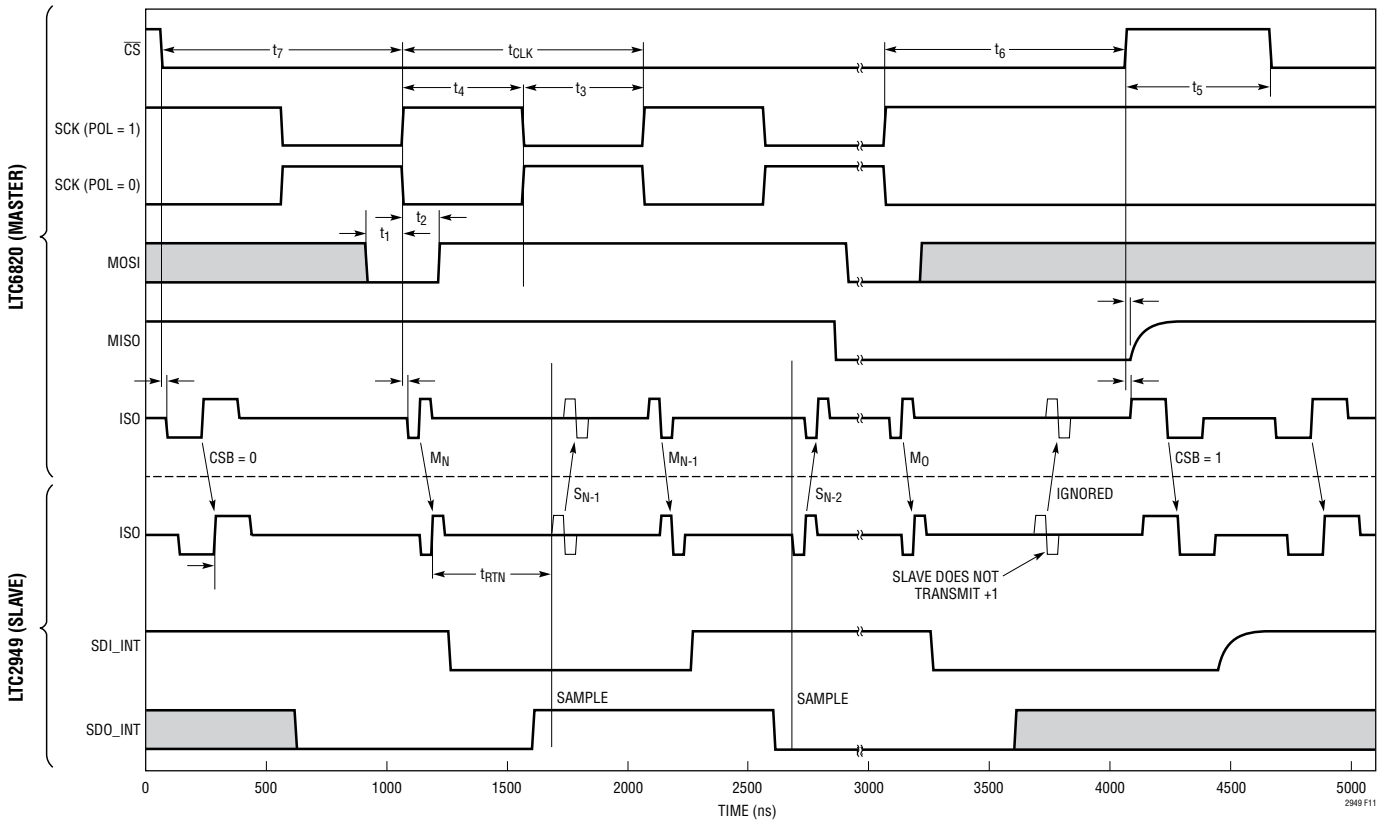


Figure 11. isoSPI Timing Diagram

LTC2949 in Addressable/Multidrop Bus Configuration

An LTC2949 can be directly connected to the master in SPI or through an LTC6820 in isoSPI mode. When operating together with LTC68xx Cell Monitors it is recommended to use the LTC2949 in a multidrop bus configuration to take advantage of the full feature set and minimize communication overhead. The LTC2949 can operate on the same SPI/isoSPI with other LTC68xx Cell Monitors (Figure 12 (A, B)). The LTC2949 responds to address 0xF. This address is hardwired and cannot be changed. Consequently, other LTC68xx Cell Monitors on the same bus must be pin-configured to different addresses. Simultaneous writing to all devices on one bus is done by issuing a broadcast command. This feature proves useful for synchronous ADC conversions of LTC2949 and LTC68xx Cell Monitors. The common SDO pin is open drain and requires a pull-up.

LTC2949 Connected to Reversible isoSPI Ring

LTC2949 can be connected to one end of a reversible isoSPI ring. In this scenario the default communication to LTC2949 is done with direct commands, equivalent to the scenario where LTC2949 is connected in parallel to a daisychain. In case the direct link between the left side LTC6820 and LTC2949 fails, the communication to LTC2949 can be routed through the daisychain via the right side LTC6820, equivalent to the scenario where LTC2949 is connected on top of a daisychain.

LTC2949 on Top of a Daisy Chain

It is recommended to operate LTC2949 in parallel to a daisy chain of LTC68xx Cell Monitors in either isoSPI or normal SPI by using its addressing feature. This is the mode with the minimum communication overhead. However, also operation as last element of a daisy chain is supported.

SERIAL INTERFACES

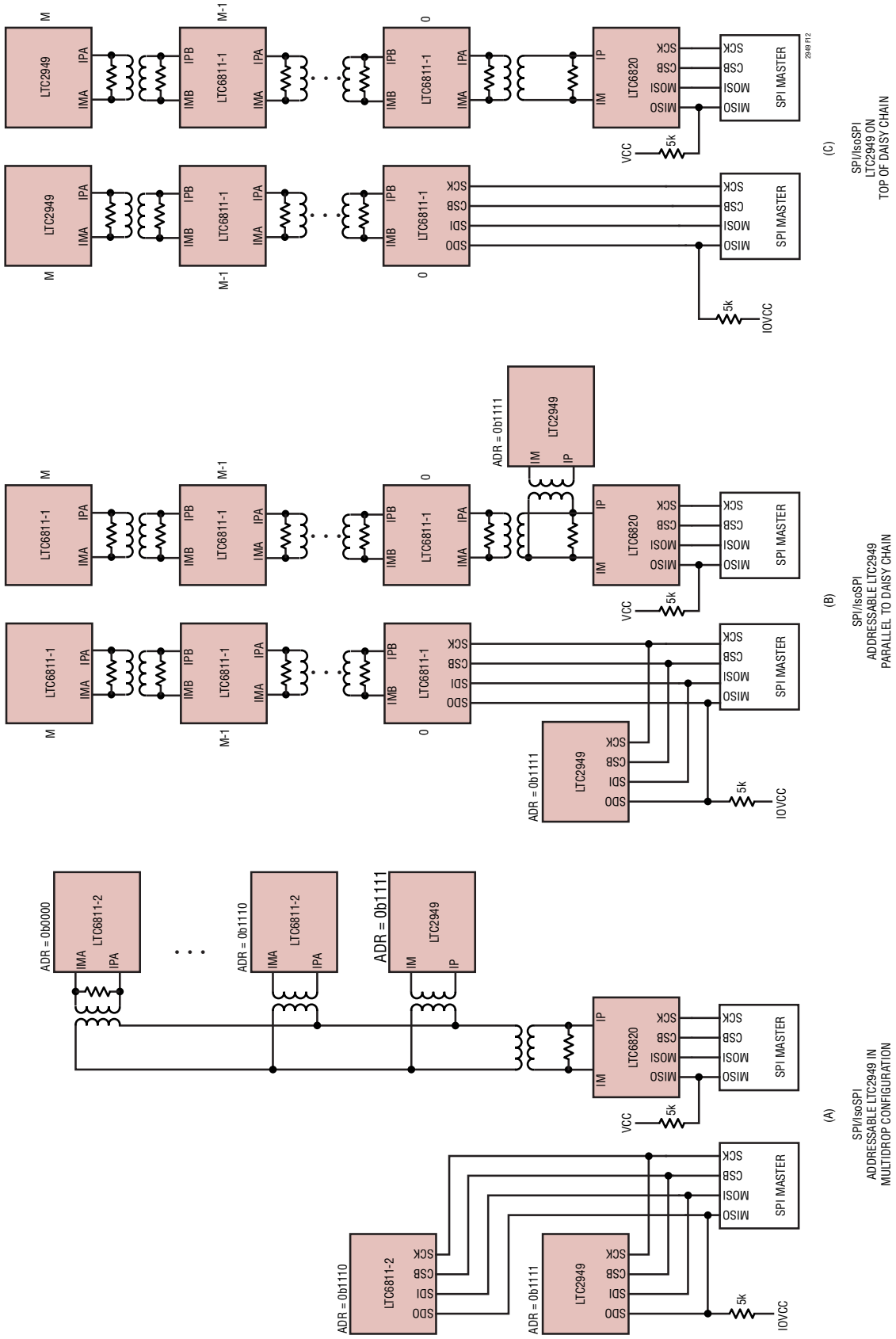


Figure 12. Supported Bus Structures. LTC6811 is shown here as an example for the whole cell monitor family LTC681x, ADBMS68xx that is supported to operate together with the LTC2949.

SERIAL INTERFACES

As the LTC2949 has only one isoSPI port it must be placed as the last (M^{th}) element in a daisy chain. The 0^{th} element communicates to the master via port A which can be configured as isoSPI or normal SPI mode, depending on the connection of the ISOMOD pin. The 0th element connects via port B to the 1st element of the daisy chain using isoSPI, and so on. When the LTC68xx Cell Monitor is operating with port A as SPI (ISOMD = V^-), the SPI detects one of four communication events: CSB falling, CSB rising, SCK rising with SDI = 0, and SCK rising with SDI = 1. Each event is converted into one of the four pulse types for transmission through the daisy chain. Long pulses are used to transmit CSB changes and short pulses are used to transmit data, as explained in Table 8. When both ports are operated in isoSPI mode, isoSPI pulses on port A are passed to port B within a short delay.

DATA LINK LAYER

All data transfers on LTC2949 occur in byte groups. Every byte consists of 8-bits. Bytes are transferred with the most significant bit (MSB) first. CSB must remain low for the entire duration of a command sequence, including between a command byte and subsequent data. A write command takes effect after a correct PEC is processed.

NETWORK LAYER

The LTC2949 registers can be accessed by a direct read/write command (DCMD) containing the registers to be written or read from followed by the register data – see following section Direct Read/Write Command (DCMD). Beside the DCMD, the LTC2949 supports the LTC68xx Cell Monitor compatible commands ADCV and RDCV.

When LTC2949 is the last element in an isoSPI daisy chain, the DCMD can be used to write to LTC2949 but not to read data from the device, because the DCMD is not supported by other LTC68xx Cell Monitors and thus they do not pass data from their port B to port A. Therefore, the RDCV command must be used to read from LTC2949 as element of a daisy chain. LTC2949 registers read by the RDCV command can be configured by a preceding DCMD.

Table 10 summarizes the possibilities to communicate to LTC2949.

Table 10. Communication with LTC2949

	PARALLEL TO DAISY CHAIN OR LTC2949 SOLE	LTC2949 ON TOP OF DAISY CHAIN
Read of Registers	DCMD	Broadcast RDCV (RDCVCONF = 0, BCREN = 1)
Write of Registers	DCMD	
Trigger of Fast ADC Conversion	Addressed ADCV Broadcast ADCV	
Read of Fast Conversion Results	Addressed RDCV (RDCVCONF = 1, BCREN = 0)	Broadcast RDCV (RDCVCONF = 1, BCREN = 1)

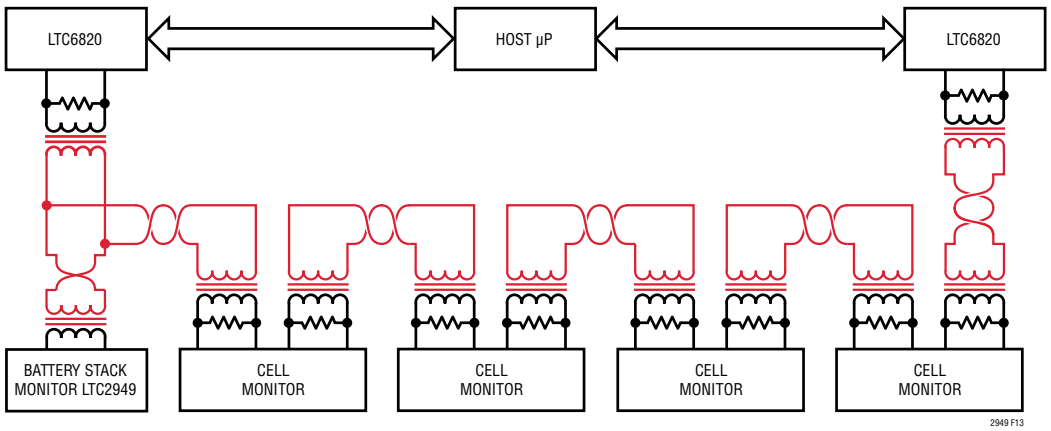


Figure 13. LTC2949 Connected to a Reversible isoSPI Ring

SERIAL INTERFACES

Fast Measurement Timings

The following timing diagrams shows LTC2949 fast single shot timing in relation to LTC6810's timing of the ADCV command for measuring all six cells. Other LTC681x Cell Monitors have similar timing diagram, just with different number of ADCs and cells. The LTC681x devices have several ADC modes with different filter bandwidth and accuracy. Typically, in the 7kHz normal mode, all cells are converted within a time window very close to LTC2949's fast conversion time which is nominal 782µs. For example, the LTC6810 converts all cells within 815µs in the normal mode.

As an example, only three (I2, BAT, AUX) of maximum four ADCs of LTC2949 are configured for fast conversions. The displayed timings are valid for any allowed combinations of fast channels.

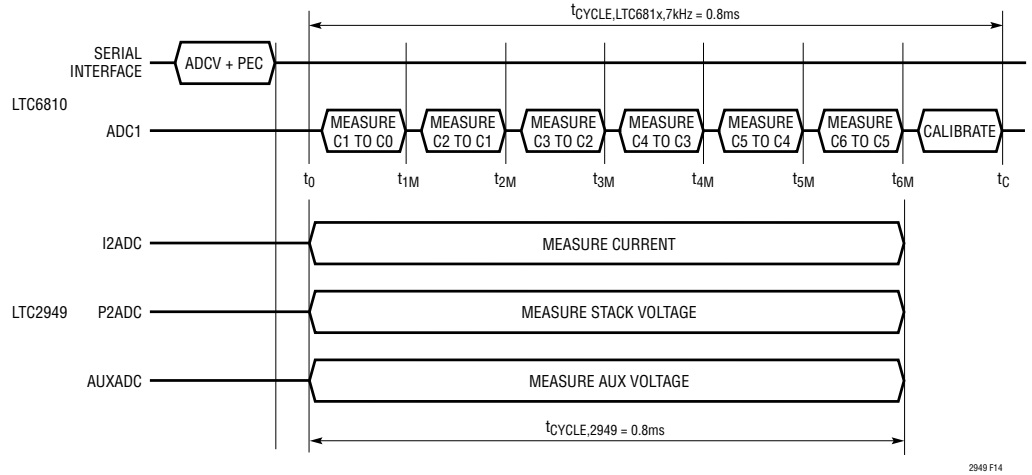


Figure 14. Timing for ADCV Command Measuring Cell Voltages and LTC2949's Current and Voltage Inputs

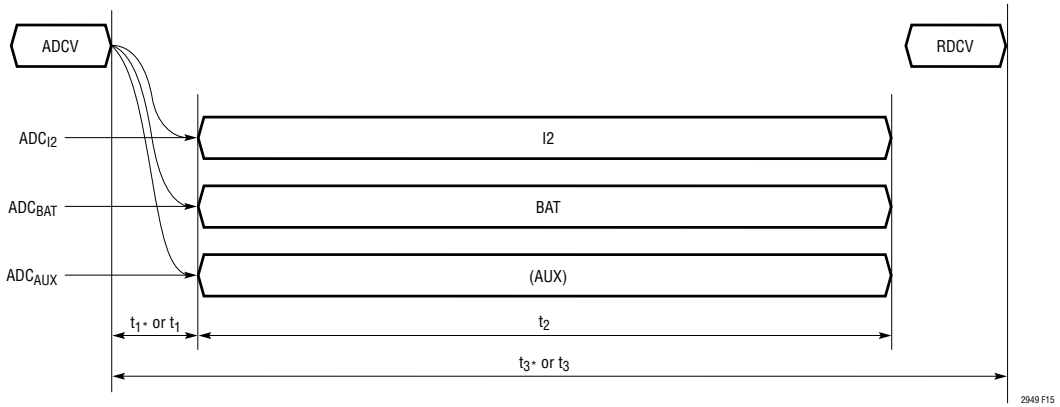


Figure 15. Timing for LTC2949's ADCV Command Measuring Current and Voltage Inputs.

DESCRIPTION	PARAMETER	VALUE/TOLERANCE
ADVC's last PEC byte to start of conversion latency without AUX conversion	t_1	6 to 8µs
ADVC's last PEC byte to start of conversion latency with AUX conversion	t_{1*}	6 to 170µs
Conversion time	t_2	742 to 821µs
ADVC's last PEC byte to HS = 0x0F (hand shake byte read by RDCV indicating conversion results ready, see note below) without AUX	t_3	855 to 945µs
ADVC's last PEC byte to HS = 0x0F (hand shake byte read by RDCV indicating conversion results ready, see note below) with AUX	t_{3*}	855 to 1260µs

SERIAL INTERFACES

Note: If the first HS byte of the RDCV data is 0x0F, the conversion results of the very same data set are already valid. If the first HS byte of the RDCV data is 0x00, the conversion results of the very same data set are not valid. A new RDCV must be issued to check for updated conversion results. If the first HS byte of the RDCV data is 0x00 the host can continue to read HS bytes until it changes to 0x0F. The following RDCV command for sure will have valid conversion results, still, the HS byte of the very same data set will be 0x00, because it was already internally cleared after it was read 0x0F in the previous RDCV.

The following diagram shows details on LTC2949's fast continuous conversion timing. Fast continuous operation is started by a direct write command that sets bit FACONV and at least one of the channel bits (CH1, CH2, AUX) in register FACTRL.

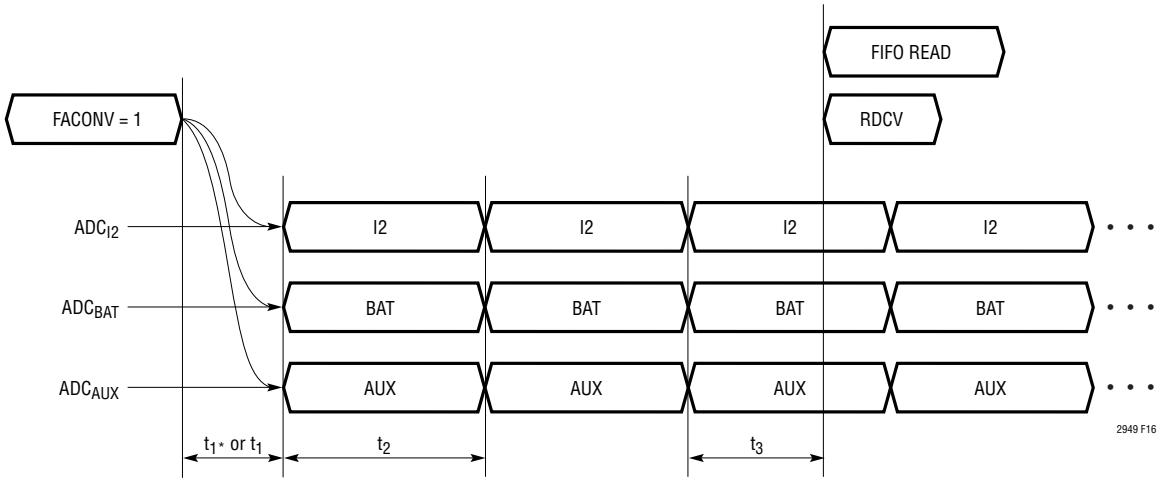


Figure 16. Timing for LTC2949's Fast Continuous Current and Voltage Measurements.

DESCRIPTION	PARAMETER	VALUE/TOLERANCE
Direct write's last PEC byte to start of conversion latency without AUX conversion	t_1	6 to 8µs
Direct write's last PEC byte to start of conversion latency with AUX conversion	t_{1*}	6 to 170µs
Conversion time	t_2	742 to 821µs
Any sample's start of conversion to HS = 0x0F (hand shake byte read by RDCV indicating conversion results ready) or to sample available via FIFO read operation	t_3	0 to 315µs

SERIAL INTERFACES

Fast AUX Measurements

It is not possible to change the AUX MUX configuration during fast continuous mode (FCM) measurements. FAMUXP, FAMUXN can be written and the same value read back at any time, but the internal MUX will only be set to the requested configuration when receiving a new fast conversion request. This is either the ADCV command for fast single shot (FSSHT) or the transition from 0 to 1 of the FACONV bit for FCM measurements.

When leaving the FCM (FACONV = 0), the host must wait for the last conversion being completed before any new fast conversion is triggered. This can be achieved by waiting at least 1.26 ms.

If both channels are configured fast, it must be ensured that either the FCM stays active for at least 128 samples or FSSHT measurements are inhibited for at least 100ms. Only after every 128 samples / 100 ms, the slow channel registers (including STATUS, FAULTS, EXTFAULTS) are updated. In applications in which it is required to enable and disable FACONV periodically or to perform repetitive FSSHT measurements it is recommended to configure CH1 for slow and CH2 for fast mode, which ensures the slow channel being updated periodically.

Fast AUX Round-Robin Measurements

FSSHT measurements shall be used in applications that require different inputs via the AUX MUX at high update rates (faster than 100 ms). Optionally, the FSSHT measurements can be surrounded by FCM periods, during which a single MUX input is converted continuously. The conversion results of the FCM periods can be read via the FIFO registers or via RDCV. Reading of conversion results from FIFOs is possible at any time. Still, the FSSHT trigger command (ADCV while CONT= 1 and FACTRL unequal zero) will clear all FIFOs.

Following table shows an example sequence of 4 FSSHT measurements that interrupt a FCM period. If only FSSHT measurements are required, the rows CONT0, CONT1 can be omitted.

NAME	MOSI / MISO	DESCRIPTION
CONT0	MOSI:FEF5EB50400EE4C6 MISO:XXXXXXXXXXXXXXXX	Write to FACTRL to disable FCM (FACONV = 0)
MUX0	MOSI:FEF3C7984500013D6E MISO:XXXXXXXXXXXXXXXXXX	Write two bytes to FAMUXN to select V1 vs. GND (NTC)
ADCV	MOSI:FB60FADE MISO:XXXXXXXX	ADCV to trigger conversion
RDCV	MOSI:F8040970FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF MISO:XXXXXXXX010000000000FE4AE8180F0F0F0FC602	RDCV to read conversion results
MUX1	MOSI:FEF3C798450016C1BA MISO:XXXXXXXXXXXXXXXXXX	Write two bytes to FAMUXN to select VREF2 vs. GND
ADCV	MOSI:FB60FADE MISO:XXXXXXXX	ADCV to trigger conversion
RDCV	MOSI:F8040970FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF MISO:XXXXXXXX000000000000C212610F0F0F0F0F76B6	RDCV to read conversion results
MUX2	MOSI:FEF3C7984517007512 MISO:XXXXXXXXXXXXXXXXXX	Write two bytes to FAMUXN to select GND vs. VREF2_250k
ADCV	MOSI:FB60FADE MISO:XXXXXXXX	ADCV to trigger conversion
RDCV	MOSI:F8040970FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF MISO:XXXXXXXX000000000000C212E7180F0F0F0F1A78	RDCV to read conversion results

SERIAL INTERFACES

NAME	MOSI / MISO	DESCRIPTION
MUX3	MOSI:FEF3C7984500174A88 MISO:XXXXXXXXXXXXXXXXXX	Write two bytes to FAMUXN to select VREF2_250k vs. GND
ADCV	MOSI:FB60FADE MISO:XXXXXXXX	ADCV to trigger conversion
RDCV	MOSI:F8040970FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF MISO:XXXXXXXX000000000000C2121AE70F0F0F0F7C26	RDCV to read conversion results
MUXCONT	MOSI:FEF3C79845111294A6 MISO:XXXXXXXXXXXXXXXXXX	Write two bytes to FAMUXN to select CF2P vs. CF2M (necessary to do the open wire check during the FCM)
CONT1	MOSI:FEF5EB50400F6FF4 MISO:XXXXXXXXXXXXXXXX	Write to FACTRL to enable FCM (FACONV = 1)

Note 1: MISO data is only shown as an example and the actual data may change. 'X' indicates don't care data.

Note 2: A delay of ≥ 1.26 ms is mandatory between any ADCV and RDCV to ensure valid conversion result readings.

Note 3: Above MUX settings convert one external pin voltage V1 vs. GND and the internal VREF2 in three different ways. This example and can be adjusted and extended to any MUX configurations required.

Note 4: CONT0 and MUX0 can be merged to a single 3-write command to FAMUXN, FAMUXP, FACTRL (MOSI: 0xFEF3C7984600010E9516)

Note 5: When LTC2949 is in STANDBY state it can be moved to MEASURE state at any time by writing CONT=1. From the write command it takes t_{IDLE_CORE} until the MEASURE state is active and then worst case 140ms until the first slow channel conversion results can be read form LTC2949's registers. First fast measurements can be performed, if FACTRL was configured appropriately, already when MEASURE state is active.

Note 6: The following sequence allows a fast and efficient initialization of LTC2949 before any fast conversions can be performed:

1. Wakeup, configure ADCCONF and perform ADJUPD as required.
2. Write 0x08 (CONT) to OPCTRL
3. 3-Byte-Write to FAMUXN (e.g. 0x00 = GND), FAMUXP (e.g. 0x16 = VREF2), FACTRL (e.g. 0x02 = FACHA or another allowed combination to perform any fast conversion)
4. Send any ADxx (e.g. ADCV, see table 17)
5. Wait at least 1.2 ms
6. Send any RDxx (e.g. RDCVA, see table 18). If HS byte is unequal 0x0F go back to 3.
7. Initialization is done. LTC2949 is now in MEASURE mode and any fast conversions can be performed subsequently (e.g. the sequence from above table)

SERIAL INTERFACES

Direct Read/Write Command (DCMD)

To access the full register map of the LTC2949, a special direct command (DCMD) is provided which is not used by other LTC68xx Cell Monitors. DCMD allows to read/write arbitrary number of bytes from/to LTC2949's register map. The LTC2949 auto-increments its address pointer after each data byte, so multiple registers can be written/read as part of a single transaction. Data packets from one to up to 16 bytes are interleaved by a two-byte data PEC. Data packets written without PEC are discarded. Read commands may stop at any byte.

Table 11. Direct Read/Write Command Format

Byte	0	1	2	3	4	5	…	N+4	N+5	N+6	N+7	…	2N+6	2N+7	2N+8	…
R/W	Master to slave (MOSI)					Write commands: Master to slave (MOSI) Read commands: Slave to master (MISO)										
Name	DCMD	RADDR	PEC0	PEC1	ID	$DATA_0$	…	$DATA_{N-1}$	PEC0	PEC1	$DATA_N$	…	$DATA2_{N-1}$	PEC0	PEC1	…

ID byte is used to distinguish between read and write commands and it defines the number of data bytes per PEC (parameter N in above table). The ID byte is not part of any PEC, instead it has intrinsic error detection via redundancy and error check bits. See following tables for details.

Table 12. Bit Definitions of Byte ID[7:0]

ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]
RW	NOT RW	PECC[3] XOR PECC[2]	PECC[3]	PECC[2]	PECC[1] XOR PECC[0]	PECC[1]	PECC[0]

Table 13. ID[7:0] Byte Format Description

NAME	DESCRIPTION
RW	ID[7] = RW indicates read (RW=1) or write (RW=0) commands. For safe data transmission redundancy is added to ID[6] which is the inverse of RW (NOT RW, meaning 0 for read and 1 for write).
PECC[3:0]	PEC Configure determines the number of data bytes after which a PEC is transmitted. Number of data bytes is DECIMAL(PECC[3:0])+1 (parameter N in above table). Allowed values for PECC are 0 to 15 (1 to 16 data bytes per PEC). ID[5] (= PECC[3] XOR PECC[2]) and ID[2] (=PECC[1] XOR PECC[0]) are error check bits for safe data transmission.

Table 14. Direct Read/Write Command Format Details

NAME	DESCRIPTION
DCMD[7:0]	Direct command. It is fixed to the value 0xFE.
RADDR[7:0]	Starting register address from which data is read or to which data is written.
PEC0,1	The Packet Error Code Bytes PEC0 and PEC1 hold a 15-bit CRC according to CAN BUS CRC15 which is right padded with 0 (see Table 22. Write/Read PEC Format). The PEC in bytes 2-3 is calculated on DCMD and RADDR. All following PECs are calculated on preceding M data-bytes. The number of data bytes per PEC is defined by the ID byte, which is not part of any PEC, see below. For read commands the MOSI line is don't care, the slave will send the data PEC on its MISO line and the master must compare it to the PEC calculated on the data received. The read command was successful of both PECs match. For write commands, the master must send the PEC on its MOSI line and LTC2949 will compare the received PEC with its internal calculated PEC. In case of a PEC mismatch the data will be discarded and an external communication PEC error (EXTCOMMERR) will be flagged in the FAULTS register.
$DATA_X$	Data bytes to be send to or read from LTC2949's register map. The starting address is given by RADDR and is auto-incremented for every data byte.

SERIAL INTERFACES

Commands Compatible with LTC68xx Cell Monitors (RDCV, ADCV)

The LTC2949 supports several RDCV and ADCV style commands compatible with LTC68xx Cell Monitors. RDCVA-RDCVF, RDAUXA-RDAUXD, RDCFGA, RDCFGB (all referred as RDCV commands in this document), ADCV, ADOW, ADOL, ADAX, ADAXD, ADCVAX and ADCVSC (all referred as ADCV commands in this document) are supported as broadcast and addressed commands. Addressed commands are used to address LTC2949 exclusively. To trigger actions on LTC2949 and LTC68xx Cell Monitors simultaneously, broadcast commands are used. This is for example useful to initiating ADC conversions of several devices at the same time. No matter if LTC2949 is connected parallel to or on top of a daisy chain, addressed ADCV commands can trigger measurements on LTC2949 only and broadcast ADCV commands can perform synchronous ADC conversions on all devices connected to the SPI / isoSPI bus. The conversion starts at the end of the PEC for all devices.

In cases where LTC2949 is connected parallel to a daisy chain, direct read commands (DCMD) must be used to read register data and addressed RDCV commands (with RDCVCONF=1) must be used to read the last fast conversion results. If LTC2949 is connected on top of a daisy chain, broadcast RDCV commands must be used to read register data (RDCVCONF=0) or to read the last fast conversion results (RDCVCONF=1) depending on setting of REGSCTRL.RDCVCONF. Write to LTC2949's register map is always done with direct write commands (DCMD) independent of the bus topology. See Table 10 (Communication with LTC2949) for a summary of all possible communication scenarios.

Before LTC2949 can react on ADCV commands it must be running in slow continuous measurement mode (bit CONT in OPCTRL), at least one fast measurement channel must be selected via the Fast Control Register (FACTRL) and optionally, to make also fast BAT conversions via one of the power ADCs (P1 or P2 in voltage mode), P1ASV and/or P2ASV in the ADC configuration register (ADCCONF) must be set. If LTC2949 is running in fast continuous mode (FACONV=1) any ADCV command is ignored and acquired samples can be read from the FIFO registers (FIFOI1, FIFOI2, FIFOBAT, FIFOAUX). Still, also in this mode, it is possible to read the last fast conversion results via RDCV (RDCVCONF=1). If fast continuous mode is disabled (FACONV=0), any ADCV command will clear all FIFOs. If needed, samples within FIFOs should be read before sending an ADCV command while FACONV is cleared.

In the configuration where LTC2949 is on top of a daisy chain, after a broadcast RDCV command, the stacked LTC68xx Cell Monitors turn into a cascaded shift register, in which data is shifted through each device to the next device in the stack. In this scenario, LTC2949 responds to RDCV commands only if the Broadcast Read Enable bit (BCREN) in the Register Control Register (REGSCTRL) is set.

In the scenario where LTC2949 is placed in parallel to a daisy chain of LTC68xx Cell Monitors, the bit BCREN must be cleared (default) to avoid bus collisions. Still, any broadcast RDCV may clear LTC2949's internal HS byte (see below) if the bit RDCVCONF is set, no matter if BCREN is set or not. For this reason, it is recommended to read LTC2949's fast conversion results before reading from the LTC68xx Cell Monitors. Or, if for software timing reasons it is necessary to read from the LTC68xx Cell Monitors first, the bit RDCVCONF must be cleared before (it must be set again afterwards to read fast conversion data from LTC2949).

The last results of any fast conversion can be read out by the RDCV command, providing sequentially the results of I1, I2, BAT and AUX (least significant bytes first to be compatible with LTC68xx Cell Monitors) followed by one or more hand shake (HS) bytes, indicating if the data is new (0x0F) or old (0x00). Once LTC2949 sends the HS byte, it will continue sending it as long as the master is reading bytes. Still, a PEC will always be send for every 6 data bytes. Per transaction, the HS byte may only change from 0x00 to 0x0F, once it is 0x0F it won't change. This allows the master to poll for conversion results being ready by checking for a transition of the HS byte from 0x00 to 0x0F. If the first HS byte is 0x0F the conversion data received with that command is already new and valid. If the first HS byte is 0x00 the data received in the same transaction was not yet updated. A subsequent RDCV

SERIAL INTERFACES

command is necessary to read the updated conversion results, still, the HS byte will be reported as 0x00 for this RDCV command, as it was internally already cleared after it was read 0x0F with the previous RDCV.

LTC2949's fast conversion time is typically 0.8ms. Additional processing time is necessary for the results being ready to be read by the master. Worst case, 1.26 ms after a conversion was triggered, the results can be read via a FIFO register (in case of fast continuous mode) or via the RDCV command. For fast single shot measurements, this limits the maximum guaranteed sample rate to ~0.8ksps.

For fast continuous measurement, the sample rate is fixed to 1.25ksps and the mentioned delay is just a latency between the actual measurements and the time the samples are available to be read. The master shall wait at least 1.26ms between the time fast continuous mode is enabled and the first time any FIFO register is read, to allow the first sample to be read from the FIFO. Alternatively, it is also possible to use a RDCV command to check when the first sample is ready (see HS byte above) and then read all samples from the FIFO registers periodically.

Table 15. Format of ADCV/RDCV Style Commands. Only for RDCV Commands the Slave Sends Data to the Master on the MISO Line

BYTE	0	1	2	3	4	…	9	10	11	12	…	17	18	19	…
R/W	Master to slave (MOSI)				Slave to master (MISO)										
Name	CMD0	CMD1	PEC0	PEC1	DATA0	…	DATA6	PEC0	PEC1	DATA7	…	DATA11	PEC0	PEC1	…

CMD0 and CMD1 are the command bytes. The format for the commands is shown in Table 16. CC[10:0] is the 11-bit command code. A list of supported command codes is shown in Table 17 and Table 18. Broadcast commands have a value 0, addressed commands have a value 1 for CMD0[7] through CMD0[3]. The PEC must be computed on the entire 16-bit command (CMD0 and CMD1).

Table 16. CMD0, CMD1 Command Bytes Format. Data is Send from Master to Slave (MOSI). A/B is 0 for Broadcast and 1 for Addressed Commands.

NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CMD0	A/B	A/B	A/B	A/B	A/B	CC[10]	CC[9]	CC[8]
CMD1	CC[7]	CC[6]	CC[5]	CC[4]	CC[3]	CC[2]	CC[1]	CC[0]

SERIAL INTERFACES

Table 17. ADCV Style Commands. LTC2949 Performs a Fast Conversion Depending on FACTRL/ADCCONF Registers Upon Those Commands

NAME	CMD0[7:3]	CC[10:0]	DESCRIPTION
ADCV	Broadcast: all 0	0 1 x x 1 1 x 0 x x x	LTC2949 reacts to all commands in the same way by triggering a fast conversion (if enabled via FACTRL register).
ADOW	Addressed: all 1	0 1 x x x 1 x 1 x x x	
ADOL		0 1 x x 0 0 x 0 0 0 1	
ADAX		1 0 x x 1 1 0 0 x x x	
ADAXD		1 0 x x 0 0 0 0 x x x	
ADCVAX		1 0 x x 1 1 x 1 1 1 1	
ADCVSC		1 0 x x 1 1 x 0 1 1 1	

Table 18. RDCV Style Commands. Used to Read Fast Conversion Results or for Indirect Memory Map Reads from LTC2949

NAME	CMD0[7:3]	CC[10:0]	DESCRIPTION
RDCFGA	Broadcast: all 0	0 0 0 0 0 0 0 0 0 1 0	LTC2949 reacts to all commands in the same way by either transmitting fast conversion results (default, RDCVCONF=1) or by transmitting register data (RDCVCONF=0)
RDCFGB	Addressed: all 1	0 0 0 0 0 1 0 0 1 1 0	
RDCVA		0 0 0 0 0 0 0 0 1 0 0	
RDCVB		0 0 0 0 0 0 0 0 1 1 0	
RDCVC		0 0 0 0 0 0 0 1 0 0 0	
RDCVD		0 0 0 0 0 0 0 1 0 1 0	
RDCVE		0 0 0 0 0 0 0 1 0 0 1	
RDCVF		0 0 0 0 0 0 0 1 0 1 1	
RDAUXA		0 0 0 0 0 0 0 1 1 0 0	
RDAUXB		0 0 0 0 0 0 0 1 1 1 0	
RDAUXC		0 0 0 0 0 0 0 1 1 0 1	
RDAUXD		0 0 0 0 0 0 0 1 1 1 1	

SERIAL INTERFACES

The RDCV command allows reading data packets much longer than the daisy chain shift register. The length of the shift register is 64 • M bits, whereas M is the number of elements in the chain excluding LTC2949. Data from the LTC2949 is received by the master after 64 • M data bits starting with bit I1[7] according to the figure below. A PEC is calculated after every 6 data bytes. After the transmission of the conversions results, the LTC2949 continuously sends the hand shake byte (HS) indicating if the data is new (0x0F) or old (0x00). A transition of the hand shake byte from 0x00 to 0x0F indicates the arrival of new data, which can be read out by a subsequent RDCV command.

Table 19. RDCV Command Format. CMD0, CMD1 According to Table 18 (RDCV Style Commands). Requires RDCVCONF=1.

CMD0	CMD1	PEC0	PEC1	I1[7:0]	I1[15:8]	I2[7:0]	I2[15:8]	BAT[7:0]
BAT[15:8]	PEC0	PEC1	AUX[7:0]	AUX[15:8]	HS	HS	HS	HS
PEC0	PEC1	HS	HS	HS	HS	HS	HS	PEC0
PEC1	HS	HS	HS	HS	HS	HS	.....	

Note: The conversion results I1, I2, BAT, AUX are converted to volts by multiplication with the LSB size 7.60371 µV for the current and 375.183 µV for the BAT and AUX channel.

Indirect Memory Access RDCV Command

DCMD is the recommended way of reading data from the LTC2949 in addressable mode. When LTC2949 is the last element in a daisy chain, an RDCV has to be used to read data from the LTC2949, as DCMD is not supported by LTC68xx Cell Monitors and therefore does not configure them as shift registers, In default, the LTC2949 will respond to RDCV with the fast mode conversion results as described above (RDCVCONF = 1).

In order to gain access to the entire register map of LTC2949 an address pointer can be set causing the LTC2949 to provide data starting at that register address on subsequent RDCV commands. To use this indirect memory access RDCV command, the RDCV Configuration Bit (RDCVCONF) has to be reset and Broadcast Read Enable bit (BCREN) has to be set in REGSCTRL and the starting pointer must be written to the RDCV Indirect Address Register (RDCVIADDR). In this way any register can be read by subsequent RDCV commands. The address pointer is auto-incremented after every data byte for reading data bursts of any length. A PEC is transmitted after every six data bytes. Once the REGSCTRL is written accordingly, only the Indirect Address Register must be updated to read from other memory locations.

Please note that the RDCVIADDR can also be written before the REGSCTRL if a single DCMD spanning from RDCVIADDR to REGSCTRL is used. For this single write burst, the two bytes between RDCVIADDR and REGSCTRL are don't care and can be written 0x00.

Figure 17. Indirect Memory Access Read Procedure Using RDCV Command

Table 20. Indirect Address RDCV Command Format, CMD0, CMD1 According to Table 18 (RDCV Style Commands), Requires RDCVCONF = 0 and BCREN = 1

CMD0	CMD0	PEC0	PEC1	$DATA_0$	$DATA_1$	$DATA_2$	$DATA_3$	$DATA_4$
$DATA_5$	PEC0	PEC1	$DATA_6$	$DATA_7$	$DATA_8$	$DATA_9$	$DATA_{10}$	$DATA_{11}$
PEC0	PEC1	.....						

$DATA_0$ is the content of the register at the starting address that was written to RDCVIADDR. $DATA_1$ is the content of the register at the following address and so on.

SERIAL INTERFACES

Packet Error Code

The packet error code (PEC) is a 15-bit cyclic redundancy check (CRC) value calculated for all of the bits in a register group in the order they are passed, using the initial PEC seed value of 000000000010000 and the following characteristic polynomial: x15 + x14 + x10 + x8 + x7 + x4 + x3 + 1. To calculate the 15-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 000000000010000 (PEC is a 15-bit register group)
2. For each bit DIN coming into the PEC register group, set
   IN0 = DIN XOR PEC [14]
   IN3 = IN0 XOR PEC [2]
   IN4 = IN0 XOR PEC [3]
   IN7 = IN0 XOR PEC [6]
   IN8 = IN0 XOR PEC [7]
   IN10 = IN0 XOR PEC [9]
   IN14 = IN0 XOR PEC [13]
3. Update the 15-bit PEC as follows
   PEC [14] = IN14,
   PEC [13] = PEC [12],
   PEC [12] = PEC [11],
   PEC [11] = PEC [10],
   PEC [10] = IN10,
   PEC [9] = PEC [8],
   PEC [8] = IN8,
   PEC [7] = IN7,
   PEC [6] = PEC [5],
   PEC [5] = PEC [4],
   PEC [4] = IN4,
   PEC [3] = IN3,
   PEC [2] = PEC [1],
   PEC [1] = PEC [0],
   PEC [0] = IN0
4. Go back to step 2 until all the data is shifted. The final PEC (16-bits) is the 15-bit value in the PEC register right padded with 0. An example to calculate the PEC for a 16-bit word (0x0001) is listed in Table 21. The PEC for 0x0001 is computed as 0x3D6E after stuffing a 0-bit at the LSB. For longer data streams, the PEC is valid at the end of the last bit of data sent to the PEC register. LTC2949 calculates PEC for any command or data received and compares it with the PEC following the command or data. The command or data is regarded as valid only if the PEC matches. LTC2949 also attaches the calculated PEC at the end of the data it shifts out. Table 22 shows the format of PEC while writing to or reading from LTC2949.

SERIAL INTERFACES

Table 21. PEC Calculation for 0x0001

PEC[14]	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	**0**
PEC[13]	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	**0**
PEC[12]	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	**1**
PEC[11]	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	**1**
PEC[10]	0	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1	**1**
PEC[9]	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[8]	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	**0**
PEC[7]	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1	**1**
PEC[6]	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0**
PEC[5]	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	**1**
PEC[4]	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	**1**
PEC[3]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	**0**
PEC[2]	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	**1**
PEC[1]	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	**1**
PEC[0]	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	**1**
IN14	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0		**0**
IN10	0	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1		**PEC Word**
IN8	0	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0		
IN7	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1	1		
IN4	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1		
IN3	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0		
IN0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
Clock Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Table 22. Write/Read PEC Format

NAME	RD/WR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEC0	RD/WR	PEC[14]	PEC[13]	PEC[12]	PEC[11]	PEC[10]	PEC[9]	PEC[8]	PEC[7]
PEC1	RD/WR	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]	0

Improved PEC Calculation

The PEC allows the user to have confidence that the serial data read from the LTC2949 is valid and has not been corrupted by any external noise source. This is a critical feature for reliable communication and the LTC2949 requires that a PEC be calculated for all data being read from and written to the LTC2949. For this reason it is important to have an efficient method for calculating the PEC. The code below demonstrates a simple implementation of a lookup table derived PEC calculation method. There are two functions, the first function init_PEC15_Table() should only be called once when the microcontroller starts and will initialize a PEC15 table array called pec15Table[]. This table will be used in all future PEC calculations. The pec15 table can also be hard coded into the microcontroller rather than running the init_PEC15_Table() function at startup. The pec15() function calculates the PEC and will return the correct 15-bit PEC for byte arrays of any given length.

SERIAL INTERFACES

```
/***********************************
Copyright 2012 Linear Technology Corp. (LTC)
Permission to freely use, copy, modify, and distribute this software for any
purpose with or without fee is hereby granted, provided that the above
copyright notice and this permission notice appear in all copies:

THIS SOFTWARE IS PROVIDED "AS IS" AND LTC DISCLAIMS ALL WARRANTIES
INCLUDING ALL IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS. IN NO
EVENT SHALL LTC BE LIABLE FOR ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL
DAMAGES OR ANY DAMAGES WHATSOEVER RESULTING FROM ANY USE OF SAME, INCLUDING
ANY LOSS OF USE OR DATA OR PROFITS, WHETHER IN AN ACTION OF CONTRACT, NEGLIGENCE
OR OTHER TORTUOUS ACTION, ARISING OUT OF OR IN CONNECTION WITH THE USE OR
PERFORMANCE OF THIS SOFTWARE.
***********************************************************/


int16 pec15Table[256];
int16 CRC15_POLY = 0x4599;
void init_PEC15_Table()
{
    for (int i = 0; i < 256; i++)
    {
        remainder = i << 7;
        for (int bit = 8; bit > 0; --bit)
        {
            if (remainder & 0x4000)
            {
                remainder = ((remainder << 1));
                remainder = (remainder ^ CRC15poly)
            }
            else
            {
                remainder = ((remainder << 1));
            }
        }
        pec15Table[i] = remainder&0xFFFF;
    }
}

unsigned int16 pec15 (char *data , int len)
{
    int16 remainder,address;

    remainder = 16;//PEC seed
    for (int i = 0; i < len; i++)
    {
        address = ((remainder >> 7) ^ data[i]) & 0xff;//calculate PEC table address
        remainder = (remainder << 8 ) ^ pec15Table[address];
    }
    return (remainder*2);//The CRC15 has a 0 in the LSB so the final value must be multiplied by 2
}
```

PAGE 0

	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
0x0	C1						E1						TB1			
	0x0						0x0						0x0			
0x10	C2						E2						TB2			
	0x0						0x0						0x0			
0x20					C3								TB3			
					0x0								0x0			
0x30					E4								TB4			
					0x0								0x0			
0x40	I1MAX		I1MIN		P1MAX		P1MIN		I2MAX		I2MIN		P2MAX		P2MIN	
	0x8000		0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF	
0x50	BATMAX		BATMIN		TEMPMAX		TEMPMIN		VCCMAX		VCCMIN		SLOT1MAX		SLOT1MIN	
	0x8000		0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF	
0x60	SLOT2MAX		SLOT2MIN													
	0x8000		0x7FFF													
0x70	WKUPACK									I1RAW			I2RAW			
	0x0									0x0			0x0			
0x80	STATUS	STATVT	STATIP	STATC	STATE	STATCEOF	STATTB	STATVCC	STATUSM	STATVTM	STATIPM	STATCM	STATEM	STATCEOFM	STATTBM	STATVCCM
	0xF	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x79	0xFF	0xFF	0x3F	0xCF	0xB7	0xFF	0x3
0x90	I1			P1			I2			P2			IAVG1			GCV
	0x0			0x0			0x0			0x0			0x0			0x0
0xA0	BAT		TEMP		VCC		SLOT1		SLOT2		VREF		IAVG2			GCI1
	0x0		0x0		0x0		0x0		0x0		0x7FFF		0x0			0x0
0xB0	I1AVG			I1H1			I1H2			I1H3			I1H4			
	0x0			0x0			0x0			0x0			0x0			
0xC0	I2AVG			I2H1			I2H2			I2H3			I2H4			
	0x0			0x0			0x0			0x0			0x0			
0xD0						DBGCNT				OCC1CTRLSHDW	OCC2CTRLSHDW		EXTFAULTS	FAULTS	OCC1CTRL	OCC2CTRL
						0x0				0x0	0x0		0x80	0x0	0x0	0x0
0xE0	GCI2	ACCCTRL1	ACCCTRL2		ACCI1DB	ACCI2DB	F24GCVH	F24GCVM	GPIO4HBCTRL	TBCTRL	F24GCVL	SLOT1MUXN	SLOT1MUXP	SLOT2MUXN	SLOT2MUXP	
	0x0	0x0	0x0		0x0	0x0	0x0	0x0	0x0	0x7	0x0	0x0	0x0	0x0	0x0	
0xF0	OPCTRL	FCURGPIOCTRL	FGPIOCTRL	FAMUXN	FAMUXP	FACTRL		FIFOI1	FIFOI2	FIFOBAT	FIFOAUX		RDCVIADDR			REGSCTRL
	0x0	0x0	0x0	0x0	0x0	0x0		0x0	0x0	0x0	0x0		0x0			0x80

PAGE 1

	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
0x0	C1TH						C1TL						TB1TH			
	0x7FFFFFFFFFFF						0x800000000000						0xFFFFFFFF			
0x10	E1TH						E1TL									
	0x7FFFFFFFFFFF						0x800000000000									
0x20	C2TH						C2TL						TB2TH			
	0x7FFFFFFFFFFF						0x800000000000						0xFFFFFFFF			
0x30	E2TH						E2TL									
	0x7FFFFFFFFFFF						0x800000000000									
0x40					C3TH								TB3TH			
					0x7FFFFFFFFFFFFF								0xFFFFFFFF			
0x50	EEPROM				C3TL								RS1TC2			
	0x0				0x8000000000000000								0x0			
0x60					E4TH								TB4TH			
					0x7FFFFFFFFFFFFF								0xFFFFFFFF			
0x70	ISO0	ISO1	ISO2		E4TL								RS2TC2			
	0x0	0x0	0x0	0x0	0x8000000000000000								0x0			
0x80	I1TH		I1TL		P1TH		P1TL		I2TH		I2TL		P2TH		P2TL	
	0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF		0x8000	
0x90	BATTH		BATTL		TEMPTH		TEMPTL		VCCTH		VCCTL					
	0x7FFF		0x8000		0x7FFF		0x8000		0x7FFF		0x8000					
0xA0	SLOT1TH		SLOT1TL		SLOT2TH		SLOT2TL			RSTUNLCK	RREF1			RREF2		
	0x7FFF		0x8000		0x7FFF		0x8000			0x0	0x0			0x0		
0xB0	RS1GC			RS2GC			RSRATIO			BATGC			MUXNSET1	MUXPSET1	MUXNSET2	MUXPSET2
	0x3F0000			0x3F0000			0x3F0000			0x3F0000			0x0	0x0	0x0	0x0
0xC0	MUX1GC			MUX2GC			MUX3GC			MUX4GC			MUXNSET3	MUXPSET3	MUXNSET4	MUXPSET4
	0x3F0000			0x3F0000			0x3F0000			0x3F0000			0x0	0x0	0x0	0x0
0xD0	NTC1A			NTC1B			NTC1C			RS1TC			RS1T0			ADCCONF
	0x0			0x0			0x0			0x0			0x0			0x0
0xE0	NTC2A			NTC2B			NTC2C			RS2TC			RS2T0		DIGINFO	ANAINFO
	0x0			0x0			0x0			0x0			0x0			

= reserved registers can be used to store custom data to external EEPROM

= registers can be used to store custom data to external EEPROM, if they are initialized by the host controller after EEPROM restore.

2949 F18

See chapter "External EEPROM Control Register" for more details on using the optional external EEPROM

Figure 18. Register Map

REGISTER DESCRIPTION

Register Naming Conventions

RW	Read-Write	DEF	Default Value
RO	Read Only	SI	Signed Integer
SO	Set Only (Note)	UI	Unsigned Integer

Note: Write 1 to SO bits to request the associated action. Successful write can be checked by a read command directly following the write command. After the action was performed the SO bit will be cleared automatically by LTC2949. Do not write to registers with SO bits, before all SO bits were read as 0. The typical processing time per action is t_{IDLE_CORE} or t_{CONT} depending on operation mode, see related bit description for details.

MEMORY MAP AND PAGING MECHANISM

The memory map of the LTC2949 is organized in two pages, PAGE0 and PAGE1. PAGE0 contains all slow channel result quantities, control and status registers while PAGE1 contains all threshold and configuration registers. Each page has a register address space ranging from 0x00 to 0xEF, with each register consisting of one 8-bit byte of data. Registers 0xF0 to 0xFF are common to both register pages. Register REGSCTRL at 0xFF is part of this range and is used to switch between pages, see below. For clarity, all register addresses on PAGE1 are expressed as p1.0xYY in the following while addresses on PAGE0 are simply referred to as 0xYY.

Multiple-byte data is stored with most significant byte at the lowest address (little-endian). For instance, the MSB C1[47:40] of the quantity C1 is stored at address 0x00 in PAGE0.

Note that reading data from LTC2949's memory map (no matter if using direct command or indirect memory access RDCV command with RDCVCONF=0) reports MSBytes first, while reading fast conversion results via RDCV (RDCVCONF=1) reports LSBytes first.

Some addresses in the register map are not used and are reserved. Bits in non-reserved registers that are not explicitly described are also reserved. Writing to unused reserved registers or reserved bits in non-reserved registers may result in unwanted behavior of the LTC2949, reserved bits in non-reserved registers should be written as 0; reading of unused registers is generally harmless but will return random data. If software detection of device revision is necessary, then contact the factory for details.

Register Control Register

The Register Control Register (0xFF) selects the active memory page, allows to configure the LTC2949 to respond to broadcast read commands, configures the RDCV command to indirect memory access mode and provides a memory locking mechanism.

Table 23. Control Register REGSCTRL (0xFF)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	PAGE	RW	0	Memory Map Page Select 0: PAGE0 of the memory map is selected. 1: PAGE1 of the memory map is selected.
2	BCREN	RW	0	Broadcast Read Enable 0: LTC2949 does not respond to broadcast read commands 1: LTC2949 responds to broadcast read commands
[5:4]	MLK[1:0]	RW	00	Memory Lock 00: Memory not locked 01: Memory lock requested by master 10: Memory locked
7	RDCVCONF	RW	1	RDCV Configuration Bit 0: Indirect memory access mode. RDCV will report data starting at address written to RDCVIADDR (0xFC). 1: RDCV command will report latest fast channel conversion results.

REGISTER DESCRIPTION

LTC2949 provides a mechanism to lock the memory to keep coherency between registers when accessing the memory. A memory locking can be requested by the master by setting bits MLK[1:0] to 01. Now the LTC2949 updates its registers, e.g. with measurement results. During this time, read and write access to the LTC2949 memory apart from registers REGSCTR and RDCVIADDR is blocked. After all registers are updated by the LTC2949, it sets MLK[1:0] to 10 to indicate to the Master that memory is locked. The LTC2949 does not update the memory map any more until the master unlocks the memory by writing MLK[1:0] to 00.

The LTC2949's internal memory is still updated while the memory is locked and thus accumulation of values and updating of alerts is not interrupted. Once the memory is locked the master can read consistent data even by single byte access. Data does not change between those single read transactions. It is also possible to manipulate result parameter values e. g. to set a certain start value for Charge or Energy etc. Coherency within a single row of 16 bytes (register ranges 0x00 to 0x0F, 0x10 to 0x1F, ... and 0xE0 to 0xEF) is always guaranteed for multiple byte read and write bursts and does not require memory locking.

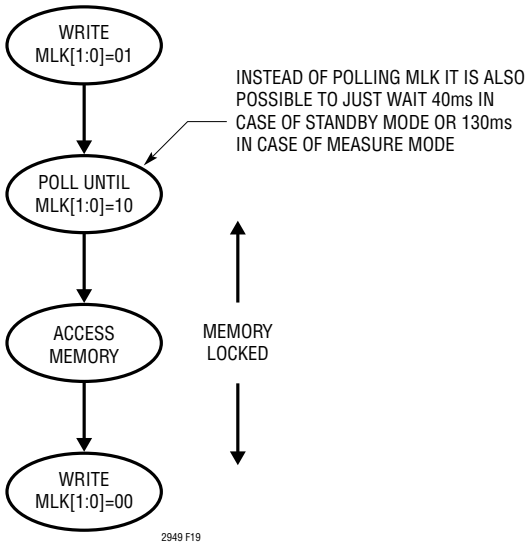


Figure 19. Memory Locking

Table 24. Operation Control OPCTRL (0xF0)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	SLEEP	RW	0	0: Normal operation 1: SLEEP. The LTC2949 will exit SLEEP state if the pin CSB is pulled low in SPI mode or if a wake-up pulse followed by another "Long -1" pulse is sent in isoSPI mode.
1	CLR	SO	0	1: Clear. The Accumulation and Tracking (max/min) registers are cleared: C1, E1, TB1, C2, E2, TB2, C3, TB4, E4, TB4 IMAX, IMIN, PMAX, PMIN, VMAX, VMIN, TEMPMAX, TEMPMIN, VDVCCMAX, VDVCCMIN, SLOTXMAX, SLOTXMIN
2	SSHOT	SO	0	1: Single Shot Measurement. LTC2949 enters state MEASURE and returns to state STANDBY after completion of a single set of measurements of Current, Voltage, Power, Temperature, V_{CC}, SLOT1, SLOT2, V_{REF}. The result registers are updated and SSHOT is cleared when returning to STANDBY. If CONT is set, it is cleared after completion of any conversion cycle in progress and the single shot measurement is executed.
3	CONT	RW	0	0: Continuous measurement is disabled 1: Continuous measurement is enabled after < t_{IDLE_CORE}. Measurement cycles run continuously. Charge, Energy and Time measurements are only active in Continuous mode.
5	ADJUPD	SO	0	To insure data coherency, changes in the 2nd page's configuration registers, except threshold settings, only become effective after an update procedure, which is initialized by setting bit ADJUPD. Once the new configuration values are valid, LTC2949 resets the bit ADJUPD. Changes to the threshold registers may be done at any time and don't require the ADJUPD procedure. 1: Request an update of configuration registers on 2nd memory page, except threshold settings. 0: Update done
7	RST	SO	0	0: Normal operation, 1: Reset device. As default the reset feature is locked and writing 1 to this bit has no effect. See RSTUNLCK for procedure how to reset the device.

Note 9: ADJUPD shall be issued when in STANDBY mode only. The recommended implementation is to set ADJUPD as the last action of the initialization routine, before entering continuous mode. Once ADJUPD is set it takes a maximum of 100ms until LTC2949 has finished the internal update process and the bit ADJUPD is cleared automatically. Thus it is also possible to poll the bit ADJUPD for being cleared to indicate when the operation is done.

In cases where it is necessary to assert ADJUPD after CONT was enabled, it is necessary to clear the bit CONT before, wait 100ms to ensure that all measurement cycles have completed and then assert ADJUPD. After ADJUPD was cleared automatically, the Continuous Mode may be entered again.

To avoid the 100ms wait time when going to STANDBY mode, it is also possible to clear CONT and set CLR at the same time and poll for the bit CLR being cleared by LTC2949. This indicates also the end of any previously ongoing measurement cycle.

REGISTER DESCRIPTION

Reading of status (0x80), faults (0xDC-0xDD) and alert (0x81-0x87) registers may always be done without memory locking. Still, once it is necessary to clear those registers, memory locking is mandatory to avoid missing any alert and faults reporting. If an alert condition occurs while the memory is locked, LTC2949 will set the corresponding bit after the memory is unlocked by the host. This rule must be followed independent of the core state, as certain faults may also be raised in STANDBY mode.

Any fast conversions are not affected by the memory locking mechanism, thus it is still possible to change FAMUX settings, trigger fast single shots, read results via RDCV. Also reading conversion results from the FIFOs during fast continuous measurements is still possible.

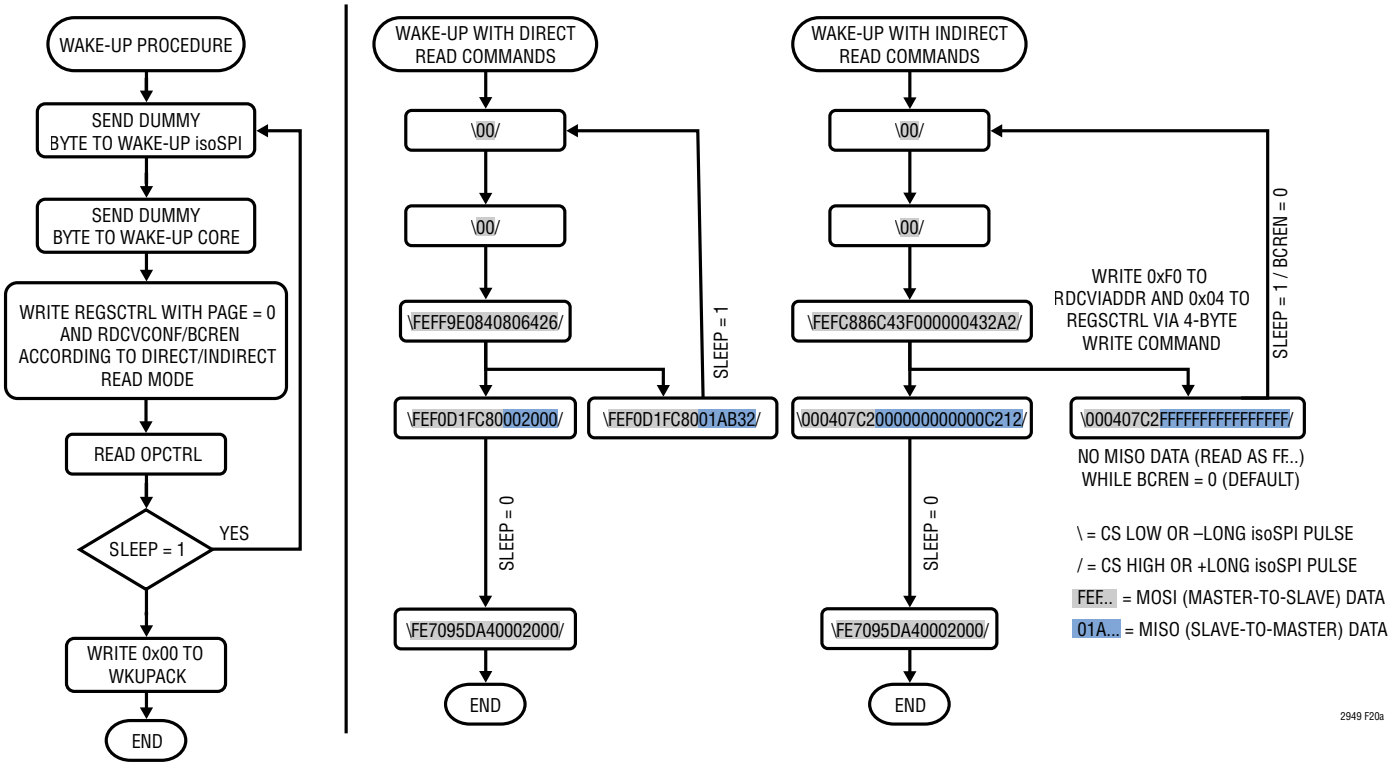
Operation Control Register

The Operation Control Register OPCTRL (0xF0) controls LTC2949's transitions between its CORE States: SLEEP, STANDBY, and MEASURE. Furthermore, it allows to clear accumulation and tracking registers, to validate changes of the configuration registers and to reset the LTC2949.

REGISTER MAP PAGE0

Wake Up Acknowledge

The LTC2949 automatically returns to SLEEP state if no wake up confirmation command is received within 1 second after entering STANDBY state. Wake up confirmation can be either writing 0x00 to register 0x70 or starting of a measurement. Before wake up confirmation, WKUPACK will report a countdown from 0xFF to 0x00 within approximately 1 second. Countdown will stop and WKUPACK will statically report 0x00 after wake up confirmation.



Note: When operating on top of a daisy chain, more than one dummy byte has to be send every time the isoSPI chain has to be woken up. See also 'Waking a Daisy Chain' chapters in latest cell monitor datasheets (e.g. LTC6812) for recommended procedures.

Figure 20a. Flow Chart of Recommended Wake-Up Procedure and Example SPI Transactions for Direct and Indirect Read Scenarios

REGISTER DESCRIPTION

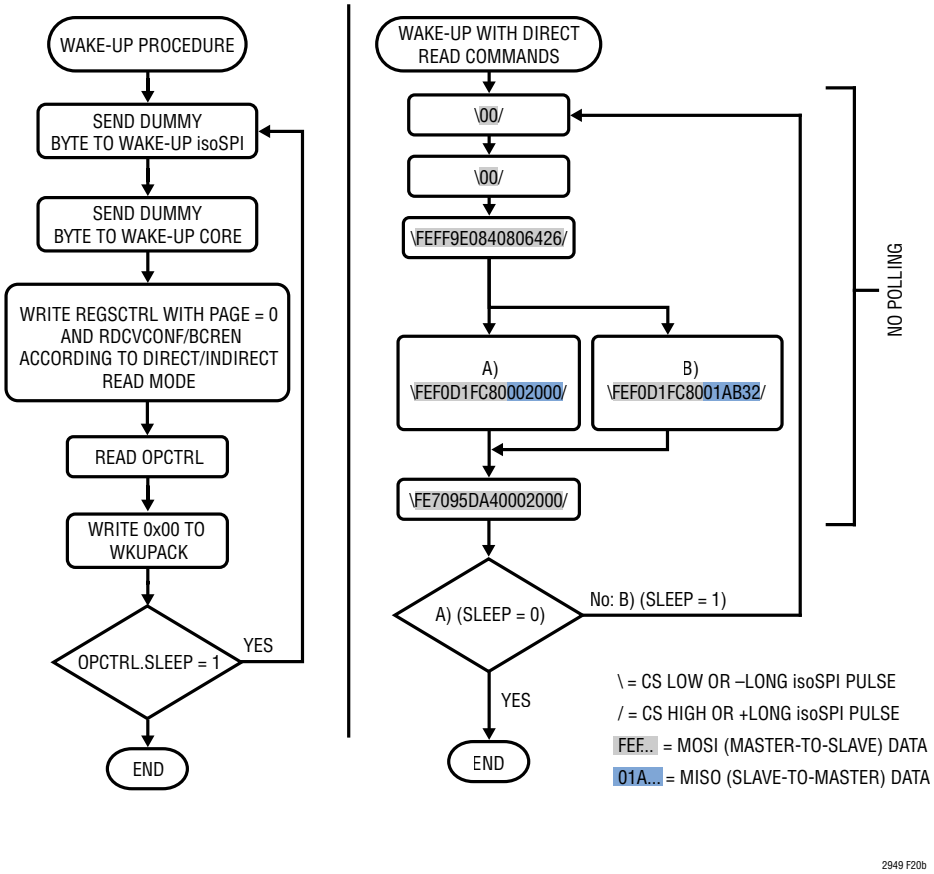


Figure 20b. Flow Chart of Recommended Wake-Up Procedure Implemented in a Sequence Without Polling

REGISTER DESCRIPTION

Table 25. Wake Up Acknowledge Register (0x70)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[7:0]	WKUPACK	RW	see above	0x00: Wake up is confirmed. Part will not return to SLEEP. Anything else: Wake up is not confirmed. Part will return to SLEEP.

In applications where LTC2949 is connected on top of a daisychain, the bit BCREN in REGSCTRL must be set before being able to read from LTC2949. This is only possible after the boot sequence has finished. Polling of the SLEEP bit being cleared can still be implemented by interleaving the read of OPCTRL with a write to REGSCTRL with BCREN=1 (all other bits 0). As this scenario also implies indirect register reads via RDCV commands (for this reason RDCVCONF=0), the write to REGSCTRL can be done in a single four byte burst together with RDCVIADDR (set to 0xF0); the two bytes between RDCVIADDR and REGSCTRL set to 0x00. Thus the four bytes to be written are 0xF0,0x00,0x00,0x04 and the following RDCV command will report the content of OPCTRL. Still, if the boot sequence is not completed, LTC2949 will ignore the broadcast RDCV command and thus the master will read always 0xFF (which is also compatible with SLEEP=1), including PEC=0xFFFF if 8 bytes are read (its not necessary to read till the PEC in this case). After the boot OPCTRL will be read as 0x00.

Accumulated Result Registers

The registers in Table 26 and Table 27 contain the accumulated quantities Charge, Energy and Time. The Time registers are unsigned integer values while the Charge and Energy registers are two's complement signed integer values. The value of each accumulated quantity can be determined by multiplying the respective register value with the corresponding LSB value from Table 26 (if the internal clock or crystal is used as a reference clock) or Table 27 (if an external reference clock is used).

Table 26. Accumulated Results Register Parameters for Use with Crystal or Internal Clock

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	LSB (4MHz CRYSTAL OR INTERNAL CLOCK)	PRE (4MHz CRYSTAL)	DIV (4MHz CRYSTAL)	UNIT	SI/UI
0x00	C1[47:0]	RW	0x00	Charge1 = C1 • LSBC1	LSBC1 = 377.887e-12	2	30	Vs	SI
0x06	E1[47:0]	RW	0x00	Energy1 = E1 • LSBE1	LSBE1 = 2.32175e-09	2	30	V^2s	SI
0x0C	TB1[31:0]	RW	0x00	Time1 = TB1 • LSBTB1	LSBTB1 = 397.777E-06	2	30	s	UI
0x10	C2[47:0]	RW	0x00	Charge2 = C2 • LSBC2	LSBC2 = 377.887e-12	2	30	Vs	SI
0x16	E2[47:0]	RW	0x00	Energy2 = E2 • LSBE2	LSBE2 = 2.32175e-09	2	30	V^2s	SI
0x1C	TB2[31:0]	RW	0x00	Time2 = TB2 • LSBTB2	LSBTB2 = 397.777E-06	2	30	s	UI
0x24	C3[63:0]	RW	0x00	Charge3 = C3 • LSBC3	LSBC3 = 377.887e-12	2	30	Vs	SI
0x2C	TB3[31:0]	RW	0x00	Time3 = TB3 • LSBTB3	LSBTB3 = 397.777E-06	2	30	s	UI
0x34	E4[63:0]	RW	0x00	Energy4 = E4 • LSBE4	LSBE4 = 2.32175e-09	2	30	V^2s	SI
0x3C	TB4[31:0]	RW	0x00	Time4 = TB4 • LSBTB4	LSBTB4 = 397.777E-06	2	30	s	UI

Charge1, Energy1 and Time1 contain accumulated quantities of Channel1. Charge2, Energy2 and Time2 contain accumulated quantities of Channel2. Charge3 and Time3 contain the weighted sum of charges monitored by Channel1 and Channel2 and the corresponding time. Similarly Energy4 and Time4 contain the weighted sum of energies monitored by Channel1 and Channel2 and the corresponding time.

If different sense resistors are used on CH1 and CH2, the LTC2949 uses the ratio of the sense resistors (RSRATIO) set in the Gain Configuration Registers to compute the correct weighted sums Charge3 and Energy4.

When the internal clock is used, PRE and DIV should be set to their default values which is done by writing 0x07 to register (0xE9), otherwise the values of PRE(0xE9)[2:0] and DIV(0xE9)[7:3] should be set according to section Timebase Control.

REGISTER DESCRIPTION

Table 27. Accumulated Results Register Parameters for Use with External Clock

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	LSB	UNIT	SI/UI
0x00	C1[47:0]	RW	0x00	Charge1 = C1 • LSBC1	LSBC1 = 1.21899e–5 • 1/fext • 2^{PRE} • (DIV+1)	Vs	SI
0x06	E1[47:0]	RW	0x00	Energy1 = E1 • LSBE1	LSBE1 = 7.4895e–5 • 1/fext • 2^{PRE} • (DIV+1)	V^2s	SI
0x0C	TB1[31:0]	RW	0x00	Time1 = TB1 • LSBTB1	LSBTB1 = 12.8315 • 1/fext • 2^{PRE} • (DIV+1)	s	UI
0x10	C2[47:0]	RW	0x00	Charge2 = C2 • LSBC2	LSBC2 = 1.21899e–5 • 1/fext • 2^{PRE} • (DIV+1)	Vs	SI
0x16	E2[47:0]	RW	0x00	Energy2 = E2 • LSBE2	LSBE2 = 7.4895e–5 • 1/fext • 2^{PRE} • (DIV+1)	V^2s	SI
0x1C	TB2[31:0]	RW	0x00	Time2 = TB2 • LSBTB2	LSBTB2 = 12.8315 • 1/fext • 2^{PRE} • (DIV+1)	s	UI
0x24	C3[63:0]	RW	0x00	Charge3 = C3 • LSBC3	LSBC3 = 1.21899e–5 • 1/fext • 2^{PRE} • (DIV+1)	Vs	SI
0x2C	TB3[31:0]	RW	0x00	Time3 = TB3 • LSBTB3	LSBTB3 = 12.8315 • 1/fext • 2^{PRE} • (DIV+1)	s	UI
0x34	E4[63:0]	RW	0x00	Energy4 = E4 • LSBE4	LSBE4 = 7.4895e–5 • 1/fext • 2^{PRE} • (DIV+1)	V^2s	SI
0x3C	TB4[31:0]	RW	0x00	Time4 = TB4 • LSBTB4	LSBTB4 = 12.8315 • 1/fext • 2^{PRE} • (DIV+1)	s	UI

Note: Values of PRE and DIV should be calculated according to Timebase Control section.

For instance, an external clock frequency of 10MHz would require values PRE to be set to 4 and DIV to be set to 19. With f_{EXT}=10MHz, LSBC1 is calculated as 390.078e-12 VS. To get the Charge1 value, the register content of C1 is multiplied with LSBC1. In this case, a C1 register value of 0x 75 5A 10 or 7690768 and the resulting Charge1 is 0.003 VS. For a sense resistor of 300µΩ this corresponds to 10As.

LSB values may be calculated easily using the Quick Eval software for the LTC2949 or by using the C/C++ header files provided in the code section of the LTC2949 (see LTC2949 evaluation board DC2732A manual for details). The registers for Charge, Energy and Time can be preset to a non-zero initial value. In Continuous Mode all bytes of the respective quantity must be written in the same multi-byte transaction or while the memory is locked.

Non-Accumulated Result Registers

Registers in Table 28 contain measured values of Currents, Powers, Voltages, Temperatures, VCC and VREF. All quantities are represented as two's complement signed integer values.

Current 1 represents the differential voltage sensed between CF1P and CF1M. Current 2 represents the differential voltage sensed between CF2P and CF2M. Battery voltage (BAT) is the differential voltage across pins VBATP and VBATM. Power 1 is the instantaneous multiplication of BAT and current 1. Power 2 is the instantaneous multiplication of BAT and current 2. Temperature is the temperature of the on-silicon temperature sensor. VCC is the voltage across pins A/DVCC and AGND. Registers SLOT1 and SLOT2 contain the results of the two multiplexer inputs choosen according to Table 58 and can be configured to give out voltage or temperature by means of the NTC Configuration Registers (Table 70). VREF is the voltage across pins VREF and AGND. The moving average of the four preceding current measurements are stored in I1AVG and I2AVG. The values of these four current measurements are retained in the Current History registers; Current 1 History 1 is the result prior to Current 1, Current 1 History 2 is the current result prior to Current 1 History 1, and so on. All measured values are scaled with the LSB values from . To calculate the physical value of the measured parameter, multiply the register value by the appropriate LSB value.

Table 28. Non-Accumulated Results Register Parameters

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	LSB	UNIT	SI/UI
0x90	I1[23:0]	RO	0x00	Current 1	950	nV	SI
0x93	P1[23:0]	RO	0x00	Power 1 (Power, P1ASV =0)	5.8368	µ[V^2]	SI
				Power 1 (Voltage, P1ASV=1)	46.875	µV	SI
0x96	I2[23:0]	RO	0x00	Current 2	950	nV	SI

REGISTER DESCRIPTION

Table 28. Non-Accumulated Results Register Parameters (continued)

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	LSB	UNIT	SI/UI
0x99	P2[23:0]	RO	0x00	Power 2 (Power, P2ASV =0)	5.8368	µ[V^2]	SI
				Power 2 (Voltage, P2ASV=1)	46.875	µV	SI
0x9C	I1AVG[23:0]	RO	0x00	Current 1 Moving Average	237.5	nV	SI
0xA0	BAT[15:0]	RO	0x00	Battery Voltage	375	µV	SI
0xA2	TEMP [15:0]	RO	0x00	Temperature	0.2	°C	SI
0xA4	VCC[15:0]	RO	0x00	Voltage at A/DVCC	2.26	mV	SI
0xA6	SLOT1[15:0]	RO	0x00	SLOT 1 (Voltage)	375	µV	SI
				SLOT 1 (Temp.)	0.2	°C	SI
0xA8	SLOT2[15:0]	RO	0x00	SLOT 2 (Voltage)	375	µV	SI
				SLOT 2 (Temp)	0.2	°C	SI
0xAA	VREF[15:0]	RO	0x00	Voltage at VREF	375	µV	SI
0xAC	I2AVG[23:0]	RO	0x00	Current 2 Moving Average	237.5	nV	SI
0xB3	I1H1[23:0]	RO	0x00	Current 1 History 1	950	nV	SI
0xB6	I1H2[23:0]	RO	0x00	Current 1 History 2	950	nV	SI
0xB9	I1H3[23:0]	RO	0x00	Current 1 History 3	950	nV	SI
0xBC	I1H4[23:0]	RO	0x00	Current 1 History 4	950	nV	SI
0xC3	I2H1[23:0]	RO	0x00	Current 2 History 1	950	nV	SI
0xC6	I2H2[23:0]	RO	0x00	Current 2 History 2	950	nV	SI
0xC9	I2H3[23:0]	RO	0x00	Current 2 History 3	950	nV	SI
0xCC	I2H4[23:0]	RO	0x00	Current 2 History 4	950	nV	SI
0xF7	FIFOI1[15:0]	RO	0x00	Fast Current 1	7.60371	µV	SI
0xF8	FIFOI2[15:0]	RO	0x00	Fast Current 2	7.60371	µV	SI
0xF9	FIFOBAT[15:0]	RO	0x00	Fast Battery Voltage	375.183	µV	SI
0xFA	FIFOAUX[15:0]	RO	0x00	Fast AUX HVMUX	375.183	µV	SI

The FIFO registers 0xF7 to 0xFA allow to read conversion results in fast continuous mode. When reading from those registers, the internal address auto-increment stops, allowing to read any number of bytes the fixed addresses. For each sample, three bytes have to be read which are MSB, LSB and TAG, see also fast mode section and below description for more details.

In Fast Mode, ADC conversion results turn negative when exceeding positive and clip when exceeding negative full-scale values. In Slow Modes, ADC conversion results clip when exceeding positive and negative full-scale values. Full-scale values are always beyond the specified input range.

Registers I1AVG (0x9C) and I2AVG (0xAC) are copied to registers 0xB0 and 0xC0, respectively. Thus, 0x9C-0x9E will report the same values as 0xB0-0xB2 and 0xAC-0xAE will report the same values as 0xC0-0xC2.

REGISTER DESCRIPTION

Table 29. FIFO Register Read Format.

DATA BYTE	NAME	DESCRIPTION
0	S_N[15:8]	MSB of measured sample N
1	S_N[7:0]	LSB of measured sample N
2	TAG_N	Tag of sample N
3	S_{N+1}[15:8]	MSB of measured sample N+1
4	S_{N+1}[7:0]	LSB of measured sample N+1
5	TAG_{N+1}	Tag of sample N+1
…	…	…
3*M	S_{N+M}[15:8]	MSB of measured sample N+M
3*M+1	S_{N+M}[7:0]	LSB of measured sample N+M
3*M+2	TAG_{N+M}	Tag of sample N+M

The column Data Byte does not count the PEC bytes, which depend on the setting of data bytes per PEC (ID-byte for DCMD or fixed to six for RDCV). For maximum data throughput it is recommended to read the FIFOs with DCMDs with 16 bytes per PEC and multiples of 16 samples (= 48 data bytes + 3 • 2 PEC bytes).

Table 30. FIFO TAG Definitions.

TAG	NAME	DESCRIPTION
0x00	OK	Valid, new sample
0x55	RDOVR	Read overrun, sample was already read
0xAA	WROVR	Write overrun, FIFO was filled completely and at least one sample was already overwritten

It is recommended to connect LTC2949 always in parallel to a daisy chain. Also, in the scenario where LTC2949 is connected at one end of a reversible isoSPI chain, the default communication should be done with direct read commands. Only in case the direct isoSPI link to LTC2949 fails, the communication would be routed through the daisy chain.

In this configuration where LTC2949 is on top of a daisy chain, after the broadcast RDCV command, the stacked LTC68xx Cell Monitors turn into a cascaded shift register, in which data is shifted through each device to the next device in the stack. In this scenario, at the end of the read transaction, there is always a fixed number of samples stuck in the shift register, that is never transmitted to the master.

Several approaches are possible to avoid or minimize the loss of samples. Either fast continuous mode is stopped (FACONV=0), the FIFO is read until empty and then fast continuous measurement is repeated (FACONV=1). This results in a time window without measurements, equal to the time it takes to read the samples. For example, at 1Mbit/s serial clock rate, it takes 0.8 ms (approximately one fast conversion time) to read 24 samples (four byte command and PEC, 72 data bytes, 24 data PEC bytes equals in total 100 bytes or 800 bits). For lower clock speeds or longer cycle times, where more samples are read per cycle, the following approach is more efficient.

Alternatively, the FIFO read burst must be long enough to always empty the FIFO and read at least one sample with TAG RDOVR. Still, also here, one sample with TAG OK can arrive after the RDOVR and would then be stuck in the daisy chain's shift register. If the latency of the shift register (number of devices in the daisy chain times eight bytes times eight bit per byte divided by SPI clock speed) is longer than one fast conversion time, even more than one sample can get stuck in the daisy chain.

REGISTER DESCRIPTION

Tracking Registers

The tracking registers keep track of the maximum and minimum values of previous conversions since the last reset. Value scaling is done in the same manner as the non-accumulated register values, using LSB values from Table 31. Negative values are treated as smaller (more minimum) than positive values as the minimum registers are updated.

For example: A register value I1MAX(0x40,0x41) of 0000 0001 1111 0100b = 01 F4h = 500d indicates a resulting maximum sense resistor signal of 500 • 3.8µV = 1.9mV. A register value I1MIN(0x42,0x43) of 1111 1010 0010 0100b = FA 24h = –1500d indicates a minimum sense resistor signal of –1500 • 3.8µV = –5.7mV. The calculation of the other tracked parameter values is done the same way with their corresponding LSB values.

Table 31. Tracking Registers

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	LSB	UNIT	SI/UI
0x40	I1MAX[15:0]	RW	0x8000	Max I1 Current	3.8	µV	SI
0x48	I2MAX[15:0]	RW	0x8000	Max I2 Current	3.8	µV	SI
0x42	I1MIN[15:0]	RW	0x7FFF	Min I1 Current	3.8	µV	SI
0x4A	I2MIN[15:0]	RW	0x7FFF	Min I2 Current	3.8	µV	SI
0x44	P1MAX[15:0]	RW	0x8000	Max Power 1 (or Battery Voltage for P1ASV=1)	23.347 (187.5)	µ[V^2] (µV)	SI
0x4C	P2MAX[15:0]	RW	0x8000	Max Power 2 (or Battery Voltage for P2ASV=1)	23.347 (187.5)	µ[V^2] (µV)	SI
0x46	P1MIN[15:0]	RW	0x7FFF	Min Power 1 (or Battery Voltage for P1ASV=1)	23.347 (187.5)	µ[V^2] (µV)	SI
0x4E	P2MIN[15:0]	RW	0x7FFF	Min Power 2 (or Battery Voltage for P2ASV=1)	23.347 (187.5)	µ[V^2] (µV)	SI
0x50	BATMAX[15:0]	RW	0x8000	Max Battery Voltage	375	µV	SI
0x52	BATMIN[15:0]	RW	0x7FFF	Min Battery Voltage	375	µV	SI
0x54	TEMPMAX[15:0]	RW	0x8000	Max Temperature	0.2	°C	SI
0x56	TEMPMIN[15:0]	RW	0x7FFF	Min Temperature	0.2	°C	SI
0x58	VCCMAX[15:0]	RW	0x8000	Max Voltage at A/DVCC	2.26	mV	SI
0x5A	VCCMIN[15:0]	RW	0x7FFF	Min Voltage at A/DVCC	2.26	mV	SI
0x5C	SLOT1MAX[15:0]	RW	0x8000	Max Voltage (or Temperature) at SLOT1	375 (0.2)	µV (°C)	SI
0x5E	SLOT1MIN[15:0]	RW	0x7FFF	Min Voltage (or Temperature) at SLOT1	375 (0.2)	µV (°C)	SI
0x60	SLOT2MAX[15:0]	RW	0x8000	Max Voltage (or Temperature) at SLOT2	375 (0.2)	µV (°C)	SI
0x62	SLOT2MIN[15:0]	RW	0x7FFF	Min Voltage (or Temperature) at SLOT2	375 (0.2)	µV (°C)	SI

Note that the tracking registers for current and power report only the 16MSBs of the respective 18-bit result registers, leading to a four times larger LSB value.

STATUS, (EXT)FAULTS, Threshold and Overflow Alert Registers

The registers described in the following chapters are used to signal certain events, like a voltage threshold violation, charger or energy overflow, supply undervoltage events and others. After power-up it is recommended to lock the memory, read STATUS, FAULTS and EXTFAULTS registers, check for the default values, clear them and finally unlock the memory. During normal operation those registers shall be checked periodically to be all zero, except for the UPDATE bit. Any other value indicates a failure.

Any bits in the STATUS, alerts (0x81-0x87), FAULTS and EXTFAULTS registers are only set to 1 by LTC2949 in case of an event, but never cleared automatically. After the master reads some bits being set, actions should be taken (e.g. to clear the charge register in case of a charge overflow), the memory must be locked (see REGSCTRL), the registers

should be read again as other events may have occurred in the meantime, registers that or not 0x00 must be written to 0x00 and finally the memory must be unlocked to proceed with normal operation.

It is not recommended to write those registers without usage of the memory lock, as this may lead to loss of failure and alert reports.

Status and Fault Registers

The STATUS register reports the status of register updates, undervoltage lockout, and reference clock errors. On power up, all undervoltage lockouts and the power-on reset are set to 1. After exit from shutdown, bits UVLOA and UVLOD are set. UPDATE is set to 1 when the LTC2949 has finished a measurement cycle and updated the result registers, the accumulation registers, and the tracking registers.

ADCERR is set to 1 if the supply voltage at AVCC is too low for a proper operation of the ADCs. The values in the result registers are not valid and should be discarded if ADCERR is set. TBERR is set to 1 if the internal time base overflows. This indicates an incorrect setting of the values PRE and DIV with respect to the external clock at CLKI. The values of accumulated results registers should be discarded if TBERR is set.

Table 32. STATUS (0x80)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	UVLOA	RW	1	1: Undervoltage in the analog domain or ADCs during a conversion
1	PORA	RW	1	1: Power-on reset has occurred due to undervoltage in the analog domain
2	UVLOSTBY	RW	1	1: Undervoltage in the standby domain
3	UVLOD	RW	1	1: Undervoltage in the digital domain
4	UPDATE	RW	0	1: Result registers have been updated
5	ADCERR	RW	0	1: The ADC conversion is not valid due to undervoltage during a conversion
6	TBERR	RW	0	1: Overflow of the internal timebase register. The values of accumulated result registers are invalid

LTC2949 has several types of internal memory that are checked during boot-up via built-in self-test (BIST) routines. Errors in individual blocks are reported by the EXTFAULTS and FAULTS registers. The FAULTS register additionally reports error in the internal (on-chip) and external (from master to slave on the SPI/isoSPI interface) communication and indicates thermal shutdown and fast channel error events.

Table 33. EXTFAULTS (0xDC)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	HD1BITERR	RW	0	1: Hamming decoder 1-bit error
1	ROMERR	RW	0	1: ROM CRC error
2	MEMERR	RW	0	1: Memory error
3	FCAERR	RW	0	1: Fast channel error
4	XRAMERR	RW	0	1: XRAM error
5	IRAMERR	RW	0	1: IRAM error
7	HWMBISTEXEC	RW	1	1: Memory BIST was executed. If SDA is externally pulled low during power-up, the memory BIST will be skipped and this bit will be zero. Connect a 4.7k-10k pull-up resistor from SDA to BYP1 to ensure correct operation of memory BIST.

REGISTER DESCRIPTION

Table 34. FAULTS (0xDD)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	PROMERR	RW	0	1: Error in trim values stored in internal PROM
1	TSD	RW	0	1: Shutdown due to over temperature
2	INTCOMMERR	RW	0	1: Parity check of internal communication failed
3	EXTCOMMERR	RW	0	1: PEC error in external communication (SPI/isoSPI) occurred
4	FAERR	RW	0	1: Fast mode error, see Safety Manual for more information
5	HWBIST	RW	0	1: Error during hardware BIST.
6	CRCCFG	RW	0	1: Internal RAM gain coefficient CRC Error
7	CRCMEM	RW	0	1: User accessible register CRC Error

Threshold and Overflow Alert Registers

Threshold and overflow alert registers are set when the respective threshold values are exceeded or when registers overflow. Thresholds are set in the Threshold Registers section.

The accumulated quantities are continuously checked against guard values to warn that a register is nearing overflow, nominally set to 90% of each register's maximum value. When any quantity crosses its guard threshold, the LTC2949 sets the corresponding overflow bit in the status register, generates an alert (if enabled) and continues accumulation. At the maximum voltage inputs, rollover typically happens several hours after an overflow alert is signaled, allowing the host time to take action to avoid data loss, by reading and clearing the concerned accumulators using the memory locking procedure. The overflow thresholds for 32-bit quantities (time) are 3865470565 LSB; for 48-bit quantities (charge and energy) is ±126663739519794 LSB.

The threshold and overflow comparators for accumulated quantities charge, energy and time use a floating point format internally. This can appear to cause slight bit-level comparison discrepancies, but the comparisons between accumulated result registers and their respective threshold registers will always have an accuracy of better than 0.001%.

An alert condition needs to be present for at least for 200ms to be reported by the alert registers (0x81-0x87). Only overcurrent conditions detected by either OCC1 or OCC2 can be signaled to the host within some µs by stopping heart beat on GPIO5.

To acknowledge and release an overcurrent alert the following steps can be performed:

1. Stop the overcurrent event
2. Lock the memory
3. Read STATUS-STATVCC, (EXT)FAULTS for any newly arrived error flags (including the asserted OCCx bits)
4. Clear STATUS-STATVCC, (EXT)FAULTS
5. Unlock the memory
6. Heartbeat on GPIO5 will start again

REGISTER DESCRIPTION

Table 35. Voltage, Temperature Threshold Alerts STATVT (0x81)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	BATH	RW	0	1: Voltage (VBATP – VBATM) high threshold exceeded
1	BATL	RW	0	1: Voltage (VBATP – VBATM) low threshold exceeded
2	TEMPH	RW	0	1: Temperature high threshold exceeded
3	TEMPL	RW	0	1: Temperature low threshold exceeded
4	SLOT1H	RW	0	1: SLOT1 high threshold exceeded
5	SLOT1L	RW	0	1: SLOT1 low threshold exceeded
6	SLOT2H	RW	0	1: SLOT2 high threshold exceeded
7	SLOT2L	RW	0	1: SLOT2 low threshold exceeded

Table 36. Current, Power Threshold Alerts STATIP (0x82)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	I1H	RW	0	1: Current1 high threshold exceeded
1	I1L	RW	0	1: Current1 low threshold exceeded
2	P1H	RW	0	1: Power1 high threshold exceeded
3	P1L	RW	0	1: Power1 low threshold exceeded
4	I2H	RW	0	1: Current2 high threshold exceeded
5	I2L	RW	0	1: Current2 low threshold exceeded
6	P2H	RW	0	1: Power2 high threshold exceeded
7	P2L	RW	0	1: Power2 low threshold exceeded

Table 37. Charge Threshold Alerts STATC (0x83)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	C1H	RW	0	1: Charge1 high threshold exceeded
1	C1L	RW	0	1: Charge1 low threshold exceeded
2	C2H	RW	0	1: Charge2 high threshold exceeded
3	C2L	RW	0	1: Charge2 low threshold exceeded
4	C3H	RW	0	1: Charge3 high threshold exceeded
5	C3L	RW	0	1: Charge3 low threshold exceeded

Table 38. Energy Threshold Alerts STATE (0x84)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	E1H	RW	0	1: Energy1 high threshold exceeded
1	E1L	RW	0	1: Energy1 low threshold exceeded
2	E2H	RW	0	1: Energy2 high threshold exceeded
3	E2L	RW	0	1: Energy2 low threshold exceeded
6	E4H	RW	0	1: Energy4 high threshold exceeded
7	E4L	RW	0	1: Energy4 low threshold exceeded

Table 39. Charge, Energy Overflow Alerts STATCEOF (0x85)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	C1OVF	RW	0	1: Charge1 overflow alert
1	C2OVF	RW	0	1: Charge2 overflow alert
2	C3OVF	RW	0	1: Charge3 overflow alert
4	E1OVF	RW	0	1: Energy1 overflow alert
5	E2OVF	RW	0	1: Energy2 overflow alert
7	E4OVF	RW	0	1: Energy4 overflow alert

REGISTER DESCRIPTION

Table 40. Time Base Alerts STATTB (0x86)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	T1TH	RW	0	1: Time1 threshold exceeded
1	T2TH	RW	0	1: Time2 threshold exceeded
2	T3TH	RW	0	1: Time3 threshold exceeded
3	T4TH	RW	0	1: Time4 threshold exceeded
4	T1OVF	RW	0	1: Time1 overflow
5	T2OVF	RW	0	1: Time2 overflow
6	T3OVF	RW	0	1: Time3 overflow
7	T4OVF	RW	0	1: Time4 overflow

Table 41. VCCOCC Threshold Alerts STATVCC (0x87)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	VCCH	RW	0	1: VCC high threshold exceeded
1	VCCL	RW	0	1: VCC low threshold exceeded
2	OCC1H	RW	0	1: Current1 above OCC1 threshold for more than deglitch time
3	OCC2H	RW	0	1: Current2 above OCC2 threshold for more than deglitch time

Note: The memory must be locked to clear status (0x80), faults (0xDC-0xDD) and alert (0x81-0x87) registers to avoid missing of any failure and alert reports. See REGSCTRL description for details.

Mask Registers

The mask registers control which alerts stop heartbeat. If a mask register bit is reset to 0, exceeding of the respective threshold causes the heartbeat on GPIO4 pin to stop, if the latter is configured accordingly in the GPIO4HBCTRL register.

When a bit of the Status Mask Register (STATUSM) is set to 0, the corresponding bits of register STATUS (0x80) will stop heartbeat. When a bit of the status mask register is set to 1, heartbeat is unaffected by the corresponding bits of register STATUS (0x80).

Table 42. Status Mask STATUSM (0x88)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	UVLOAM	RW	1	Mask UVLOA of STATUS(0x80)
3	UVLODM	RW	1	Mask UVLOD of STATUS(0x80)
4	UPDATEM	RW	1	Mask UPDATE of STATUS(0x80)
5	ADCERRM	RW	1	Mask ADCERR of STATUS(0x80)
6	TBCERRM	RW	1	Mask TBCERR of STATUS(0x80)

When bits of STATVTM are set to 0, corresponding bits of register STATVT (0x81) will stop heartbeat. When a bit of STATVTM is set to 1, heartbeat is unaffected by the corresponding bits of register STATVT (0x81).

Table 43. Voltage, Temperature Threshold Alert Mask STATVTM (0x89)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	BATHM	RW	1	Mask BATH of STATVT(0x81)
1	BATLM	RW	1	Mask BATL of STATVT(0x81)
2	TEMPHM	RW	1	Mask TEMPH of STATVT(0x81)
3	TEMPLM	RW	1	Mask TEMPL of STATVT(0x81)
4	SLOT1HM	RW	1	Mask SLOT1H of STATVT(0x81)
5	SLOT1LM	RW	1	Mask SLOT1L of STATVT(0x81)
6	SLOT2HM	RW	1	Mask SLOT2H of STATVT(0x81)
7	SLOT2LM	RW	1	Mask SLOT2L of STATVT(0x81)

REGISTER DESCRIPTION

When bits from STATIPM are set to 0, bits from register STATIP(0x82) will stop heartbeat. When a bit of STATIPM register is set to 1, heartbeat is unaffected by the corresponding bits of register STATIP(0x82).

Table 44. Current, Power Threshold Alert Mask STATIPM (0x8A)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	I1HM	RW	1	Mask I1H of STATIP (0x82)
1	I1LM	RW	1	Mask I1L of STATIP (0x82)
2	P1HM	RW	1	Mask P1H of STATIP (0x82)
3	P1LM	RW	1	Mask P1L of STATIP (0x82)
4	I2HM	RW	1	Mask I2H of STATIP (0x82)
5	I2LM	RW	1	Mask I2L of STATIP (0x82)
6	P2HM	RW	1	Mask P2H of STATIP (0x82)
7	P2LM	RW	1	Mask P2L of STATIP (0x82)

When bits from STATCM are set to 0, bits from register STATC(0x83) will stop heartbeat. When a bit of STATCM register is set to 1, heartbeat is unaffected by the corresponding bits of register STATC(0x83).

Table 45. Charge Threshold Alerts Mask STATCM (0x8B)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	C1HM	RW	1	Mask C1H of STATC (0x83)
1	C1LM	RW	1	Mask C1L of STATC (0x83)
2	C2HM	RW	1	Mask C2H of STATC (0x83)
3	C2LM	RW	1	Mask C2L of STATC (0x83)
4	C3HM	RW	1	Mask C3H of STATC (0x83)
5	C3LM	RW	1	Mask C3L of STATC (0x83)

When bits from STATEM are set to 0, bits from register STATE(0x84) will stop heartbeat. When a bit of STATEM register is set to 1, heartbeat is unaffected by the corresponding bits of register STATE(0x84).

Table 46. Energy Threshold Alerts Mask STATEM (0x8C)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	E1HM	RW	1	Mask E1H of STATE (0x84)
1	E1LM	RW	1	Mask E1L of STATE (0x84)
2	E2HM	RW	1	Mask E2H of STATE (0x84)
3	E2LM	RW	1	Mask E2L of STATE (0x84)
6	E4HM	RW	1	Mask E4H of STATE (0x84)
7	E4LM	RW	1	Mask E4L of STATE (0x84)

When bits from STATCEOFM are set to 0, bits from register STATCEOF(0x85) will stop heartbeat. When a bit of STATCEOFM register is set to 1, heartbeat is unaffected by the corresponding bits of register STATCEOF(0x85).

Table 47. Charge, Energy Overflow Alerts Mask STATCEOFM (0x8D)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	C1OFM	RW	1	Mask C1OVF of STATCEOF(0x85)
1	C2OFM	RW	1	Mask C2OVF of STATCEOF(0x85)
2	C3OFM	RW	1	Mask C3OVF of STATCEOF(0x85)
4	E1OFM	RW	1	Mask E1OVF of STATCEOF(0x85)
5	E2OFM	RW	1	Mask E2OVF of STATCEOF(0x85)
7	E4OFM	RW	1	Mask E4OVF of STATCEOF(0x85)

REGISTER DESCRIPTION

When bits from STATTBM are set to 0, bits from register STATTB (0x86) will stop heartbeat. When a bit of STATTBM register is set to 1, heartbeat is unaffected by the corresponding bits of register STATTB (0x86).

Table 48. Time Base Alerts STATTBM (0x8E)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	T1THM	RW	1	Mask T1TH of STATTB(0x86)
1	T2THM	RW	1	Mask T2TH of STATTB(0x86)
2	T3THM	RW	1	Mask T3TH of STATTB(0x86)
3	T4THM	RW	1	Mask T4TH of STATTB(0x86)
4	T1OFM	RW	1	Mask T1OVF of STATTB(0x86)
5	T2OFM	RW	1	Mask T2OVF of STATTB(0x86)
6	T3OFM	RW	1	Mask T3OVF of STATTB(0x86)
7	T4OFM	RW	1	Mask T4OVF of STATTB(0x86)

When bits from STATVCCM are set to 0, bits from register STATVCC (0x87) will stop heartbeat. When a bit of STATVCCM register is set to 1, heartbeat is unaffected by the corresponding bits of register STATVCC (0x87).

Table 49. V_{CC} Threshold Alerts STATVCCM (0x8F)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	VCCH	RW	1	Mask VCCH of STATVCC (0x87)
1	VCCL	RW	1	Mask VCCL of STATVCC (0x87)

Note that the bits reporting the result of the overcurrent comparators OCC1 and OCC2 in STATVCC (0x87) do not have a corresponding mask bit in STATVCCM. Therefore the impact of OCC1 and OCC2 on heartbeat either on GPIO4 or GPIO5 cannot be masked. If overcurrent comparison is not desired the enable bit in OCCxCTRL has to be cleared (default).

Control Registers

The control registers select the multiplexer input, control the accumulation of charge, energy and time, configure the GPIO pins, set the overcurrent comparator thresholds, and setup the timebase if an external clock is used.

The Overcurrent Control Registers allow to set the overcurrent comparator thresholds and deglitch filters, see also the Overcurrent Comparators section.

Table 50. OCC1CTRL (0xDE)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	OCC1EN	RW	0	OCC1 enable bit. GPIO5 is configured as heartbeat
[3:1]	OCC1DAC [2:0]	RW	000	OCC1 threshold setting bits, see Table 6 (OCC Thresholds)
[5:4]	OCC1DGLT [1:0]	RW	00	OCC1 deglitch time setting bits, see Table 7 (OCC Deglitch Time)
[7:6]	OCC1POL [1:0]	RW	00	OCC1 polarity setting bits, see Table 5 (OCC Polarity Configuration)

Table 51. OCC2CTRL (0xDF)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	OCC2EN	RW	0	OCC2 enable bit. GPIO5 is configured as heartbeat
[3:1]	OCC2DAC [2:0]	RW	000	OCC2 threshold setting bits, see Table 6 (OCC Thresholds)
[5:4]	OCC2DGLT [1:0]	RW	00	OCC2 deglitch time setting bits, see Table 7 (OCC Deglitch Time)
[7:6]	OCC2POL [1:0]	RW	00	OCC2 polarity setting bits, see Table 5 (OCC Polarity Configuration)

REGISTER DESCRIPTION

The Accumulator Control and Deadband Registers allow to control the accumulation of Charge1, Energy1, Charge2, Energy2, Charge3 and Energy4 (C1, E1, C2, E2, C3, E4). Accumulation can be enabled, disabled or conditionally enabled based on the sign and absolute value of a measured current. C1 contains accumulated I1, C2 contains accumulated I2, E1 contains accumulated P1 and E2 contains accumulated P2. C3 contains the accumulated sum of I1 and I2 weighted by the gain setting parameters (see Gain Configuration Registers section) and E4 the accumulated weighted sum of P1 and P2.

For example, by setting bit 0 of the ACCCTRL1 and bit 1 of ACCCTRL2, C1 contains the accumulation of positive currents I1 and C3 contains the accumulation of negative currents.

Table 52. Accumulator Control ACCCTRL1(0xE1)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[1:0]	ACC1I1[1:0]	RW	00	Accumulation control of Charge1/Charge2 and Energy1/Energy2. 00: Accumulation takes place always, 01: Only if the current is positive, 10: Only if the current is negative, 11: No accumulation takes place.
[3:2]	ACC2I2[1:0]	RW	00	

Table 53. Accumulator Control ACCCTRL2(0xE2)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[1:0]	ACC3I1[1:0]	RW	00	Accumulation control of Charge3 and Energy4. 00: Accumulation takes place always, 01: Only if the current is positive, 10: Only if the current is negative, 11: No accumulation takes place.
[3:2]	ACC3I2[1:0]	RW	00	
[5:4]	ACC4I1[1:0]	RW	00	
[7:6]	ACC4I2[1:0]	RW	00	

Small offset voltages in the current measurement path lead to large charge errors after a long integration time. The accumulator dead band registers allow to set a minimum absolute value of I1 and I2 before being accumulated.

Table 54. Accumulation Dead Band ACCIDB1(0xE4)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[7:0]	ACCIDB1	RW	0x0	Current 1 deadband for accumulation. If the absolute value of I1 is higher than or equal this value, I1 and P1 are accumulated and C1, E1, C3, E4 are updated. A comparison to the respective thresholds takes place right after an update. If the absolute value of I1 is lower, I1 and P1 are not accumulated and C1 and E1 are not updated. Unit is the same as LSB of current I1(0x90).

Table 55. Accumulation Dead Band ACCIDB2(0xE5)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[7:0]	ACCIDB2	RW	0x0	Current 2 deadband for accumulation .If the absolute value of I2 is higher than or equal this value, I2 and P2 are accumulated and C2, E2, C3, E4 are updated. A comparison to the respective thresholds takes place right after an update. If the absolute value of I2 is lower, I2 and P2 are not accumulated and C2 and E2 are not updated. Unit is the same as LSB of current I2(0x96).

REGISTER DESCRIPTION

The Time Base Control Register selects between the internal and an external reference clock, and sets the time base parameters when an external reference clock is used. Set PRE[2:0] = 111b or 7d (default) to enable the internal reference clock. To use an external reference clock, set the values of PRE[2:0] and DIV[4:0] according to the external clock frequency; see the Timebase Control section for more information.

Table 56. Timebase Control TBCTRL (0xE9), DEFAULT VALUE: 0x07

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[2:0]	PRE [2:0]	RW	111	Prescaler value [2:0], binary coded, see Table 2. Parameter PRE with External Clock
[7:3]	DIV [4:0]	RW	00000	Divider value [4:0], binary coded, see Table 3

The multiplexer inputs are selected by the Multiplexer Control Registers. For each of the multiplexer outputs MUXP and MUXN, a 5-bit word selects the connected input.

Table 57. MUX Settings

MUXP/MUXN Setting		Selected Input
Binary [4:0]	Dec	
11XXX	31-24	Reserved
10111	23	VREF2 via 250k, see Safety Manual for more information
10110	22	VREF2
10101	21	Reserved
10100	20	CF1P
10011	19	CF1M
10010	18	CF2P
10001	17	CF2M
10000	16	VBATP
01111	15	VBATM
01110	14	IPT, see Safety Manual for more information
01101	13	IMT, see Safety Manual for more information
01100	12	V12
01011	11	V11
01010	10	V10
01001	9	V9
01000	8	V8
00111	7	V7
00110	6	V6
00101	5	V5
00100	4	V4
00011	3	V3
00010	2	V2
00001	1	V1
00000	0	AGND

REGISTER DESCRIPTION

In slow, high precision mode the auxiliary channel (CHAUX) converts in Round Robin mode two differential inputs signals. For each of the two slots, the inputs multiplexed to MUXP and MUXN can be chosen by programming the corresponding 5-bit setting in the following four registers.

In fast mode, the auxiliary channel (CHAUX) converts only one differential input signal, which can be chosen by choosing the corresponding 5-bit setting in the Fast MUXP and MUXN Control registers.

During fast continuous measurements it is not possible to change the AUX MUX configuration. See note in chapter 'Fast Measurement Timings'.

Table 58. Multiplexer Control Registers in Slow Mode

ADDR	BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0xEB	[4:0]	SLOT1MUXN [4:0]	RW	00000	Slot1 MUXN [4:0] setting, binary coded, see Table 57
0xEC	[4:0]	SLOT1MUXP [4:0]	RW	00000	Slot1 MUXP [4:0] setting, binary coded, see Table 57
0xED	[4:0]	SLOT2MUXN [4:0]	RW	00000	Slot2 MUXN [4:0] setting, binary coded, see Table 57
0xEE	[4:0]	SLOT2MUXP [4:0]	RW	00000	Slot2 MUXP [4:0] setting, binary coded, see Table 57

Table 59. Multiplexer Control Registers for Fast Mode

ADDR	BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0xF3	[4:0]	FAMUXN [4:0]	RW	00000	Fast Mode MUXN [4:0] setting, binary coded, see Table 57
0xF4	[4:0]	FAMUXP [4:0]	RW	00000	Fast Mode MUXP[4:0] setting, binary coded, see Table 57

The Fast Control Register allows to configure and trigger fast conversions.

There is a timing constraint when writing to FGPIOCTRL and FACTRL, see description for FGPIOCTRL.

Table 60. Fast Control Register FACTRL (0xF5)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	FACONV	RW	0	Continuous fast conversion enable (1) / disable (0). Conversion results are written to a FIFO if at least one of bits FACHA, FACH1, FACH2 is set.
1	FACHA	RW	0	Channel AUX fast mode configuration bit. Fast conversion starts within some us after rising edge of FACONV or when issuing the ADCV command.
2	FACH1	RW	0	Channel 1 fast mode configuration bit. Fast conversion starts within some us after rising edge of FACONV or when issuing the ADCV command.
3	FACH2	RW	0	Channel 2 fast mode configuration bit. Fast conversion starts within some us after rising edge of FACONV or when issuing the ADCV command.

REGISTER DESCRIPTION

The GPIO control registers allow to configure the GPIO pins to be either tristate, low, high or toggling at 400kHz by setting the corresponding GPIO CTRL bits in 0xF1 and 0xF2.

GPIO4 and GPIO5 can be used as heartbeat pins toggling with a frequency of 400kHz and become static low upon an alert. While GPIO5 is activated by enabling any of the overcurrent comparators and is dedicated to alerts issued by these comparators, GPIO4 can be configured by the GPIO4 heartbeat control register (0xE8) to respond on any alert not masked by the mask registers. The setting in the GPIO4 heartbeat control register overrules the GPIO4CTRL setting in 0xF2. Similarly GPIO5CTRL setting in 0xF1 is overruled by enabling the overcurrent comparators.

Table 61. GPIO4 Heartbeat Control GPIO4HBCTRL (0xE8)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	GPIO4HBEN	RW	0	GPIO4 heartbeat master enable control 0: GPIO4 is not configured as heart beat. 1: GPIO4 is configured as heart beat and unmasked alerts (see mask registers) stop heart beat of GPIO4

Table 62. Current Source and GPIO5 Control FCURGPIOCTRL (0xF1)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[1:0]	GPIO5CTRL [1:0]	RW	00	GPIO5 CTRL: [00]=Tristate [01]=LOW(DGND), [10]=Toggle at 400kHz [11] =HIGH(DVCC)
4	MUXPCURPOL	RW	0	0: MUXP sinks 250µA of current 1: MUXP sources 250µA of current
5	MUXPCUREN	RW	0	0: MUXP current source off 1: MUXP current source on
6	MUXNCURPOL	RW	0	0: MUXN sinks 250µA of current 1: MUXN sources 250µA of current
7	MUXNCUREN	RW	0	0: MUXN current source off 1: MUXN current source on

The 250µA current sources at MUXP and MUXN allow open wire detection at all multiplexer inputs. If enabled, the current sources connect to the inputs during the time the ADC is connected and performs the conversion, no matter if it is the fast or slow channel. Typically, open wire detection is performed using the fast channel by first writing current source, GPIO and MUX control (4-byte write to 0xF1-0xF4), triggering the fast conversion by sending the ADCV, reading the results with RDCV and finally by writing again 4 bytes to 0xF1-0xF4 to set the next MUX input and current source configuration. This way, the time when current sources are enabled on a dedicated pin, is precisely timed. See the safety manual for more information.

Enabled current source on MUXP will alter the internal measurement of VREF (~4V/~0.7V when MUXPCURPOL = 1 / 0) and this change won't be visible on the external VREF pin. If enabled, also the NTC temperature measurement and the compensation of a shunt resistor's temperature drift will be altered, as they depend on the internal VREF measurement. The correct VREF voltage can always be measured via an external connection to one Vx pin, see also section Unused Input Pins V1-V12.

REGISTER DESCRIPTION

Table 63. GPIO Control FGPIOCTRL (0xF2)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[1:0]	GPIO1CTRL [1:0]	RW	00	GPIO1-4 CTRL: [00]=Tristate [01]=LOW(DGND), [10]=Toggle at 400kHz [11] =HIGH(DVCC)
[3:2]	GPIO2CTRL [1:0]	RW	00	
[5:4]	GPIO3CTRL [1:0]	RW	00	
[7:6]	GPIO4CTRL [1:0]	RW	00	

If set to tristate, the GPIO pins can be used as analog inputs (V8-V12) to the auxiliary channel by choosing the corresponding multiplexer settings according to Table 57.

Write to register FCURGPIOCTRL does not take effect immediately. Instead any changes will only become active once FGPIOCTRL is written. Thus it is recommended to always write both registers in a single burst.

Additionally there is a timing constraint when writing to FGPIOCTRL and FACTRL. Writing to those registers must always be delayed by a minimum of 1ms. Thus, its not allowed to write FGPIOCTRL and FACTRL in a single burst. Usually this can be easily achieved by partitioning code sections properly that control those registers.

Table 64. RDCV Indirect Address (0xFC)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
[7:0]	RDCVIADDR	RW	0	Address pointer for indirect memory access via RDCV command, see section Indirectly Addressed RDCV Command

The following register is provided for software debug purposes only. It allows synchronization of the host controller to the CORE system tick. DBGCNT is reset by the CORE after the last register of memory page 0 was updated. This happens typically 23ms after the end of a slow mode current/power conversion (EOC of I1, I2, P1, P2).

Table 65. DBGCNT (0xD5)

SYMBOL	SI/UI	OPERATION
DBGCNT	UI	Debug counter, counts milliseconds, resets once per core cycle. In MEASURE mode it typically counts 0 to 100; in STANDBY mode it typically counts 0 to 17.

REGISTER DESCRIPTION

REGISTER MAP PAGE1

PAGE1 of the LTC2949 register map contains threshold and configuration registers. The threshold registers allow to set threshold values for each measured quantity. The configuration registers allow to store application and board specific parameters and settings, which usually do not need to be modified during operation.

Software Reset

The LTC2949 has a software reset feature, described in following table.

Table 66. RSTUNLCK (p1.0xA9)

SYMBOL	OPERATION
RSTUNLCK	Writing 0x55 to this register will unlock the RESET function within OPCTRL. After putting LTC2949 into SLEEP mode a writing command to OPCTR with the value 0x80 will issue the reset. Detailed steps to reset LTC2949 are: 1. Write 0 to OPCTRL (0xF0) 2. Write 0x55 to RSTUNLCK (0xA9 on page 1) 3. Wait 130ms 4. Go to SLEEP (set bit SLEEP in OPCTRL) 5. Wait 20ms 6. Write 0x80 to OPCTRL (0xF0)

Threshold Registers

The threshold registers set threshold values for each measured quantity. When a measured value exceeds its threshold, an alert is triggered and the corresponding bits in the threshold and overflow alert registers (0x81 to 0x87) are set. When GPIO4 heartbeat is enabled in register GPIO4HBCTRL (0xE8), unmasked alerts in registers (0x88 to 0x8F) stop heartbeat on GPIO4. Value scaling is done in the same manner as in the corresponding result register values, using LSB values from Table 26, Table 27 and Table 28. Non-Accumulated Results Register Parameters.

Table 67. Threshold Registers

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER
p1.0x00	C1TH[47:0]	RW	0x7FFF FFFF FFFF	Charge1 threshold high
p1.0x06	C1TL[47:0]	RW	0x8000 0000 0000	Charge1 threshold low
p1.0x0C	TB1TH[31:0]	RW	0xFFFF FFFF	Timebase1 threshold high
p1.0x10	E1TH[47:0]	RW	0x7FFF FFFF FFFF	Energy1 threshold high
p1.0x16	E1TL[47:0]	RW	0x8000 0000 0000	Energy1 threshold low
p1.0x20	C2TH[47:0]	RW	0x7FFF FFFF FFFF	Charge2 threshold high
p1.0x26	C2TL[47:0]	RW	0x8000 0000 0000	Charge2 threshold high
p1.0x2C	TB2TH[31:0]	RW	0xFFFF FFFF	Timebase2 threshold high
p1.0x30	E2TH[47:0]	RW	0x7FFF FFFF FFFF	Energy2 threshold high
p1.0x36	E2TL[47:0]	RW	0x8000 0000 0000	Energy2 threshold low
p1.0x44	C3TH[63:0]	RW	0x7FFF FFFF FFFF FFFF	Charge3 threshold high
p1.0x4C	TB3TH[31:0]	RW	0xFFFF FFFF	Timebase3 threshold high
p1.0x54	C3TL[63:0]	RW	0x8000 0000 0000 0000	Charge3 threshold low

REGISTER DESCRIPTION

Table 67. Threshold Registers (continued)

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER
p1.0x64	E4TH[63:0]	RW	0x7FFF FFFF FFFF FFFF	Energy4 threshold high
p1.0x6C	TB4TH[31:0]	RW	0xFFFF FFFF	Timebase4 threshold high
p1.0x74	E4TL[63:0]	RW	0x8000 0000 0000 0000	Energy4 threshold low
p1.0x80	I1TH[15:0]	RW	0x7FFF	Current1 threshold high
p1.0x82	I1TL[15:0]	RW	0x8000	Current1 threshold low
p1.0x84	P1TH[15:0]	RW	0x7FFF	Power1 threshold high
p1.0x86	P1TL[15:0]	RW	0x8000	Power1 threshold low
p1.0x88	I2TH[15:0]	RW	0x7FFF	Current2 threshold high
p1.0x8A	I2TL[15:0]	RW	0x8000	Current2 threshold low
p1.0x8C	P2TH[15:0]	RW	0x7FFF	Power2 threshold high
p1.0x8E	P2TL[15:0]	RW	0x8000	Power2 threshold low
p1.0x90	BATTH[15:0]	RW	0x7FFF	BAT threshold high
p1.0x92	BATTL[15:0]	RW	0x8000	BAT threshold low
p1.0x94	TEMPTH[15:0]	RW	0x7FFF	Die temperature threshold high
p1.0x96	TEMPTL[15:0]	RW	0x8000	Die temperature threshold low
p1.0x98	VCCTH[15:0]	RW	0x7FFF	VCC threshold high
p1.0x9A	VCCTL[15:0]	RW	0x8000	VCC threshold low
p1.0xA0	SLOT1TH[15:0]	RW	0x7FFF	Slot1 threshold high
p1.0xA2	SLOT1TL[15:0]	RW	0x8000	Slot1 threshold low
p1.0xA4	SLOT2TH[15:0]	RW	0x7FFF	Slot2 threshold high
p1.0xA6	SLOT2TL[15:0]	RW	0x8000	Slot2 threshold low

FLOAT24 Format

The NTC configuration parameters and the gain correction factors described in the following paragraphs are stored as floating point numbers represented by the FLOAT24 format according to IEEE 754 standard. The LTC2949 implementation uses 1-bit for sign, a 7-bit exponent in two's complement format with 63 as bias and 16-bits for the mantissa, with an implicit leading bit of value 1 unless the exponent is stored with all zeros. As an example the value of 0.95 is represented by the 3 bytes number 0x3EE666 as shown below:

Table 68. FLOAT24 Example

3E								E6								66							
0	0	1	1	1	1	1	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
Sign	Exponent							Mantissa MSB								Mantissa LSB							
1 x	2^(62-63) x							(1+0.899994)															

= 0.5 • 1.899994 = 0.94999

The GUI controlling the LTC2949 demo board supports converting numbers to FLOAT24. The code section of the LTC2949 (https://www.analog.com/en/products/ltc2949.html#product-tools) also provides conversion functions written in C/C++ for this purpose.

LTC2949.cpp contains following conversion functions:

```
void LTC2949_FloatToF24Bytes(float f32, byte* bytes)

void LTC2949_F24BytesToFloat(byte* bytes, float* f32)
```

REGISTER DESCRIPTION

Configuration Registers

The following registers allow to configure LTC2949 application specific. Please note that LTC2949 must be in STANDBY and an update of these registers must be requested by setting the ADJUPD bit in the Operation Control Register (OPCTRL) to make changes effective.

ADC Configuration Register

The ADC Configuration Register allows to disable power multiplication on P1ADC and P2ADC, and to turn on NTC linearization of Slot1/2 measurements.

Table 69. ADC Configuration ADCCONF (p1.0xDF)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION
0	P1ASV	RW	0	0: P1ADC configured to power mode 1: P1ADC configured to voltage mode
1	P2ASV	RW	0	0: P2ADC configured to power mode 1: P2ADC configured to voltage mode
3	NTC1	RW	0	0: SLOT1 voltage measurement. SLOT1 output LSB = 375µV 1: SLOT1 NTC temperature measurement. SLOT1 output LSB = 0.2°C
4	NTC2	RW	0	0: SLOT2 voltage measurement. SLOT2 output LSB = 375µV 1: SLOT2 NTC temperature measurement. SLOT2 output LSB = 0.2°C
6	NTCSLOT1	RW	0	0: TC compensation of shunt for I1 (I2) is linked to temperature measurement via SLOT1 (SLOT2). 1: TC compensation of shunt for I1 and I2 is linked to temperature measurement via SLOT1 only.

See NTC Configuration Registers and section Temperature Measurement for more information regarding NTC temperature measurement.

See Table 28 and Table 31 for effect of P1ASV/P2ASV on LSB sizes or Power-ADC related measurements/settings.

Table 70. Allowed Combinations of FACTRL and ADCVCONF (PxASV) Configurations.

FACONV	FACH1	FACH2	P1ASV	P2ASV	FAST BAT (b)	SLOW P1	SLOW P2
0 or 1	1	0	0 or 1	0 or 1	Not Supported!		
0 or 1	0	1	1	1			
0 or 1	0	0	0 or 1	0 or 1	N/A	18-Bit Power or Voltage	
0 or 1	0	1	0	0	N/A	18-Bit Power	N/A
0 or 1	0	1	0	1	P2	18-Bit Power	N/A
0 or 1	0	1	1	0	N/A	18-Bit Voltage	N/A
1	1	1	0	0	N/A	11-Bit Power (c)	
1	1	1	0	1	P2	11-Bit Power (c)	11-Bit Voltage (c)
1	1	1	1	0	P1	11-Bit Voltage (c)	11-Bit Power (c)
1	1	1	1	1	P1	11-Bit Voltage (c)	
0	1	1	0	0	N/A	18-Bit Power (a)	
0	1	1	0	1	P2	18-Bit Power (a)	18-Bit Voltage (a)
0	1	1	1	0	P1	18-Bit Voltage (a)	18-Bit Power (a)
0	1	1	1	1	P1	18-Bit Voltage (a)	

a) Any fast single shot measurement will interrupt the slow channel measurements. Slow channel will only resume to be updated if there was no fast single shot measurement for at least 160ms.

b) 15-bit Fast BAT (VBATP-VBATM) voltage measurement via one power ADC. It is always possible to measure VBATP-VBATM via AUX ADC in fast (FACHA=1) or slow mode.

c) Power ADCs (PxASV=0) of channels configured to fast mode will provide 11-bit conversions at an update rate of 100ms via P1/P2 registers. The LSB size stays the same, but the resolution in this case is only guaranteed to be 11-bit.

REGISTER DESCRIPTION

NTC Configuration Registers

When bits NTC1 and NTC2 in the ADC Configuration Register are set, LTC2949 reports the result of the corresponding CHAUX slot in temperature by comparing NTC resistance to reference resistors and solving Steinhart-Hart equations. The NTC Configuration Registers allow to set values of Steinhart-Hart coefficients (A,B,C) and reference resistors.

Furthermore, linear temperature coefficients of up to two external sense resistors can be compensated by thermally closely coupled NTC thermistors. Temperature compensation is enabled by writing the respective temperature coefficient and its reference temperature (T_0) in the NTC Configuration Register. See section Temperature Measurement and Sense Resistor Temperature Compensation for more details.

Table 71. NTC Configuration Registers

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	UNIT	FORMAT
p1.0xAA	RREF1[23:0]	RW	0x000000	NTC1 reference resistor	Ω	Float24
p1.0xAD	RREF2[23:0]	RW	0x000000	NTC2 reference resistor	Ω	Float24
p1.0xD0	NTC1A[23:0]	RW	0x000000	NTC1 Coefficient A		Float24
p1.0xD3	NTC1B[23:0]	RW	0x000000	NTC1 Coefficient B		Float24
p1.0xD6	NTC1C[23:0]	RW	0x000000	NTC1 Coefficient C		Float24
p1.0xD9	RS1TC[23:0]	RW	0x000000	Sense resistor 1 (RS1) temperature coefficient (TC)	1/K	Float24
p1.0xDC	RS1T0[16:0]	RW	0x0000	Reference temperature for TC compensation of RS1	°C	Float24
p1.0xE0	NTC2A[23:0]	RW	0x000000	NTC2 Coefficient A		Float24
p1.0xE3	NTC2B[23:0]	RW	0x000000	NTC2 Coefficient B		Float24
p1.0xE6	NTC2C[23:0]	RW	0x000000	NTC2 Coefficient C		Float24
p1.0xE9	RS2TC[23:0]	RW	0x000000	Sense resistor 2 (RS2) temperature coefficient (TC)	1/K	Float24
p1.0xEC	RS2T0[16:0]	RW	0x0000	Reference temperature for TC compensation of RS2	°C	Float24
p1.0x5C	RS1TC2[23:0]	RW	0x000000	2nd order TC of sense resistor 1	$1/K^2$	Float24
p1.0x7C	RS2TC2[23:0]	RW	0x000000	2nd order TC of sense resistor 2	$1/K^2$	Float24

Note that for the two 16-bit registers storing reference temperature RS1T0 and RS2T0 the least significant byte (LSB) of the mantissa is implicitly 0

Gain Configuration Registers

The LTC2949 can store gain correction factors for two current sense resistor, the battery voltage divider and four multiplexer inputs to compensate tolerances of external components in its Gain Setting Registers located between 0xB0 and 0xCF on measured page 1 of the register map. When these factors are set different than their default value of 1.0, the LTC2949 corrects the computed values of current, voltage, power, charge and energy accordingly. As the LTC2949 accumulators can be configured to compute the sums of charge and energy flown through two sense resistors, also the nominal ratio between the two sense resistors RSRATIO = R_{S1}/R_{S2} can be stored. The LTC2949 then multiplies the measurements of CH2 (I2, P2) by RSRATIO before adding them to the sum of charge (C3) or energy (E4). All these factors are stored in the Float24 format according to IEEE 754 standard described earlier.

Table 72. Gain Configuration Registers

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	FORMAT
p1.0xB0	RS1GC[23:0]	RW	0x3F00 00	Sense resistor 1(R_{S1}) gain correction factor	Float24
p1.0xB3	RS2GC[23:0]	RW	0x3F00 00	Sense resistor 2(R_{S2}) gain correction factor	Float24
p1.0xB6	RSRATIO[23:0]	RW	0x3F00 00	Nominal ratio of R_{S1} to R_{S2}	Float24
p1.0xB9	BATGC[23:0]	RW	0x3F00 00	BAT gain correction factor	Float24
p1.0xC0	MUX1GC[23:0]	RW	0x3F00 00	Gain correction factor for MUX setting 1	Float24
p1.0xC3	MUX2GC[23:0]	RW	0x3F00 00	Gain correction factor for MUX setting 2	Float24
p1.0xC6	MUX3GC[23:0]	RW	0x3F00 00	Gain correction factor for MUX setting 3	Float24
p1.0xC9	MUX4GC[23:0]	RW	0x3F00 00	Gain correction factor for MUX setting 4	Float24

REGISTER DESCRIPTION

Table 72. Gain Configuration Registers (continued)

ADDRESS	NAME	TYPE	DEFAULT	PARAMETER	FORMAT
p1.0xBC	MUXNSET1[4:0]	RW	0x00	MUXN gain correction setting 1	MUXN binary coded, see Table 57
p1.0xBD	MUXPSET1[4:0]	RW	0x00	MUXP gain correction setting 1	MUXP binary coded, see Table 57
p1.0xBE	MUXNSET2[4:0]	RW	0x00	MUXN gain correction setting 2	MUXN binary coded, see Table 57
p1.0xBF	MUXPSET2[4:0]	RW	0x00	MUXP gain correction setting 2	MUXP binary coded, see Table 57
p1.0xCC	MUXNSET3[4:0]	RW	0x00	MUXN gain correction setting 3	MUXN binary coded, see Table 57
p1.0xCD	MUXPSET3[4:0]	RW	0x00	MUXP gain correction setting 3	MUXP binary coded, see Table 57
p1.0xCE	MUXNSET4[4:0]	RW	0x00	MUXN gain correction setting 4	MUXN binary coded, see Table 57
p1.0xCF	MUXPSET4[4:0]	RW	0x00	MUXP gain correction setting 4	MUXP binary coded, see Table 57

As an example, if a sense resistor of nominal 100µΩ is used for CH1, but a board calibration reveals the sense resistor value to be 102µΩ, a factor of 100/102 = 0.9804 should be written to RS1GC [23:0] = float24(0.9804) = 0x3EF5F5.

Assuming a sense resistor of nominal value 10mΩ but real value of 9.8mΩ is used for CH2 the factor 1.024 should be programmed in RS2GC [23:0] = float24(1.024) = 0x3F0624 and a factor 0.01 should be programmed in RSRATIO[23:0] = float24(0.01) = 0x3847AE.

In many applications the LTC2949 measures high voltages using external resistor dividers which suffer from gain errors due to resistor tolerances. The LTC2949 allows to store gain correction factors for the measurement of battery voltage and four programmable MUX settings. E.g.: The LTC2949 will apply gain correction of 0.9 to differential measurements between V1 and V2 if registers MUX1GC[23:0] = 0x3ECCCC, MUXPSET1[7:0] = 0x01 and MUXNSET1[7:0] = 0x02, see also Table 57.

The assignment between MUX[1-4]GC and MUX[P,N]SET[1-4] is independent of the polarity of the MUX settings. Related to the example above the same gain correction is applied for measurements V1-V2 and V2-V1. Also swapping the register values of MUXPSET1 and MUXNSET1 leads to the same behaviour. The link between gain correction parameters and measurements is summarized in Table 73.

All Gain Configuration Registers can be copied to an external EEPROM, enabling a modular approach to factory calibration of application boards.

Table 73. Relation Between Gain Correction Parameters and Measurements

NAME	AFFECTED MEASUREMENTS
BATGC	BAT for slow and fast measurements P1, P2, E1, E2, E4 SLOT[1,2] AUX measurements if SLOT[1,2]MUX[P,N] is set to VBATP, VBATM of any polarity Fast AUX conversions if FAMUX[P,N] is set to VBATP, VBATM of any polarity
MUX[1-4]GC	Slow and fast AUX measurements if SLOT[1,2]MUX[P,N] or FAMUX[P,N] matches MUX[P,N]SET[1-4] of any polarity
RS[1,2]GC	I1, I2, P1, P2, C1, C2, C3, E1, E2, E4
RSRATIO	C3, E4 (Note: The charge that is accumulated to C3 is (I1 + RSRATIO • I2) • dT, the energy that is accumulated to E4 is (P1 + RSRATIO • P2) • dT.)

REGISTER DESCRIPTION

External EEPROM Control Register

To prevent data loss when the LTC2949 is not powered, it can store its entire register content in an external EEPROM via its dedicated I^2C interface. The communication to an EEPROM is controlled by the EEPROM Control Register (EEPROMCTRL).

Table 74. EEPROM Control Register EEPROMCTRL (p1.0x50)

BIT	SYMBOL	TYPE	DEFAULT	OPERATION	DURATION
0	INIT	SO	0	Write signature to EEPROM	40ms
1	CHECK	SO	0	Check the signature in EEPROM	25ms
2	SAVE	SO	0	Save MEM (but special row) to EEPROM	1100ms
3	RESTORE	SO	0	Restore EEPROM to MEM (but special row)	1250ms
4	INITRSL	RW	0	Result of INIT	
5	CHECKRSL	RW	0	Result of CHECK	
6	SAVERSL	RW	0	Result of SAVE	
7	RESTORERSL	RW	0	Result of RESTORE	

The lower 4-bits of the EEPROMCTRL are SET ONLY and trigger dedicated communications with the EEPROM, while the higher 4-bits are read/write and are set by the LTC2949 after the typical time given in the column Duration upon a successful termination of a communication and must be reset by a write command from the host before the next communication is requested.

Before any other interaction, the EEPROM must be initialized by setting the INIT bit, which causes LTC2949 to write a defined signature to the EEPROM. Once the signature is written, LTC2949 will reset the INIT bit and set the INITRSL bit if the EEPROM has acknowledged according to the I^2C protocol. Any other interaction with the EEPROM will be preceded by reading and checking this signature – additionally the signature can be checked by setting bit CHECK and verifying that bit CHECKRSL is set after bit CHECK was reset by LTC2949.

Setting bit SAVE causes the LTC2949 to save its entire memory except the last common row of both register pages to the EEPROM together with a CRC calculated from the entire register content. LTC2949 signals a successful save operation by setting bit SAVERSL, based on the check of the signature and the acknowledge of the EEPROM.

Setting bit RESTORE causes the LTC2949 to copy the content of the EEPROM to its internal RAM, calculate the CRC and set bit RESTORERSL if the CRC was found correct.

Any communication with the external EEPROM requires the LTC2949 to be in STANDBY mode to prevent data loss or data corruption.

Many applications require to store additional custom data, e.g. serial number. The reserved registers p1.0x1C - p1.0x1F (4 bytes) and p1.0x3C - p1.0x3F (4 bytes) can be used for that purpose. Additionally, registers of LTC2949 that do not require a board specific initialization and thus are initialized by the host controller, can be used to store custom data. For example, all accumulators are either just initialized with zero or via some state-of-charge algorithm. All threshold values are typically hard coded or initialized by some higher instance in the system. Mux setting registers are adjusted programmatically. Min/max tracking registers can be initialized by the host controller. The register map shown in Figure 18 gives an overview of those registers. Using all of them allows to increase the number of custom data bytes to 240 bytes.

To access this data the host commands an EEPROM RESTORE, reads all registers with custom data and initializes the registers afterwards to their desired value.

REGISTER DESCRIPTION

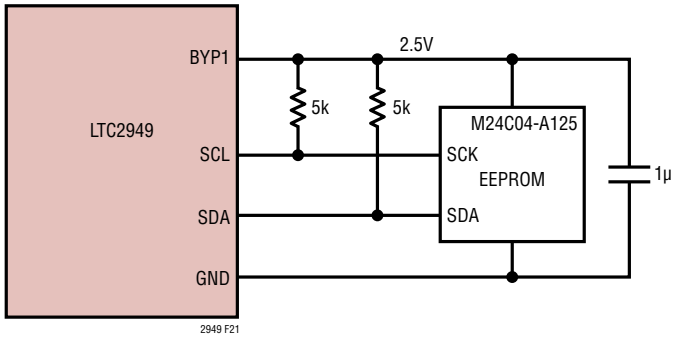


Figure 21. EEPROM Connection. Recommended 4k Bit Automotive Qualified EEPROM with Internal EEC: M24C04-A125 from STMicroelectronics or without Internal EEC: AT24C04C or 24AA04 from Microchip.

APPLICATION INFORMATION

TEMPERATURE MEASUREMENT

The LTC2949s high impedance inputs V1-V12 can be used to measure temperature by means of thermistors and a reference resistor as shown below.

When bits NTC1 or NTC2 in the ADC Configuration Register are set, LTC2949 reports the result of the corresponding CHAUX slot in slow high precision mode in temperature by comparing the resistance of a thermistor (NTC) R_{NTC} to a reference resistor and solving the Steinhart-Hart equation.

$$\frac{1}{T} = A + B \bullet \ln R_{NTC} + C \bullet (\ln R_{NTC})^3$$

The value of the reference resistor R_{REF} and the Steinhart-Hart coefficients (A, B, C) need to be stored in the NTC Configuration Registers. Steinhart-Hart coefficients are commonly specified parameters provided by thermistor manufacturers or can be deduced from provided resistance tables.

The following table shows the relevant registers from the NTC configuration register for the application shown in Figure 22.

As VREF is measured with the same ADC as V1-V12, imperfections of VREF and gain error of the ADC do not impact the temperature measurement accuracy.

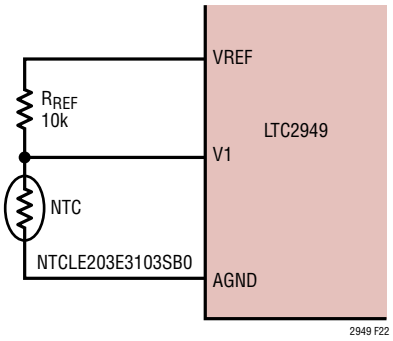


Figure 22. Connecting Thermistors

Table 75. NTC1 Values in NTC Configuration Register

PARAMETER	VALUE	UNIT	ADDRESS	NAME	VALUE	FORMAT
NTC1 reference resistor	10k	Ω	p1.0xAA	RREF1[23:0]	0x4C3880	Float24
NTC1 Coefficient A	1.1382e-3		p1.0xD0	NTC1A[23:0]	0x352A5F	Float24
NTC1 Coefficient B	2.3267e-4		p1.0xD3	NTC1B[23:0]	0x32E7F1	Float24
NTC1 Coefficient C	0.93243e-7		p1.0xD6	NTC1C[23:0]	0x279079	Float24

APPLICATION INFORMATION

SENSE RESISTOR TEMPERATURE COMPENSATION

The LTC2949 can be configured to compensate the temperature dependency of the used current sense resistors up to 2nd order based on temperature measurements with external NTCs. The compensation is enabled by writing the temperature coefficients (TC,TC2) of the sense resistor and the reference temperature (T_0) in the NTC configuration register. The LTC2949 will then compensate for the temperature induced deviation of the sense resistor from its nominal value R_0 according to:

$$R_{SENSE} = R_0 \bullet [1 + TC \bullet (T - T_0) + TC2 \bullet (T - T0)^2]$$

The temperature coefficient and reference temperature can be set for each sense resistor individually in the NTC configuration register. Table 76 shows the programmed coefficients for a copper sense resistor with a temperature coefficient of 3900ppm/K whose nominal value R_0 was measured at 20°C.

If temperature compensation is enabled for one or both channels, the sense resistor connected to CH1 is compensated with the temperature of NTC1 measured during the first slot of CHAUX, while the sense resistor connected to CH2 is compensated with the temperature of NTC2 measured during the second slot of CHAUX. The multiplexer settings must be set such that the input pin connected to the corresponding NTC is selected during the respective slot. If CHAUX is changed to fast mode, the last NTC temperature measurements taken in Round Robin mode are used for temperature compensation.

The following linear equation system has to be solved to calculate A,B,C using three values, R1(T1), R2(T2), R3(T3) from a R versus T (in K) resistor table:

$$\begin{pmatrix} T_1^{-1} \\ T_2^{-1} \\ T_3^{-1} \end{pmatrix} = \begin{pmatrix} 1 & \ln R_1 & \ln^3 R_1 \\ 1 & \ln R_2 & \ln^3 R_2 \\ 1 & \ln R3 & \ln^3 R_3 \end{pmatrix} \begin{pmatrix} A \\ B \\ C \end{pmatrix}$$

After solving the linear equation system, A, B, C can be expressed as:

$$I_1 = \ln R_1$$

$$I_2 = \ln R_2$$

$$I_3 = \ln R_3$$

$$m_2 = \frac{T_2^{-1} - T_1^{-1}}{I_2 - I_1}$$

$$m_3 = \frac{T_3^{-1} - T_1^{-1}}{I_3 - I_1}$$

$$C = \frac{\frac{m_3 - m_2}{I_3 - I_2}}{I_3 + I_2 + I_1}$$

$$B = m_2 - C \bullet (I_1^2 + I_1 \bullet I_2 + I_2^2)$$

$$A = T_1^{-1} - (B + I_1^2 \bullet C) \bullet I_1$$

APPLICATION INFORMATION

For single shunt scenarios the temperature measured by one NTC with SLOT1 can be used to compensate both channels. See ADCCONF, bit NTCSLOT1.

isoSPI Setup

The LTC2949 allows the isoSPI link in each application to be optimized for power consumption or for noise immunity. The power and noise immunity of an isoSPI system is determined by the programmed I_B current. The I_B current can range from 100µA to 1mA. A low I_B reduces the isoSPI power consumption in the READY and ACTIVE states, while a high I_B increases the amplitude of the differential signal voltage V_A across the matching termination resistor, R_M. I_B is programmed by the sum of the R_{B1} and R_{B2} resistors connected between the I_{BIAS} pin and GND as shown in Figure 23. For most applications setting I_B to 0.5mA is a good compromise between power consumption and noise immunity. Using this I_B setting with a 1:1 transformer and R_M = 100Ω, R_{B1} should be set to 2.8k and R_{B2} set to 1.2k. In a typical CAT5 twisted pair these settings will allow for communication up to 50m. For applications that require cables longer than 50m it is recommended to increase the I_B to 1mA. This compensates for the increased insertion loss in the cable and maintains high noise immunity. So when using cables over 50m and, again, using a transformer with a 1:1 turns ratio and R_M = 100Ω, R_{B1} would be 1.4k and R_{B2} would be 600Ω. Other I_B settings can be used to reduce power consumption or increase the noise immunity as required by the application. In these cases when setting threshold voltage V_{ICMP} and choosing R_{B1} and R_{B2} resistor values the following rules should be used:

Table 76. Sense Resistor Temperature Coefficients

PARAMETER	VALUE	UNIT	ADDRESS	NAME	VALUE	FORMAT
Sense resistor 1 (RS1) temperature coefficient (TC)	0.0039	1/K	p1.0xD9	RS1TC[23:0]	0x36FF2E	Float24
Reference temperature for TC compensation of RS1	20	°C	p1.0xDC	RS1T0[16:0]	0x4340	Float24, 2 bytes

Note: For copper only the first order temperature coefficient is relevant and thus TC2=0.0 (default).

Table 77. Procedure to Enable Temperature Compensation of Sense Resistor

	WHAT	HOW AND WHERE	ADDRESS
Step 1	Set LTC2949 to Standby Mode	CONT= 0 in OPCTRL	0xF0
Step 2	Write NTC and R_{SENSE} DATA	NTC configuration Registers	See Table 71.
Step 3	Set AUX Slot to Temperature Mode	NTCx = 1 in ADC Configuration Register	p1.0xDF
Step 4	Select MUX input channel with connected NTC	Mux Setting Registers	0xEB-0xEE
Step 5	Update Configuration Registers	ADJUP = 1 in OPCTRL	0xF0
Step 6	Set LTC2949 to Continuous Mode	CONT = 1 in OPCTRL	0xF0

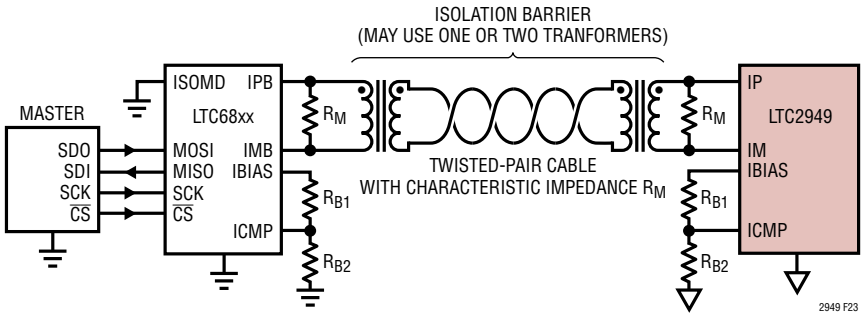


Figure 23. isoSPI Circuit

Rev A

APPLICATION INFORMATION

For cables under 50m:

$I_B = 0.5mA$

$V_A = (20 \bullet I_B) \bullet (R_M/2)$

$V_{TCMP} = ½ \bullet V_A$

$V_{ICMP} = 2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$R_{B1} = (2/I_B) – R_{B2}$

For cables over 50m:

$I_B = 1mA$

$V_A = (20 \bullet I_B) \bullet (R_M/2)$

$V_{TCMP} = 1/4 \bullet V_A$

$V_{ICMP} = 2 \bullet V_{TCMP}$

$R_{B2} = V_{ICMP}/I_B$

$R_{B1} = (2/I_B) – R_{B2}$

The maximum data rate of an isoSPI link is determined by the length of the cable used. For cables 10 meters or less the maximum 1MHz SPI clock frequency is possible. As the length of the cable increases the maximum possible SPI clock rate decreases. This is a result of the increased propagation delays through the cable creating possible timing violations. Figure 24 shows how the maximum data rate is reduced as the cable length increases when using a CAT 5 twisted pair. Cable delay affects three timing specifications, t_{CLK}, t_6 and t_7. In the Electrical Characteristics table, each is derated by 100ns to allow for 50ns of cable delay. For longer cables, the minimum timing parameters may be calculated as shown below:

t_{CLK}, t6 and t7 > 0.9µs + 2 • t_{CABLE}

Transformer Selection Guide

As shown in Figure 23, a transformer or pair of transformers isolates the isoSPI signals between two isoSPI ports. The isoSPI signals have programmable pulse amplitudes up to $1.6V_{P-P}$ and pulse widths of 50ns and 150ns. To be able to transmit these pulses with the necessary fidelity the system requires that the transformers have primary inductances above 60µH and a 1:1 turns ratio. It is also necessary to use a transformer with less than 2.5µH of leakage inductance. In terms of pulse shape the primary inductance will mostly effect the pulse droop of the 50ns and 150ns pulses. If the primary inductance is too low, the pulse amplitude will begin to droop and decay over the pulse period. When the pulse droop is severe enough, the effective pulse width seen by the receiver will drop substantially, reducing noise margin. Some droop is acceptable as long as it is a relatively small percentage of the total pulse amplitude. The leakage inductance primarily affects the rise and fall times of the pulses. Slower rise and fall times will effectively reduce the pulse width. Pulse width is determined by the receiver as the time the signal is above the threshold set at the ICMP pin. Slow rise and fall times cut into the timing margins. Generally it is best to keep pulse edges as fast as possible. When evaluating transformers, it is also worth noting the parallel winding capacitance. While transformers have very good CMRR at low frequency, this rejection will degrade at higher frequencies, largely due to the winding to winding capacitance. When choosing a transformer, it is best to pick one with less parallel winding capacitance when possible.

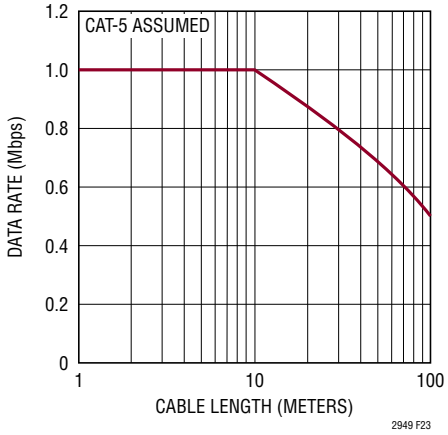


Figure 24. Data Rate vs Cable Length

APPLICATION INFORMATION

When choosing a transformer, it is equally important to pick a part that has an adequate isolation rating for the application. The working voltage rating of a transformer is a key spec when selecting a part for an application. Interconnecting daisy-chain links, devices see <60V stress in typical applications and ordinary pulse and LAN type transformers will suffice. Multi-drop connections and connections to the LTC6820, in general, may need much higher working voltage ratings for good long-term reliability. Usually, matching the working voltage to the voltage of the entire battery stack is conservative. Unfortunately, transformer vendors will often only specify one-second HV testing, and this is not equal to the long-term (permanent) rating of the part. For example, according to most safety standards a 1.5kV rated transformer is expected to handle 230V continuously, and a 3kV device is capable of 1100V long-term, though manufacturers may not always certify to those levels (refer to actual vendor data for specifics). Usually, the higher voltage transformers are called high isolation or reinforced insulation types by the suppliers. Table 78 shows a list of transformers that have been evaluated in isoSPI links.

EMC

For the best electromagnetic compatibility (EMC) performance, it is recommended to use one of the circuits in Figure 25 and Figure 26. The center tap of the transformer should be bypassed with a 10nF capacitor. The center tap capacitor will help attenuate common mode signals. Large center tap capacitors greater than 10nF should be avoided as they will prevent the isoSPI transmitters common mode voltage from settling. If a transformer without a center tap is used, the termination resistor should be split into two equal halves and connected in series across the IP and IM lines. The center of the two resistors should be bypassed with a capacitor as shown. To improve common mode current rejection a common mode choke should also be placed in series with the IP and IM lines of the LTC2949. The common mode choke will both increase EMI immunity and reduce EMI emission. When choosing a common mode choke, the differential mode impedance should be 20Ω or less for signals 50MHz and below. Common mode chokes similar to what is used in Ethernet applications are recommended.

Layout of the isoSPI signal lines also plays a significant role in maximizing the immunity of a circuit. The following layout guidelines should be followed:

1. The transformer should be placed as close to the isoSPI cable connector as possible. The distance should be kept less than 2cm. The LTC2949 should be placed at least 1cm to 2cm away from the transformer to help isolate the IC from magnetic field coupling.
2. On the top component layer, no ground plane should be placed under the transformer, the isoSPI connector, or in between the transformer and the connector.
3. The isoSPI signal traces should be isolated from surrounding circuits and traces by ground metal or space. No traces should cross the isoSPI signal lines, unless separated by a ground plane on an inner layer.

The isoSPI drive currents are programmable and allow for a trade-off between power consumption and noise immunity. The noise immunity of the LTC2949 has been evaluated using a bulk current injection (BCI) test. The BCI test injects current into the twisted-pair lines at set levels over a frequency range of 1MHz to 400MHz. With the minimum I_B current, 100µA, the isoSPI serial link was capable of passing a 40mA BCI test with no bit errors. A 40mA BCI test level is sufficient for industrial applications. Automotive applications have a much higher BCI requirement so the LTC2949 I_B is set to 1mA, the maximum power level. The isoSPI system is capable of passing a 200mA BCI test with no transmitted bit errors. The 200mA test level is typical for automotive requirements.

APPLICATION INFORMATION

Table 78. Recommended Transformers

SUPPLIER	PART NUMBER	TEMP RANGE	$V_{WORKING}$	V_{HIPOT}/60S	CT	CMC	H	L	W (W/ LEADS)	PINS	AEC-Q200
Recommended Dual Transformers											
Pulse	HX1188FNL	–40°C to 85°C	60V (est)	1.5kV$_{RMS}$	●	●	6.0mm	12.7mm	9.7mm	16SMT	–
Pulse	HX0068ANL	–40°C to 85°C	60V (est)	1.5kV$_{RMS}$	●	●	2.1mm	12.7mm	9.7mm	16SMT	–
Pulse	HM2100NL	–40°C to 105°C	1000V	4.3kVDC	–	●	3.4mm	14.7mm	14.9mm	10SMT	●
Pulse	HM2112ZNL	–40°C to 125°C	1000V	4.3kVDC	●	●	4.9mm	14.8mm	14.7mm	12SMT	●
Sumida	CLP178-C20114	–40°C to 125°C	1000V (est)	3.75kV$_{RMS}$	●	●	9mm	17.5mm	15.1mm	12SMT	–
Sumida	CLP0612-C20115		600V$_{RMS}$	3.75kV$_{RMS}$	●	–	5.7mm	12.7mm	9.4mm	16SMT	–
Wurth	7490140110	–40°C to 85°C	250V$_{RMS}$	4kV$_{RMS}$	●	●	10.9mm	24.6mm	17.0mm	16SMT	–
Wurth	7490140111	0°C to 70°C	1000V (est)	4.5kV$_{RMS}$	●	–	8.4mm	17.1mm	15.2mm	12SMT	–
Wurth	749014018	0°C to 70°C	250V$_{RMS}$	4kV$_{RMS}$	●	●	8.4mm	17.1mm	15.2mm	12SMT	–
Halo	TG110-AE050N5LF	–40°C to 85/125°C	60V (est)	1.5kV$_{RMS}$	●	●	6.4mm	12.7mm	9.5mm	16SMT	●
Recommended Single Transformers											
Pulse	PE-68386NL	–40°C to 130°C	60V (est)	1.5kVDC	–	–	2.5mm	6.7mm	8.6mm	6SMT	–
Pulse	HM2101NL	–40°C to 105°C	1000V	4.3kVDC	–	●	5.7mm	7.6mm	9.3mm	6SMT	●
Pulse	HM2113ZNL	–40°C to 125°C	1600V	4.3kVDC	●	●	3.5mm	9mm	15.5mm	6SMT	●
Wurth	750340848	–40°C to 105°C	250V	3kV$_{RMS}$	–	–	2.2mm	4.4mm	9.1mm	4SMT	–
Wurth	750317011	–40°C to 125°C	800V	3kV$_{RMS}$	●	–	7.62mm	9.14mm	12.95mm	6SMT	–
Halo	TGR04-6506V6LF	–40°C to 125°C	300V	3kV$_{RMS}$	●	–	10mm	9.5mm	12.1mm	6SMT	–
Halo	TGR04-A6506NA6NL	–40°C to 125°C	300V	3kV$_{RMS}$	●	–	9.4mm	8.9mm	12.1mm	6SMT	●
Halo	TDR04-A550ALLF	–40°C to 105°C	1000V	5kV$_{RMS}$	●	–	6.4mm	8.9mm	16.6mm	6TH	●
TDK	ALT4532V-201-T001	–40°C to 105°C	60V (est)	~1kV	●	–	2.9mm	3.2mm	4.5mm	6SMT	●
Sumida	CEEH96BNP-LTC6804/11	–40°C to 125°C	600V	2.5kV$_{RMS}$	–	–	7mm	9.2mm	12.0mm	4SMT	–
Sumida	CEP99NP-LTC6804	–40°C to 125°C	600V	2.5kV$_{RMS}$	●	–	10mm	9.2mm	12.0mm	8SMT	–
Sumida	ESMIT-4180/A	–40°C to 105°C	250V$_{RMS}$	3kV$_{RMS}$	–	–	3.5mm	5.2mm	9.1mm	4SMT	●
TDK	VGT10/9EE-204S2P4	–40°C to 125°C	250V (est)	2.8kV$_{RMS}$	●	–	10.6mm	10.4mm	12.7mm	8SMT	–

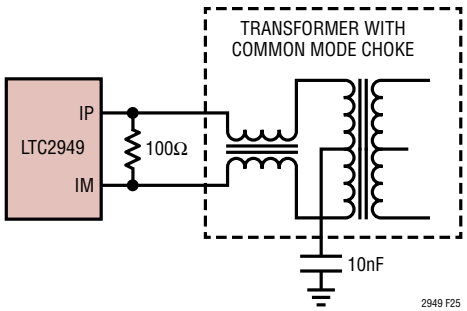


Figure 25. Recommended isoSPI Circuit for EMC

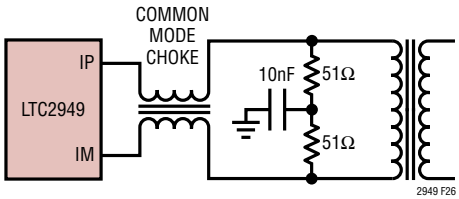


Figure 26. Recommended isoSPI Circuit for Best EMC Performance when Using a Transformer without Center Tap

Table 79. Recommended Common Mode Chokes

MANUFACTURER	PART NUMBER
TDK	ACT45B-220-2P
Murata	DLW43SH510XK2
Wurth	744232102

APPLICATION INFORMATION

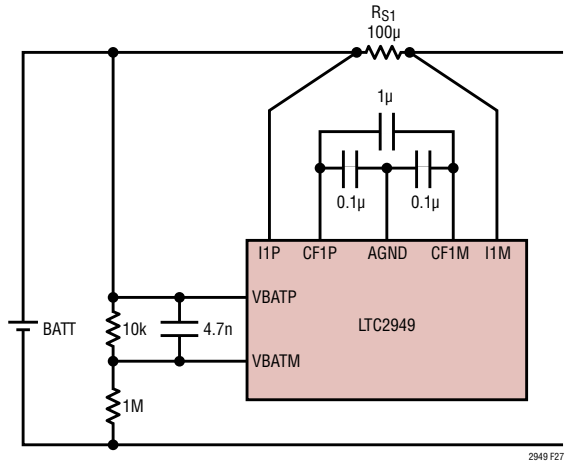


Figure 27. Input Filtering

CURRENT AND VOLTAGE INPUT FILTERING

To ensure the full electrical performance of the ADCs for current, power and voltage, apply the input filtering circuitry as depicted in Figure 27 to pins CFP, CFM, VBATP and VBATM. These components ensure an optimized input filtering for noise reduction. Equal time constants at current and voltage inputs minimize errors in power measurement of transient signals due to different delays in both paths.

Unused Input Pins V1-V12

Input pins V1-V12 can be left floating or connected to GND if not used. Still, it is not recommended to connect V8-V12 to GND as those pins can be driven high optionally when used as digital outputs.

Depending on the application and the configuration of LTC2949, it might be beneficial or sometimes even necessary to apply following external connections to inputs, which were unused.

1. Connect pin VREF to one of V1-V12
   a. See last paragraph of section Fast Mode Configurations for effect of fast AUX measurement on internal slow AUX Round-Robin. Register VREF is not updated while performing fast AUX conversions.
   b. The internal VREF measurement is altered while the current sources (see register FCURGPIOCTRL) are enabled. Connecting VREF to one Vx pin always measurement of the correct VREF pin voltage at any time.
   c. VREF can be used to bias resistive dividers to allow measurement of voltages below GND. In those scenarios the differential voltage between Vx and VREF must be measured which is only possible if VREF is connected to one of V1-V12 pins.
2. Connect divided supply voltage AVCC/DVCC (e.g. 10k between GND/Vx and 20k between Vx and AVCC/DVCC) to one of V1-V12
   a. Same as 1.a. Register VCC is not updated while performing fast AUX conversions.
3. Connect NTC to one of V1-V12
   a. See section Temperature Measurement
4. Connect pin VREF via an external 4k resistor to one of V1-V12
   a. Allows to diagnose the internal current sources.
5. Connect pins BYP1 and BYP2 to separate unused pins of V1-V12.
   a. Allows to diagnose internal generated supply voltages additionally to built-in self-tests.

High-Ohmic Resistive Dividers

Any high voltage to be measured by LTC2949 must be divided down and optionally biased via VREF to move it into the LTC2949's supply voltage rails ±100mV and into the ADC's differential input voltage range (±4.8V). Typically, several resistors are connected in series, to minimize the voltage drop and power dissipation of individual resistors (Figure 28). LTC2949 Operation State Diagram shows a typical schematic, as an example the signal is measured via V1 by the AUX ADC. The measurement is performed similarly via the BAT inputs (VBATP, VBATM) by the AUX or the Power ADCs (P1/P2 as voltage).

All voltage inputs of LTC2949 are buffered. The differential input impedance during measurements is guaranteed to be >50Meg. For typical resistive dividers, like those shown in the typical application, the effect of this equivalent >50Meg resistor is negligible. The error can be calculated as following:

Nominal gain factor: $g = R_{low}/(R_{low}+R_{high})$

APPLICATION INFORMATION

Effective low side resistor: $R_{lowd} = R_{low} \bullet R_d / (R_{low}+R_d)$, R_d = 50e5

Effective gain factor: $g_d = R_{lowd}/(R_{lowd}+R_{high})$

Example values: R_{low}=30[3], R_{high}=5 • 1.3e6

Gain factor error: err = g_d/g–1 = –0.06%

The differential input impedance during measurements is nonlinear, it increases with decreasing input signal and it may also change over temperature. For this reason, it can be calibrated only partially during a post-production board test procedure. Still, its guaranteed to be >50Meg over the full-scale input range and the whole operating temperature range and thus the error calculated above gives the worst-case error.

The high voltage is calculated from the ADC measurement the following way:

Divider connected to GND: $V_{HVa} = V_{ADC}/g$

Divider connected to VREF: $V_{HVb} = V_{ADC}/g+VREF$

As any resistive divider is affected by static tolerances, it can be calibrated by applying a known input signal and calculating greal from the ADC measurement. LTC2949 can compensate for this error by writing the gain correction factor GC=gnominal/greal to one of the related gain correction registers (BATGC, MUX1GC-MUX4GC). The optional external EEPROM can be used as a nonvolatile storage for those calibration factors.

LTC2949's gain correction registers are not limited to values around 1.0, for example it is possible to write a value of 10.0 and this factor would be applied just as any other. Still, there is a limitation by the size of the result registers which is 16-bit (including sign) for any AUX-ADC measurement like BAT, SLOT1/2 and the fast AUX measurement results. This leads to an absolute maximum register value of roughly 12.3V (375µV • [2^{15}-1]). To avoid clipping or overflowing of the results, it is always recommended to use gain correction factors that correct the deviation from nominal factors (e.g. deviation from nominal resistor divider ratio) like in the example above. The host controller software then holds the hard-coded nominal factor (e.g. 6.53Meg/30k) and LTC2949 is applying the fine-trim based on the values that were stored into the external EEPROM during board calibration.

POWERING THE LTC2949

The LTC2949 requires a single supply voltage of 4.5 to 14V. The maximum supply current is 20mA when active and 120µA when sleeping. If isoSPI is selected up to 7mA are required additionally during communication. Any current that is necessary to drive circuits connected to the GPIO pins must also be considered when selecting and designing a suitable power supply.

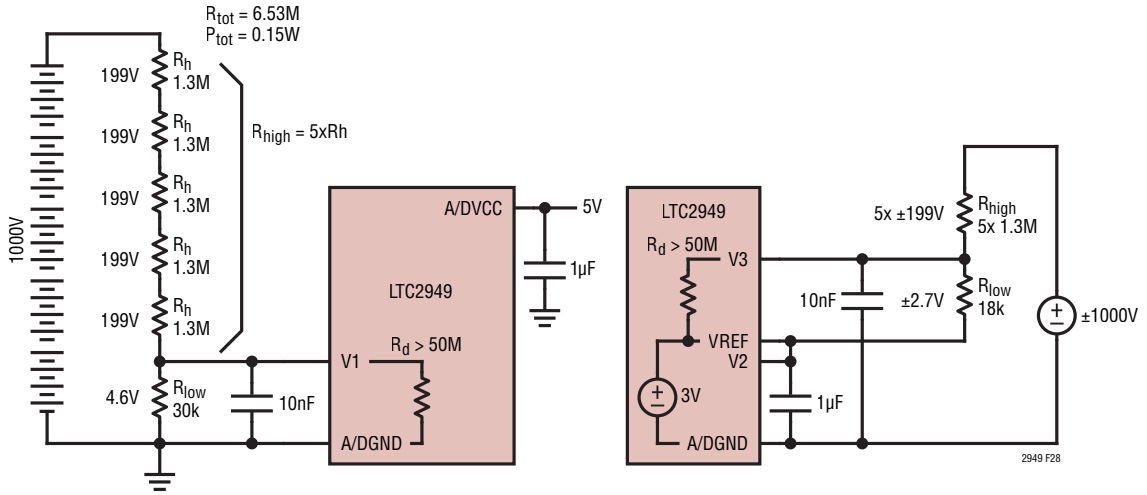


Figure 28. Left: High-Ohmic Resistive Divider for Measuring 1000V Battery Voltage Via the AUX ADC Input V1. Right: Resistive Divider Connected to VREF Allows to Measure ±1000V.

APPLICATION INFORMATION

Non-Isolated Supply

LTC provides a broad spectrum of non-isolated power supply solutions including LDOs, switched mode power supplies and µModuleregulators. As the LTC2949 is mainly targeting high voltage battery applications the LT8315 can be considered. Using the LT8315 it is possible to supply the LTC2949 directly out of a high voltage battery of up to 560V as shown in Figure 29.

Isolated supply

Most high voltage battery applications where the LTC2949 cannot be supplied directly out of the battery require an isolated power supply. A simple DC/DC converter is shown in Figure 30 using Linear Technology's LT3999 DC/DC converter and a high isolation-rated transformer.

The LT830X family of flyback converters with a suitable transformer is also a possible choice.

PART NUMBER	V_{IN} RANGE	POWER SWITCH	MAX. P_{OUT}	PACKAGE
LT8300	6V to 100V	0.26A/150V	2W	SOT23-5
LT8303	5.5V to 100V	0.45A/150V	5W	SOT23-5
LT8301	2.7V to 42V	1.2A/65V	6W	SOT23-5
LT8302	2.8V to 42V	3.6A/65V	18W	SO-8E
LT8304/-1	3V to 100V	2A/150V	24W	SO-8E

Minimum load requirement of the flyback converters must be considered which is typically much higher than the sleep current of the LTC2949. To prevent the output voltage from rising above LTC2949's operating ratings a 12V Zener diode (e.g. NXP: BZX384-B12,115) should be placed.

Transformer specification and design is possibly the most critical part of successfully applying the above mentioned DC/DC converters. Data sheets of the suggested parts give detailed information about critical parameters like saturation current, inductance, isolation voltage rating and creepage distance.

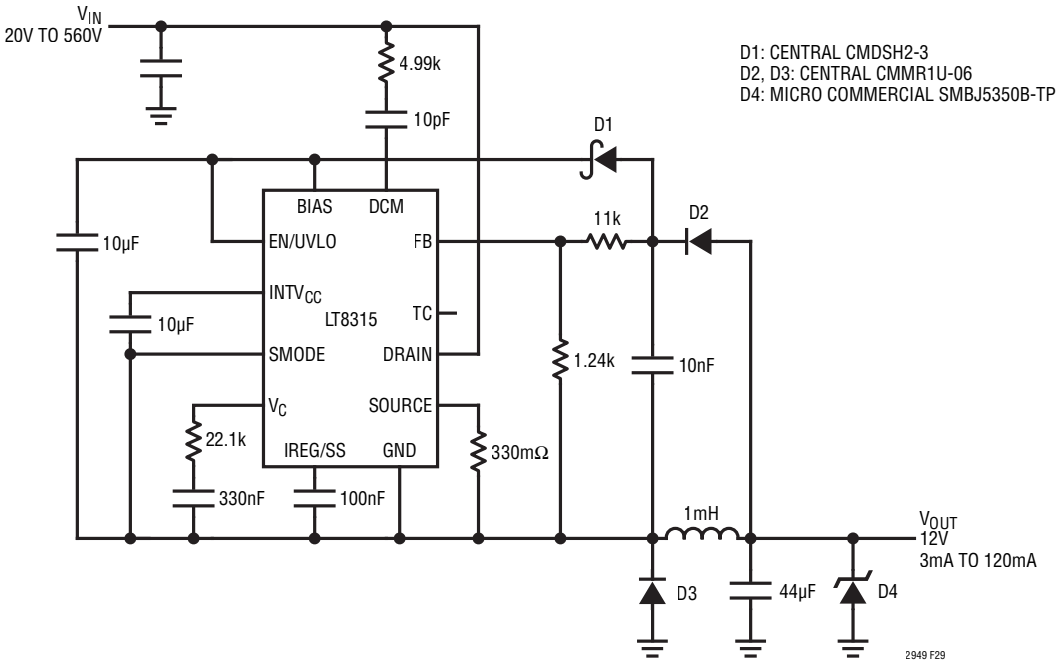


Figure 29. Nonisolated Supply Generation

APPLICATION INFORMATION

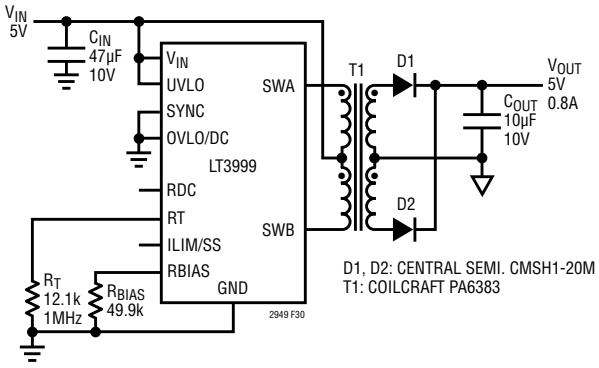


Figure 30. Isolated Supply Generation with Push-Pull Transformer

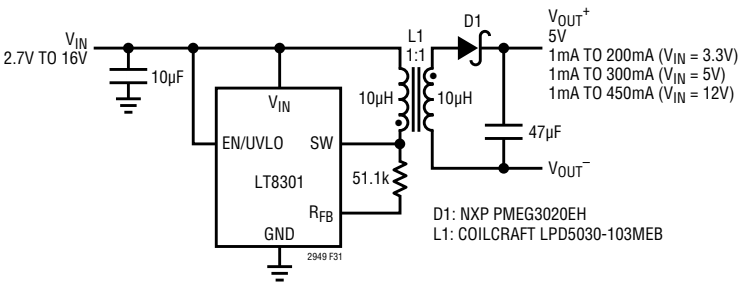


Figure 31. Isolated Supply Generation with Flyback Converter

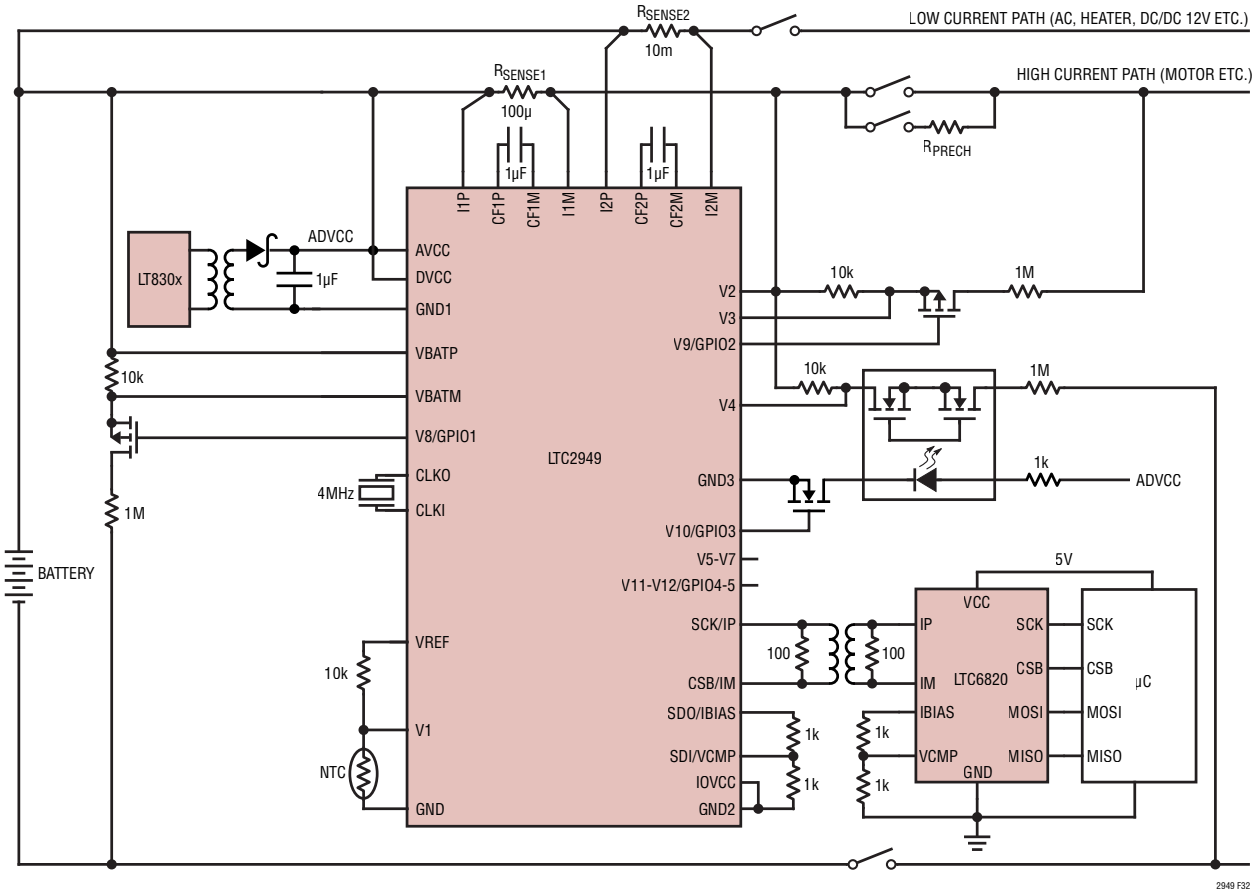
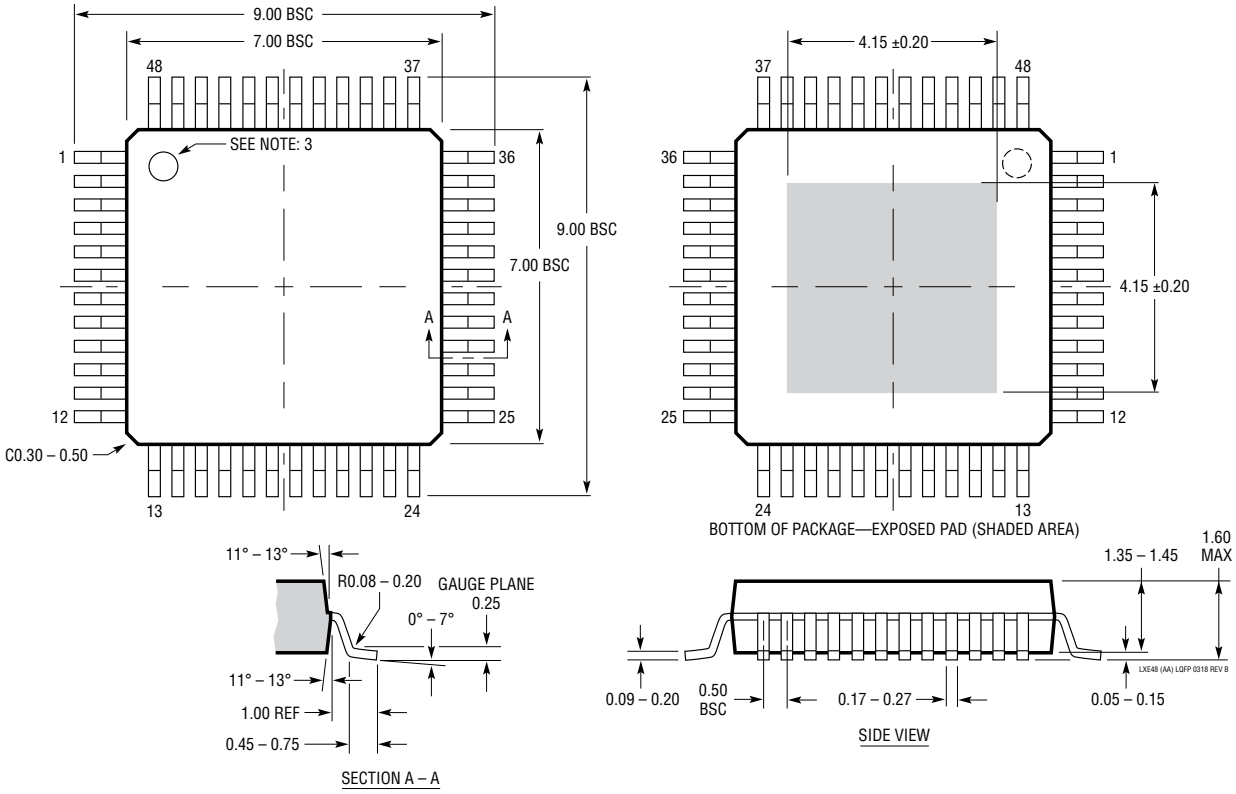


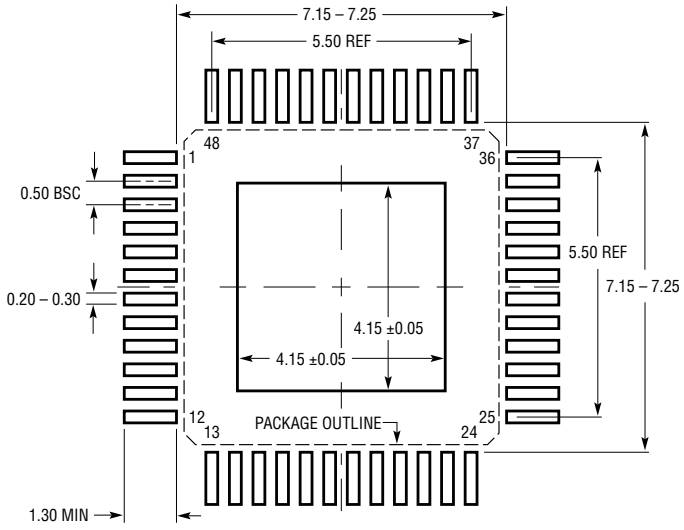
Figure 32. Battery Monitoring with High Side Current Sensing Over Two Sense Resistors, Battery Voltage Measurement, Temperature Measurement and Pre-Charge Voltage Measurement Using Isolated Supply and Isolated NMOS Gate Drive as Well as PhotoMos Relay.

PACKAGE DESCRIPTION

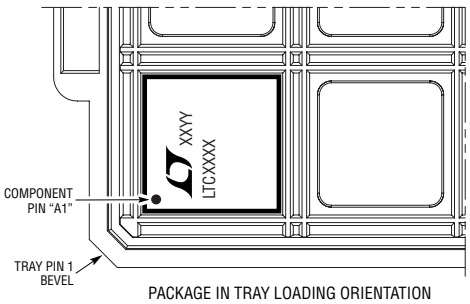
LXE Package
48-Lead Plastic Exposed Pad LQFP (7mm × 7mm)
(Reference LTC DWG #05-08-1927 Rev B)
Exposed Pad Variation AA



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND ON ANY SIDE OF EXPOSED PAD, MAX 0.50mm (20 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION
4. DRAWING IS NOT TO SCALE



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



PACKAGE IN TRAY LOADING ORIENTATION

Rev A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/20	Changed GPOx to GPIOx.	Throughout
		Moved Temperature Measurement into sub-section Application Information.	2
		Adapted Abs Max of SDO.	3
		Changed TYP value of V_{BYP2} in EC-table.	4
		Changed Input Leakage current for CFPx from 40nA to 60nA.	4
		Adapted I_{CC} Average Supply Current in EC table and in text Modes of Operation.	4,15
		Changed Input Leakage current for Voltage Measurement by Power ADC from 10nA to 60nA.	5
		Symbol names corrections in EC table.	6
		Changed Input Leakage current for Voltage Measurement by AUXILIARY ADC from 10nA to 60nA.	6
		EC-Table External Clock Frequency adapted MIN value.	7
		Adapted t_{IDLE} MAX value.	8
		Adapted V_A Transmitter Pulse Amplitude MAX value.	8
		Corrected symbol A_{TCMP} in V_{ICMP}.	8
		Corrected symbol V_{ICM} in A_{TCMP} wrong.	8
		Corrected Pin 6 missing in list of DNC-pins.	12
		Core states vs fast conversions: Update of Figure 1.	15
		Corrected wrong Figure 29.	16
		Corrected wrong minimum frequency of 200kHz.	20
		Corrected missing unit at first column of Table 3.	21
		ISORPT still in register map table: Removed.	41
		Register name typos: Corrected Register Map.	41
		ADC limit behavior: Added sentence after Table 28.	48
		Register name typos: Corrected Tables 71 and 72.	65, 66
		Adapted Description of MUX[1-4]GC in Table 73.	66
		Corrected Wrong Figure 1.	74
		MOSFET polarities: Update of several transistor symbols.	77, 80