36V Nano-Current Two-Input Voltage Monitor

FEATURES

- **850nA Quiescent Current**
- **Operating Range: 2.5V < V_{CC} < 36V**
- **1.5% (Max) Accuracy Over Temperature**
- **Adjustable Reset Threshold**
- **Wide Temperature Range (–40°C to 125°C)**
- **Adjustable IN^+/IN^- Threshold**
- Manual Reset Input
- Compact 2mm × 2mm 8-lead DFN and TSOT-23 (ThinSOT™) Packages

APPLICATIONS

- Portable Equipment
- Battery Powered Equipment
- Security Systems
- Automotive Systems

LTC2960 Option Table

Option	Inputs	Reset Timeout Period	Output Type
LTC2960-1	ADJ/IN^+	15ms/200ms	36V Open-Drain
LTC2960-2	ADJ/IN^-	15ms/200ms	36V Open-Drain
LTC2960-3	ADJ/IN^+	200ms	Active Pull-Up
LTC2960-4	ADJ/IN^-	200ms	Active Pull-Up

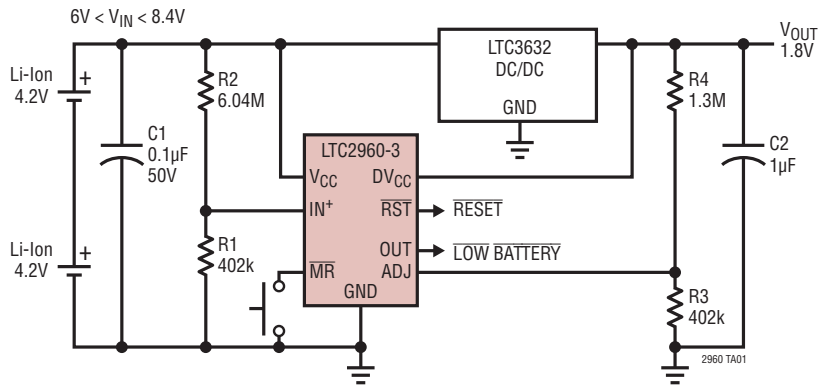
DESCRIPTION

The LTC®2960 is a nano-current, high voltage two-input voltage monitor, ideally suited for multicell battery applications. External resistive dividers configure custom comparator thresholds. The supervisory circuit monitors the ADJ input and pulls the $\overline{RST}$ output low when the input drops below threshold. A reset timeout period delays the return of the $\overline{RST}$ output to a high state when the input rises above the threshold. The spare comparator allows voltage conditions to be detected with either a non-inverting input, IN^+(LTC2960-1/LTC2960-3) or an inverting input, IN^- (LTC2960-2/LTC2960-4). A manual reset ($\overline{MR}$) input is provided for external activation of the reset output.

Other options provided on the LTC2960-1/LTC2960-2 include a reset timeout period select pin, RT, to select between 15ms or 200ms reset timeout periods. The LTC2960-3/LTC2960-4 have a fixed 200ms reset timeout period. The $\overline{RST}$ and OUT outputs are available with active pull-up circuits to an output logic supply pin (LTC2960-3/LTC2960-4) or 36V open-drain outputs (LTC2960-1/LTC2960-2).

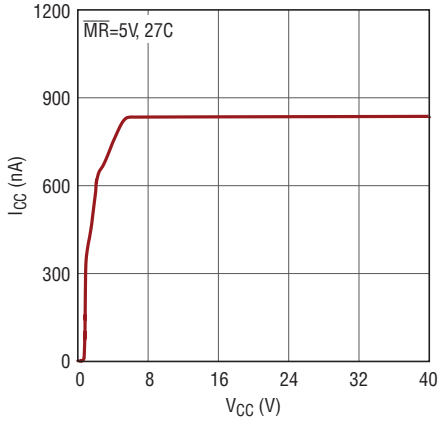
TYPICAL APPLICATION

Battery and Regulator Monitor



POWER-FAIL FALLING THRESHOLD = 6.410V
RESET FALLING THRESHOLD = 1.693V

Supply Current vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

(Notes 1 & 2)

Input Voltages
- V_{CC}, RT, $\overline{MR}$ ..... –0.3V to 40V
- DV_{CC} ..... –0.3V to 6V
- ADJ, IN^+, IN^- ..... –0.3V to 3.5V

Output Voltages (LTC2960-1/LTC2960-2)
- $\overline{RST}$, OUT ..... –0.3V to 40V

Output Voltages (LTC2960-3/LTC2960-4)
- $\overline{RST}$, OUT ($DV_{CC} \geq 1.6V$) ..... –0.3V to (DV_{CC} + 0.3V)
- $\overline{RST}$, OUT (DV_{CC} = GND) ..... –0.3V to 6.3V

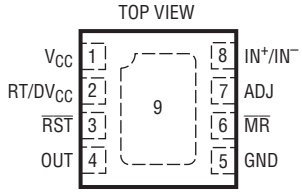
Average Currents
- $\overline{RST}$, OUT ..... ±5mA

Operating Ambient Temperature Range
- LTC2960C ..... 0°C to 70°C
- LTC2960I ..... –40°C to 85°C
- LTC2960H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

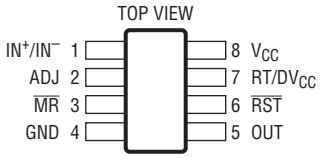
Lead Temperature (Soldering, 10 sec)
- TSOT-23 Package ..... 300°C

PIN CONFIGURATION



DC8 PACKAGE
8-LEAD (2mm × 2mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 80.6°C/W
EXPOSED PAD (PIN 9) PCB GND
CONNECTION OPTIONAL



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 195°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2960CDC-1#TRMPBF	LTC2960CDC-1#TRPBF	LFZZ	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2960IDC-1#TRMPBF	LTC2960IDC-1#TRPBF	LFZZ	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2960HDC-1#TRMPBF	LTC2960HDC-1#TRPBF	LFZZ	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC2960CDC-2#TRMPBF	LTC2960CDC-2#TRPBF	LGBC	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2960IDC-2#TRMPBF	LTC2960IDC-2#TRPBF	LGBC	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2960HDC-2#TRMPBF	LTC2960HDC-2#TRPBF	LGBC	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC2960CDC-3#TRMPBF	LTC2960CDC-3#TRPBF	LFSF	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2960IDC-3#TRMPBF	LTC2960IDC-3#TRPBF	LFSF	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2960HDC-3#TRMPBF	LTC2960HDC-3#TRPBF	LFSF	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C
LTC2960CDC-4#TRMPBF	LTC2960CDC-4#TRPBF	LGBF	8-Lead (2mm × 2mm) Plastic DFN	0°C to 70°C
LTC2960IDC-4#TRMPBF	LTC2960IDC-4#TRPBF	LGBF	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 85°C
LTC2960HDC-4#TRMPBF	LTC2960HDC-4#TRPBF	LGBF	8-Lead (2mm × 2mm) Plastic DFN	–40°C to 125°C

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2960CTS8-1#TRMPBF	LTC2960CTS8-1#TRPBF	LTFZY	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2960ITS8-1#TRMPBF	LTC2960ITS8-1#TRPBF	LTFZY	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2960HTS8-1#TRMPBF	LTC2960HTS8-1#TRPBF	LTFZY	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC2960CTS8-2#TRMPBF	LTC2960CTS8-2#TRPBF	LTGBB	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2960ITS8-2#TRMPBF	LTC2960ITS8-2#TRPBF	LTGBB	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2960HTS8-2#TRMPBF	LTC2960HTS8-2#TRPBF	LTGBB	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC2960CTS8-3#TRMPBF	LTC2960CTS8-3#TRPBF	LTFSD	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2960ITS8-3#TRMPBF	LTC2960ITS8-3#TRPBF	LTFSD	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2960HTS8-3#TRMPBF	LTC2960HTS8-3#TRPBF	LTFSD	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC2960CTS8-4#TRMPBF	LTC2960CTS8-4#TRPBF	LTGBD	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2960ITS8-4#TRMPBF	LTC2960ITS8-4#TRPBF	LTGBD	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC2960HTS8-4#TRMPBF	LTC2960HTS8-4#TRPBF	LTGBD	8-Lead Plastic TSOT-23	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 7V, DV_{CC} = 3.3V unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Input Supply Operating Range		●	2.5		36	V
V_{UVLO}	V_{CC} Undervoltage Lockout V_{CC} Undervoltage Lockout Hysteresis	V_{CC} Rising	●	1.85	 100	2.3	V mV
I_{CC}	V_{CC} Input Supply Current	$\overline{MR}$ = 5V, V_{CC} = 36V, –40°C ≤ T_A ≤ 85°C $\overline{MR}$ = 5V, V_{CC} = 36V, –40°C ≤ T_A ≤ 125°C	● ●	400 400	850 850	1250 2000	nA nA
DV_{CC}	DV_{CC} Input Supply Operating Range		●	1.6		5.5	V
I_{DVCC}	DV_{CC} Input Current	$\overline{RST}$ = OUT = LOW DV_{CC} = 5.5V	●			±50	nA
THRESHOLD ADJUSTMENT INPUTS: ADJ, IN⁺/IN⁻							
V_{TH}	ADJ/IN⁺ Input Threshold IN⁻ Input Threshold	Monitored Voltage Falling Monitored Voltage Rising	● ●	394 394	400 400	406 406	mV mV
V_{THM}	ADJ to IN⁺/IN⁻ Threshold Matching		●		±2	±6	mV
V_{RHYS}	ADJ Threshold Hysteresis	Monitored Voltage Rising	●	8	10	15	mV
V^+_{HYS}	IN⁺ Threshold Hysteresis	Monitored Voltage Rising	●	18	20	25	mV
V^-_{HYS}	IN⁻ Threshold Hysteresis	Monitored Voltage Falling	●	18	20	25	mV
t_{UV}	Under Voltage Detect to $\overline{RST}$, OUT Falling	V = V_{TH} – 40mV	●	80	170	500	µs
$I_{TH(LKG)}$	Input Leakage Current	V = 420mV, –40°C ≤ T_A ≤ 85°C V = 420mV, –40°C ≤ T_A ≤ 125°C	● ●		±0.1 ±0.1	±1 ±10	nA nA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 7V, DV_{CC} = 3.3V unless otherwise noted (Note 2).

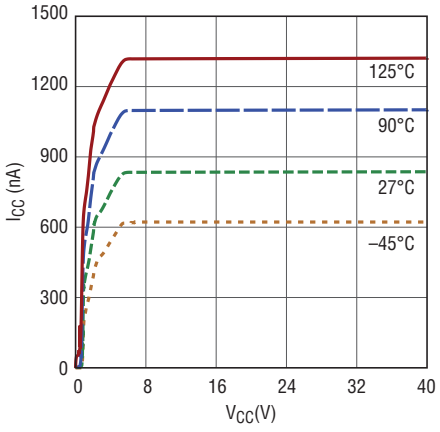
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CONTROL INPUTS: $\overline{MR}$, RT							
V_{RT}	Control Input Threshold RT		●	0.4		1.4	V
V_{MR}	Control Input Threshold $\overline{MR}$		●	0.4		1.4	V
t_{PW}	$\overline{MR}$ Minimum Detectable Pulse Width		●	20			µs
t_{PD}	Propagation Delay to $\overline{RST}$ Falling	Manual Reset Falling	●	1	7	20	µs
V_{MR}	Manual Reset Open Voltage	$\overline{MR}$ Open, $\overline{MR}$ Load = 100nA	●	2.6		4	V
I_{MR}	Manual Reset Low Current	$\overline{MR}$ = 400mV, $V_{CC} \geq$ 2.5V	●	–0.35	–1	–3	µA
I_{LK}	Input Leakage Current	RT = 15V $\overline{MR}$ = 15V	● ●			±100 ±100	nA nA
STATUS OUTPUTS: $\overline{RST}$, OUT							
V_{OL}	Voltage Output Low	V_{CC} = 1.2V, I = 10µA (LTC2960-1/LTC2960-3) V_{CC} = 3V, I = 500µA	● ●		25 100	100 400	mV mV
V_{OH}	Voltage Output High	I = –100µA (LTC2960-3/LTC2960-4)	●	0.7•DV_{CC}			V
I_{OH}	Leakage Current, Output High	V = 5.5V V = 15V (LTC2960-1/LTC2960-2) V = 5.5V, DV_{CC} = GND	● ● ●			±50 ±100 ±50	nA nA nA
I_{SC}	Output Short-Circuit Current	$\overline{RST}$ = GND DV_{CC} = 6V (LTC2960-3/ LTC2960-4) OUT = GND DV_{CC} = 6V (LTC2960-3/ LTC2960-4)	● ●	0.8 0.8		3 3	mA mA
t_{RST}	Reset Timeout Period	LTC2960-3/LTC2960-4 RT Input High RT Input Low	● ● ●	140 140 10	200 200 15	280 280 25	ms ms ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

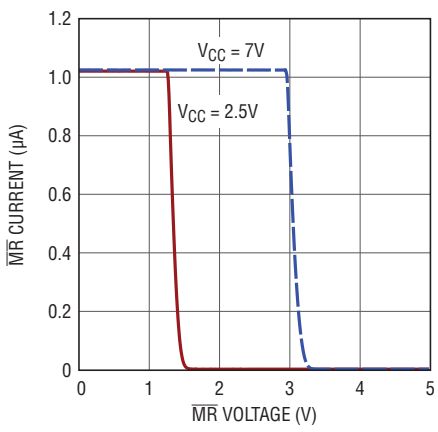
Note 2. All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS

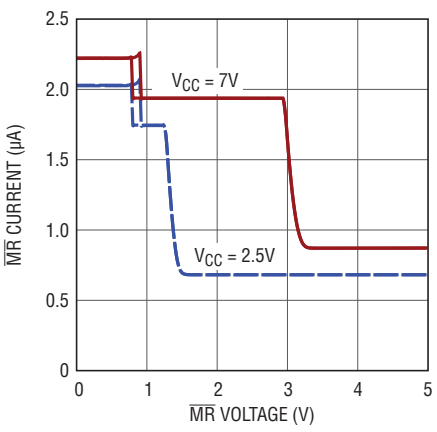
Supply Current vs Supply Voltage



$\overline{MR}$ Current vs $\overline{MR}$ Voltage

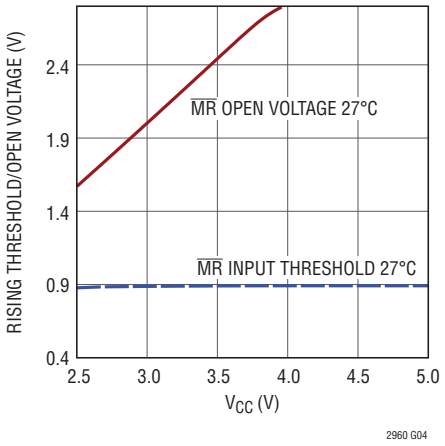


Supply Current vs $\overline{MR}$ Voltage

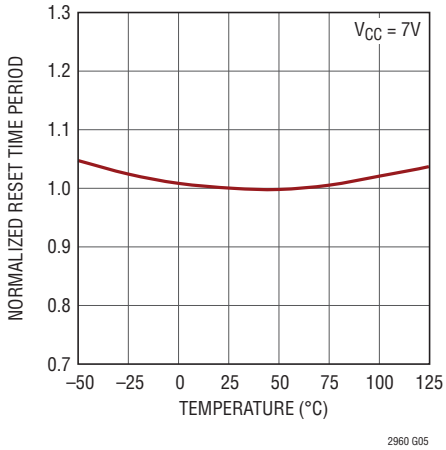


TYPICAL PERFORMANCE CHARACTERISTICS

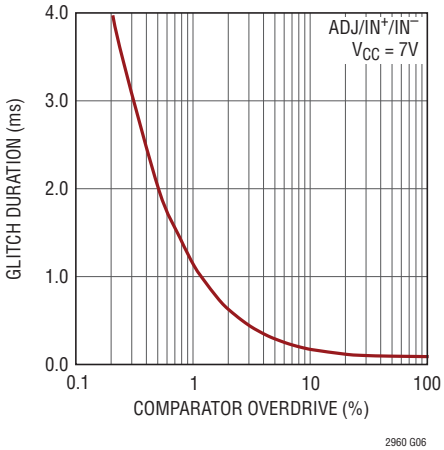
$\overline{MR}$ Rising Threshold/Open Voltage vs V_{CC}



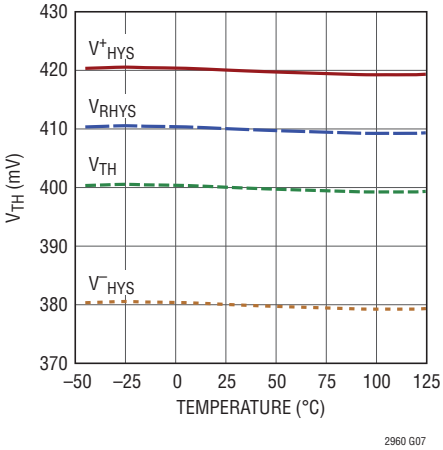
Normalized Reset Timeout Period vs Temperature



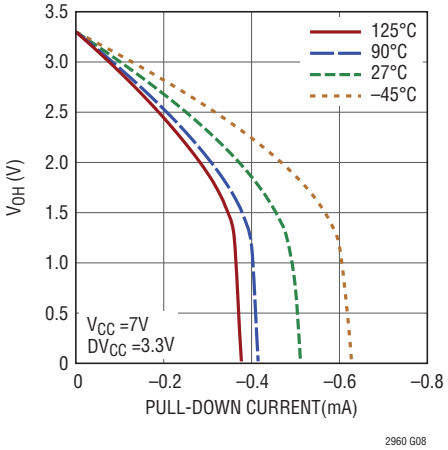
Comparator Overvoltage/ Undervoltage Glitch Immunity



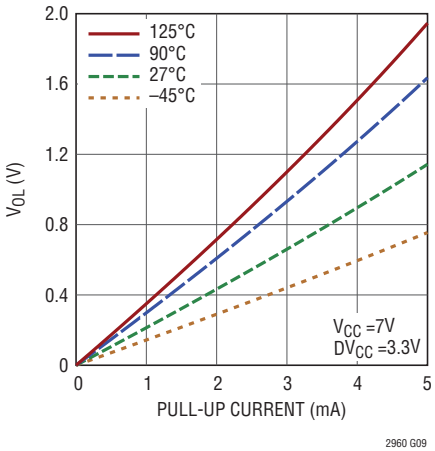
ADJ, IN^+, IN^- Threshold vs Temperature



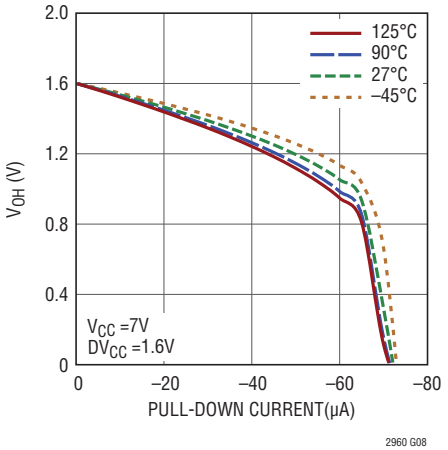
Voltage Output HIGH vs Pull-Down Current ($\overline{RST}$/OUT)



Voltage Output LOW vs Pull-Up Current ($\overline{RST}$/OUT)



Voltage Output HIGH vs Pull-Down Current ($\overline{RST}$/OUT)



PIN FUNCTIONS

ADJ: Reset Threshold Adjustment Input. Tie to resistive divider to configure desired reset threshold.

DV_{CC}: (LTC2960-3/LTC2960-4) Logic Supply Input. Used for setting the logic swing of the $\overline{RST}$ and OUT outputs. Useful for interfacing with logic voltages different from V_{CC}. Bypass DV_{CC} with 0.1µF to GND. Grounding DV_{CC} allows OUT and $\overline{RST}$ to act as open drain outputs.

Exposed Pad (DFN Only): Exposed pad may be left floating or connected to device ground.

GND: Device ground.

IN^-: (LTC2960-2/LTC2960-4) IN^- Threshold Adjustment Input. Tie to resistive divider to configure required threshold. Tie to GND if unused.

IN^+: (LTC2960-1/LTC2960-3) IN^+ Threshold Adjustment Input. Tie to resistive divider to configure required threshold. Tie to GND if unused.

$\overline{MR}$: Manual Reset Input. Attach a push-button switch or logic signal between this input and ground. A logic low on this input pulls $\overline{RST}$ low. When the $\overline{MR}$ input returns to logic high, $\overline{RST}$ returns high after a reset timeout period has expired. Leave open if unused.

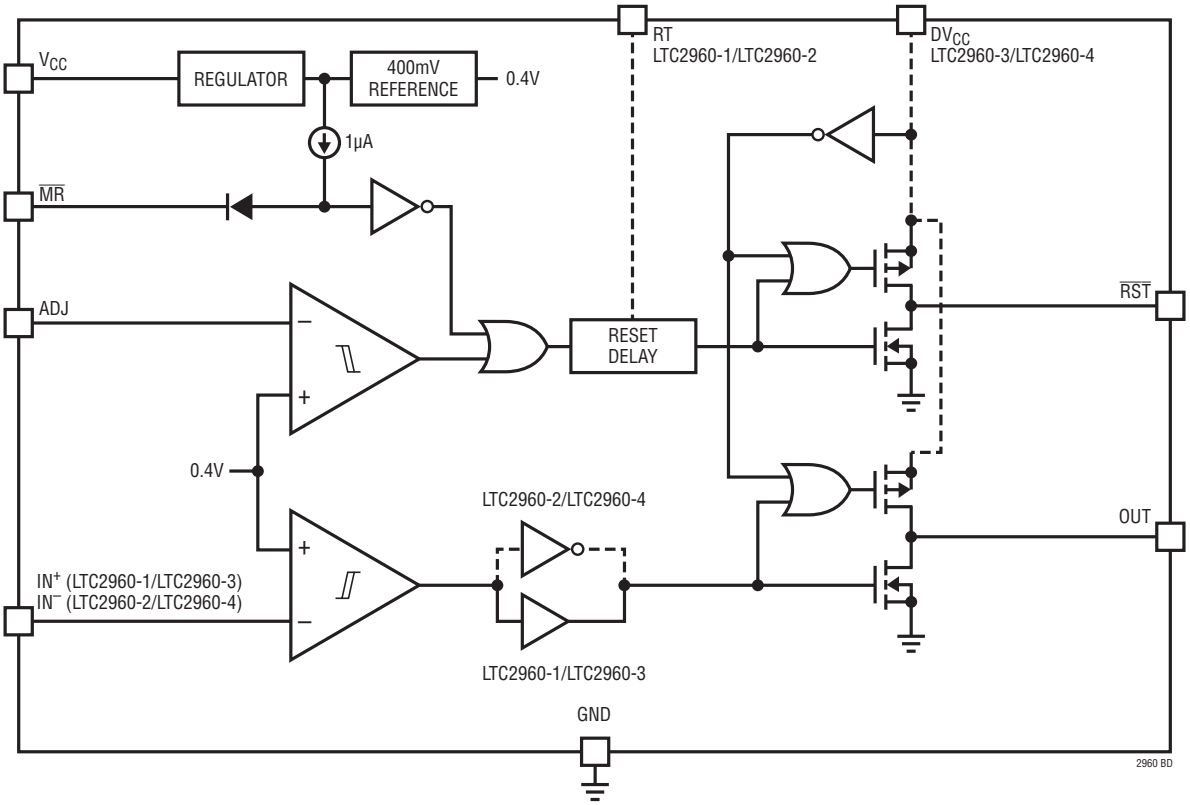
OUT: (LTC2960-1/LTC2960-3) Pulls low when monitored voltage falls below the IN^+ threshold. Released when the IN^+ voltage rises above its threshold by 5%. For the LTC2960-3, OUT is driven by DV_{CC} when logic high. OUT is open drain if DV_{CC} is grounded. Leave open if unused. (LTC2960-2/LTC2960-4) OUT pulls low when the monitored voltage rises above the IN^- threshold. Released when monitored voltage falls below IN^- threshold by 5%. For the LTC2960-4, OUT is driven to DV_{CC} for a logic high. OUT is open drain if DV_{CC} is grounded. Leave open if unused.

$\overline{RST}$: Reset Output. Pulls low when monitored voltage falls below the reset (ADJ) threshold. $\overline{RST}$ is released after monitored voltage exceeds the reset threshold plus 2.5% hysteresis and after reset timeout period has expired. For the LTC2960-3/LTC2960-4, $\overline{RST}$ is driven to DV_{CC} for a logic high. $\overline{RST}$ is open drain if DV_{CC} is grounded. Leave open if unused.

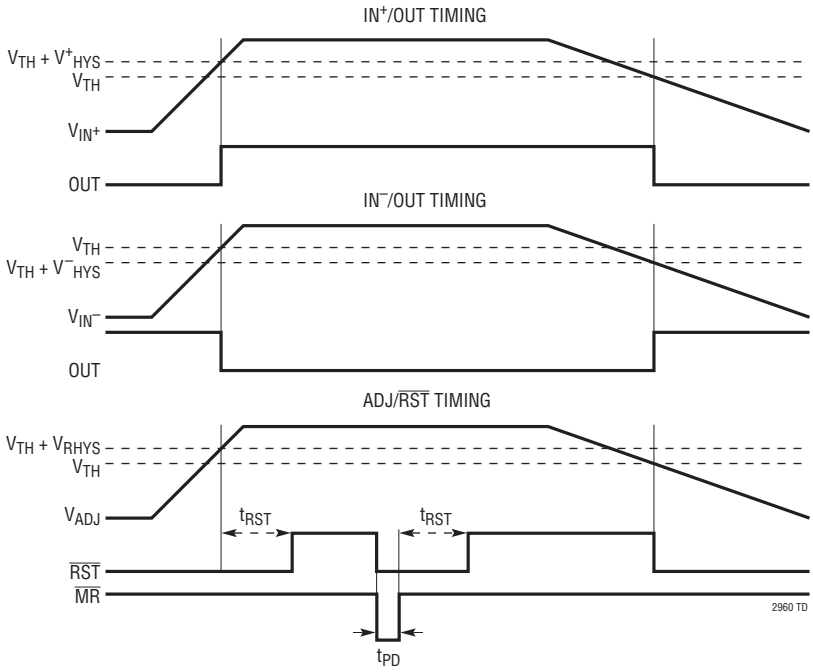
RT: (LTC2960-1/LTC2960-2) Reset Timeout Period Selection Input. Tie to GND for 15ms delay. Tie to V_{CC} for 200ms delay.

V_{CC}: Power Supply Input. When V_{CC} falls below the falling UVLO threshold, the outputs are pulled low. If V_{CC} falls below 1.2V the logic state of the outputs cannot be guaranteed. Bypass V_{CC} with 0.1µF to GND. Use appropriate voltage rating for bypass capacitor.

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

VOLTAGE MONITORING

The LTC2960 is a voltage supervisor with a wide operating voltage range up to 36V with only 850nA quiescent current. The supervisor has two outputs, $\overline{RST}$ and OUT that provide voltage monitoring capabilities for system power-up, power-down and brown-out conditions. Built-in hysteresis and a reset timeout period ensure that fluctuations due to load transients or supply noise do not cause chattering of the status outputs. The LTC2960 can provide reset and voltage status signals to a microprocessor based system or can alternatively be used as an Under Voltage Lock Out (UVLO) for DC/DC switchers or LDOs for control over a battery operated system.

If the monitored voltage drops below the reset threshold, $\overline{RST}$ pulls low until the ADJ input rises above 0.4V plus 2.5% hysteresis. An internal reset timer delays the return of the $\overline{RST}$ output to a high state to provide monitored voltage settling and initialization time. The $\overline{RST}$ output is typically connected to a processor reset input.

If the monitored supply voltage falls to the IN^+ (LTC2960-1/LTC2960-3) threshold, the spare comparator pulls OUT low. OUT remains low until the IN^+ input rises above 0.4V plus 5% hysteresis. OUT is typically used to signal preparation for controlled shutdown. For example, the OUT output may be connected to a processor nonmaskable interrupt (NMI). Upon interrupt, the processor begins shutdown procedures such as supply sequencing and/or storage/erasure of system state in nonvolatile memory.

If the monitored supply voltage rises to the IN^- threshold (LTC2960-2/LTC2960-4), the spare comparator pulls OUT low. OUT remains low until the IN^- falls below 0.4V minus 5% hysteresis. The LTC2960-2/LTC2960-4 operates as an undervoltage and overvoltage monitor.

Few, if any, external components are necessary for reliable operation. However, a decoupling capacitor between V_{CC} and ground is recommended (0.01µF minimum). Use a capacitor with a compatible voltage rating.

THRESHOLD CONFIGURATION

The LTC2960 monitors voltage applied to its inputs IN^+/IN^- and ADJ. A resistive divider connected between a monitored voltage and ground is used to bias the inputs. Figure 1 demonstrates how the inputs can be made dependent upon a single voltage (V1). Only three resistors are required. To calculate their values, specify desired falling reset (V_R) and IN^+ (V_{IN+}) thresholds with $V_{IN+} > V_R$. For example:

$V_{IN+} = 6.4V$, $V_R = 6V$

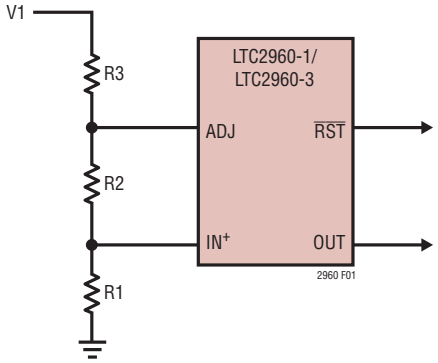


Figure 1. Configuration for Single Voltage Monitoring

The solution for R1, R2 and R3 provides three equations and three unknowns. Maximum resistor size is governed by maximum input leakage current. For the LTC2960, the maximum input leakage current below 85°C is 1nA. For a maximum error of 1% due to both input currents, the resistor divider current should be at least 100 times the sum of the leakage currents, or 0.2µA. If the total divider resistance is chosen arbitrarily to be 8MΩ, such as in this example, then the current is 750nA at the reset threshold. This results in a leakage current error well below 1%. For R_{SUM} = 8MΩ, then:

$R_{SUM} = R1 + R2 + R3$

Both the falling reset and IN^+ thresholds are 0.4V, so:

$$R1 = \frac{V_{TH} \bullet R_{SUM}}{V_{IN+}} = \frac{0.4V \bullet 8M\Omega}{6.4V} = 500k$$

The closest 1% value is 499k. R2 can be determined from:

$$R2 = \frac{V_{TH} \bullet R_{SUM}}{V_R} - R1 = \frac{0.4V \bullet 8M\Omega}{6V} - 499k$$

$R2 = 34.33k$

APPLICATIONS INFORMATION

The closest 1% resistor value is 34k. R3 is easily obtained from:

$R3 = R_{SUM} – R1 – R2 = 8M – 499k – 34k$

$R3 = 7.467M\Omega$

The closest 1% resistor value is 7.5MΩ. Plugging the standard values back into the equations yields the design values for the falling reset and IN^+ voltages:

$V_{IN^+} = 6.4V$, $V_{RST} = 6.028V$

Figure 2 demonstrates how the inputs can be biased to monitor two voltages (V1, V2). In this example, four resistors are required. Calculate each divider ratio for the desired falling threshold (V_{FT}) using:

$$\frac{RnB}{RnA} = \frac{V_{FT}}{V_{TH}} - 1 = \frac{V_{FT}}{0.4V} - 1$$

In Figure 2, OUT is tied back to the $\overline{MR}$ input, making the state of the $\overline{RST}$ output dependent upon both V1 and V2. If V1 and V2 are both above the configured falling threshold plus hysteresis, $\overline{RST}$ is allowed to pull high. If independent operation of the status outputs is desired, simply omit the OUT and $\overline{MR}$ connection.

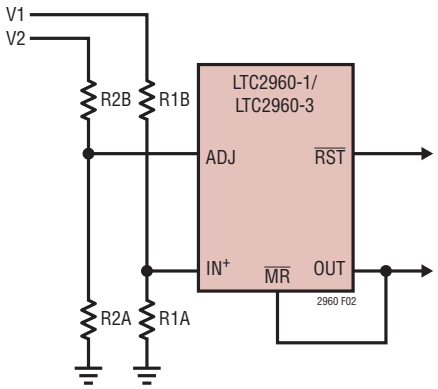


Figure 2. Dual Voltage Monitoring

SELECTING OUTPUT LOGIC STYLE

The LTC2960 status outputs are available in two options: open-drain (LTC2960-1/LTC2960-2) or active pull-up with the DV_{CC} pin replacing the RT pin (LTC2960-3/LTC2960-4). The open-drain option allows the outputs to be pulled up to a user defined voltage up to 36V with a resistor. The open-drain pull-up voltage may be greater than V_{CC}. Select a resistor compatible with desired output rise time and load current specifications. Figure 3 demonstrates typical LTC2960-1 OUT output behavior. When the status outputs are low, power is dissipated in the pull-up resistors.

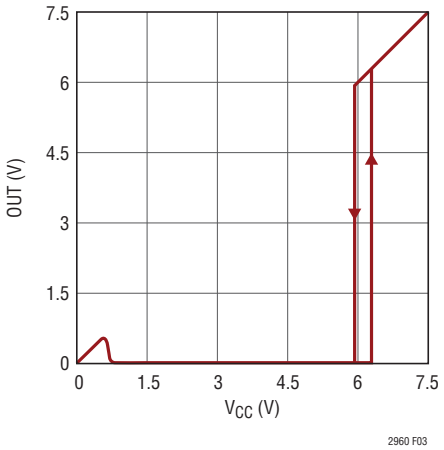


Figure 3. OUT vs V_{CC} (LTC2960-1) Externally Configured for 6V Threshold with $\overline{RST}$ Tied to V_{CC} Through Pull-Up Resistor

The outputs of both the LTC2960-3 and LTC2960-4 can be configured as either low voltage active pull-up or open-drain. This is done by tying the DV_{CC} pin to either a supply or GND. Using the active pull-up configuration, DV_{CC} tied to a supply, lowers power dissipation by eliminating the static current drawn by pull-up resistors when the outputs are low and improves output rise time. In Figure 4(a), an LTC2960-3 has active pull-up outputs configured by tying DV_{CC} to a 1.6V to 5.5V supply. In Figure 4(b), the LTC2960-3 has open-drain outputs configured by tying the DV_{CC} pin to ground. When DV_{CC} is connected to ground both outputs are open-drain and pull-up resistors are required.

Some applications require $\overline{RST}$ and/or OUT outputs to be valid with V_{CC} down to ground when DV_{CC} is tied to V_{CC}. Active pull-up satisfies this requirement with the addition of an optional external resistor from the output to ground. The resistor provides a path for leakage currents, preventing the output from floating to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the

APPLICATIONS INFORMATION

pull-up circuitry. A 100k resistor from output to ground is satisfactory for most applications. When the status outputs are high, power is dissipated in the pull-down resistors.

If V_{CC} falls below the falling UVLO threshold, the outputs are pulled to ground. The outputs are guaranteed to stay low for $V_{CC} \geq 1.2V$ regardless of the output logic configuration. When $V_{CC} < 1.2V$, the active pull-up output behaves similarly to an open-drain output with a pull-up resistor.

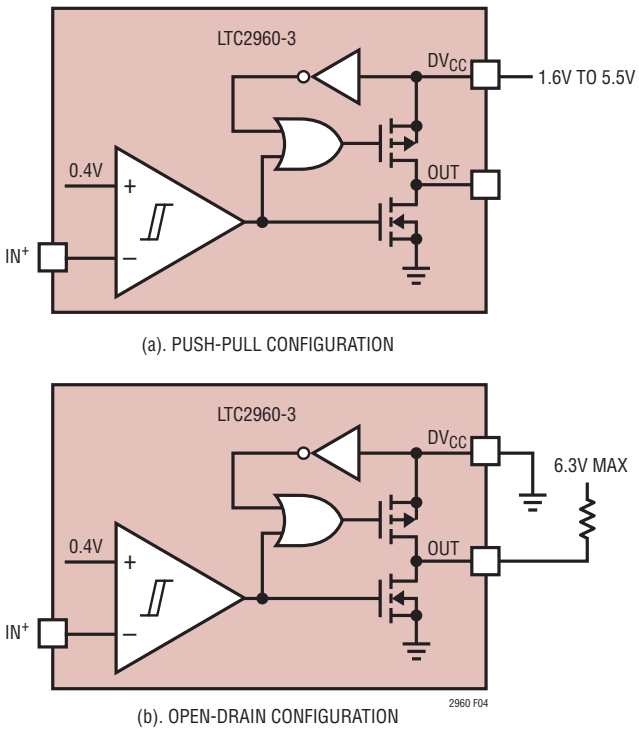


Figure 4. LTC2960-3 (LTC2960-4) $\overline{RST}$ and OUT Outputs Are Configurable as Push-Pull or Open-Drain

MANUAL RESET INPUT

When ADJ is above its reset threshold and the manual reset input ($\overline{MR}$) is pulled low, the $\overline{RST}$ output is forced low. $\overline{RST}$ remains low for the selected reset timeout period after the manual reset input is released and pulled high. The manual reset input is pulled up internally through a 1µA current source to an internal bias voltage (see Electrical Characteristics). If external leakage currents have the ability to pull down the manual reset input below its logic threshold, a pull-up resistor placed between V_{CC} and $\overline{MR}$ is a solution to this issue. The $\overline{MR}$ input can be pulled to 36V maximum and will not affect the internal circuitry. Input $\overline{MR}$ is often pulled down through the use of a pushbutton switch.

SELECTING THE RESET TIMEOUT PERIOD

Use the RT input (LTC2960-1/ LTC2960-2) to select between two fixed reset timeout periods. Connect RT to ground for a 15ms timeout. Connect RT to V_{CC} for a 200ms timeout. The reset timeout period occurs after the ADJ input is driven above threshold and the $\overline{MR}$ input transitions above its logic threshold. After the reset timeout period, the $\overline{RST}$ output is allowed to pull up to a high state as shown in Figure 5. The RT input is replaced by the DV_{CC} input in the LTC2960-3/LTC2960-4 options and the reset timeout period defaults to 200ms.

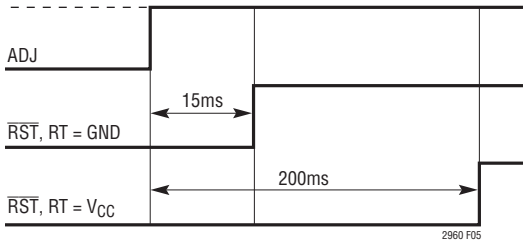


Figure 5. Selectable Reset Timeout Period

EXTERNAL HYSTERESIS

The LTC2960 IN^+ comparator hysteresis is 20mV (V^+_{HYS}), or 5% referred to V_{TH}. Certain applications require more than the built-in native hysteresis. The application schematic in Figure 6 adds one additional resistor (R6) to a typical attenuator network. The procedure below is used to determine a value for R6 to provide an increase over the native hysteresis. In this example, it is desired to double the native hysteresis from 300mV to 600mV and achieve a falling threshold of 6V.

Before including R6, the rising threshold (V_R) is 6.293V while the falling threshold (V_F) is 5.993V. The hysteresis referred to V_A is calculated from:

$$V_{HYST(VA)} = V_{PHYS}\left(1+\frac{R4}{R5}\right)=20mV \bullet 15 = 300mV$$

APPLICATIONS INFORMATION

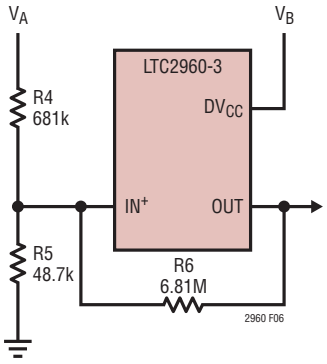


Figure 6. External Hysteresis

The addition of R6 allows OUT to sink or source current to the summing junction at IN+. Neglecting internal switch resistances and providing that R6 >> R5, the externally modified hysteresis (referred to V_A) becomes:

$$V_{HEXT} \approx V_{HYS(VA)} + V_B\left(\frac{R4}{R6}\right)$$

Since the amount of hysteresis is to be doubled, the second term in the above expression needs to be about 300mV. With a logic supply, V_B, equal to 3V, the ratio R4/R6 should be about 0.1. Choosing R6 to be 6.81M satisfies the design criteria.

The addition of R6 modifies the rising and falling thresholds originally determined by R4 and R5. The modified rising threshold becomes:

$$V_R = \left(V_{TH} + V^+_{HYS}\right) \bullet \left(1 + \frac{R4}{R5} + \frac{R4}{R6}\right)$$

$$= (400mV + 20mV) \bullet (1 + 13.98 + 0.1)$$

$$= 6.3336V$$

It is apparent that the R4/R6 term does not affect the rising threshold significantly resulting in a change of only +0.645%. The falling threshold incorporating R6 is:

$$V_F = V_{TH}\left(1 + \frac{R4}{R5} + \frac{R4}{R6}\left(\frac{V_{TH} - V_B}{V_{TH}}\right)\right)$$

$$= 0.4V \bullet (1 + 13.98 - 0.65) = 5.732V$$

The falling threshold can be restored to the original value by reducing the value of R5. Under the assumption that the addition of R6 has a negligible impact on the rising threshold, a new R4/R5 ratio can be calculated as shown:

$$\frac{R4}{R5} = \frac{V_R}{\left(V_{TH} + V^+_{HYS}\right)} - 1 = \frac{6.6V}{420mV} - 1 = 14.71$$

Given the ratio of R4/R5, the closest 1% resistor value for R5 is 46.4k. With the actual resistor values now known, the final thresholds can be calculated by plugging the values into the equations above for V_R and V_F to obtain:

$$V_R = 6.626V,\ V_F = 6.010V,\ V_{HYST} = 616mV$$

As a result of the added current component through R6 an error term exists that is a function of the pull-up voltage, V_B in Figure 6.

Operation with Supply Transients over 40V and Hot Swapping

The circuit in Figure 7(a) allows the LTC2960 to withstand high voltage transients. The magnitude of the voltage transients that can be absorbed is set by the voltage rating of RZ. A TT-IRC pulse-withstanding surface mount 1206 resistor with a nominal voltage rating of 200V is used. The external 30V Zener diode (Z1) and the 143kΩ current limiting resistor (RZ) protect the V_{IN} supply pin of the LTC2960. Note that there is a speed penalty which is the time constant determined by RZ and C1, 14.3ms in this example. If V_{IN} is below 30V, there is a voltage drop across RZ that is dependent on the quiescent current of the LTC2960 which is nominally less than 150mV but can be as high as 290mV if $\overline{MR}$ is pulled low. The maximum voltage drop is determined by the maximum specified I_{CC} and $\overline{MR}$ pull-up currents. For conditions where the Zener conducts current, it can be biased in the microamp range owing to the low quiescent current of the LTC2960. For a supply voltage of 150V, the Zener is biased <1mA. When input pins are used to sense V_{IN}, the input pins ADJ/IN+/IN– absolute maximum rating of 3.5V must not be exceeded. V_{IN} can be a maximum of 8.75x the lowest programmed threshold to satisfy this condition. For a maximum V_{IN} of 150V, the lowest programmable threshold is >17V.

APPLICATIONS INFORMATION

When a supply voltage is abruptly connected to the input resonant ringing can occur as a result of series inductance. The peak voltage could rise to 2x the input supply but in practice can reach 2.5x if a capacitor with a strong voltage coefficient is present. If a 12V supply is hot plugged the resulting ringing could reach the abs max of V_{CC}. Any circuit with an input of more than 7V should be scrutinized for ringing. Circuit board trace inductances of as little as 10nH can produce significant ringing.

One effective means to eliminate ringing is to include a 10–100Ω resistance in series with the supply input before the V_{CC} capacitor shown in Figure 7(b). This provides damping for the resonant circuit but imposes a time constant to V_{CC}. In Figure 7(b), the time constant of RS and C1 is 2µs.

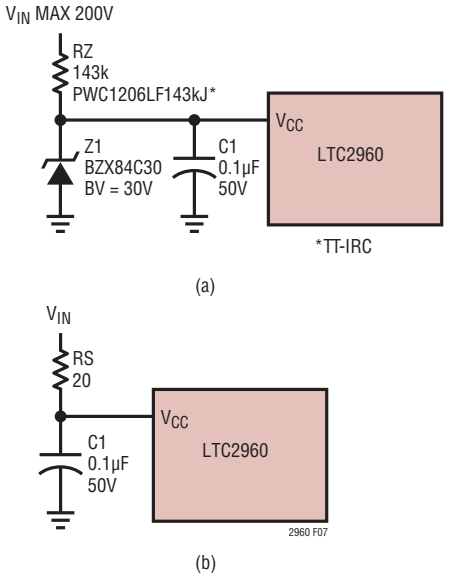


Figure 7. Operation with High Voltage Transients and Hot Swapping

TYPICAL APPLICATIONS

Configurable Regulator UVLO and Low Battery Indicator

In the circuit of Figure 8, the high voltage open drain OUT output is used as a configurable UVLO signal for a switching regulator. A Li-Ion battery can contain protection circuitry that open circuits its terminals through an internal switch when it reaches 2.5V. With a threshold of 5.537V the LTC2960 OUT output disables the load before this occurs in order to prevent damage to the batteries. In addition to the UVLO signal, the LTC2960 provides a low battery indicator for the system. Figure 9 shows an alternative arrangement in which the LTC2960 monitors the output of the 3.3V regulator to provide a reset signal.

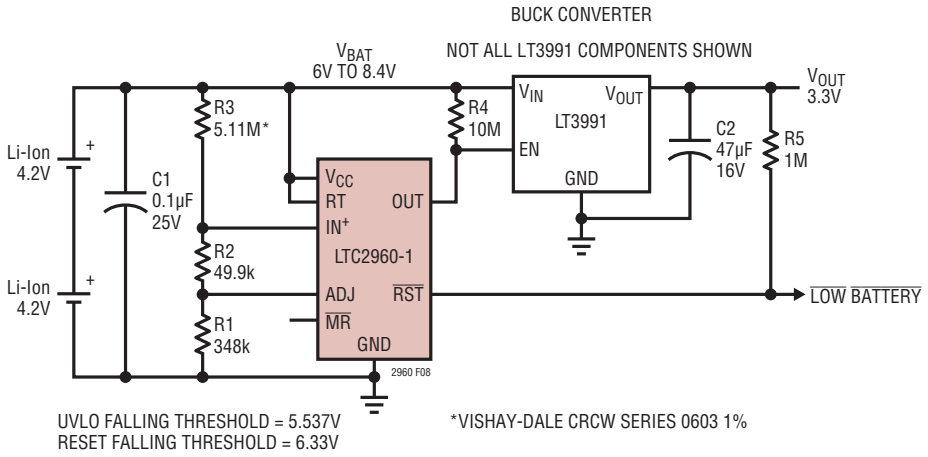


Figure 8. Configurable Regulator UVLO and Low Battery Indicator

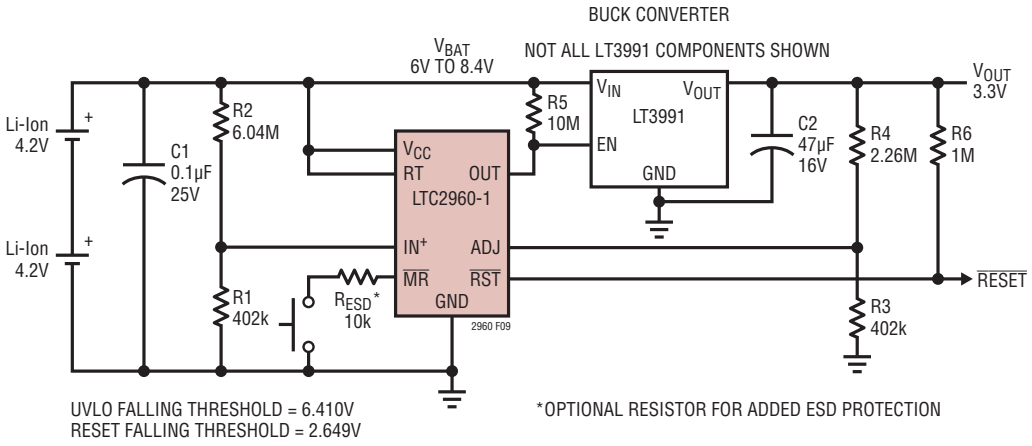


Figure 9. Configurable Regulator UVLO and Supervisor

TYPICAL APPLICATIONS

The LTC2960-2 in Figure 10 is yet another way to prevent excessive discharge of a battery. The high voltage OUT output is used to drive the gate of a PMOS switch to interrupt the path to V_{OUT} in the event of an undervoltage condition. When the battery stack voltage is above the IN^- rising threshold of 5.972V, the PMOS switch is turned on. The LTC2960-2 also supervises V_{OUT} to provide a low battery signal as an early warning of impending shutdown. A 10k resistor is included in series with the V_{CC} pin to limit current in the event of a reverse battery condition. In all three examples, the load drops to <2.5µA typically and excessive battery drain is prevented.

Automotive Supervisor (LTC2960 H-Grade)

The circuit in Figure 11 uses the LTC2960-3 (H-grade) as a low voltage supervisor capable of operating in temperatures up to 125°C in automotive environments. The LT4356 surge stopper limits V_{IN} to 27V under the alternator load

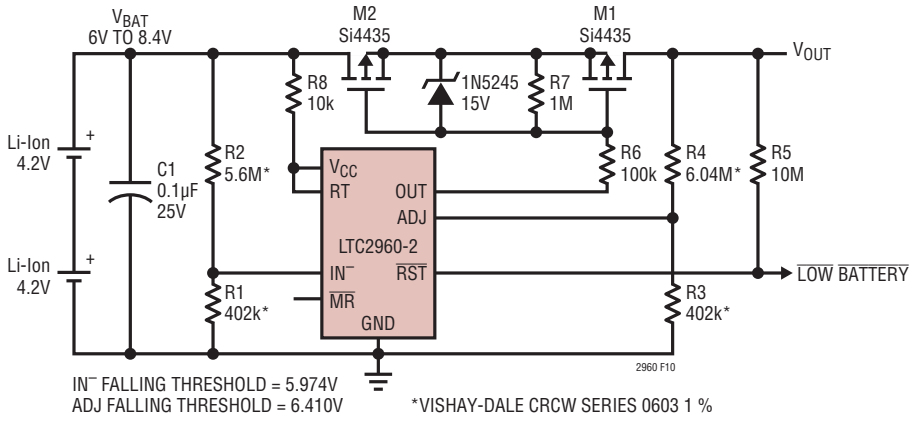


Figure 10. Battery Disconnect to Protect Against Deep Discharge

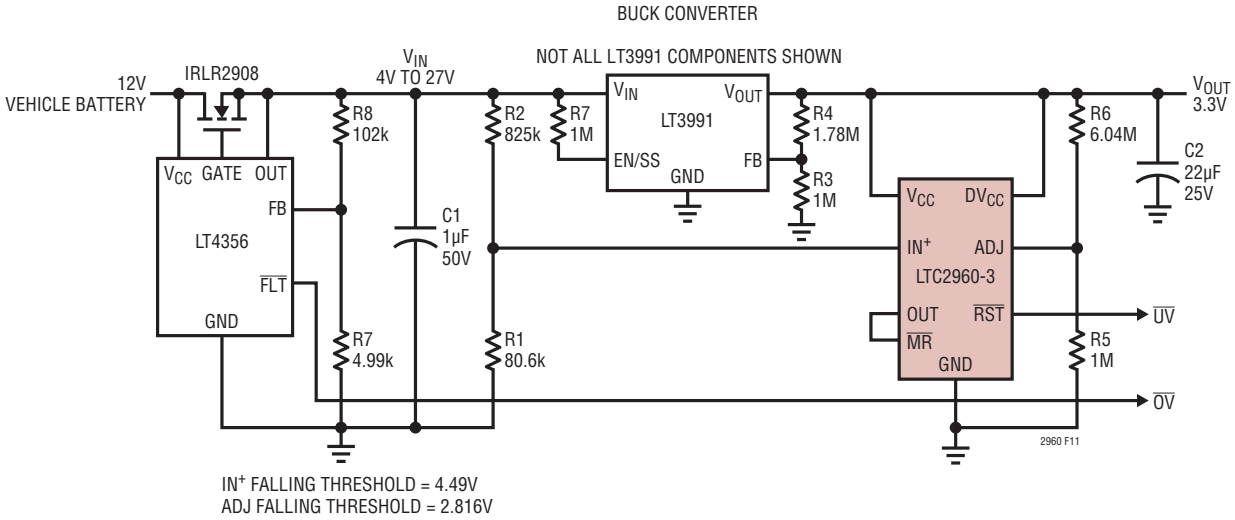


Figure 11. Automotive Supervisor

TYPICAL APPLICATIONS

dump condition. The LT3991 buck regulator in conjunction with the LTC2960 draw <10µA quiescent current for no load, which limits the drain on the vehicle battery even after long periods of inactivity.

Window Comparator for High Voltage Input

The LTC2960-4 can be configured as a window comparator to monitor high voltage supplies or battery stacks as shown in Figure 12. A fault signal is generated if V_{IN} is out of regulation. The OUT output of the LTC2960-4 is fed back into the $\overline{MR}$ input to drive the $\overline{RST}$ output. A micropower LDO provides bias to the active pull-up DV_{CC} supply for low static current draw in the outputs.

Micropower Power Supply Sequencer and Supervisor

Figure 13 illustrates multiple uses for the LTC2960 in a power supply system. U1 is a power supply sequencer whose IN^+ input monitors V_{IN} and enables the 5V switching regulator. The ADJ input monitors the output of the 5V switching regulator and enables the 1.8V LDO after a 16ms Reset Timeout Period. U2 is a supervisor monitoring the 5V and 1.8V outputs. The OUT output by virtue of the $\overline{MR}$ pin, keeps the $\overline{RST}$ output low until the 1.8V supply is ready.

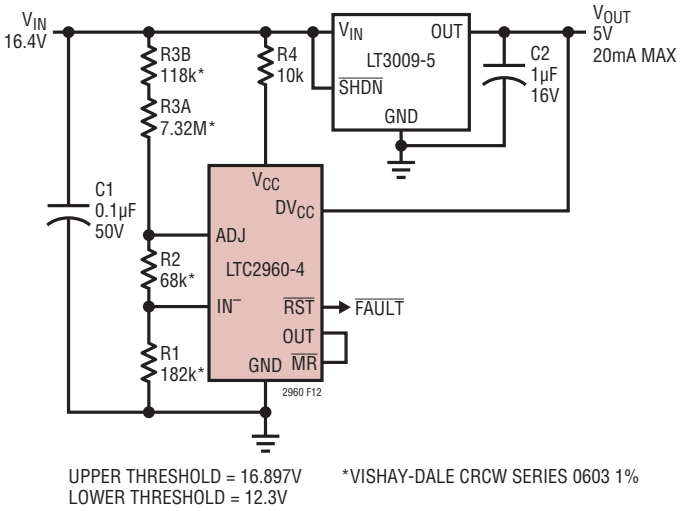
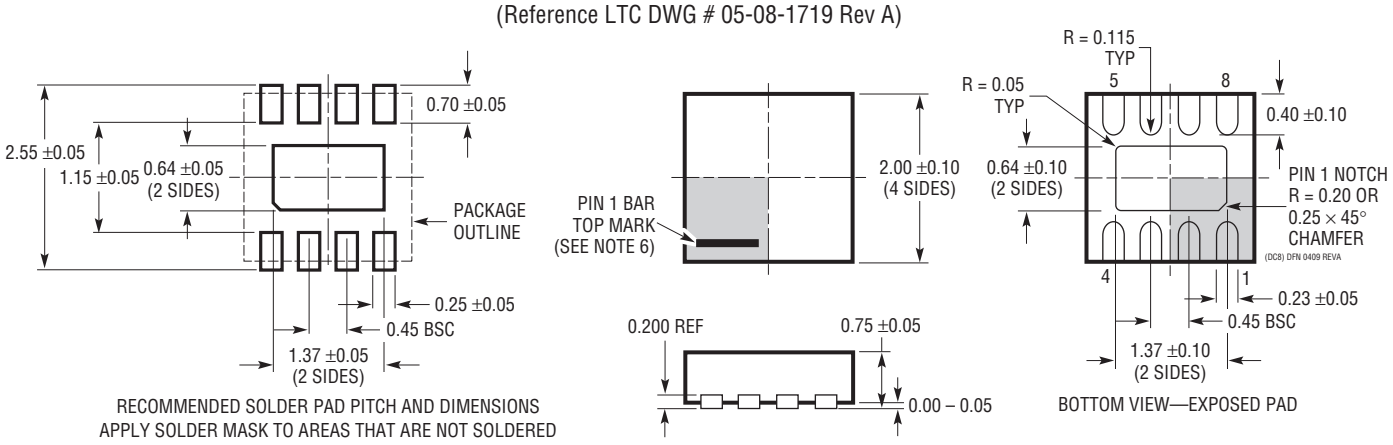


Figure 12. Window Comparator for High Voltage Input

PACKAGE DESCRIPTION

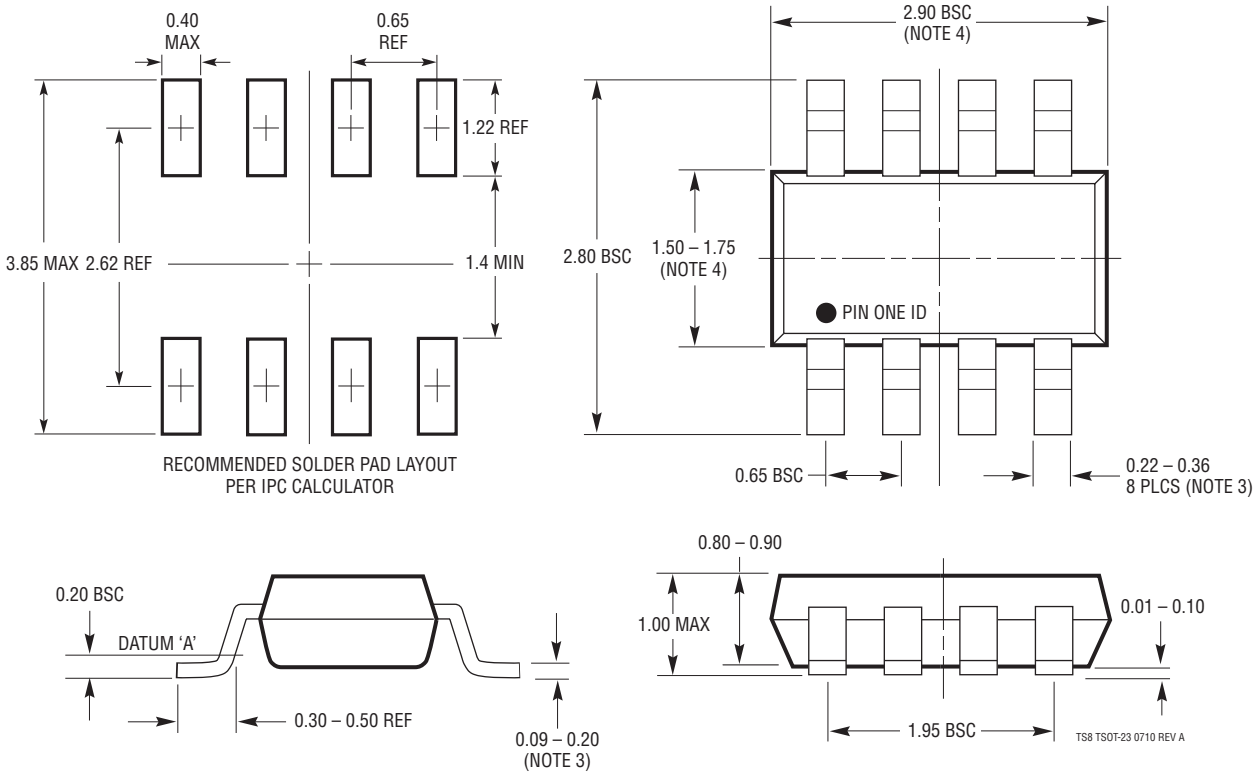
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DC8 Package
8-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1719 Rev A)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/13	Inverted OUT waveform in $\overline{IN}$/OUT Timing Diagram	7