Dual I²C Power Supply Monitor and Margining Controller

FEATURES

- **Less Than ±0.5% Total Unadjusted Error 14-Bit ΔΣ ADC with On-Chip Reference**
- **Dual, 8-Bit IDACs with 1x Voltage Buffers**
- **Linear, Voltage Servo Adjusts Supply Voltages by Ramping IDAC Outputs Up/Down**
- I²C Bus Interface (SMBus Compatible)
- Extensive, User Configurable Fault Monitoring
- On-Chip Temperature Sensor
- Available in 24-Pin 4mm × 5mm QFN Package

APPLICATIONS

- Dual Power Supply Voltage Servo
- Monitoring Supply Voltage and Current
- Programmable Power Supplies
- Programmable Reference

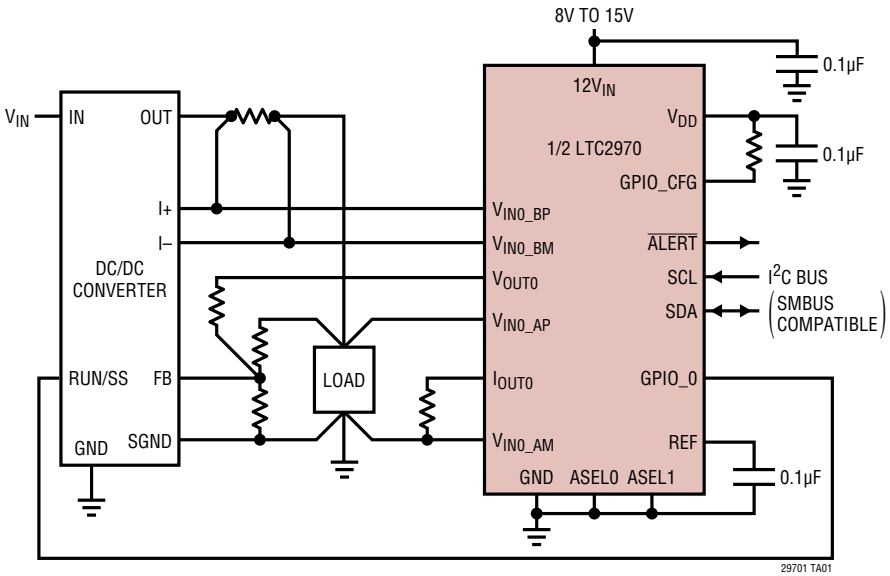
DESCRIPTION

The LTC®2970 is a dual power supply monitor and margining controller with an SMBus compatible I²C bus interface. A low-drift, on-chip reference and 14-bit ΔΣ A/D converter allow precise measurements of supply voltages, load currents or internal die temperature. Fault management allows $\overline{\text{ALERT}}$ to be asserted for configurable overvoltage and undervoltage fault conditions. Two voltage buffered, 8-bit IDACs allow highly accurate programming of DC/DC converter output voltages. The IDACs can be configured to automatically servo the power supplies to the desired voltages using the ADC. The LTC2970-1 adds a tracking feature that can be used to turn multiple power supplies on or off in a controlled manner.

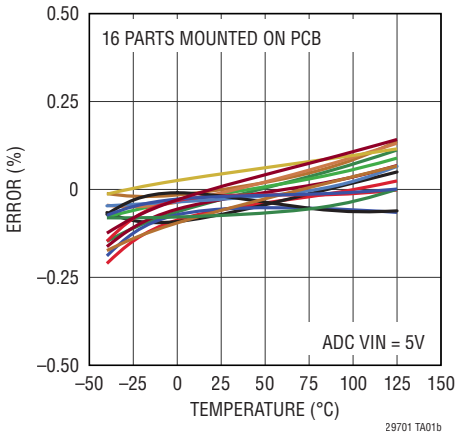
The bus address is set to 1 of 9 possible combinations by pin strapping the ASEL0 and ASEL1 pins. The LTC2970/LTC2970-1 are packaged in a 24-pin, 4mm × 5mm QFN package.

TYPICAL APPLICATION

Dual Power Supply Monitor and Controller (One of Two Channels Shown)



ADC Total Unadjusted Error vs Temperature



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltages:
- V_{DD} ..... –0.3V to 6V
- $12V_{IN}$ ..... –0.3V to 15V

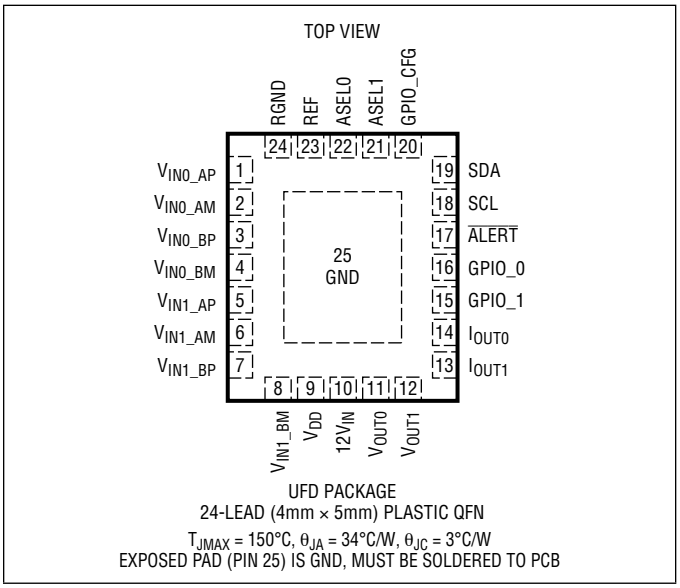
Digital Input/Output Voltages:
- ASEL0, ASEL1 ..... –0.3V to V_{DD} + 0.3V
- SDA, SCL, GPIO_CFG, $\overline{\text{ALERT}}$, GPIO_0, GPIO_1 ..... –0.3V to 6V

Analog Voltages:
- V_{IN0_AP}, V_{IN0_AM}, V_{IN0_BP}, V_{IN0_BM}, V_{IN1_AP}, V_{IN1_AM}, V_{IN1_BP}, V_{IN1_BM}, V_{OUT0}, V_{OUT1} ..... –0.3V to 6V
- I_{OUT0}, I_{OUT1}, REF ..... –0.3V to V_{DD} + 0.3V
- RGND ..... –0.3V to 0.3V

Operating Ambient Temperature Range:
- LTC2970C ..... 0°C to 70°C
- LTC2970I ..... –40°C to 85°C
- LTC2970H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2970#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2970CUFD#PBF	LTC2970CUFD#TRPBF	2970	24-Pin (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC2970CUFD-1#PBF	LTC2970CUFD-1#TRPBF	29701	24-Pin (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC2970IUFD#PBF	LTC2970IUFD#TRPBF	2970	24-Pin (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC2970IUFD-1#PBF	LTC2970IUFD-1#TRPBF	29701	24-Pin (4mm × 5mm) Plastic QFN	–40°C to 85°C
LTC2970HUFD#PBF	LTC2970HUFD#TRPBF	2970	24-Pin (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC2970HUFD-1#PBF	LTC2970HUFD-1#TRPBF	29701	24-Pin (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{12VIN} = 12V, V_{DD} and REF pins floating unless otherwise indicated, C_{VDD} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Characteristics							
I_{V12}	$12V_{IN}$ Supply Current	V_{12VIN} = 12V, V_{DD} Floating	●		4.24	7.5	mA
I_{DD}	V_{DD} Supply Current	V_{DD} = 5V, V_{12VIN} = V_{DD}	●		3.7	5	mA
V_{LKO}	V_{DD} Undervoltage Lockout	V_{DD} Ramping-Down, V_{12VIN} = V_{DD}	●	3.7	4.14	4.4	V
	V_{DD} Undervoltage Lockout Hysteresis				118		mV
V_{DD}	Supply Input Operating Range		●	4.5		5.75	V
	Regulator Output Voltage	8V ≤ V_{12VIN} ≤ 15V, –1mA ≤ I_{VDD} ≤ 0	●	4.75	4.95	5.25	V
	Regulator Output Voltage Temperature Coefficient				10		ppm/°C
	Regulator Output Voltage Load Regulation	–1mA ≤ I_{VDD} ≤ 0			160		ppm/mA
	Regulator Line Regulation	8V ≤ V_{12VIN} ≤ 15V, I_{VDD} = 0mA			80		ppm/V
	Regulator Output Short-Circuit Current	V_{12VIN} = 12V, V_{DD} = 0V	●	–5	–34	–63	mA
V_{12VIN}	$12V_{IN}$ Supply Operating Range		●	8		15	V
Voltage Reference Characteristics							
V_{REF}	Reference Output Voltage				1.229		V
	Reference Voltage Temperature Coefficient				2		ppm/°C
	Reference Overdrive Voltage Input Range		●	1		1.5	V
ADC Characteristics							
N_ADC	Resolution	N_ADC = 8.192V/16384			500		µV/LSB
TUE_ADC	Total Unadjusted Error	V_{IN} = 3V, V_{IN} = V_{INn_xP} – V_{INn_xM} (Note 3)	●			±0.5	%
INL_ADC	Integral Nonlinearity	(Note 4)	●	–4.5	2	4.5	LSB
DNL_ADC	Differential Nonlinearity	(Note 7)	●			±0.5	LSB
V_{IN_ADC}	Input Voltage Range		●	0		6	V
V_{OS_ADC}	Offset Error		●	–1000	–316	1000	µV
	Offset Error Drift				0.19		µV/°C
GAIN_ADC	Gain Error	Full-Scale V_{IN} = 6V	●			±0.4	%
	Gain Error Drift				3		ppm/°C
T_{CONV_ADC}	Conversion Time				33.3		ms
C_{IN_ADC}	Input Sampling Capacitance				3		pF
F_{IN_ADC}	Input Sampling Frequency				61.4		kHz
I_{LEAK_ADC}	Input Leakage Current	0V < V_{IN} < 6V	●			±0.1	µA
IDAC Output Current Characteristics							
N_I_{OUT}	Resolution (Guaranteed Monotonic)			8			Bits
INL_I_{OUT}	Integral Nonlinearity	V_{IOUTn} < V_{DD} – 1.5V	●			±1	LSB
DNL_I_{OUT}	Differential Nonlinearity	V_{IOUTn} < V_{DD} – 1.5V	●			±1	LSB
I_{FS}-I_{OUT}	Full-Scale Output Current	V_{IOUTn} < V_{DD} – 1.5V, DAC Code = 'hff	●	–236	–255	–276	µA
I_{DRIFT}-I_{OUT}	Output Current Drift	DAC Code = 'hff			32		ppm/°C
I_{OS}-I_{OUT}	Offset Current	DAC Code = 'h00	●			±0.1	µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Buffered IDAC Output Characteristics							
INL_V_{OUT}	Integral Nonlinearity	R_{IOUTn} = 10kΩ, No Load on V_{OUTn} (Note 5)	●			±1	LSB
DNL_V_{OUT}	Differential Nonlinearity	R_{IOUTn} = 10kΩ, No Load on V_{OUTn} (Note 5)	●			±1	LSB
V_{OS}-V_{OUT}	Offset Voltage	$V_{OS} = V_{OUTn} - V_{IOUTn}$, No Load on V_{OUTn}	●		1.6	±10	mV
	Output Voltage Drift	No Load on V_{OUTn}			0.17		µV/°C
V_{OUT}	Load Regulation	0.1V < V_{OUTn} < V_{DD} – 1.5V, I_{VOUTn} Source = 1mA			–57		ppm/mA
		0.1V < V_{OUTn} < V_{DD} – 1.5V, I_{VOUTn} Sink = 1mA			100		ppm/mA
	Leakage Current	V_{OUTn} High-Z, 0V ≤ V_{OUTn} ≤ V_{DD}	●		1	±100	nA
	Short-Circuit Current Low	V_{OUTn} Shorted to GND	●			–50	mA
	Short-Circuit Current High	V_{OUTn} Shorted to V_{DD}	●			50	mA
Soft Connect Comparator Characteristics (CMP0, CMP1)							
V_{OS}	Offset Voltage				±3		mV
Temperature Sensor Characteristics							
TMP	Gain				0.25		°C/LSB
12V_{IN} Voltage Divider Characteristics							
GAIN_12V_{IN}	Gain		●	0.329	0.333	0.335	V/V
Digital Inputs SCL, SDA, GPIO_CFG, GPIO_0, GPIO_1							
V_{IH}	High Level Input Voltage	SDA, SCL	●	2.1			V
		GPIO_CFG, GPIO_0, GIPO_1	●	1.6			V
V_{IL}	Low Level Input Voltage	SDA, SCL	●			1.5	V
		GPIO_CFG, GPIO_0, GIPO_1	●			1.0	V
V_{HYST}	Input Hysteresis				0.08		V
I_{LEAK}	Input Leakage Current	0V ≤ V_{IN} ≤ 6V	●			±1	µA
C_{IN}	Input Capacitance				10		pF
Three State Inputs ASEL[1:0]							
V_{IH_ASEL}	Input High Threshold Voltage		●			V_{DD} – 0.5	V
V_{IL_ASEL}	Input Low Threshold Voltage		●	0.5			V
$I_{IN,HL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD}	●			±20	µA
$I_{IN,Z}$	High Z Input Current		●	±2			µA
Open Drain Outputs SDA, GPIO_CFG, GPIO_0, GPIO_1, $\overline{\text{ALERT}}$							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
I_{OH}	Input Leakage Current	0V ≤ V_{IN} ≤ 6V	●			±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Interface Timing Characteristics							
f_{SCL}	Serial Clock Frequency	(Note 6)	●	10		400	kHz
t_{LOW}	Serial Clock Low Period	(Note 6)	●	1.3			µs
t_{HIGH}	Serial Clock High Period	(Note 6)	●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start	(Note 6)	●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time	(Note 6)	●	600			ns
$t_{SU,STA}$	Start Condition Setup Time	(Note 6)	●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time	(Note 6)	●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2970 Receiving Data) Data Hold Time (LTC2970 Transmitting Data)	(Note 6)	●	0 300		 900	ns ns
$t_{SU,DAT}$	Data Setup Time (LTC2970 Receiving Data)	(Note 6)	●	100			ns
t_{SP}	Pulse Width of Spike Suppressed	(Note 6)	●		98		ns
t_{SETUP_GPIO}	GPIO_0 and GPIO_1 Setup Time	GPIO_0 and GPIO_1 input setup time prior to the 26th rising SCL of an IO() I²C read. These inputs must be valid and stable by this time to be returned in the IO() read result. (Note 6)	●	2.5			µs
t_{HOLD_GPIO}	GPIO_0 and GPIO_1 Hold Time	GPIO_0 and GPIO_1 input hold time after the 26th rising SCL of an IO() I²C read. These inputs must be held until this amount of time has elapsed to be returned in the IO() read result. (Note 6)	●	2.5			µs
t_{OUT_GPIO}	GPIO_0 and GPIO_1 Output Time	GPIO_0 and GPIO_1 output delay after the 35th rising SCL of an I²C write. These outputs will become high impedance or begin driving low by this time. (Note 6)	●			2.5	µs
Internal Timers							
$t_{TIMEOUT\_SMB}$	Stuck BUS Timer	The LTC2970 will release the I²C bus and terminate the current command if the command is not completed before this amount of time has elapsed.		24	32	39	ms
t_{SETUP_ADC}	ADC Channel Setup Time	After selecting a new ADC channel, the LTC2970 will wait this amount of time to allow the analog input to settle before beginning an ADC conversion.			304		µs
$t_{TIMEOUT\_SYNC}$	Tracking SYNC Failure Timer	LTC2970-1 Only: The LTC2970-1 will abort a pending SYNC() command if a tracking command is not received before this amount of time has elapsed.			255		ms
t_{HOLD_TRACK}	Tracking IDAC Disconnect Delay	LTC2970-1 Only: After the tracking algorithm asserts CPIO_CFG low, the LTC2970-1 will delay disconnecting the IDACs from the power supply feedback nodes by this amount of time. Used while tracking power supplies on.			32		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SETUP_TRACK}	Tracking IDAC Disconnect Delay	LTC2970-1 Only: After the tracking algorithm asserts CPIO_CFG high, the LTC2970-1 will wait this amount of time before starting to decrement Ch*n*_a_delay_track[9:0]. Used while tracking power supplies off.			32		ms
t_{DEC_TRACK}	Tracking IDAC Decrement Rate	LTC2970-1 Only: The LTC2970-1 changes Ch*n*_a_delay_track[9:0] at this rate.			88		µs/LSB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: TUE (%) is defined as:

$$\%\ \text{Gain Error} + \frac{(\text{INL} \bullet 500\mu\text{V/LSB} + V_{OS})}{V_{IN}} \bullet 100$$

Note 4: Integral nonlinearity (INL) is defined as the deviation of a code from a straight line passing through the actual endpoints (0V and 6V) of the transfer curve. The deviation is measured from the center of the quantization band.

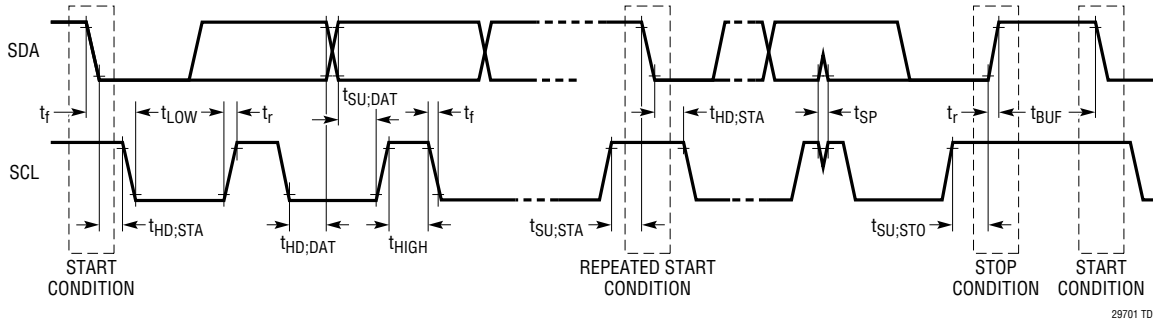
Note 5: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 255 (full-scale).

Note 6: Maximum capacitive load, CB, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: $(20 + 0.1 \bullet C_B)(ns) < t_r < 300ns$ and $(20 + 0.1 \bullet C_B)(ns) < t_f < 300ns$. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is $3V < V_{IO} < 5.5V$.

Note 7: This specification is guaranteed by design.

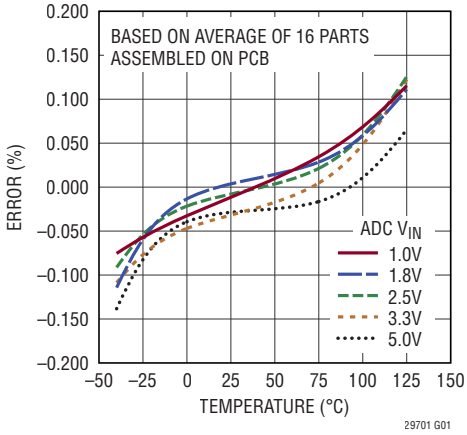
TIMING DIAGRAM

The I²C Bus Specification

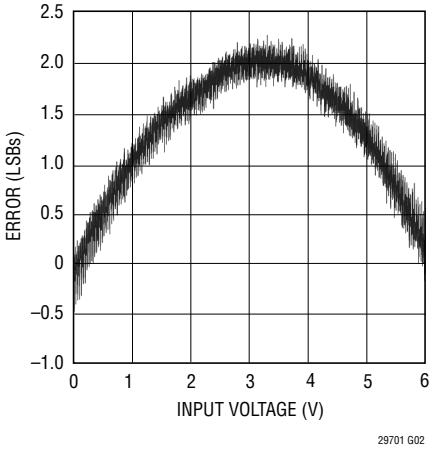


TYPICAL PERFORMANCE CHARACTERISTICS

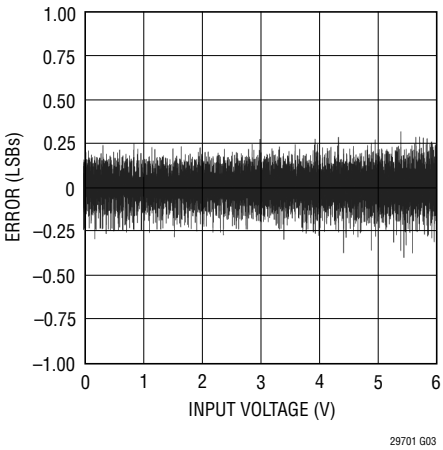
ADC Total Unadjusted Error vs Temperature



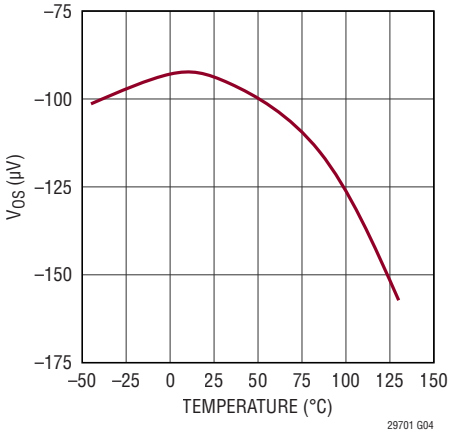
ADC INL



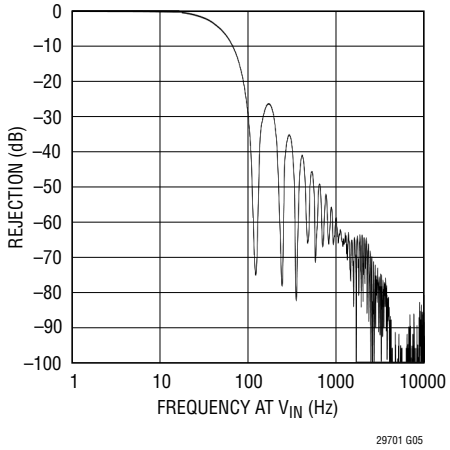
ADC DNL



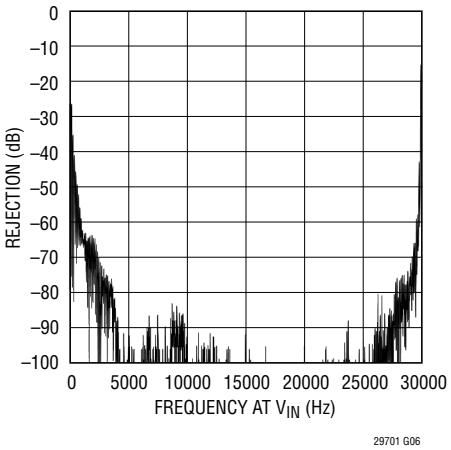
ADC Zero Code Center Offset Voltage vs Temperature



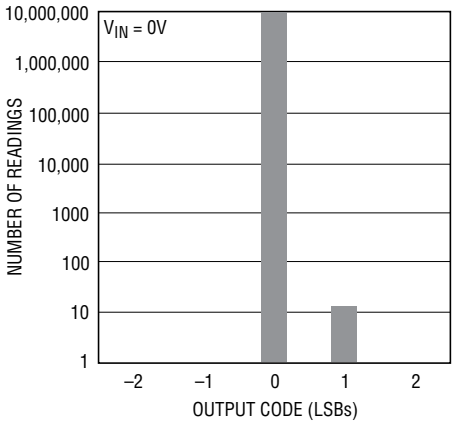
ADC Rejection vs Frequency at V_{IN}



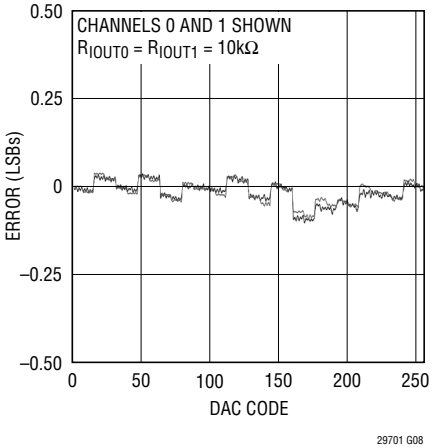
ADC Rejection vs Frequency at V_{IN}



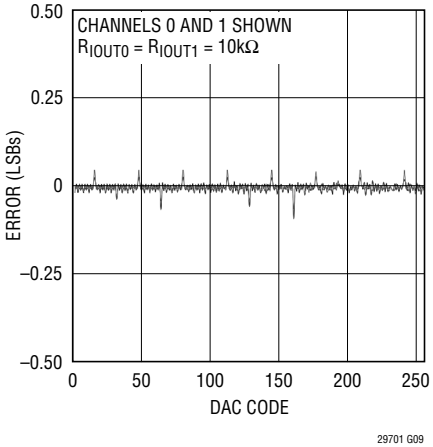
ADC Noise Histogram



Voltage Buffered IDAC INL

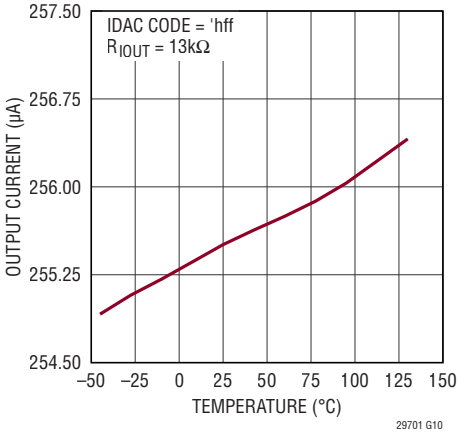


Voltage Buffered IDAC DNL

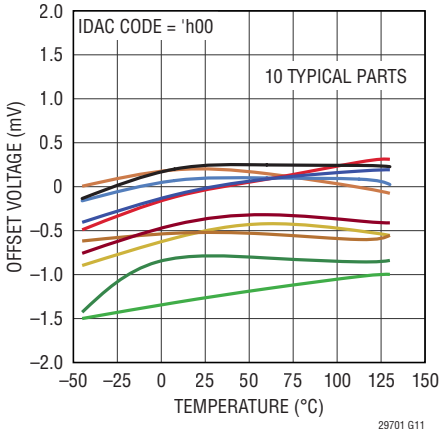


TYPICAL PERFORMANCE CHARACTERISTICS

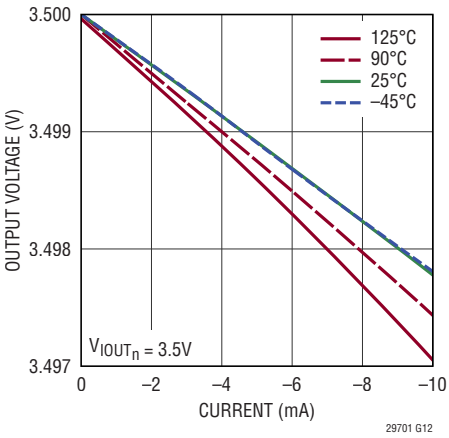
IDAC Output Current vs Temperature



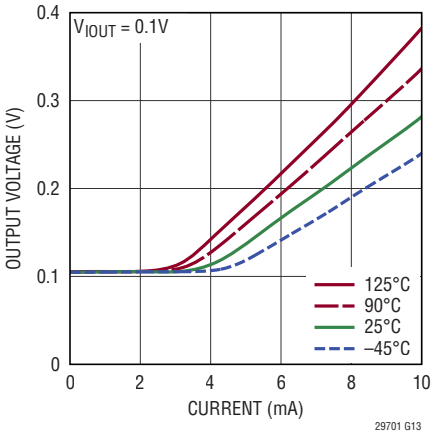
V_{OUTn} Offset Voltage vs Temperature



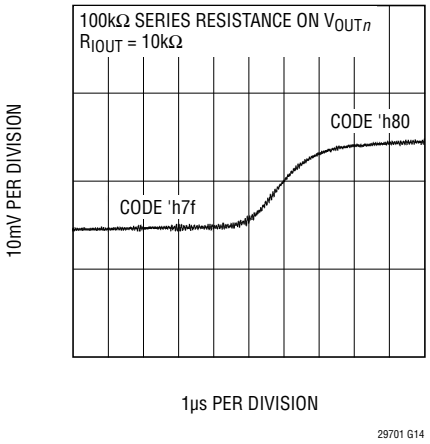
Voltage Buffered IDAC Load Regulation Sourcing



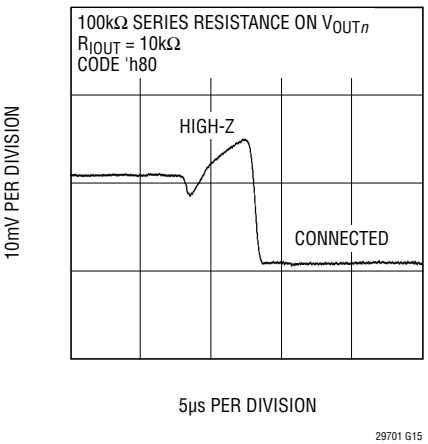
Voltage Buffered IDAC Load Regulation Sinking



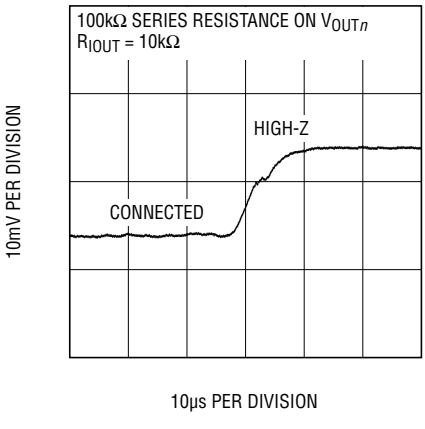
Voltage Buffered IDAC Transient Response to 1LSB DAC Code Change



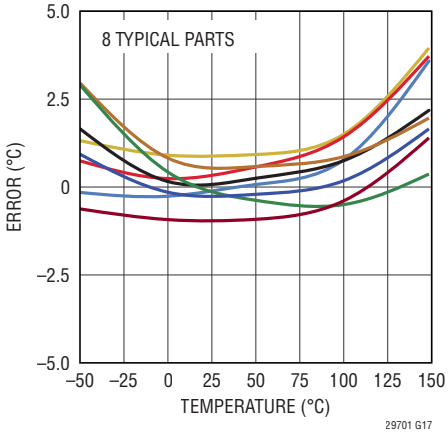
Voltage Buffered IDAC Soft-Connect Transient Response



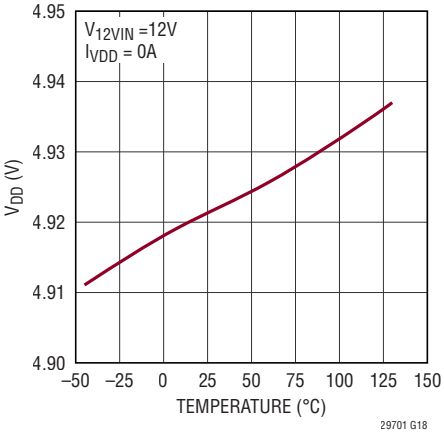
Voltage Buffered IDAC Transient Response During Transition from On State to High-Z State



Temperature Sensor Error vs Temperature

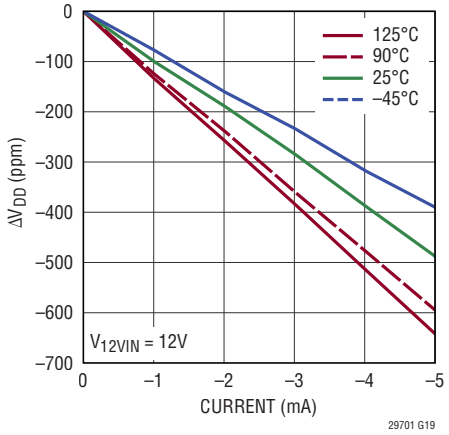


V_{DD} Regulator Output Voltage vs Temperature

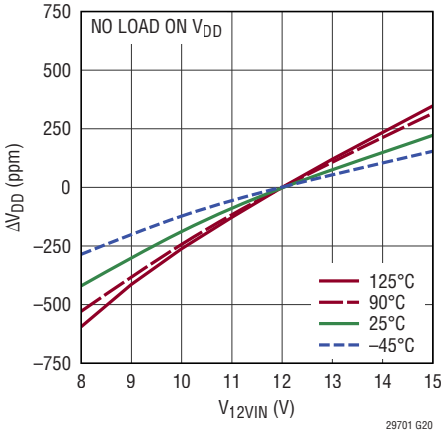


TYPICAL PERFORMANCE CHARACTERISTICS

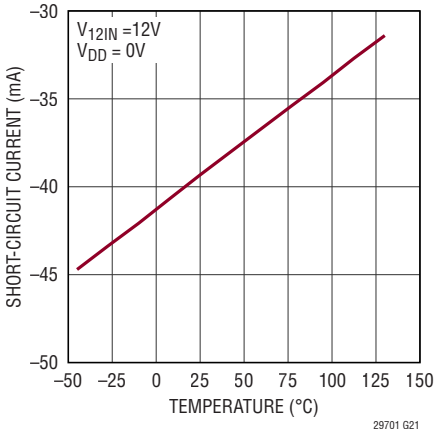
V_{DD} Regulator Load Regulation



V_{DD} Regulator Line Regulation



V_{DD} Regulator Short-Circuit Current vs Temperature



PIN FUNCTIONS

V_{IN0_AP} (Pin 1): Positive CH0_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0_A can be configured to servo IDAC0.

V_{IN0_AM} (Pin 2): Negative CH0_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0_A can be configured to servo IDAC0.

V_{IN0_BP} (Pin 3): Positive CH0_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0_B is a voltage monitor input only.

V_{IN0_BM} (Pin 4): Negative CH0_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0_B is a voltage monitor input only.

V_{IN1_AP} (Pin 5): Positive CH1_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1_A can be configured to servo IDAC1.

V_{IN1_AM} (Pin 6): Negative CH1_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1_A can be configured to servo IDAC1.

V_{IN1_BP} (Pin 7): Positive CH1_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1_B is a voltage monitor input only.

V_{IN1_BM} (Pin 8): Negative CH1_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1_B is a voltage monitor input only.

V_{DD} (Pin 9): V_{DD} Power Supply, Voltage Monitor Input, and Internal 5V Regulator Output. The supply input range is 4.5V to 5.75V. The V_{DD} pin voltage can be connected to the ADC through an internal mux. Bypass the V_{DD} pin to device ground with a 100nF capacitor (C_{VDD}). If no 5V input voltage supply is available, float the V_{DD} pin and power the LTC2970 from the $12V_{IN}$ pin.

$12V_{IN}$ (Pin 10): 12V Power Supply and Voltage Monitor Input. An internal regulator generates 5V from $12V_{IN}$. The input range for $12V_{IN}$ is 8V to 15V. Bypass this pin with a 100nF capacitor. The regulator's output is connected to the V_{DD} pin. The $12V_{IN}$ pin voltage can also be monitored by the ADC through a 3:1 attenuator and the internal mux. If no 12V supply input is available, tie the $12V_{IN}$ to the V_{DD} pin and operate from 4.5V to 5.75V.

V_{OUT0} (Pin 11): CH0 Voltage Output. Buffered version of IDAC0 output voltage.

PIN FUNCTIONS

V_{OUT1} (Pin 12): CH1 Voltage Output. Buffered version of IDAC1 output voltage.

I_{OUT1} (Pin 13): IDAC1 Current Output. Connect a resistor between this pin and the point-of-load ground for channel 1. The IDAC sources between 0 and 255µA.

I_{OUT0} (Pin 14): IDAC0 Current Output. Connect a resistor between this pin and the point-of-load ground for channel 0. The IDAC sources between 0 and 255µA.

GPIO_1 (Pin 15): General Purpose Input or Open Drain Digital Output. GPIO_1 can be configured as the IDAC Fault or Faults output, a digital input, or an open-drain digital output.

GPIO_0 (Pin 16): General Purpose Input or Open Drain Digital Output. GPIO_0 can be configured as the voltage monitor power-good or power-good bar output, a digital input, or a programmable open-drain output. Power good is the NOR of all instantaneous OV and UV faults; it does not include IDAC faults.

$\overline{\text{ALERT}}$ (Pin 17): Open Drain Digital Output. Connect the SMBALERT signal to this pin. $\overline{\text{ALERT}}$ is asserted low when either IDAC0 or IDAC1 rails out (optional), or when one of the monitored voltages ventures outside its UV and OV thresholds (also optional).

SCL (Pin 18): Serial Bus Clock Input.

SDA (Pin 19): Serial Bus Data Input and Output.

GPIO_CFG (Pin 20): GPIO Configuration Digital Input and Open Drain Output. Pulling GPIO_CFG high will cause the GPIO_0 and GPIO_1 open-drain outputs to automatically assert low after a power-on reset. If GPIO_CFG is pulled low, then GPIO_0 and GPIO_1 do not assert low after power-up.

ASEL1 (Pin 21): Slave Address Select Bit 1. Tie this pin to the V_{DD} pin, ground, or float in order to select the address location (see Table 2).

ASEL0 (Pin 22): Slave Address Select Bit 0. Tie this pin to the V_{DD} pin, ground, or float in order to select the address location (see Table 2).

REF (Pin 23): Internal Reference Output or ADC Reference Overdrive Input. The voltage at this pin determines the full-scale input voltage of the delta-sigma ADC ($V_{FULL-SCALE}$ = 6.65 • V_{REF}, typically). An internal 3.5k resistor decouples the reference output from this pin. Bypass this pin to RGND with a 100nF capacitor (C_{REF}).

RGND (Pin 24): Reference Ground. Connect to device ground.

GND (Pin 25): Device Ground. Must be soldered to ground.

BLOCK DIAGRAM

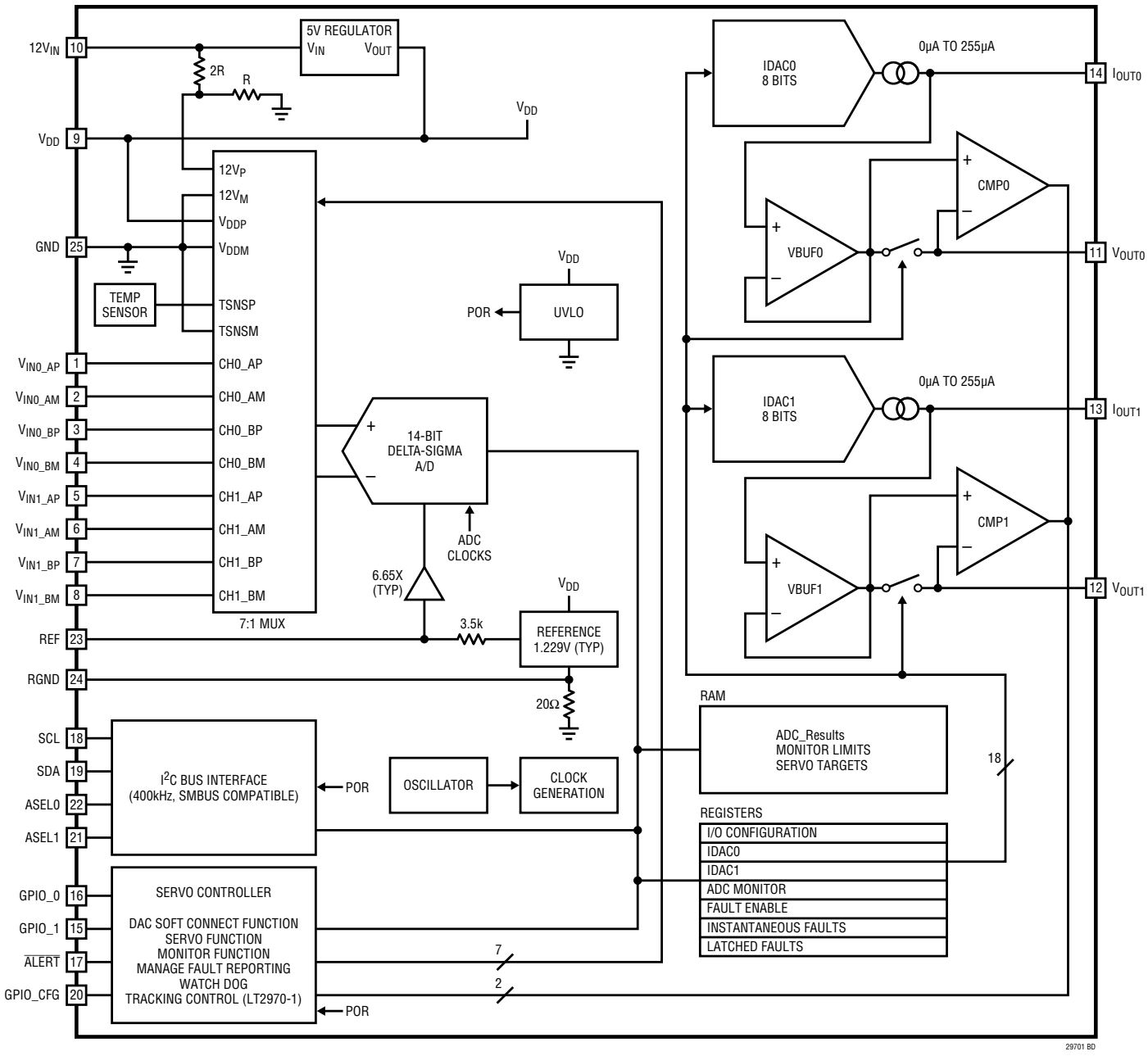


TABLE OF CONTENTS (For Operations Sections)

OPERATION

1. LTC2970 Operation Overview

The LTC2970 is designed to control and monitor two power supplies. The LTC2970's superior accuracy allows it to precisely servo each supply's output voltage over a wide range of operating conditions; increasing accuracy, reducing power requirements and component costs. Margining may be performed with equal ease and precision. The monitoring functions allow for increased reliability by alerting a system host about incipient failures before they occur. The seven channel ADC may also be used to monitor current, temperature, and the 5V or optional 12V supply.

The LTC2970's unique architecture and control algorithm have been especially tailored for power supply management. The soft connect feature allows the LTC2970 to begin controlling a power supply without perturbing its initial value. The delta-sigma ADC architecture was specifically chosen to average out power-supply noise and allow the LTC2970 to ignore fast transients. Unlike discrete time DACs, the LTC2970's continuous time, voltage buffered IDAC is ideal for noise sensitive applications. The servo algorithm limits the IDAC step size to one LSB per iteration in order to minimize power supply transients. The point of load ground reference for the IDAC outputs minimize errors that would otherwise occur in a power system that experiences ground bounce. By selecting two resistor values, the user can choose the appropriate resolution while providing an important hardware range limit beyond which the supply may not be driven. The servo on fault option allows the LTC2970 to further reduce output voltage disturbances by only stepping the IDAC when the output voltage drifts outside of a user programmable window. The LTC2970 powers up in a high impedance state and will not interfere with default power supply operation. Similarly, powering down the LTC2970 will restore its high impedance state.

All communication with the LTC2970 is performed over an industry standard I^2C bus. The LTC2970 I^2C interface also meets all SMBus setup times, hold times, and timeout requirements. The $\overline{\text{ALERT}}$ pin may be used to signal that one or more of the fourteen configurable fault limits have been reached. Each fault may be individually masked. The I^2C interface supports word reads, word writes and the SMBus Alert Response Address protocol. Two general purpose IO pins may be used to provide additional fault information or user defined system control. Powering down the LTC2970 will not interfere with I^2C operation.

The LTC2970-1 enables power supply tracking and sequencing with the addition of a few external components. A special global address and synchronization command allow multiple LTC2970-1's to track and sequence multiple pairs of power supplies.

The LTC2970 can perform the following operations:

- Accept all programming commands and report status over the I^2C or SMBus bus.
- Command each voltage buffered IDAC to connect to the corresponding power supply's feedback node through an external resistor using the IDAC code that most closely approximates the feedback node's regulation voltage (Soft Connect).
- Command each voltage buffered IDAC output to connect to the corresponding power supply's feedback node through an external resistor with a user-selected IDAC code (Hard Connect).
- Change the code of a previously connected IDAC.
- Disconnect each voltage buffered IDAC output from the power supply's feedback node.
- *LTC2970-1 Only:* Track two power supplies up or down. Multiple LTC2970-1's can be configured to track simultaneously or in a sequence.

OPERATION

- Continuously servo one or both supplies to a programmed voltage.
- Perform a one-time servo of one or both supplies to a programmed voltage and hold the servo codes in the controlling IDAC.
- Perform a one time servo of one or both supplies to a programmed voltage and hold the code(s) in the controlling IDAC(s) until over/under voltage monitoring detects a fault, at which point a control bit may be used to allow the LTC2970 to servo back to the initial voltage target.
- Select any combination of seven possible ADC channels to be monitored by the ADC.
- Generate instantaneous faults based on user programmable overvoltage and undervoltage limits and fixed IDAC limits. The status of OR'd voltage limit faults and IDAC faults may be output over GPIO_0 and GPIO_1, respectively.
- Enable instantaneous faults to set associated latched faults using the FAULT_EN register. The status of OR'd latched faults may be signalled using $\overline{\text{ALERT}}$.
- Configure the GPIO_0 and GPIO_1 pins to act as inputs or outputs.

2. I²C Serial Digital Interface

The LTC2970 communicates with a host (master) using the 2-wire, I²C serial bus interface. The Timing Diagram shows the timing relationship of the signals on the bus.

The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2970 I²C interface is SMBus compatible; it meets all SMBus setup times, hold times and timeout requirements.

The LTC2970 is a receive-only (slave) device. The LTC2970 can signal the host through the SMBALERT protocol that it wants to talk by asserting $\overline{\text{ALERT}}$ low. The LTC2970 supports the three I²C protocols summarized in Table 1.

Slave Address

The LTC2970 can respond to one of nine 7-bit addresses. The two slave address select pins (ASEL1 and ASEL0) are programmed by the user and determine the slave address, as shown in Table 2.

The LTC2970 also supports the ARA address and a global address that allows multiple LTC2970s to be programmed with the same data simultaneously, as shown in Table 3.

Table 1. Supported I²C Command Types

READ DATA WORD:
S:ADR:W:A:CMD:A:Sr:ADR:R:A:DATA:A:DATA:NACK:P
WRITE DATA WORD:
S:ADR:W:A:CMD:A:DATA:A:DATA:A:P
ALERT RESPONSE
S:ARA:R:A:ADR:NACK:P:

OPERATION

Table 2. LTC2970 Address Table

ADDRESS[7:0] (R/W = 0)	ADDRESS[7:1]	ASEL1	ASEL0
8'hB8	7'h5C	L	L
8'hBA	7'h5D	L	F
8'hBC	7'h5E	L	H
8'hBE	7'h5F	F	L
8'hD6	7'h6B	F	F
8'hD8	7'h6C	F	H
8'hDA	7'h6D	H	L
8'hDC	7'h6E	H	F
8'hDE	7'h6F	H	H

L: $V_{ASELn} < V_{IL\_ASEL}$ F: ASEL*n* Floating H: $V_{ASELn} > V_{IH\_ASEL}$

Table 3. Special LTC2970 Addresses

	ADDRESS[7:0] (R/W = 0)	ADDRESS[7:1]	FUNCTION
ARA	8'h18	7'h0C	This is the standard Alert Response Address for all SMBus devices. This address is independent of the value of the ASEL1 and ASEL0 pins.
Global	8'hB6	7'h5B	This a global address to which all LTC2970s will respond. This address is independent of the value of the ASEL1 and ASEL0 pins.

3. Register Command Set

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH	COMMAND BYTE VALUE
FAULT()	Instantaneous Fault Status For All Channels	Read Only	16 Bits	'h00
FAULT_EN()	Enable For All Latched Faults and Servo On Fault	Read/Write	16 Bits	'h08
FAULT_LA_INDEX()	Index to All Latched Faults	Read Only	16 Bits	'h10
FAULT_LA()	Latched Fault Status For All Channels	Read Only	16 Bits	'h11
IO()	IO Control and Status Register	Read/Write	16 Bits	'h17
ADC_MON()	Control Register For Selecting ADC Channels to Monitor	Read/Write	16 Bits	'h18
*SYNC()	Control Register For Synchronizing Tracking Across Multiple Devices	Read/Write	16 Bits	'h1F
VDD_ADC()	V_{DDIN} ADC Conversion Result Register	Read Only	16 Bits	'h28
VDD_OV()	V_{DDIN} Overvoltage Monitor Control Register	Read/Write	16 Bits	'h29
VDD_UV()	V_{DDIN} Undervoltage Monitor Control Register	Read/Write	16 Bits	'h2A
V12_ADC()	$12V_{IN}$ ADC Conversion Result Register	Read Only	16 Bits	'h38
V12_OV()	$12V_{IN}$ Overvoltage Monitor Control Register	Read/Write	16 Bits	'h39
V12_UV()	$12V_{IN}$ Undervoltage Monitor Control Register	Read/Write	16 Bits	'h3A
CH0_A_ADC()	CH0_A ADC Conversion Result Register	Read Only	16 Bits	'h40
CH0_A_OV()	CH0_A Overvoltage Monitor Control Register	Read/Write	16 Bits	'h41
CH0_A_UV()	CH0_A Undervoltage Monitor Control Register	Read/Write	16 Bits	'h42
CH0_A_SERVO()	CH0_A Voltage Servo Control Register	Read/Write	16 Bits	'h43
CH0_A_IDAC()	CH0_A IDAC Control Register	Read/Write	16 Bits	'h44
*CH0_A_IDAC_TRACK()	CH0_A IDAC Track Final Value Register	Read/Write	16 Bits	'h45
*CH0_A_DELAY_TRACK()	CH0_A IDAC Track Delay Register	Read/Write	16 Bits	'h46
CH0_B_ADC()	CH0_B ADC Conversion Result Register	Read Only	16 Bits	'h48
CH0_B_OV()	CH0_B Overvoltage Monitor Control Register	Read/Write	16 Bits	'h49
CH0_B_UV()	CH0_B Undervoltage Monitor Control Register	Read/Write	16 Bits	'h4A
CH1_A_ADC()	CH1_A ADC Conversion Result Register	Read Only	16 Bits	'h50
CH1_A_OV()	CH1_A Overvoltage Monitor Control Register	Read/Write	16 Bits	'h51
CH1_A_UV()	CH1_A Undervoltage Monitor Control Register	Read/Write	16 Bits	'h52

OPERATION

3. Register Command Set (Cont.)

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH	COMMAND BYTE VALUE
CH1_A_SERVO()	CH1_A Voltage Servo Control Register	Read/Write	16 Bits	‘h53
CH1_A_IDAC()	CH1_A IDAC Control Register	Read/Write	16 Bits	‘h54
*CH1_A_IDAC_TRACK()	CH1_A IDAC Track Control Register	Read/Write	16 Bits	‘h55
*CH1_A_DELAY_TRACK()	CH1_A IDAC Track Delay Register	Read/Write	16 Bits	‘h56
CH1_B_ADC()	CH1_B ADC Conversion Result Register	Read Only	16 Bits	‘h58
CH1_B_OV()	CH1_B Overvoltage Monitor Control Register	Read/Write	16 Bits	‘h59
CH1_B_UV()	CH1_B Undervoltage Monitor Control Register	Read/Write	16 Bits	‘h5A
TEMP_ADC()	Temperature ADC Conversion Result Register	Read/Write	16 Bits	‘h68
RESERVED()	All other commands are reserved for future expansion and should not be written or read.	Read/Write	16 Bits	‘hXX

*LTC2970-1 Only. LTC2970 will not acknowledge these commands.

4. Detailed I²C Command Register Descriptions

FAULT: Instantaneous Fault Register – Read

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_ch0_a_ov	0 = The associated channel is clear of instantaneous faults. 1 = The associated channel has an instantaneous fault. The reported faults are instantaneous and not latched. When used in conjunction with latched faults they may indicate faults that are transient in nature.
b[1]	Fault_ch0_a_uv	
b[2]	Fault_ch0_a_idac	
b[3]	Fault_ch0_b_ov	
b[4]	Fault_ch0_b_uv	
b[5]	Fault_ch1_a_ov	
b[6]	Fault_ch1_a_uv	
b[7]	Fault_ch1_a_idac	
b[8]	Fault_ch1_b_ov	
b[9]	Fault_ch1_b_uv	
b[10]	Fault_vdd_ov	
b[11]	Fault_vdd_uv	
b[12]	Fault_v12_ov	
b[13]	Fault_v12_uv	
b[15:14]	Reserved	Always Returns 0

FAULT_EN: Fault Enabling Register – Read/Write

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_en_ch0_a_ov	0 = The associated bit in the FAULT_LA register will always be 0. (default) 1 = Instantaneous faults reported in the FAULT register will set associated bit in the FAULT_LA register.
b[1]	Fault_en_ch0_a_uv	
b[2]	Fault_en_ch0_a_idac	
b[3]	Fault_en_ch0_b_ov	
b[4]	Fault_en_ch0_b_uv	
b[5]	Fault_en_ch1_a_ov	
b[6]	Fault_en_ch1_a_uv	
b[7]	Fault_en_ch1_a_idac	
b[8]	Fault_en_ch1_b_ov	
b[9]	Fault_en_ch1_b_uv	
b[10]	Fault_en_vdd_ov	
b[11]	Fault_en_vdd_uv	
b[12]	Fault_en_v12_ov	
b[13]	Fault_en_v12_uv	
b[14]	Fault_en_ch0_a_servo	0 = Do not re-servo CH0_A in response to instantaneous OV or UV fault. 1 = Repeat a one time servo of CH0_A in response to instantaneous OV or UV fault. CH0_A must have servo operation enabled with Ch0_a_idac_servo_repeat set low, and Adc_mon_ch0_a set high.
b[15]	Fault_en_ch1_a_servo	0 = Do not re-servo CH1_A in response to instantaneous OV or UV fault. 1 = Repeat a one time servo of CH1_A in response to instantaneous OV or UV fault. CH1_A must have servo operation enabled with Idac_ch1_a_servo_repeat set low, and Adc_mon_ch1_a set high.

OPERATION

4. Detailed I²C Command Register Descriptions (Cont.)

FAULT_INDEX: Latched Fault Index Register – Read

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_la_index	0 = All faults indicated by FAULT_LA are clear. 1 = One or more faults indicated by FAULT_LA are set. This register allows a summary of all latched faults to be viewed in a single read without resetting latched faults.
b[15:1]	Reserved	Always Returns 0

FAULT_LA: Latched Fault Register – Read

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_la_ch0_a_ov	0 = The associated channel is clear of faults. 1 = The associated channel has faulted and is enabled. The latched faults are set and held when the associated channel's instantaneous fault has occured with faults enabled. Clearing the enable bit for the associated channel in FAULT_EN will immediately clear its corresponding latched fault bit. All latched channel faults are cleared when this register is read. They may be set again if the instantaneous fault condition and fault_en have not changed.
b[1]	Fault_la_ch0_a_uv	
b[2]	Fault_la_ch0_a_idac	
b[3]	Fault_la_ch0_b_ov	
b[4]	Fault_la_ch0_b_uv	
b[5]	Fault_la_ch1_a_ov	
b[6]	Fault_la_ch1_a_uv	
b[7]	Fault_la_ch1_a_idac	
b[8]	Fault_la_ch1_b_ov	
b[9]	Fault_la_ch1_b_uv	
b[10]	Fault_la_vdd_ov	
b[11]	Fault_la_vdd_uv	
b[12]	Fault_la_v12_ov	
b[13]	Fault_la_v12_uv	
b[15:14]	Reserved	Always Returns 0

IO: Input/Output Data and General Purpose Control Register – Read/Write unless specified otherwise.

BIT(s)	SYMBOL	OPERATION
b[1:0]	Io_cfg_0[1:0]	Io_cfg_0[1:0] is used to configure the function of the GPIO_0 pin and IO(Io_gpio_0). 00: Io_gpio_0 = GPIO_0 = Power_good. Power_good asserts high if there are no instantaneous overvoltage or undervoltage faults. 01: Io_gpio_0 = GPIO_0 = Power_good_bar. Power_good_bar is the complement of Power_good. 10: GPIO_0 is a general-purpose open-drain output and mirrors the value written to Io_gpio_0 (default). 11: GPIO_0 is a general-purpose digital input with Io_gpio_0 = GPIO_0
b[3:2]	Io_cfg_1[1:0]	Io_cfg_1[1:0] is used to configure the function of the GPIO_1 pin and IO(Io_gpio_1). 00: Io_gpio_1 = GPIO_1 = Idac_fault. Idac_fault asserts if either IDAC value is faulted (Ch*n*_idac[7:0] = 8'h00 or 8'hff) 01: Io_gpio_1 = GPIO_1 = Idac_fault_bar. Idac_fault_bar is the complement of Idac_fault. 10 = GPIO_1 is a general-purpose open-drain output and mirrors the value written to Io_gpio_1 (default). 11 = GPIO_1 is a general-purpose digital input with Io_gpio_1 = GPIO_1
b[4]	Io_gpio_0	See Io_cfg_0. If the GPIO_CFG pin is pulled-high during a power on reset, Io_gpio_0 is cleared and the GPIO_0 open-drain output will assert low.
b[5]	Io_gpio_1	See Io_cfg_1. If the GPIO_CFG pin is pulled-high during a power on reset, Io_gpio_1 is cleared and the GPIO_1 open-drain output will assert low.
b[6]	Io_alertb	Mirrors the value of the $\overline{\text{ALERT}}$ pin. Read only.
b[7]	Io_alertb_enb	1 = $\overline{\text{ALERT}}$ pin never asserts (default). 0 = $\overline{\text{ALERT}}$ pin asserts low when one or more FAULT_LA bits are set.
b[8]	Io_i2c_adc_wen	1 = Special test mode that inhibits ADC from writing to ADC result register and allows user to update registers over the I²C serial interface. 0 = Normal operation (default).
b[9]	Io_gpio_cfg	Read only. GPIO_CFG digital input and open-drain output. Reading this bit returns the current state of the GPIO_CFG pin voltage.
b[10]	Io_track_start	Writing a 1 to this bit will start tracking all enabled channels. Returns a 1 when tracking is pending (LTC2970-1). Reserved on LTC2970 and always returns 0.
b[15:11]	Reserved	Always Returns 0

OPERATION

4. Detailed I²C Command Register Descriptions (Cont.)

ADC_MON: ADC Monitoring Mux Control Register – Read/Write

BIT(s)	SYMBOL	OPERATION
b[0]	Adc_mon_vdd	0 = ADC will not convert associated channel. (Default)
b[1]	Adc_mon_v12	1 = ADC will continuously convert associated channel.
b[2]	Adc_mon_ch0_a	
b[3]	Adc_mon_ch0_b	
b[4]	Adc_mon_ch1_a	
b[5]	Adc_mon_ch1_b	
b[6]	Adc_mon_temp	
b[15:7]	Reserved	Always Returns 0

SYNC: Tracking Synchronization Control Register – Read/Write LTC2970-1 Only

BIT(s)	SYMBOL	OPERATION
b[0]	Sync_track	Write 0 = Do not synchronize. 1 = Synchronize all tracking enabled registers to the same starting point. Read 0 = The LTC2970-1 is not synchronized for tracking (default). 1 = The LTC2970-1 is synchronized for tracking. Use of the global address will allow the synchronization status of multiple LTC2970-1s to be verified in a single read; since a one can only be returned if all LTC2970-1s are synchronized. The IO_track_start command may then be issued with the same global address to begin synchronized tracking across multiple ICs.
b[15:1]	Reserved	Always Returns 0

VDD_ADC, V12_ADC, CH0_A_ADC, CH0_B_ADC, CH1_A_ADC, CH1_B_ADC, and TEMP_ADC: ADC Conversion Result Registers – Read Only Unless Specified Otherwise

BIT(s)	SYMBOL	OPERATION
b[14:0]	Vdd_adc[14:0] V12_adc[14:0] Ch0_a_adc[14:0] Ch0_b_adc[14:0] Ch1_a_adc[14:0] Ch1_b_adc[14:0] Temp_adc[14:0]	Measured data from ADC conversion. 'h4000 corresponds to negative full-scale input voltage. 'h0000 corresponds to 0V. 'h3fff corresponds to full-scale input voltage. $12V_{IN}$ is divided by 3 before being measured by the ADC. 2's complement format, b[14] = sign. Read/Write when Io_i2c_adc_wen = 1. Default value is undefined.
b[15]	Vdd_adc_new V12_adc_new Ch0_a_adc_new Ch0_b_adc_new Ch1_a_adc_new Ch1_b_adc_new Temp_adc_new	1 = The ADC has updated the associated result register since the last time the data was read. 0 = Previously read data. (Default)

VDD_OV, V12_OV, CH0_A_OV, CH0_B_OV, CH1_A_OV, CH1_B_OV: Over Voltage Limit Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[14:0]	Vdd_ov[14:0] V12_ov[14:0] Ch0_a_ov[14:0] Ch0_b_ov[14:0] Ch1_a_ov[14:0] Ch1_b_ov[14:0]	ADC overvoltage threshold limit. The associated instantaneous over voltage fault is asserted if the channel's ADC result is greater than this limit. Code 'h3fff disables OV threshold detect feature for that channel. $12V_{IN}$ is divided by 3 before being measured by the ADC. 2's complement format, b[14] = sign. Default value is undefined.
b[15]	Reserved	Always Returns 0

VDD_UV, V12_UV, CH0_A_UV, CH0_B_UV, CH1_A_UV, CH1_B_UV: Under Voltage Limit Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[14:0]	Vdd_uv[14:0] V12_uv[14:0] Ch0_a_uv[14:0] Ch0_b_uv[14:0] Ch1_a_uv[14:0] Ch1_b_uv[14:0]	ADC undervoltage threshold limit. The associated instantaneous under voltage fault is asserted if the channel's ADC result is greater than this limit. Code 'h4000 disables UV threshold detect feature for that channel. $12V_{IN}$ is divided by 3 before being measured by the ADC. 2's complement format, b[14] = sign. Default value is undefined.
b[15]	Reserved	Always Returns 0

OPERATION

4. Detailed I²C Command Register Descriptions (Cont.)

CH0_A_SERVO, CH1_A_SERVO: Voltage Servo Control Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[14:0]	Ch0_a_servo[14:0] Ch1_a_servo[14:0]	During servo operation Ch*n*_a_idac[7:0] output current is stepped to force Ch*n*_a_adc[14:0] code to equal target code stored in Ch*n*_a_servo[14:0]. 2's complement format, b[14] = sign Default value is undefined.
b[15]	Ch0_a_servo_en Ch1_a_servo_en	0 = Ch*n*_a servo disabled (default). 1 = Ch*n*_a servo enabled.

CH0_A_IDAC, CH1_A_IDAC: IDAC Control/Data Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[7:0]	Ch0_a_idac[7:0] Ch1_a_idac[7:0]	Ch*n*_a IDAC data value.
b[8]	Ch0_a_idac_en Ch1_a_idac_en	0 = V_{OUTn} output tri-stated. 1 = V_{OUTn} output enabled. There are two ways to enable V_{OUTn}. 1) When Ch*n*_a_idac_en is set high with Ch*n*_a_idac_con low, the LTC2970 will perform a soft connect. During a soft connect, the V_{OUTn} voltage buffer output will not be connected to the V_{OUTn} pin until the internal algorithm has servo'd the voltage at the IDAC*n* pin to match the V_{OUTn} pin voltage. Resolution is one Ch*n*_a_idac LSB. 2) When Ch*n*_a_idac_en is enabled with Ch*n*_a_idac_con high, the LTC2970 will perform a hard connect. The V_{OUTn} voltage buffer will be immediately connected to the V_{OUTn} pin.
b[9]	Ch0_a_idac_con Ch1_a_idac_con	0 = V_{OUTn} is not enabled or has been enabled but is not yet connected to the output of the CH*n* voltage buffer. (Default) 1 = V_{OUTn} is enabled and has been connected to the output of the CH*n* voltage buffer. See Ch*n*_a_idac_en for additional information.
b[10]	Ch0_a_idac_pol Ch1_a_idac_pol	0 = Use this setting when increasing V_{OUTn} causes (VIN*n*_AP-VIN*n*_AM) to decrease. Inverting configuration common to DC/DC converters with external feedback networks. 1 = Use this setting when increasing V_{OUTn} causes (VIN*n*_AP-VIN*n*_AM) to increase. Non-inverting configuration common to DC/DC converters with trim pins.
b[11]	Ch0_a_idac_servo_repeat Ch1_a_idac_servo_repeat	0 = During servo operation, servo Ch*n*_a until the measured result is stable and matches the target code. 1 = During servo operation, continuously servo Ch*n*_a to the target code.
b[15:12]	Reserved	Always Returns 0

CH0_A_IDAC_TRACK and CH1_A_IDAC_TRACK: IDAC Tracking data and control registers – Read/Write LTC2970-1 Only

BIT(s)	SYMBOL	OPERATION
b[7:0]	Ch0_a_idac_track[7:0] Ch1_a_idac_track[7:0]	Final target value for of Ch*n*_a_idac[7:0]. During tracking, Ch*n*_a_idac[7:0] is incremented/decremented by 1 until it is equal to this value.
b[8]	Ch0_a_idac_track_en Ch1_a_idac_track_en	0 = inhibit tracking of Ch*n*_a_idac[7:0]. 1 = enable tracking of Ch*n*_a_idac[7:0]
b[15:9]	Reserved	Always Returns 0

CH0_A_DELAY_TRACK and CH1_A_DELAY_TRACK: IDAC Tracking delay register – Read/Write LTC2970-1 Only

BIT(s)	SYMBOL	OPERATION
b[9:0]	Ch0_a_delay_track[9:0] Ch1_a_delay_track[9:0]	Delay used to synchronize or offset tracking events.
b[1510]	Reserved	Always Returns 0

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5. Soft Connecting the LTC2970 to the Power Supply Feedback Node

The soft connect feature allows the LTC2970 to connect to the power supply's feedback node with minimal disturbance to the supply's output voltage. This is accomplished by comparing the buffered voltage of I_{OUTn} to the voltage at V_{OUTn} and incrementing or decrementing Ch*n*_a_idac[7:0] until the comparator output (COMP*n*) changes. The value of Ch*n*_a_idac[7:0] when the comparator transitions is the appropriate value for a soft connect. The voltage buffer output is only connected to V_{OUTn} if the IDAC reaches this soft connect value without generating an instantaneous IDAC fault (Fault_ch*n*_a_idac).

Soft-Connect Procedure:

Determine the appropriate polarity for Ch*n*_a_idac_pol. Select Ch*n*_a_idac_pol = 1 if incrementing V_{OUTn} causes differential voltage (VIN*n*_AP – VIN*n*_AM) to increase. When properly programmed, lowering the value in Ch*n*_a_idac[7:0] will always cause the output of the controlled power supply to decrease.

Ensure that the channel's IDAC is not currently enabled for connection, i.e., the Ch*n*_a_idac_en bit must be 0.

Update CH*n*_A_IDAC() with Ch*n*_a_idac_pol, Ch*n*_a_idac_con = 0, Ch*n*_a_idac_en = 1, and Ch*n*_a_idac[7:0] = 0x80. The value programmed into Ch*n*_a_idac[7:0] is ignored and Ch*n*_a_idac[7:0] is initially set to 8'h80.

The LTC2970 will now ramp Ch*n*_a_idac[7:0] while monitoring the output of the soft connect comparator. If the soft connect comparator trips, the LTC2970 will connect the output of V_{BUFn} to V_{OUTn} and set Ch*n*_a_idac_con high. If the soft connect comparator does not trip before the IDAC value reaches 'h00 or 'hFF, then the soft connection will fail, an IDAC fault will be indicated (Fault_ch*n*_a_idac), and Ch*n*_a_idac_con will remain low.

Soft-Connect Rules:

When both channels are requesting a soft connect, channel 0 has priority.

Soft connect requests will be ignored and the user will not be able to change Ch*n*_a_idac_pol or Ch*n*_a_idac[7:0] if the LTC2970 is servicing a previously issued soft connect on that channel or the previously issued soft connect failed with an IDAC fault (Fault_ch*n*_a_idac = 1). Recall that the Ch*n*_a_idac_en bit must initially have been set to 0.

LTC2970-1 Only: Soft connect requests will be ignored and the user will not be able to change Ch*n*_a_idac_pol or Ch*n*_a_idac[7:0] if GPIO_CFG is high and either GPIO_0 or GPIO_1 are high.

LTC2970-1 Only: Soft connect requests will be ignored and the user will not be able to change the Ch*n*_a_idac_pol bit if there is a pending tracking operation.

6. Hard Connecting the LTC2970 to the Power Supply Trim Pin

The hard connect feature allows the LTC2970 to bypass the soft connect algorithm and connect directly to the power supply's feedback node using the value programmed into Ch*n*_a_idac[7:0]. This feature is useful for systems that have calculated or measured an acceptable voltage at which to connect the IDAC's buffered voltage V_{BUFn} to V_{OUTn}.

Hard Connect Procedure:

Determine the appropriate polarity for Ch*n*_a_idac_pol. Select Ch*n*_a_idac_pol = 1 if incrementing V_{OUTn} causes (VIN*n*_AP – VIN*n*_AP) to increase. When properly programmed, lowering the value in the IDAC will always cause the output of the controlled power supply to decrease.

Determine the value for Ch*n*_a_idac[7:0]. The values 'h00 or 'hff are allowed, but they will trip the IDAC's fault bit (Fault_ch*n*_a_idac = 1).

When the IDAC is already connected, the value Ch*n*_a_idac[7:0] and Ch*n*_a_idac_pol will be programmed into the IDAC provided all other conditions are met. See "Programming a Previously Connected Current DAC" for details

Update CH*n*_A_IDAC() with Ch*n*_a_idac_pol, Ch*n*_a_idac_con = 1, Ch*n*_a_idac_en = 1, and Ch*n*_a_idac[7:0].

Hard Connect Rules:

Hard connect requests will be ignored and the user will not be able to change Ch*n*_a_idac_pol, Ch*n*_a_idac_con or Ch*n*_a_idac[7:0] if the LTC2970 is servicing a previously issued soft connect on that channel or the previously issued

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soft connect failed with an IDAC fault (Fault_ch*n*_a_idac = 1). Recall that a new hard connection requires the previous value of Ch*n*_a_idac_en = 0.

LTC2970-1 Only: Hard connect requests will be ignored and the user will not be able to change Ch*n*_a_idac_pol, Ch*n*_a_idac_con or Ch*n*_a_idac[7:0] if GPIO_CFG is high and either GPIO_0 or GPIO_1 are high.

LTC2970-1 Only: Hard connect requests will be ignored and the user will not be able to change Ch*n*_a_idac_pol, Ch*n*_a_idac_con or Ch*n*_a_idac[7:0] if there is a pending tracking operation.

7. Programming a Previously Connected IDAC

The LTC2970 IDAC's may be programmed after they have been connected with a soft connect or a hard connect provided a servo operation is not enabled on the associated channel.

Procedure:

Determine the value for Ch*n*_a_idac[7:0]. The values 'h00 or 'hff are allowed, but will trip the IDAC's fault bit (Fault_ch*n*_a_idac = 1).

Verify that the IDAC is already connected, and that Ch*n*_a_idac_con is high.

Ensure that servo mode is not enabled for the channel being programmed. Ch*n*_a_servo_en must be low. This requirement prevents the user from interfering with a previously requested servo operation.

Update the CH*n*_A_IDAC() register with Ch*n*_a_idac_pol, Ch*n*_a_idac_con = 1, Ch*n*_a_idac_en = 1, and Ch*n*_a_idac[7:0].

Note: Care should be taken to preserve the current value of the Ch*n*_a_idac_pol bit, since the LTC2970 does not prevent the user from changing this value when writing to the IDAC control registers.

Rules:

Setting Ch*n*_a_idac_con to zero will not disconnect the DAC unless Ch*n*_a_idac_en is also set low.

All Hard Connect rules apply.

8. Disconnecting the LTC2970 from the Power Supply Trim Pin

V_{OUTn} can be placed in a high impedance state simply by clearing the Ch*n*_a_idac_en bit. In order to minimize the resulting disturbance to the power supply voltage, the IDAC code should not be changed from its current value when clearing the Ch*n*_a_idac_en bit. This is not an issue if the channel's associated servo_en bit is high.

Disconnect Procedure:

Update CH*n*_IDAC() with Ch*n*_a_idac_en set low.

The LTC2970 will immediately disconnect the buffered I_{OUTn} from V_{OUTn}.

Disconnect Rules:

Clearing Ch*n*_a_idac_con with Ch*n*_a_idac_en high will not disconnect the IDAC. Only setting Ch*n*_a_idac_en low will clear Ch*n*_a_idac_con.

LTC2970-1 Only: Ch*n*_a_idac_en may not be changed if the feedback node connection is configured for tracking. Tracking is enabled when GPIO_CFG is high and either GPIO_0 or GPIO_1 are high.

9. Tracking Power Supplies Overview (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I^2C interface to initiate a controlled power up or power down of two or more supplies (Figure 2 shows a typical LTC2970-1 application circuit). Multiple LTC2970-1's with different addresses may be simultaneously programmed using the LTC2970 group address and the SYNC() command. Tracking is enabled when GPIO_CFG is pulled high and either GPIO_0 or GPIO_1 are high.

10. Tracking Power Supplies On (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I^2C to initiate a controlled power up of two or more supplies.

Procedure: This procedure describes all the steps necessary to track up two or more power supplies. Steps that require I^2C interaction are prefixed with the required I^2C command function.

Power-up the LTC2970-1 with GPIO_CFG pulled high.

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This causes open-drain outputs GPIO_1 and GPIO_0 to automatically pull the power supplies' run/soft-start pins to ground.

CH*n*_A_IDAC(): Hard connect Ch*n*_a_idac[7:0] with a value that forces the power supplies off when GPIO_CFG = 1. Verify that Ch*n*_a_idac_pol is at the appropriate value.

CH*n*_A_IDAC_TRACK(): Set Ch*n*_a_idac_track_en = 1, and set the Ch*n*_a_idac_track[7:0] target value to the code that causes V_{OUTn} to most closely approximate the corresponding power supply's feedback node voltage when it is in regulation.

CH*n*_A_DELAY_TRACK(): Set the value by which the incrementing of IDAC*n* should be delayed with respect to the start of tracking event. This controls whether the power supplies track up coincidentally or sequentially.

IO(): Release the run/soft-start pins by programming io_gpio_*n* = 1. This will enable the power supplies without allowing their outputs to move since these are held low by Ch*n*_a_idac[7:0]. Wait until power supplies have had sufficient time to start running before starting tracking.

SYNC(): Optional command that allows multiple LTC2970-1's to be synchronized for tracking. Writing Sync_track = 1 will allow the LTC2970-1 to finish its current ADC conversion before having it wait to receive io_track_start = 1. The LTC2970-1 will timeout this wait command after $t_{TIMEOUT\_SYNC}$. Reading back Sync_track = 1 using the global address will ensure all LTC2970-1's are synchronized before proceeding with the tracking operation.

IO(): Set Io_track_start = 1 and keep the run/soft-start pins enabled. Use the global I²C address to simultaneously track up power supplies across multiple LTC2970-1's.

LTC2970-1 response: For each tracking enabled channel, the LTC2970-1 will decrement the CH*n*_A_delay_track counter at a rate of t_{DEC_TRACK}. As soon as a channel's tracking counter reaches zero, the LTC2970-1 will begin stepping the value of Ch*n*_a_idac[7:0] by one count until the final value of Ch*n*_a_idac_track[7:0] is reached, at which point Ch*n*_a_idac_track_en is de-asserted. When the final value is reached for all channels, GPIO_CFG is asserted low. After a time delay of t_{HOLD_TRACK}, Ch*n*_a_idac_en is de-asserted.

Power-Up Tracking Rules:

Tracking cannot begin if Ch*n*_a_idac_con is not connected. This condition is met when the previous procedure is followed.

Ch*n*_a_idac_track_pol, Ch*n*_a_idac_track_en, and ch0_idac[7:0] updates will be ignored after IO(Io_track_start) is asserted until tracking is complete or whenever tracking is pending, i.e., GPIO_CFG pulled high with either GPIO_0 or GPIO_1 asserted pulled high.

11. Tracking Power Supplies Off (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I²C to initiate a controlled power down of two or more supplies.

Procedure: This procedure describes all steps necessary to track down two or more power supplies. Steps that require I²C interaction are prefixed with the required I²C command function.

CH*n*_IDAC(): Disable the IDAC's for each tracking enabled channel (Ch*n*_a_idac_en = 0). Ensure Ch*n*_a_idac_pol is at the appropriate value.

CH*n*_IDAC_TRACK(): Select the channels to be tracked by setting Ch*n*_a_idac_track_en = 1, and set the target value for each Ch*n*_a_idac_track[7:0] to that which forces the supply off.

CH*n*_A_DELAY_TRACK(): Set the value by which the decrementing of that channel's DAC should be delayed with respect to the start of the tracking event. This controls whether the supplies track down coincidentally or sequentially.

SYNC(): Optional command that allows multiple LTC2970-1's to be synchronized for tracking. Writing Sync_track = 1 will allow the LTC2970-1 to finish its current ADC conversion before having it wait to receive io_track_start = 1. The LTC2970-1 will timeout this wait command after $t_{TIMEOUT\_SYNC}$. Reading back Sync_track = 1 using the global address will ensure all LTC2970's are synchronized before proceeding with the tracking operation.

IO(): Set Io_track_start = 1. Use the global I²C address to simultaneously track down power supplies across multiple LTC2970's.

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LTC2970-1 response: Each tracking enabled channel is soft connected. The GPIO_CFG pin is released allowing it to be pulled high. The LTC2970-1 waits t_{SETUP_TRACK} to allow GPIO_CFG to settle. For each tracking enabled channel, the Ch*n*_a_delay_track counter is decremented at a rate of t_{DEC_TRACK}. As soon as a channel's tracking counter reaches zero, the LTC2970-1 will begin stepping the value of Ch*n*_a_idac[7:0] by one count until the final value of Ch*n*_a_idac_track[7:0] is reached. The tracking enable bit is then cleared for both channels (Ch*n*_a_idac_track_en = 0).

IO(): The I^2C interface may then be used to set GPIO_1 and GPIO_0 low, disabling the power supplies.

Power Down Tracking Rules:

Power down tracking requests will be ignored until the user has disabled the IDAC's by setting Ch*n*_a_idac_en = 0 for each tracking enabled channel.

Ch*n*_a_idac_track_pol, Ch*n*_a_idac_track_en, and ch0_idac[7:0] updates will be ignored after IO(IO_track_start) is asserted until tracking is complete and whenever tracking range is configured; (GPIO_CFG high with either GPIO_0 or GPIO_1 asserted high).

12. Continuous Power Supply Voltage Servo

The continuous voltage servo feature allows the LTC2970 to servo an external power supply to a programmed value. The voltage of the external supply is monitored over Ch*n*_A_ADC and compared to a target value stored in Ch*n*_a_servo. After each conversion, Ch*n*_A_IDAC is incremented by 1, decremented by 1, or held; whichever brings or keeps the measured voltage closer to the targeted servo value.

Procedure:

Follow procedure for hard connecting or soft connecting the LTC2970 to power supply trim pin; when updating CH*n*_A_IDAC(), Ch*n*_a_idac_servo_repeat should be asserted high. The servo channel's IDAC must be enabled before Ch*n*_A_servo_en can be set high.

Determine the target servo voltage, Ch*n*_a_servo[14:0].

Update CH*n*_A_SERVO() with Ch*n*_a_servo_en = 1, and Ch*n*_a_servo[14:0].

Update CH*n*_A_IDAC() with Ch*n*_a_idac_servo_repeat = 1. This step may be skipped if Ch*n*_a_idac_servo_repeat was set high during the soft or hard connect procedure.

LTC2970 response: The LTC2970 will continuously increment, decrement or hold Ch*n*_a_idac[7:0] in order to match the measured value of (VIN*n*_AP-VIN*n*_AM) to Ch*n*_a_servo[14:0].

Whenever the CH*n*_A_SERVO() register is updated an internal flag is cleared indicating that a successful servo has not been completed. This internal flag, Ch*n*_a_servo_done, initially causes the ADC to operate in an accelerated 12-bit mode. Once the channel reaches the servo target, the ADC switches back to 14-bit mode for two conversions before asserting Ch*n*_a_servo_done high.

In continuous voltage servo mode the Ch*n*_a_servo_done flags allow the initial servo target to be reached quickly. During this time, ADC conversions for all non-servo channels are temporarily inhibited.

Rules:

The IDAC associated with the servo channel must be enabled. If Ch*n*_a_idac_en is low the servo enable bit Ch*n*_a_servo_en is always forced low.

The IDAC associated with the servo channel must be connected (Ch*n*_a_idac_con = 1).

An IDAC fault may be generated during a continuous servo operation. The LTC2970 will report the fault and continue trying to servo that channel.

LTC2970-1 Only: There must be no pending tracking commands. A pending tracking command will clear Ch*n*_a_servo_en.

LTC2970-1 Only: The tracking range must not be enabled; (GPIO_CFG high with either GPIO_0 or GPIO_1 asserted high). An enabled tracking range will clear Ch*n*_a_servo_en low.

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13. One Time Power Supply Voltage Servo

The one time voltage servo feature allows the LTC2970 to servo an external power supply to a programmed value and then stop updating the IDAC once the target value has been reached.

Procedure:

Follow procedure for hard connecting or soft connecting the LTC2970 to power supply trim pin; when updating CH*n*_A_IDAC(), Ch*n*_a_idac_servo_repeat should be de-asserted low. The servo channel's IDAC must be enabled before Ch*n*_a_servo_en may be set high.

Update CH*n*_A_IDAC() with Ch*n*_a_idac_servo_repeat = 0. This step may be skipped if Ch*n*_a_idac_servo_repeat was cleared low during the soft or hard connect procedure.

Update FAULT_EN() with Fault_en_ch*n*_a_servo = 0. This prevents the LTC2970 from reinitiating a servo after an overvoltage or undervoltage fault.

Determine the target servo voltage, Ch*n*_a_servo[14:0].

Update CH*n*_A_SERVO() register with Ch*n*_a_servo_en = 1, and Ch*n*_a_servo[14:0].

LTC2970 response: The LTC2970 will increment, decrement or hold Ch*n*_a_idac[7:0] in order to match the measured value of (VIN*n*_AP-VIN*n*_AM) to Ch*n*_a_servo[14:0]. The servo procedure will end when the internal Ch*n*_a_servo_done flag is set (see "Continuous Power Supply Voltage Servo"). At this point the IDAC is either programmed to the appropriate servo value or faulted.

Rules:

All "Continuous Power Supply Voltage Servo" rules apply.

14. One Time Power Supply Voltage Servo with Repeat On Fault

The LTC2970 one time voltage servo feature may be modified to allow the LTC2970 to perform an additional power supply servo operation after an undervoltage or overvoltage fault is detected on the servo channel.

Procedure:

Follow procedure outlined for "One Time Power Supply Voltage Servo".

Update FAULT_EN() with Fault_en_ch*n*_a_servo = 1.

Enable detection of the appropriate instantaneous faults for all servo channels; see "Generating and Monitoring Instantaneous Faults".

LTC2970 response: Any time an instantaneous undervoltage or overvoltage fault is detected on the servo channel (Fault_ov_a_ch*n* or Fault_uv_a_ch*n*), the internal Ch*n*_a_servo_done flag for that channel is cleared, and the LTC2970 will perform a complete one time servo. This allows the LTC2970 to precisely restore the power supply to the target servo value, after it has drifted beyond a user defined operating window.

Rules:

All "Continuous Power Supply Voltage Servo" rules apply.

During a permanent undervoltage or overvoltage fault the LTC2970 will continuously try to correct the faulted channel, after each failed attempt all other channels that need monitoring by the ADC will be serviced.

15. Configuring ADC to Monitor Input Channels and Internal Temperature Sensor

The LTC2970 is able to perform ADC conversions on any combination of seven different input channels. A channel is converted if its associated ADC_MON() bit is set high. Refer to Table 7 for details.

Procedure:

Update ADC_MON() with the control bit of each channel that is to be monitored set high.

LTC2970 response: All enabled channels will be sequentially converted. The result of the most recent conversion may be read from the ADC result register. Each time a conversion is completed the new data bit associated with the result register is asserted high. The new data bit is reset each

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Table 7. LTC2970 ADC Conversion and Fault Limit Registers

INPUT CHANNEL	ADC_MON() CONTROL BIT	ADC RESULT REGISTER (2s COMPLEMENT)	OV FAULT REGISTER (2s COMPLEMENT)	UV FAULT REGISTER (2s COMPLEMENT)
TEMPERATURE	Adc_mon_temp	Temp_adc[14:0]	-	-
VIN1_BP-VIN1_BM	Adc_mon_b_ch1	Ch1_b_adc[14:0]	Ch1_b_ov[14:0]	Ch1_b_uv[14:0]
VIN1_AP-VIN1_AM	Adc_mon_a_ch1	Ch1_a_adc[14:0]	Ch1_a_ov[14:0]	Ch1_a_uv[14:0]
VIN0_BP-VIN0_BM	Adc_mon_b_ch0	Ch0_b_adc[14:0]	Ch0_b_ov[14:0]	Ch0_b_uv[14:0]
VIN0_AP-VIN0_AM	Adc_mon_a_ch0	Ch0_a_adc[14:0]	Ch0_a_ov[14:0]	Ch0_a_uv[14:0]
12VIN	Adc_mon_v12	V12_adc[14:0]	V12_ov[14:0]	V12_uv[14:0]
VDD	Adc_mon_vdd	Vdd_adc[14:0]	Vdd_ov[14:0]	Vdd_uv[14:0]

time the result register is read. This provides a simple mechanism for supervisory software to determine if a new conversion has been completed since data was last read.

Rules:

The LTC2970 assigns priority to ADC conversions of CH1_A_ADC and CH0_A_ADC when these channels are in their initial fast servo mode.

The IO() register control bit Io_i2c_adc_wen must be low in order for ADC conversions to be performed.

LTC2970-1 Only: ADC conversions are suspended during any pending tracking requests.

16. Generating and Monitoring Instantaneous Faults

The LTC2970 supports fourteen different types of instantaneous faults. These faults together with the conditions that trigger them are defined in Table 8. There are six undervoltage faults, six overvoltage faults and two IDAC limit faults. The FAULT() command may be used to read the status of all instantaneous fault bits. The IO() command may be used to configure GPIO_0 and GPIO_1 to view voltage limit and IDAC faults respectively. The state of GPIO_0 and GPIO_1 may be read using IO().

Table 8. LTC2970 Fault Reporting Bits and Conditions

CONDITION THAT GENERATES AN INSTANTANEOUS FAULT	FAULT() INSTANTANEOUS FAULT REPORTING	FAULT_EN() ENABLE FOR LATCHED FAULT REPORTING	FAULT_LA() LATCHED FAULT REPORTING
V12_adc[14:0] < V12_uv[14:0]	Fault_v12_uv	Fault_en_v12_uv	Fault_la_v12_uv
V12_adc[14:0] > V12_ov[14:0]	Fault_v12_ov	Fault_en_v12_ov	Fault_la_v12_ov
Vdd_adc[14:0] < Vdd_uv[14:0]	Fault_vdd_uv	Fault_en_vdd_uv	Fault_la_vdd_uv
Vdd_adc[14:0] > Vdd_ov[14:0]	Fault_vdd_ov	Fault_en_vdd_ov	Fault_la_vdd_ov
Ch1_b_adc[14:0] < Ch1_b_uv[14:0]	Fault_ch1_b_uv	Fault_en_ch1_b_uv	Fault_la_ch1_b_uv
Ch1_b_adc[14:0] > Ch1_b_ov[14:0]	Fault_ch1_b_ov	Fault_en_ch1_b_ov	Fault_la_ch1_b_ov
Idac_a_ch1[7:0] = 8'ff or 8'h00	Fault_ch1_a_idac	Fault_en_ch1_a_idac	Fault_la_ch1_a_idac
Ch1_a_adc[14:0] < Ch1_a_uv[14:0]	Fault_ch1_a_uv	Fault_en_ch1_a_uv	Fault_la_ch1_a_uv
Ch1_a_adc[14:0] > Ch1_a_ov[14:0]	Fault_ch1_a_ov	Fault_en_ch1_a_ov	Fault_la_ch1_a_ov
Ch0_b_adc[14:0] < Ch0_b_uv[14:0]	Fault_ch0_b_uv	Fault_en_ch0_b_uv	Fault_la_ch0_b_uv
Ch0_b_adc[14:0] > Ch0_b_ov[14:0]	Fault_ch0_b_ov	Fault_en_ch0_b_ov	Fault_la_ch0_b_ov
Idac_a_ch0[7:0] = 8'ff or 8'h00	Fault_ch0_a_idac	Fault_en_ch0_a_idac	Fault_la_ch0_a_idac
Ch0_a_adc[14:0] < Ch0_a_uv[14:0]	Fault_ch0_a_uv	Fault_en_ch0_a_uv	Fault_la_ch0_a_uv
Ch0_a_adc[14:0] > Ch0_a_ov[14:0]	Fault_ch0_a_ov	Fault_en_ch0_a_ov	Fault_la_ch0_a_ov

OPERATION

Procedure:

Update the overvoltage limit register with the value above which the ADC result should generate an overvoltage fault. Instantaneous overvoltage faults are updated after each ADC conversion. They are asserted high when the ADC result is greater than the overvoltage limit. They are cleared if the ADC result is less than or equal to the overvoltage limit. Setting the overvoltage limit to 14'h3fff inhibits instantaneous faults for the associated channel.

Update the undervoltage limit register with the value below which the ADC result should generate an undervoltage fault. Instantaneous undervoltage faults are updated after each ADC conversion. They are asserted high when the ADC result is less than the undervoltage limit. They are cleared if the ADC result is greater than or equal to the undervoltage limit. Setting the overvoltage limit to 14'h4000 inhibits instantaneous faults for the associated channel.

Update ADC_MON() control bits to allow ADC conversions on all channels that are to be monitored for over and under voltage limits. Instantaneous IDAC faults are polled after all ADC conversions are completed and set when the associated IDAC registers are at 'h00 of 'hff.

Read FAULT() to view the value of all instantaneous faults.

The IO(Io_cfg_0) command may be used to configure the GPIO_0 pin to output the internal Power_good flag. Power_good is asserted high if there are no instantaneous overvoltage or undervoltage faults. IO() may be used to read the value of Power_good through io_gpio_0.

The IO(Io_cfg_1) command may be used to configure the GPIO_1 pin to output the internal Idac_fault flag. Idac_fault is asserted high if either IDAC value is faulted. IO() may be used to read the value of Idac_fault through io_gpio_1.

Rules:

The overvoltage and undervoltage limits must be initialized; they do not have a default value.

All overvoltage limits, undervoltage limits and ADC results use 2's complement notation with bit position [14] of register [14:0] being used for the sign.

Instantaneous Ch0_a and Ch1_a faults may be used to trigger a servo on fault event.

Overvoltage and undervoltage faults require that the associated ADC_MON control bit be asserted high for instantaneous fault detection to be updated.

17. Generating and Monitoring Latched Faults

The LTC2970 is able to selectively latch instantaneous faults in the latched fault register FAULT_LA. Each instantaneous fault has an associated latched fault bit in FAULT_LA and a fault enable bit in FAULT_EN; (see Table 8) for details. When an instantaneous fault enable bit is high, any event that sets the instantaneous fault will simultaneously set the latched fault. The latched fault will remain set even if conditions permit the instantaneous fault to be cleared. The latched faults are immediately cleared whenever the associated fault enable bit is cleared. All latched faults are also cleared when the latched fault register is read over FAULT_LA().

The FAULT_INDEX() command may be read to determine if any latched faults are asserted. Reading FAULT_INDEX() does not clear latched faults. The $\overline{\text{ALERT}}$ output may also be configured to view whether any latched faults are asserted.

Procedure:

Follow procedure for generating instantaneous faults.

Write FAULT_EN() to enable any combination of latched faults.

Read FAULT_INDEX() to determine if any latched faults are asserted without clearing latched faults.

Read FAULT_LA() to monitor all latched faults. Reading FAULT_LA() will clear all latched faults. These will remain clear until the next time the LTC2970 polls and sets an associated instantaneous fault.

Setting IO(Io_alert_enb) low will cause $\overline{\text{ALERT}}$ to be asserted low whenever any one of the fourteen latched faults is asserted high. The value of the $\overline{\text{ALERT}}$ pin may also be read through IO(Alertb).

OPERATION

Rules:

See “Generating and Monitoring Instantaneous Faults”.

18. General Purpose Input/Output Pins

The GPIO_0 and GPIO_1 may be used to: (1) monitor instantaneous faults (see “Generating and Monitoring Instantaneous faults”); (2) control switcher run/start pins during tracking (see “Tracking Power Supplies Overview”); or (3) provide general purpose input/output pins.

Procedure:

To program GPIO_*n* as an open drain output set Io_cfg_*n* = 2’b10. The value written to Io_gpio_*n* will be output over GPIO_*n*.

To program GPIO_*n* as an input set Io_cfg_*n* = 2’b11. The value of GPIO_*n* may now be read through Io_gpio_*n*.

Rules:

The power on reset configurations for GPIO_0 and GPIO_1 are output pins with a value equal to the complement of the GPIO_CFG level.

19. Advanced Development Features

The internal ADC may be disabled with the ADC result registers accepting written I^2C data. This feature allows faults to be generated for diagnostic purposes, without having to generate an actual overvoltage or undervoltage event.

Procedure:

Set IO(Io_i2c_adc_wen) high to enable ADC result register writes and disable internal ADC updates.

Rules:

Io_i2c_adc_wen must be clear for normal operation.

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Margining DC/DC Converters with External Feedback Resistors

Figure 1 shows a typical application circuit for margining a power supply with an external feedback network. The V_{IN0_AP} and V_{IN0_AM} differential inputs sense the load voltage directly, and differential inputs V_{IN0_BP} and V_{IN0_BM} are connected across load current sense resistor R50. A correction voltage is developed at the I_{OUT0} pin by sourcing IDAC0’s current into resistor R40. R40 is Kelvin connected to the point-of-load GND in order to isolate V_{IOUT0} from ground bounce due to load current changes. V_{IOUT0} is replicated at V_{OUT0} by an on-chip, unity-gain voltage buffer. V_{OUT0} is then connected to the feedback node of the power supply through resistor R30. The feedback node can be isolated from the DAC’s correction voltage by placing the V_{OUT0} pin in high-impedance mode. Since the GPIO_CFG pin is pulled-up to V_{DD}, the LTC2970’s GPIO_0 pin will automatically hold the power supply’s RUN/SS pin low after power-up until the I^2C interface releases it.

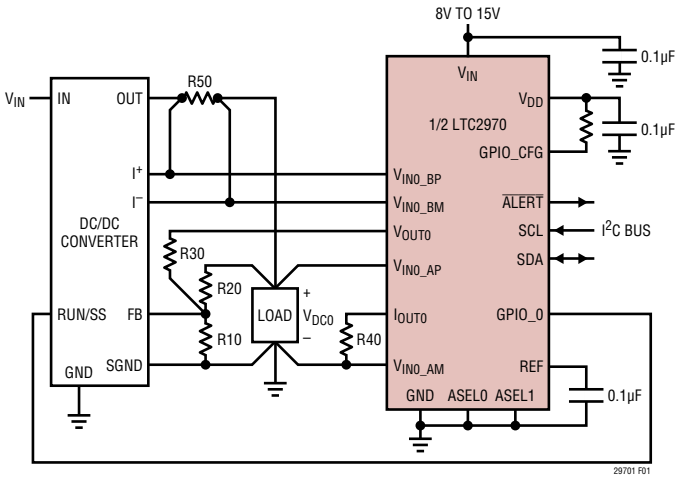

Figure 1. Typical LTC2970 Application Circuit for DC/DC Converters with External Feedback Resistors

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4-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors

The following 4-step procedure should be used to quickly calculate the resistor values shown for the Typical Application Circuit shown in Figure 1.

1. Assume values for feedback resistor R20 and the nominal DC/DC converter output voltage $V_{DC0,NOM}$, and solve for R10.

$V_{DC0,NOM}$ is the desired output voltage of the DC/DC converter when the LTC2970's V_{OUT0} pin is in a high impedance state. V_{FB0} is the voltage at the converter's feedback node when the loop is in regulation, and I_{FB0} is the feedback node's input current.

$$R10 = \frac{R20 \bullet V_{FB0}}{V_{DC,NOM} - I_{FB0} \bullet R20 - V_{FB0}} \quad (1)$$

2. Solve for the maximum value of R30 that yields the maximum required DC/DC converter output voltage $V_{DC0,MAX}$.

When V_{OUT0} is at 0V, the output of the DC/DC converter is at its maximum voltage. Note that the 10mV term corresponds to the maximum offset voltage of the IDAC 1X voltage buffer.

$$R30 \le \frac{R20 \bullet (V_{FB} - 10mV)}{V_{DC,MAX} - V_{DC,NOM}} \quad (2)$$

3. Solve for the minimum value of R40 that's needed to yield the minimum required DC/DC converter output voltage $V_{DC0,MIN}$.

The DC/DC converter output voltage will be a minimum when IDAC0 is at its full-scale current. In order to guarantee that R40 is large enough, assume that IDAC0's full-scale current is at the data sheet minimum of 236µA.

$$R40 \ge \frac{(V_{DC,NOM} - V_{DC,MIN}) \bullet \frac{R30}{R20} + V_{FB} + 10mV}{236\mu A} \quad (3)$$

4. Re-calculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

$$V_{DC0,NOM} = V_{FB} \bullet \left(1 + \frac{R20}{R10}\right) + I_{FB} \bullet R20 \quad (4)$$

$$V_{DC0,MIN} \le V_{DC0,NOM} - \frac{R20}{R30} \bullet \left(R40 \bullet 236\mu A - V_{FB0} - 10mV\right) \quad (5)$$

$$V_{DC0,MAX} \ge V_{DC0,NOM} + \frac{R20}{R30} \bullet \left(V_{FB0} - 10mV\right) \quad (6)$$

The margining resolution is bounded by:

$$V_{RES} \le \frac{\frac{R20}{R30} \bullet R40 \bullet 276\mu A}{256} \text{ volts/DAC LSB} \quad (7)$$

Margining DC/DC Converters with a TRIM Pin

Figure 2 illustrates a typical application circuit for margining the output voltage of a DC/DC converter with a TRIM Pin. The LTC2970's V_{OUT0} pin connects directly to the TRIM pin through resistor R30 and the I_{OUT0} pin is terminated at the converter's point-of-load ground through R40. Resistors R30 and R40 give this application circuit two degrees of freedom so that the margin-up and margin-down percentages can be specified independently.

Following power-up, the LTC2970's V_{OUT0} pin defaults to a high-impedance state. If the soft-connect feature

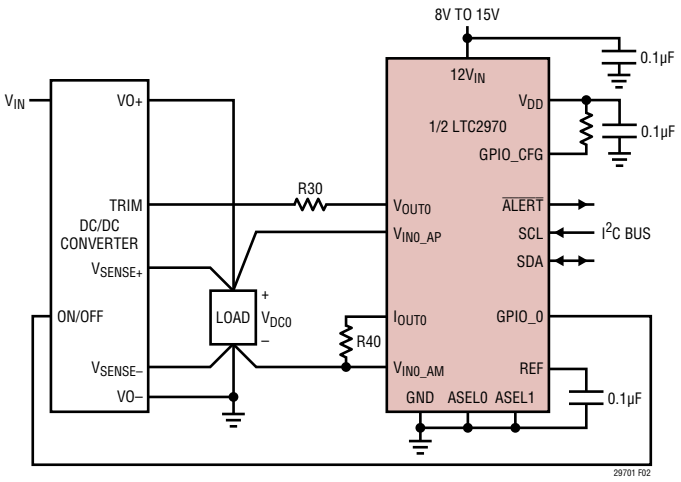

Figure 2. LTC2970 Application Circuit for DC/DC Converters with a TRIM Pin

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is used, the LTC2970 will automatically find the IDAC code that most closely approximates the TRIM pin's open-circuit voltage before enabling V_{OUT0}. Note: The relationship between V_{TRIM} and the converter's output is typically non-inverting, so be sure to set the LTC2970's CH0_a_idac_pol bit to 1 in order to allow the voltage servo feature to function properly.

DC/DC converters with a TRIM pin are usually margined high or low by connecting an external resistor between the TRIM pin and either the V_{SENSE}^+ or V_{SENSE}^- pin. The relationships between these resistors and the D% change in the output voltage of the DC/DC converter are typically expressed as:

$$R_{TRIM\_DOWN} = \frac{R_{TRIM} \bullet 50}{\Delta_{DOWN}\%} - R_{TRIM} \quad (8)$$

$$R_{TRIM\_UP} = \left[\frac{R_{TRIM} \bullet V_{DC} \bullet (100 + \Delta_{UP}\%)}{2 \bullet V_{REF} \bullet \Delta_{UP}\%} - \frac{R_{TRIM} \bullet 50}{\Delta_{UP}\%} - R_{TRIM}\right] \quad (9)$$

where R_{TRIM} is the resistance looking into the TRIM pin, V_{REF} is the TRIM pin's opern-circuit output voltage and V_{DC} is the DC/DC converter's nominal output voltage. Δ_{UP}% and Δ_{DOWN}% denote the percentage change in the converter's output voltage when margining up or down respectively.

2-Step Resistor Selection Procedure for DC/DC Converters with a TRIM Pin

The following two-step procedure should be used to calculate values for resistors R30 and R40 shown in Figure 2.

1. Solve for R30:

$$R30 \le R_{TRIM} \bullet \left(\frac{50 - \Delta_{DOWN}\%}{\Delta_{DOWN}\%}\right) \quad (10)$$

2. Solve for R40:

$$R40 \ge \left(1 + \frac{\Delta_{UP}\%}{\Delta_{DOWN}\%}\right) \bullet \frac{V_{REF}}{236\mu A} \quad (11)$$

Tracking with the LTC2970-1

A typical LTC2970-1 tracking application circuit is shown in Figure 3 (the sequence of events for tracking are described in sections 9 and 10 of the Operation section). The GPIO_0 and GPIO_1 pins are tied directly to their respective DC/DC converter RUN/SS pins. Since GPIO_CFG is pulled-up to V_{DD}, the LTC2970-1 will automatically hold off the DC/DC converters after power-up by asserting open drain outputs GPIO_0 and GPIO_1 low. N-channel FETs Q10/11 and diodes D10/11 form unidirectional range switches around resistors R30A/31A while GPIO_CFG is high. These range switches allow the LTC2970-1's V_{OUT0} and V_{OUT1} pins to drive the converter outputs all the way to/from ground through resistors R30B/31B. When GPIO_CFG pulls low, N-channel FETs Q10 and Q11 will turn off. R30A/31A and R30B/31B then combine in series for normal margin operation. The 100k/0.1µF low-pass filter in series with the gates of Q10/11 minimizes charge injection into the feedback nodes of the DC/DC converters when GPIO_CFG pulls low.

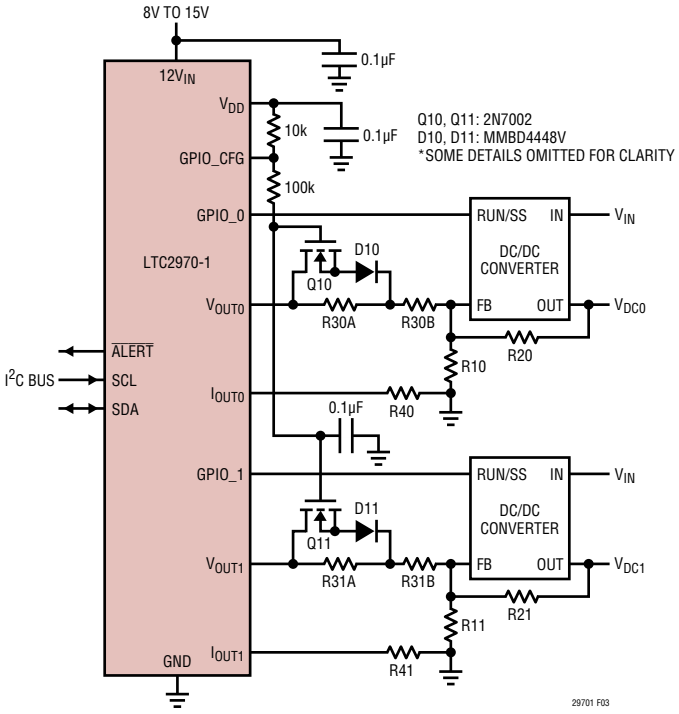

Figure 3. LTC2970-1 Tracking Application Circuit

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7-Step Procedure for Calculating Tracking Application Circuit Resistor Values, Counter Delay Values, and Terminal IDAC Codes

The following 7-step procedure should be used to calculate the resistor values, tracking counter delays, and terminal IDAC codes for the Tracking Application Circuit shown in Figure 3.

1. Assume a value for R20 and solve for R21.

$V_{DCn,NOM}$ is the output voltage of the DC/DC converter when the LTC2970's V_{OUTn} pin is in a high impedance state.

$$R21 = R20 \bullet \frac{V_{DC1,NOM}}{V_{DC0,NOM}} \quad (12)$$

2. Solve for R10 and R11.

$$R1n = \frac{R2n}{\left(\frac{V_{DCn,NOM}}{V_{FBn}} - 1\right)} \quad (13)$$

3. Solve for R40 and R41.

For simplicity, this procedure assumes that R40 = R41. $V_{DCn,MAX}$ and $V_{DCn,MIN}$ are the maximum and minimum converter output margin voltages, respectively.

The value of R40 = R41 is constrained by:

$$R40 = R41 \geq \quad (14)$$

$$\frac{V_{FBn} \bullet \left[\left(\frac{\left(V_{DCn,NOM} - V_{DCn,MIN}\right)}{\left(V_{DCn,MAX} - V_{DCn,NOM}\right)}\right) + 1\right] + 10mV}{236\mu A}$$

Due to the forward drop of diodes D10 and D11 (0.8V max), the minimum value for R40 = R41 from expression (14) may result in small or even negative values of R30 and R31 in Step 4. If this is the case, assume a minimum allowable value for R3*n*B, and use the following expression to calculate the minimum value R40 = R41:

$$R40 = R41 \geq \quad (15)$$

$$\frac{V_{FBn} \bullet \left(1 + \frac{R3nB}{R1n} + \frac{R3nB}{R2n}\right) + 0.8V + 10mV}{236\mu A}$$

Note: Use the channel whose parameters yield the maximum value for R40 = R41.

4. Solve for R30B and R31B.

Solve for the upper limits of R30B and R31B and then determine which resistor value constrains the maximum value of the other resistor using Equation 17.

$$R3nB \leq \frac{\left(R4n \bullet 236\mu A - V_{FBn} - 0.8V - 10mV\right)}{V_{FBn} \bullet \left(\frac{1}{R1n} + \frac{1}{R2n}\right)} \quad (16)$$

$$\frac{R30B}{R20} = \frac{R31B}{R21} \quad (17)$$

5. Solve for R30A and R31A.

R30A and R31A are constrained by:

$$R3nA \leq \quad (18)$$

$$\frac{R2n}{\left(1 + \frac{R2n}{R1n}\right) \bullet \left(\frac{V_{DCn,MAX} - V_{DCn,NOM}}{V_{DCn,NOM}}\right)} - R3nB$$

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6. Solve for Channel 1's tracking counter delay relative to Channel 0, CH1_A_DELAY_TRACK().

$$CH1\_A\_DELAY\_TRACK() = \frac{\left(V_{DC1,NOM}{}' - V_{DC0,NOM}{}'\right) \bullet \frac{R31B}{R21}}{1\mu A / count \bullet R41} (counts) \quad (19)$$

Note: $V_{DCn,NOM}{}'$ is based on the final values of R2*n* and R1*n*. If the result for CH1_A_DELAY_TRACK() is less than 0, apply the unsigned result to the CH0_A_DELAY_TRACK() register.

7. Solve for the IDAC0 and IDAC1 terminal tracking codes, Ch*n*_a_idac_track[7:0].

$$Chn\_a\_idac\_track[7:0] = 255 - \frac{V_{FBn}}{1\mu A / LSB \bullet R4n} (LSB's) \quad (20)$$

Note: This formula assumes that the Ch*n*_a_idac_pol bit is set to 0.

Margining Application Circuit Design Example

Consider the LTC2970 application circuit shown in Figure 1. Channel 0 is a DC/DC converter whose output needs to be varied between 3.63V and 1.62V. V_{FB0} = 0.8V and assume that I_{FB0} = 0A.

1. Assume values for feedback resistor R20 and the nominal DC/DC converter output voltage $V_{DC0,NOM}$, and solve for R10.

Let $V_{DC0,NOM}$ = 2.625V (the average of 3.63V and 1.62V) and assume that R20 = 10kΩ. From Equation 1:

$$R10 = \frac{R20 \bullet V_{FB0}}{V_{DC,NOM} - I_{FB0} \bullet R20 - V_{FB0}} = \frac{10k\Omega \bullet 0.8V}{2.625V - 0.8V} = 4,384\Omega$$

Let R10 = 4.37kΩ (the nearest E192 series resistor value).

2. Solve for the value of R30 that yields the maximum required DC/DC converter output voltage $V_{DC0,MAX}$

From Equation 2:

$$R30 \le \frac{R20 \bullet \left(V_{FB} - 10mV\right)}{V_{DC,MAX} - V_{DC,NOM}} = \frac{10.0k\Omega \bullet \left(0.8V - 10mV\right)}{3.63V - 2.625V} = 7,861\Omega$$

Let R30 = 7.68kΩ.

3. Solve for the value of R40 that's needed to yield the minimum required DC/DC converter output voltage $V_{DC0,MIN}$.

From Equation 3:

$$R40 \ge \frac{\left(V_{DC,NOM} - V_{DC,MIN}\right) \bullet \frac{R30}{R20} + V_{FB}}{236\mu A} = \frac{\left(2.625V - 1.62V\right) \bullet \frac{7.96k\Omega}{10k\Omega} + 0.8V}{236\mu A} = 6,780\Omega$$

Let R40 = 6.81kΩ.

4. Re-calculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

From Equations 4, 5, and 6:

$$V_{DC0,NOM} = V_{FB} \bullet \left(1 + \frac{R20}{R10}\right) + I_{FB} \bullet R20 = 0.8V \bullet \left(1 + \frac{10k\Omega}{4.37k\Omega}\right) = 2.631V$$

$$V_{DC0,MIN} < V_{DC0,NOM} - \frac{R20}{R30} \bullet \left(236\mu A \bullet R40 - V_{FB0}\right)$$

$$\rightarrow V_{DC0,MIN} < 2.631V - \frac{10k\Omega}{7.68k\Omega} \bullet \left(236\mu A \bullet 6.81k\Omega - 0.8V - 10mV\right) = 1.59V$$

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$$V_{DC0,MAX} > V_{DC0,NOM} + \frac{R20}{R30} \bullet \left(V_{FB0} - 10mV\right)$$

$$\rightarrow V_{DC0,MAX} > 2.631V + \frac{10k\Omega}{7.68k\Omega} \bullet \left(0.8V - 10mV\right) = 3.660V$$

From Equation 7, the margining resolution will be less than:

$$V_{RES} < \frac{\frac{R20}{R30} \bullet R40 \bullet 276\mu A}{256} = \frac{\frac{10k\Omega}{7.68k\Omega} \bullet 6.65k\Omega \bullet 276\mu A}{256} = 9.33mV/LSB$$

Margining DC/DC Converter with TRIM Pin Design Example

The output voltage of the DC/DC converter in Figure 2 needs to be margined ±10% about its nominal value. Assume that R_{TRIM} = 10.22kΩ and V_{REF} = 1.225V.

1. Solve for R30 using Equation 10:

$$R30 \le R_{TRIM} \bullet \left(\frac{50 - \Delta_{DOWN}\%}{\Delta_{DOWN}\%}\right)$$

$$= 10.22k\Omega \bullet \left(\frac{50 - 10}{10}\right) = 40,880\Omega$$

Let R30 = 39.2kΩ.

2. Solve for R40 using Equations 11:

$$R40 \ge \left(1 + \frac{\Delta_{UP}\%}{\Delta_{DOWN}\%}\right) \bullet \frac{V_{REF}}{236\mu A}$$

$$= \left(1 + \frac{10}{10}\right) \bullet \frac{1.225V}{236\mu A} = 10,381\Omega$$

Let R40 = 10.5kΩ.

Tracking Application Circuit Design Example

Consider the LTC2970-1 application circuit shown in Figure 3. Channel 0 is a 1.8V DC/DC converter while channel 1 is a 2.5V switching power supply. Both converters have a feedback node voltage of 0.8V and need to track on and off coincidentally. In addition, a margin range of +5% and –10% is required for each supply.

1. Assume a value for R20 and solve for R21.

Let R20 = 5,970Ω. From Equation 12:

$$R21 = R20 \bullet \frac{V_{DC1,NOM}}{V_{DC0,NOM}} = 5,970\Omega \bullet \frac{2.5V}{1.8V} = 8,292\Omega$$

Let R21 = 8,250Ω (the nearest E192 Series resistor value).

2. Solve for R10 and R11.

From Equation 13:

$$R10 = \frac{R20}{\left(\frac{V_{DC0,NOM}}{V_{FB0}} - 1\right)} = \frac{5,970\Omega}{\left(\frac{1.8V}{0.8V} - 1\right)} = 4,776\Omega$$

$$R11 = \frac{R21}{\left(\frac{V_{DC1,NOM}}{V_{FB1}} - 1\right)} = \frac{8,250\Omega}{\left(\frac{2.5V}{0.8V} - 1\right)} = 3,882\Omega$$

Let R10 = 4,750Ω and R11 = 3,880Ω.

3. Solve for R40 and R41.

Assume that R40 = R41.

$$R40 = R41 \ge \frac{V_{FBn} \bullet \left(\frac{\left(V_{DCn,NOM} - V_{DCn,MIN}\right)}{\left(V_{DCn,MAX} - V_{DCn,NOM}\right)} + 1\right) + 10mV}{236\mu A} = \frac{0.8V \bullet \left(\frac{(1 - 0.9)}{(1.05 - 1)} + 1\right) + 10mV}{236\mu A} = 10,212\Omega$$

Let R40 = R41 = 10.5kΩ

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4. Solve for R30B and R31B.

$$R30B \le \frac{(R40 \bullet 236\mu A - V_{FB0} - 0.8V - 10mV)}{V_{FB0} \bullet \left(\frac{1}{R10} + \frac{1}{R20}\right)} =$$

$$\frac{(10.5k\Omega \bullet 236\mu A - 0.8V - 0.8V - 10mV)}{0.8V \bullet \left(\frac{1}{4,750\Omega} + \frac{1}{5,970\Omega}\right)} = 2,870\Omega$$

$$R31B \le \frac{(R41 \bullet 236\mu A - V_{FB1} - 0.8V - 10mV)}{V_{FB1} \bullet \left(\frac{1}{R11} + \frac{1}{R21}\right)} =$$

$$\frac{(10.5k\Omega \bullet 236\mu A - 0.8V - 0.8V - 10mV)}{0.8V \bullet \left(\frac{1}{3,880\Omega} + \frac{1}{8,250\Omega}\right)} = 2,863\Omega$$

For coincident tracking to occur Equation 17 also must be satisfied:

$$\frac{R30B}{R20} = \frac{R31B}{R21}$$

$$\rightarrow R30B = \frac{R31B}{R21} \bullet R20 = \frac{2,863\Omega}{8,250\Omega} \bullet 5,970\Omega = 2,078\Omega$$

$$\rightarrow R31B = \frac{R30B}{R20} \bullet R21 = \frac{2,870\Omega}{5,970\Omega} \bullet 8,250\Omega = 3,957\Omega$$

Let R30B = 2,100Ω and R31B = 2,890Ω.

5. Solve for R30A and R31A.

Referring to Equation 18:

$$R30A \le \frac{R20}{\left(1 + \frac{R20}{R10}\right) \bullet \left(\frac{V_{DC0,MAX} - V_{DC0,NOM}}{V_{DC0,NOM}}\right)} - R30B =$$

$$\frac{5,970\Omega}{\left(1 + \frac{5,970\Omega}{4,750\Omega}\right) \bullet \left(\frac{1.05 - 1}{1}\right)} - 2,100\Omega = 50,806\Omega$$

$$R31A \le \frac{R21}{\left(1 + \frac{R21}{R11}\right) \bullet \left(\frac{V_{DC1,MAX} - V_{DC1,NOM}}{V_{DC1,NOM}}\right)} - R31B =$$

$$\frac{8,250\Omega}{\left(1 + \frac{8,250\Omega}{3,880\Omega}\right) \bullet \left(\frac{1.05 - 1}{1}\right)} - 2,890\Omega = 49,888\Omega$$

Let R30A = 49.9kΩ and R31A = 48.7kΩ.

6. Solve for Channel 1's tracking counter delay relative to Channel 0, CH1_A_DELAY_TRACK().

First, recalculate the values of $V_{DCn,NOM}$ based on the final values of R1*n* and R2*n*:

$$V_{DC0,NOM}{}' = V_{FB} \bullet \left(1 + \frac{R20}{R10}\right) + I_{FB} \bullet R20 =$$

$$0.8V \bullet \left(1 + \frac{5,970\Omega}{4,750\Omega}\right) + 0 = 1.805V$$

$$V_{DC1,NOM}{}' = 0.8V \bullet \left(1 + \frac{8,250\Omega}{3,880\Omega}\right) + 0 = 2.501V$$

Next, apply Equation 19:

$$CH1\_A\_DELAY\_TRACK() =$$

$$\frac{\left(V_{DC1,NOM}{}' - V_{DC0,NOM}{}'\right) \bullet \frac{R31B}{R21}}{1\mu A / count \bullet R41} =$$

$$\frac{(2.501V - 1.805V) \bullet \frac{2,890\Omega}{8,250\Omega}}{1\mu A / count \bullet 10.5k\Omega} = 23 counts$$

7. Solve for the IDAC0 and IDAC1 terminal tracking codes, Ch*n*_a_idac_track[7:0].

$$Ch0\_a\_idac[7:0] = Ch1\_a\_idac[7:0] =$$

$$255 - \frac{0.8V}{1\mu A / LSB \bullet 10.5k\Omega} = 179$$

APPLICATIONS INFORMATION

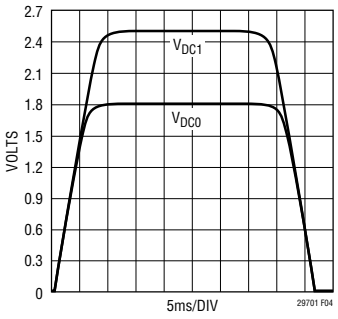


Figure 4. Tracking Design Example DC/DC Converter Output Waveforms

Figure 4 shows the DC/DC converter output voltages for this design example tracking-up and tracking-down.

Temperature Sensor Conversion

The LTC2970's internal temperature sensor output is proportional to absolute temperature (PTAT). In order to convert the ADC reading to degrees Celsius, apply the following formula:

$$\text{result}(°C) = \frac{\text{ADC\_temp\_sensor\_reading}}{4} - 273.15 \quad (21)$$

Negative Power Supply Application Circuit

Figure 5 shows the LTC2970 controlling a negative power supply. The R30/R40 resistor divider translates the point of load voltage to the LTC2970's V_{IN0_A} inputs while the V_{IN0_B} inputs monitor the converter's input current I • R drop across resistor R_{SENSE}. Since the V_{DD} pin voltage is monitored by the LTC2970, its tolerance can be accounted for when calculating the point of load voltage. Transistor Q1 allows the I_{OUT0} pin to force current into the converter's feedback node without forward biasing the LTC2970's I_{OUT0} body diode. Note that I_{OUT0}'s output current defaults to 128mA after the LTC2970 comes out of power-on reset.

15-Bit Programmable Power Supply Application Circuit

Figure 6 illustrates how both servo channels of the LTC2970 can be configured to adjust a single DC/DC converter over a 15-bit dynamic range. R30 and R31 are sized to force 1 bit of overlap between the coarse (channel 0) and fine (channel 1) servo loops. One coarse servo iteration should be performed first on channel 0 with IDAC1 programmed to mid-scale, and then channel 1 can be programmed to servo to the desired voltage.

Programmable Reference Application Circuit

Figure 7 shows a LTC2970 configured as a programmable reference that can span a 0V to 3.5V range with a resolution of 100µV and an absolute accuracy of less than ±0.5%. The two IDAC's are paralleled by terminating IDAC1's output resistor in the V_{OUT0} output and taking the output of the composite DAC from V_{OUT1}. IDAC0 should servo once with IDAC1 set to mid-scale, and then IDAC1 can servo once, continuously, or trigger on drift to the desired target voltage.

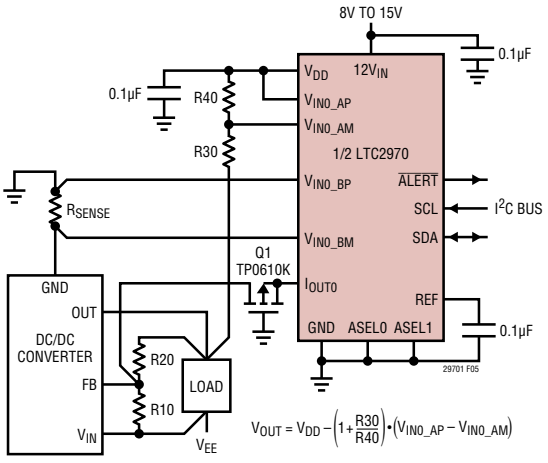


Figure 5. Negative Power Supply Application Circuit

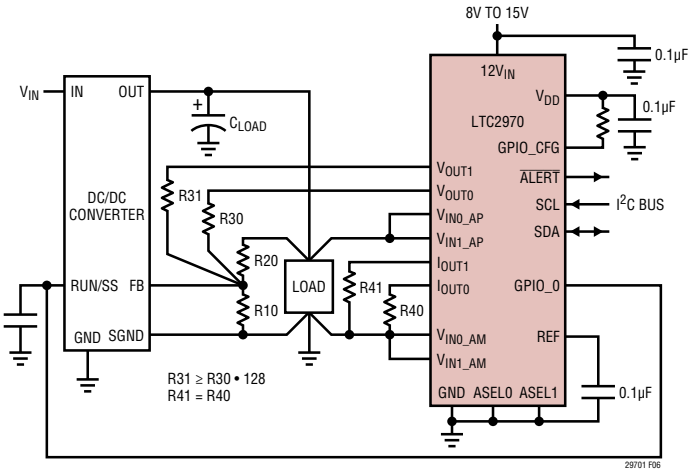


Figure 6. Programmable Power Supply Application Circuit

TYPICAL APPLICATIONS

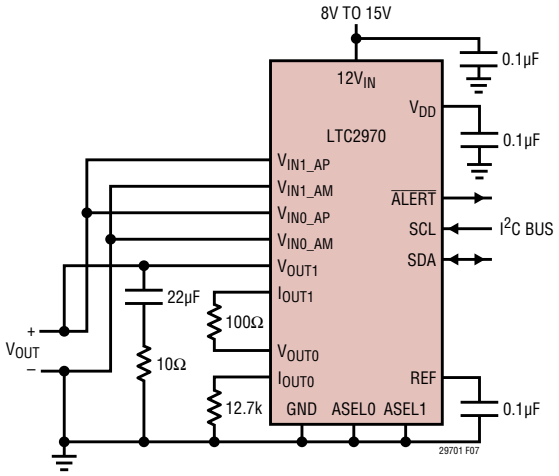
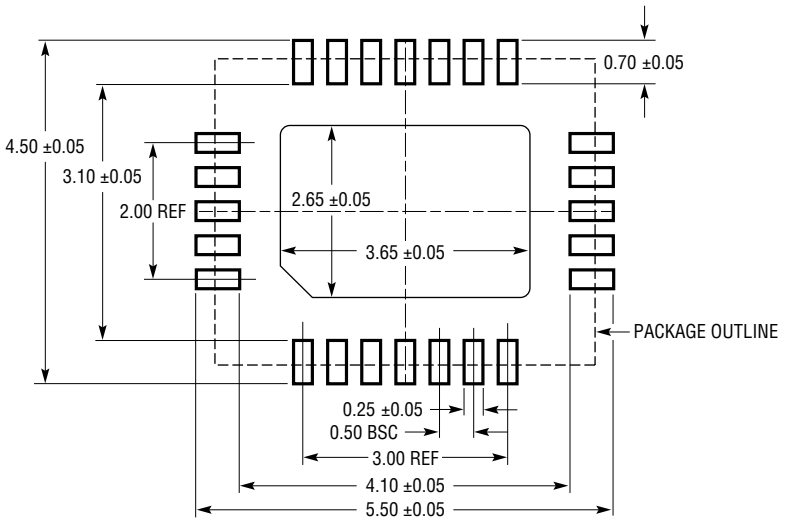


Figure 7. Programmable Reference Application Circuit

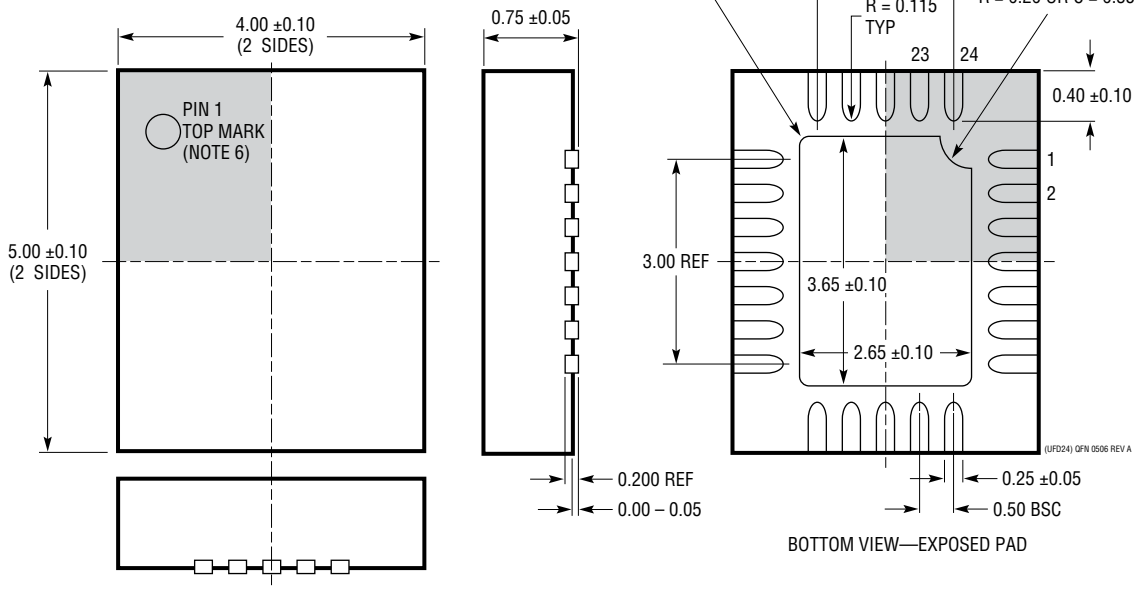
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2970#packaging for the most recent package drawings.

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	06/14	Order Information: Corrected DFN to QFN	2
		Figure 5: Corrected top R10 to R30, top R20 to R40	34
E	10/16	Added H-grade information	2
		Fixed V_{IH} and V_{IL} specification column placement	4
		Updated temperature dependent curves to include H-grade temperature range	7, 8, 9
		Clarified that the $12V_{IN}$ ADC measurement has a divide by 3	18