Ultralow Voltage Step-Up Converter and Power Manager

FEATURES

- **Operates from Inputs of 20mV**
- **Complete Energy Harvesting Power Management System**
  - **Selectable V_{OUT} of 2.5V, 3V, 3.7V or 4.5V**
  - **LDO: 2.2V at 3mA**
  - **Logic Controlled Output**
  - **Reserve Energy Output**
- **Power Good Indicator**
- Uses Compact Step-Up Transformers
- Small 12-Lead (3mm × 4mm) DFN or 16-Lead SSOP Packages

APPLICATIONS

- Remote Sensors and Radio Power
- Surplus Heat Energy Harvesting
- HVAC Systems
- Industrial Wireless Sensing
- Automatic Metering
- Building Automation
- Predictive Maintenance

DESCRIPTION

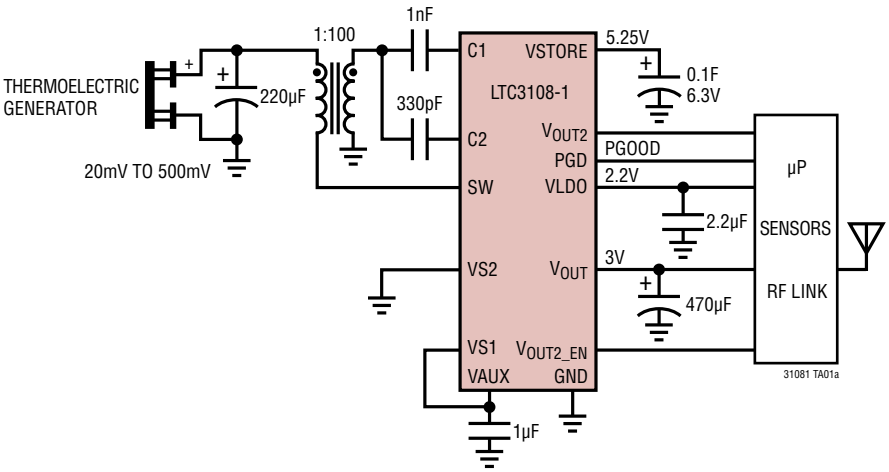
The LTC®3108-1 is a highly integrated DC/DC converter ideal for harvesting and managing surplus energy from extremely low input voltage sources such as TEGs (thermoelectric generators), thermopiles and small solar cells. The step-up topology operates from input voltages as low as 20mV.

Using a small step-up transformer, the LTC3108-1 provides a complete power management solution for wireless sensing and data acquisition. The 2.2V LDO powers an external microprocessor, while the main output is programmed to one of four fixed voltages to power a wireless transmitter or sensors. The power good indicator signals that the main output voltage is within regulation. A second output can be enabled by the host. A storage capacitor provides power when the input voltage source is unavailable. Extremely low quiescent current and high efficiency design ensure the fastest possible charge times of the output reservoir capacitor. The LTC3108-1 is functionally equivalent to the LTC3108 except for its unique fixed V_{OUT} options.

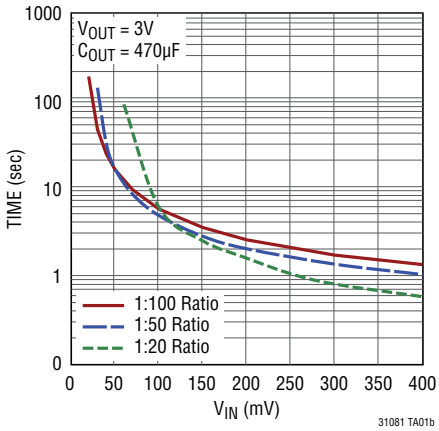
The LTC3108-1 is available in a small, thermally enhanced 12-lead (3mm × 4mm) DFN package and a 16-lead SSOP package.

TYPICAL APPLICATION

Wireless Remote Sensor Application Powered From a Peltier Cell



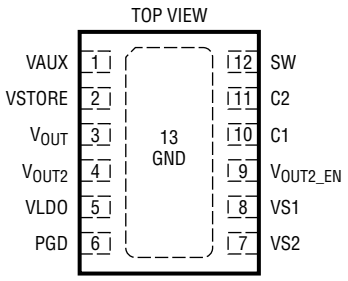
V_{OUT} Charge Time



ABSOLUTE MAXIMUM RATINGS (Note 1)

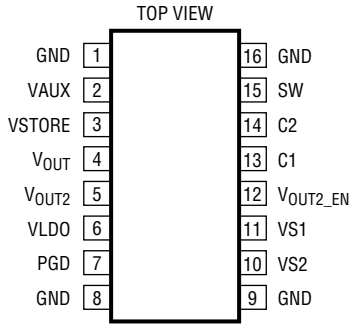
SW Voltage .....–0.3V to 2V
C1 Voltage.....–0.3V to 6V
C2 Voltage (Note 5).....–8V to 8V
V_{OUT2}, V_{OUT2_EN}.....–0.3V to 6V
VAUX.....15mA into VAUX
VS1, VS2, VAUX, V_{OUT}, PGD.....–0.3V to 6V
VLDO, VSTORE.....–0.3V to 6V
Operating Junction Temperature Range
(Note 2)..... –40°C to 125°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB (NOTE 4)



GN PACKAGE
16-LEAD PLASTIC SSOP NARROW

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3108EDE-1#PBF	LTC3108EDE-1#TRPBF	31081	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3108IDE-1#PBF	LTC3108IDE-1#TRPBF	31081	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3108EGN-1#PBF	LTC3108EGN-1#TRPBF	31081	16-Lead Plastic SSOP	–40°C to 125°C
LTC3108IGN-1#PBF	LTC3108IGN-1#TRPBF	31081	16-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified for other fixed output voltages or wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). VAUX = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	Using 1:100 Transformer Turns Ratio, VAUX = 0V			20	50	mV
No-Load Input Current	Using 1:100 Transformer Turns Ratio; V_{IN} = 20mV, V_{OUT2_EN} = 0V; All Outputs Charged and in Regulation			3		mA
Input Voltage Range	Using 1:100 Transformer Turns Ratio	●	$V_{STARTUP}$		500	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). VAUX = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	VS1 = VS2 = GND VS1 = VAUX, VS2 = GND VS1 = GND, VS2 = VAUX VS1 = VS2 = VAUX	● ● ● ●	2.45 2.94 3.626 4.41	2.50 3.00 3.70 4.50	2.55 3.06 3.774 4.59	V V V V
V_{OUT} Quiescent Current	V_{OUT} = 3.7V, V_{OUT2_EN} = 0V			0.2		µA
VAUX Quiescent Current	No Load, All Outputs Charged			6	9	µA
LDO Output Voltage	0.5mA Load	●	2.134	2.2	2.266	V
LDO Load Regulation	For 0mA to 2mA Load			0.5	1	%
LDO Line Regulation	For VAUX from 2.5V to 5V			0.05	0.2	%
LDO Dropout Voltage	I_{VLDO} = 2mA	●		100	200	mV
LDO Current Limit	VLDO = 0V	●	4	11		mA
V_{OUT} Current Limit	V_{OUT} = 0V	●	2.8	4.5	7	mA
VSTORE Current Limit	VSTORE = 0V	●	2.8	4.5	7	mA
VAUX Clamp Voltage	Current into VAUX = 5mA	●	5	5.25	5.55	V
VSTORE Leakage Current	VSTORE = 5V			0.1	0.3	µA
V_{OUT2} Leakage Current	V_{OUT2} = 0V, V_{OUT2_EN} = 0V			0.1		µA
VS1, VS2 Threshold Voltage		●	0.4	0.85	1.2	V
VS1, VS2 Input Current	VS1 = VS2 = 5V			0.01	0.1	µA
PGD Threshold (Rising)	Measured Relative to the V_{OUT} Voltage			–7.5		%
PGD Threshold (Falling)	Measured Relative to the V_{OUT} Voltage			–9		%
PGD V_{OL}	Sink Current = 100µA			0.15	0.3	V
PGD V_{OH}	Source Current = 0		2.1	2.2	2.3	V
PGD Pull-Up Resistance				1		MΩ
V_{OUT2_EN} Threshold Voltage	V_{OUT2_EN} Rising	●	0.4	1	1.3	V
V_{OUT2_EN} Pull-Down Resistance				5		MΩ
V_{OUT2} Turn-On Time				5		µs
V_{OUT2} Turn-Off Time	(Note 3)			0.15		µs
V_{OUT2} Current Limit	V_{OUT} = 3.7V	●	0.15	0.3	0.45	A
V_{OUT2} Current Limit Response Time	(Note 3)			350		ns
V_{OUT2} P-Channel MOSFET On-Resistance	V_{OUT} = 3.7V (Note 3)			1.3		Ω
N-Channel MOSFET On-Resistance	C2 = 5V (Note 3)			0.5		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3108-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3108-1E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3108-1I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and other environmental factors. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$, where θ_{JA} is the package thermal impedance.

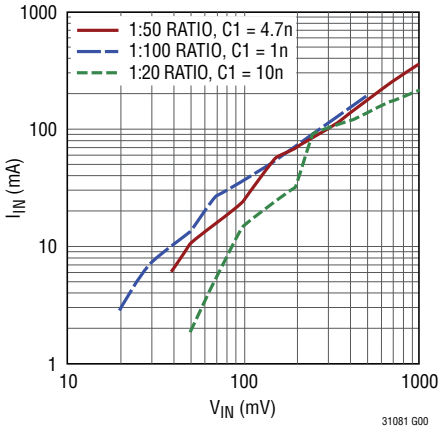
Note 3: Specification is guaranteed by design and not 100% tested in production.

Note 4: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much higher than 43°C/W.

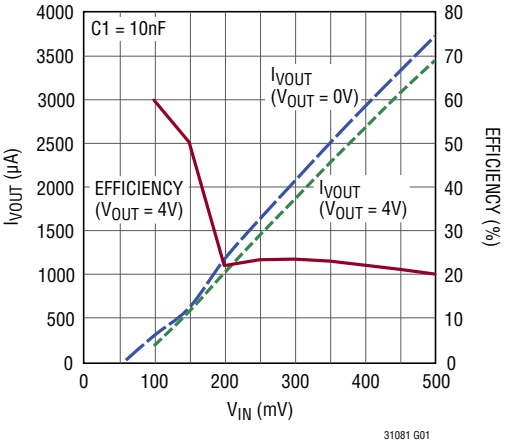
Note 5: The absolute maximum rating is a DC rating. Under certain conditions in the applications shown, the peak AC voltage on the C2 pin may exceed ±8V. This behavior is normal and acceptable because the current into the pin is limited by the impedance of the coupling capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

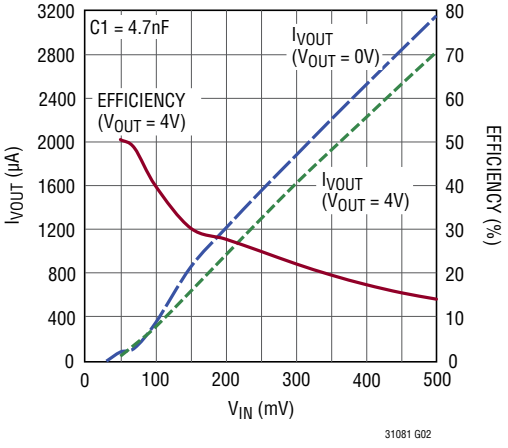
I_{IN} vs V_{IN}, (V_{OUT} = 0V)



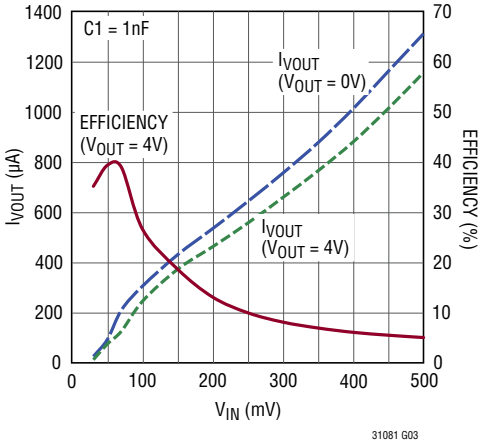
I_{VOUT} and Efficiency vs V_{IN}, 1:20 Ratio Transformer



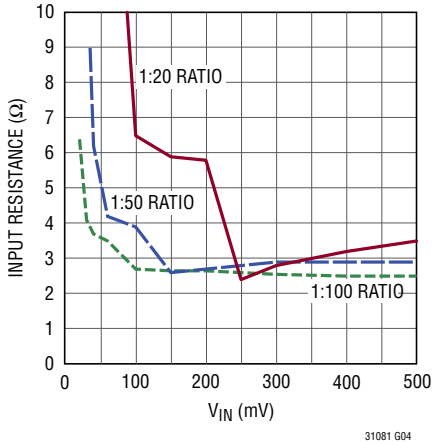
I_{VOUT} and Efficiency vs V_{IN}, 1:50 Ratio Transformer



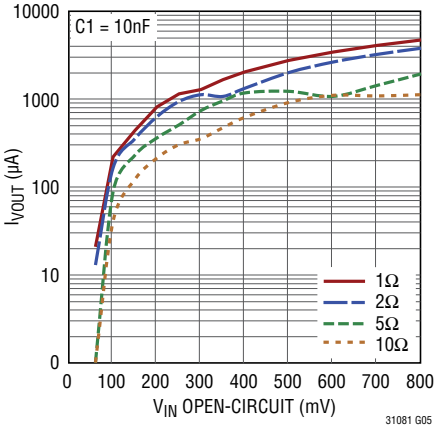
I_{VOUT} and Efficiency vs V_{IN}, 1:100 Ratio Transformer



Input Resistance vs V_{IN} (V_{OUT} Charging)

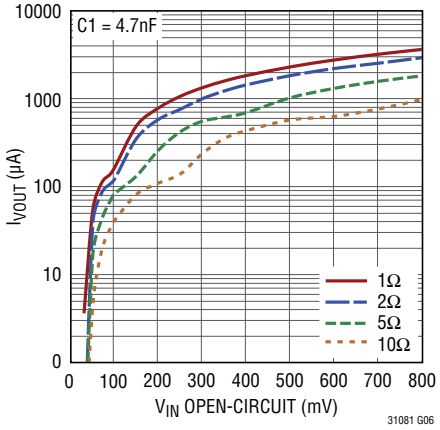


I_{VOUT} vs V_{IN} and Source Resistance, 1:20 Ratio

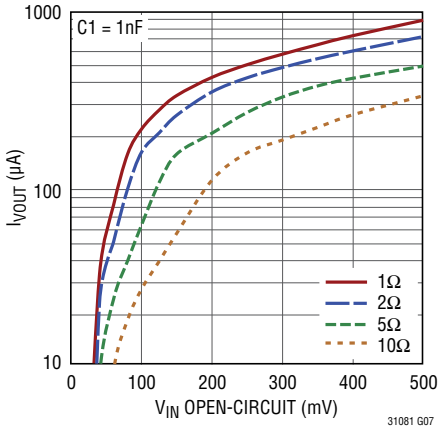


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

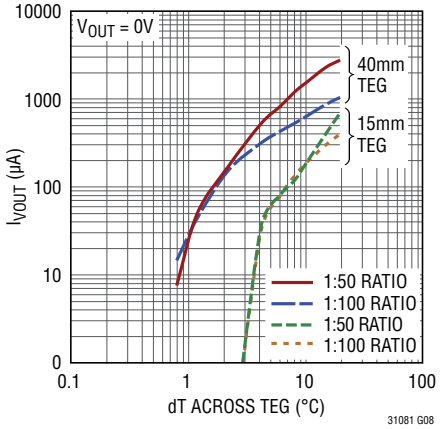
I_{VOUT} vs V_{IN} and Source Resistance, 1:50 Ratio



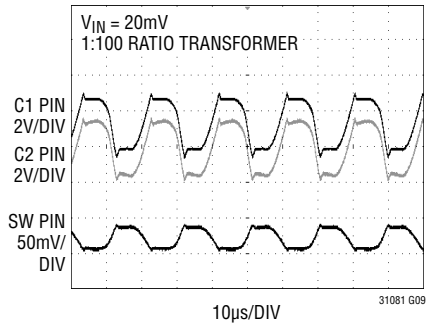
I_{VOUT} vs V_{IN} and Source Resistance, 1:100 Ratio



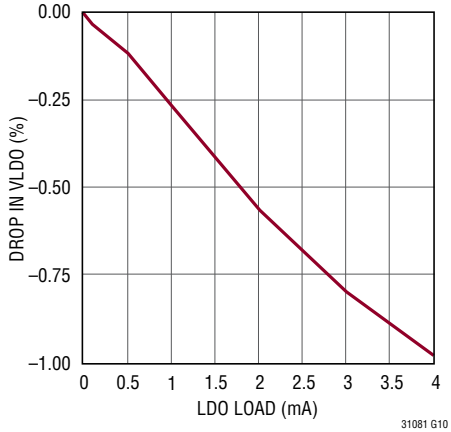
I_{VOUT} vs dT and TEG Size, 1:100 Ratio



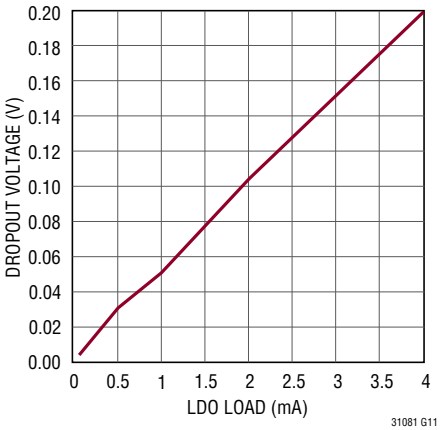
Resonant Switching Waveforms



LDO Load Regulation

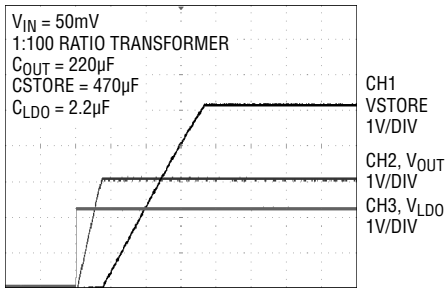


LDO Dropout Voltage

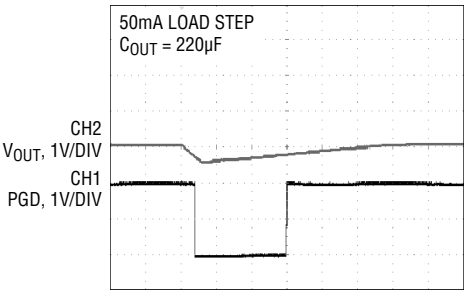


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

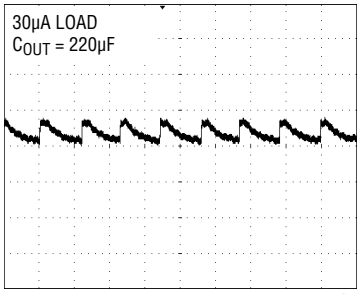
Start-Up Voltage Sequencing



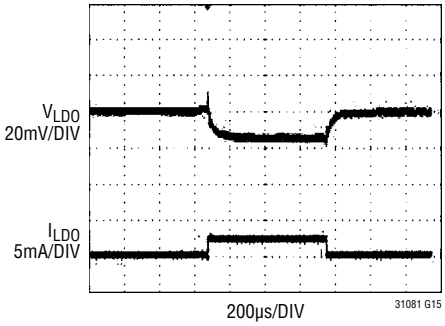
V_{OUT} and PGD Response During a Step Load



V_{OUT} Ripple

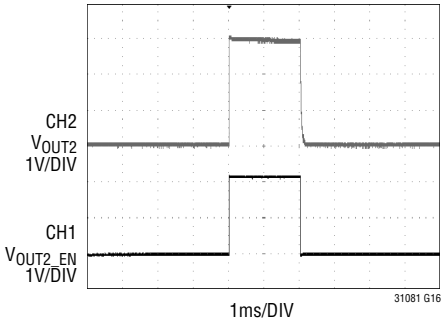


LDO Step Load Response



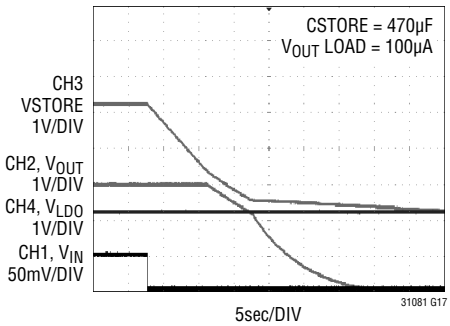
0mA TO 3mA LOAD STEP
C_{LDO} = 2.2µF

Enable Input and V_{OUT2}



10mA LOAD ON V_{OUT2}
C_{OUT} = 220µF

Running on Storage Capacitor



PIN FUNCTIONS (DFN/SSOP)

VAUX (Pin 1/Pin 2): Output of the Internal Rectifier Circuit and V_{CC} for the IC. Bypass VAUX with at least 1µF of capacitance. An active shunt regulator clamps VAUX to 5.25V (typical).

VSTORE (Pin 2/Pin 3): Output for the Storage Capacitor or Battery. A large capacitor may be connected from this pin to GND for powering the system in the event the input voltage is lost. It will be charged up to the maximum VAUX clamp voltage. If not used, this pin should be left open or tied to VAUX.

V_{OUT} (Pin 3/Pin 4): Main Output of the Converter. The voltage at this pin is regulated to the voltage selected by VS1 and VS2 (see Table 1). Connect this pin to an energy storage capacitor or to a rechargeable battery.

V_{OUT2} (Pin 4/Pin 5): Switched Output of the Converter. Connect this pin to a switched load. This output is open until V_{OUT2_EN} is driven high, then it is connected to V_{OUT} through a 1.3Ω P-channel switch. If not used, this pin should be left open or tied to V_{OUT}. The peak current in this output is limited to 0.3A typical.

VLDO (Pin 5/Pin 6): Output of the 2.2V LDO. Connect a 2.2µF or larger ceramic capacitor from this pin to GND. If not used, this pin should be tied to VAUX.

PGD (Pin 6/Pin 7): Power Good Output. When V_{OUT} is within 7.5% of its programmed value, PGD will be pulled up to VLDO through a 1MΩ resistor. If V_{OUT} drops 9% below its programmed value PGD will go low. This pin can sink up to 100µA.

VS2 (Pin 7/Pin 10): V_{OUT} Select Pin 2. Connect this pin to ground or VAUX to program the output voltage (see Table 1).

VS1 (Pin 8/Pin 11): V_{OUT} Select Pin 1. Connect this pin to ground or VAUX to program the output voltage (see Table 1).

V_{OUT2_EN} (Pin 9/Pin 12): Enable Input for V_{OUT2}. V_{OUT2} will be enabled when this pin is driven high. There is an internal 5M pull-down resistor on this pin. If not used, this pin can be left open or grounded.

C1 (Pin 10/Pin 13): Input to the Charge Pump and Rectifier Circuit. Connect a capacitor from this pin to the secondary winding of the step-up transformer.

C2 (Pin 11/Pin 14): Input to the N-Channel Gate Drive Circuit. Connect a capacitor from this pin to the secondary winding of the step-up transformer.

SW (Pin 12/Pin 15): Drain of the Internal N-Channel Switch. Connect this pin to the primary winding of the transformer.

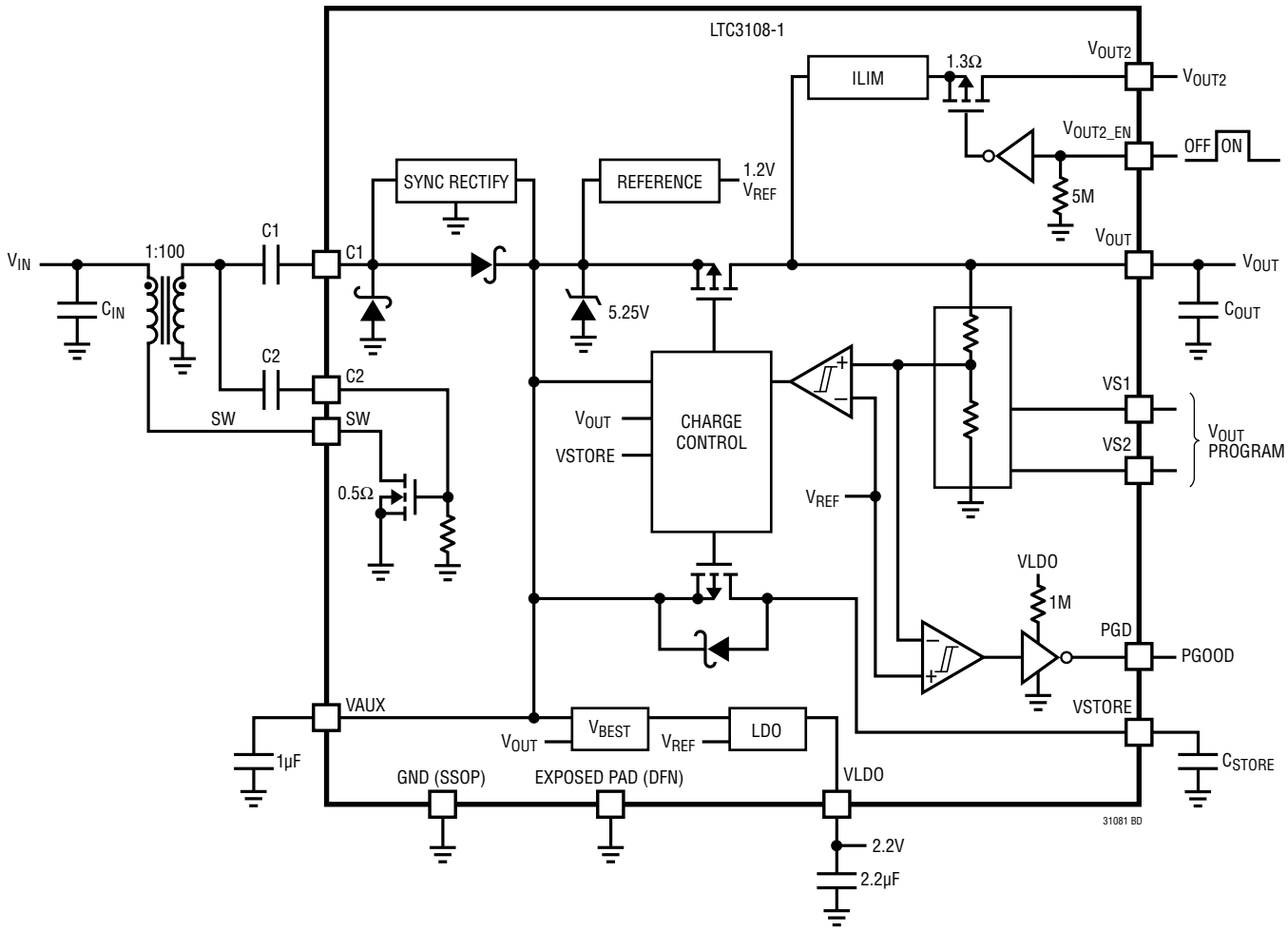
GND (Pins 1, 8, 9, 16) SSOP Only: Ground

GND (Exposed Pad Pin 13) DFN Only: Ground. The DFN exposed pad must be soldered to the PCB ground plane. It serves as the ground connection, and as a means of conducting heat away from the die.

Table 1. Regulated Voltage Using Pins VS1 and VS2

VS2	VS1	V_{OUT}
GND	GND	2.5V
GND	VAUX	3V
VAUX	GND	3.7V
VAUX	VAUX	4.5V

BLOCK DIAGRAM



OPERATION (Refer to the Block Diagram)

The LTC3108-1 is designed to use a small external step-up transformer to create an ultralow input voltage step-up DC/DC converter and power manager. It is ideally suited for low power wireless sensors and other applications in which surplus energy harvesting is used to generate system power because traditional battery power is inconvenient or impractical.

The LTC3108-1 is designed to manage the charging and regulation of multiple outputs in a system in which the average power draw is very low, but there may be periodic pulses of higher load current required. This is typical of wireless sensor applications, where the quiescent power draw is extremely low most of the time, except for transmit bursts when circuitry is powered up to make measurements and transmit data.

The LTC3108-1 can also be used to trickle charge a standard capacitor, supercapacitor or rechargeable battery, using energy harvested from a Peltier or photovoltaic cell.

OPERATION

Oscillator

The LTC3108-1 utilizes a MOSFET switch to form a resonant step-up oscillator using an external step-up transformer and a small coupling capacitor. This allows it to boost input voltages as low as 20mV high enough to provide multiple regulated output voltages for powering other circuits. The frequency of oscillation is determined by the inductance of the transformer secondary winding and is typically in the range of 10kHz to 100kHz. For input voltages as low as 20mV, a primary-secondary turns ratio of about 1:100 is recommended. For higher input voltages, this ratio can be lower. See the Applications Information section for more information on selecting the transformer.

Charge Pump and Rectifier

The AC voltage produced on the secondary winding of the transformer is boosted and rectified using an external charge pump capacitor (from the secondary winding to pin C1) and the rectifiers internal to the LTC3108-1. The rectifier circuit feeds current into the VAUX pin, providing charge to the external VAUX capacitor and the other outputs.

VAUX

The active circuits within the LTC3108-1 are powered from VAUX, which should be bypassed with a 1µF capacitor. Larger capacitor values are recommended when using turns ratios of 1:50 or 1:20 (refer to the Typical Application examples). Once VAUX exceeds 2.5V, the main V_{OUT} is allowed to start charging.

An internal shunt regulator limits the maximum voltage on VAUX to 5.25V typical. It shunts to GND any excess current into VAUX when there is no load on the converter or the input source is generating more power than is required by the load.

Voltage Reference

The LTC3108-1 includes a precision, micropower reference, for accurate regulated output voltages. This reference becomes active as soon as VAUX exceeds 2V.

Synchronous Rectifiers

Once VAUX exceeds 2V, synchronous rectifiers in parallel with each of the internal diodes take over the job of rectifying the input voltage, improving efficiency.

Low Dropout Linear Regulator (LDO)

The LTC3108-1 includes a low current LDO to provide a regulated 2.2V output for powering low power processors or other low power ICs. The LDO is powered by the higher of VAUX or V_{OUT}. This enables it to become active as soon as VAUX has charged to 2.3V, while the V_{OUT} storage capacitor is still charging. In the event of a step load on the LDO output, current can come from the main V_{OUT} capacitor if VAUX drops below V_{OUT}. The LDO requires a 2.2µF ceramic capacitor for stability. Larger capacitor values can be used without limitation, but will increase the time it takes for all the outputs to charge up. The LDO output is current limited to 4mA minimum.

V_{OUT}

The main output voltage on V_{OUT} is charged from the VAUX supply, and is user programmed to one of four regulated voltages using the voltage select pins VS1 and VS2, according to Table 2. Although the logic threshold voltage for VS1 and VS2 is 0.85V typical, it is recommended that they be tied to ground or VAUX.

Table 2. Regulated Voltage Using Pins VS1 and VS2

VS2	VS1	V_{OUT}
GND	GND	2.5V
GND	VAUX	3V
VAUX	GND	3.7V
VAUX	VAUX	4.5V

When the output voltage drops slightly below the regulated value, the charging current will be enabled as long as VAUX is greater than 2.5V. Once V_{OUT} has reached the proper value, the charging current is turned off.

The internal programmable resistor divider sets V_{OUT}, eliminating the need for very high value external resistors that are susceptible to board leakage.

OPERATION

In a typical application, a storage capacitor (typically a few hundred microfarads) is connected to V_{OUT}. As soon as VAUX exceeds 2.5V, the V_{OUT} capacitor will be allowed to charge up to its regulated voltage. The current available to charge the capacitor will depend on the input voltage and transformer turns ratio, but is limited to about 4.5mA typical.

PGOOD

A power good comparator monitors the V_{OUT} voltage. The PGD pin is an open-drain output with a weak pull-up (1MΩ) to the LDO voltage. Once V_{OUT} has charged to within 7.5% of its regulated voltage, the PGD output will go high. If V_{OUT} drops more than 9% from its regulated voltage, PGD will go low. The PGD output is designed to drive a microprocessor or other chip I/O and is not intended to drive a higher current load such as an LED. Pulling PGD up externally to a voltage greater than VLDO will cause a small current to be sourced into VLDO. PGD can be pulled low in a wire-OR configuration with other circuitry.

V_{OUT2}

V_{OUT2} is an output that can be turned on and off by the host, using the V_{OUT2_EN} pin. When enabled, V_{OUT2} is connected to V_{OUT} through a 1.3Ω P-channel MOSFET switch. This output, controlled by a host processor, can be used to power external circuits such as sensors and amplifiers, that do not have a low power sleep or shutdown capability. V_{OUT2} can be used to power these circuits only when they are needed.

Minimizing the amount of decoupling capacitance on V_{OUT2} will allow it to be switched on and off faster, allowing shorter burst times and, therefore, smaller duty cycles in pulsed applications such as a wireless sensor/transmitter. A small V_{OUT2} capacitor will also minimize the energy that will be wasted in charging the capacitor every time V_{OUT2} is enabled.

V_{OUT2} has a soft-start time of about 5µs to limit capacitor charging current and minimize glitching of the main output when V_{OUT2} is enabled. It also has a current limiting circuit that limits the peak current to 0.3A typical.

The V_{OUT2} enable input has a typical threshold of 1V with 100mV of hysteresis, making it logic-compatible. If V_{OUT2_EN} (which has an internal pull-down resistor) is low, V_{OUT2} will be off. Driving V_{OUT2_EN} high will turn on the V_{OUT2} output.

Note that while V_{OUT2_EN} is high, the current limiting circuitry for V_{OUT2} draws an extra 8µA of quiescent current from V_{OUT}. This added current draw has a negligible effect on the application and capacitor sizing, since the load on the V_{OUT2} output, when enabled, is likely to be orders of magnitude higher than 8µA.

VSTORE

The VSTORE output can be used to charge a large storage capacitor or rechargeable battery after V_{OUT} has reached regulation. Once V_{OUT} has reached regulation, the VSTORE output will be allowed to charge up to the VAUX voltage. The storage element on VSTORE can be used to power the system in the event that the input source is lost, or is unable to provide the current demanded by the V_{OUT}, V_{OUT2} and LDO outputs. If VAUX drops below VSTORE, the LTC3108-1 will automatically draw current from the storage element. Note that it may take a long time to charge a large capacitor, depending on the input energy available and the loading on V_{OUT} and VLDO.

Since the maximum current from VSTORE is limited to a few milliamps, it can safely be used to trickle-charge NiCd or NiMH rechargeable batteries for energy storage when the input voltage is lost. Note that the VSTORE capacitor cannot supply large pulse currents to V_{OUT}. Any pulse load on V_{OUT} must be handled by the V_{OUT} capacitor.

Short-Circuit Protection

All outputs of the LTC3108-1 are current limited to protect against short-circuits to ground.

Output Voltage Sequencing

A timing diagram showing the typical charging and voltage sequencing of the outputs is shown in Figure 1. Note: time not to scale.

OPERATION

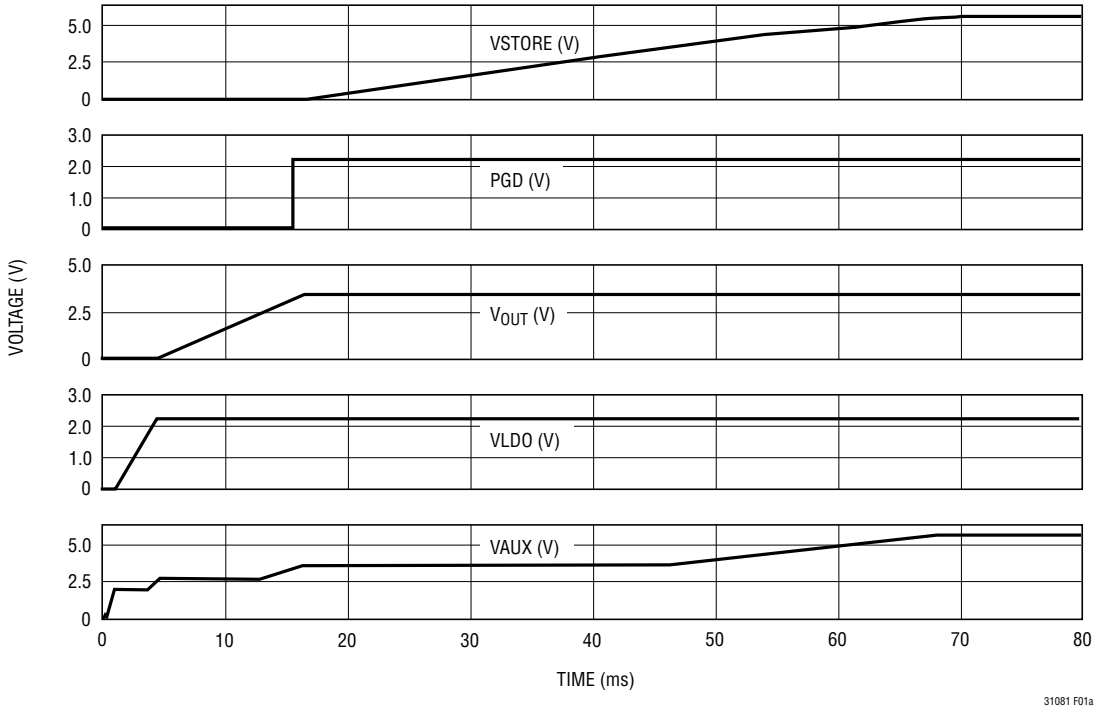


Figure 1. Output Voltage Sequencing with V_{OUT} Programmed for 3V (Time Not to Scale)

APPLICATIONS INFORMATION

Introduction

The LTC3108-1 is designed to gather energy from very low input voltage sources and convert it to usable output voltages to power microprocessors, wireless transmitters and analog sensors. Such applications typically require much more peak power, and at higher voltages, than the input voltage source can produce. The LTC3108-1 is designed to accumulate and manage energy over a long period of time to enable short power bursts for acquiring and transmitting data. The bursts must occur at a low enough duty cycle such that the total output energy during the burst does not exceed the average source power integrated over the accumulation time between bursts. For many applications, this time between bursts could be seconds, minutes or hours.

The PGD signal can be used to enable a sleeping microprocessor or other circuitry when V_{OUT} reaches regulation, indicating that enough energy is available for a burst.

Input Voltage Sources

The LTC3108-1 can operate from a number of low input voltage sources, such as Peltier cells, photovoltaic cells or thermopile generators. The minimum input voltage required for a given application will depend on the transformer turns ratio, the load power required, and the internal DC resistance (ESR) of the voltage source. Lower ESR will allow the use of lower input voltages, and provide higher output power capability.

Refer to the I_{IN} vs V_{IN} curves in the Typical Performance Characteristics section to see what input current is required for the source for a given input voltage.

For a given transformer turns ratio, there is a maximum recommended input voltage to avoid excessively high secondary voltages and power dissipation in the shunt regulator. It is recommended that the maximum input voltage times the turns ratio be less than 50.

Note that a low ESR bulk decoupling capacitor will usually be required across the input source to prevent large voltage droop and ripple caused by the source's ESR and the peak primary switching current (which can reach hundreds of milliamps). The time constant of the filter capacitor and the ESR of the voltage source should be much longer than the period of the resonant switching frequency.

Peltier Cell (Thermoelectric Generator)

A Peltier cell (also known as a thermoelectric cooler) is made up of a large number of series-connected P-N junctions, sandwiched between two parallel ceramic plates. Although Peltier cells are often used as coolers by applying a DC voltage to their inputs, they will also generate a DC output voltage, using the Seebeck effect, when the two plates are at different temperatures. The polarity of the output voltage will depend on the polarity of the temperature differential between the plates. The magnitude of the output voltage is proportional to the magnitude of the temperature differential between the plates. When used in

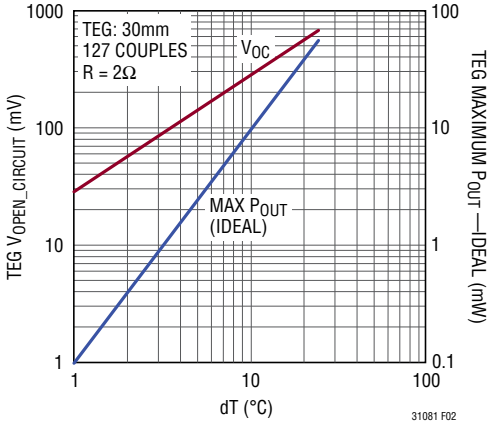


Figure 2. Typical Performance of a Peltier Cell Acting as a Thermoelectric Generator

APPLICATIONS INFORMATION

this manner, a Peltier cell is referred to as a thermoelectric generator (TEG).

The low voltage capability of the LTC3108-1 design allows it to operate from a TEG with temperature differentials as low as 1°C, making it ideal for harvesting energy in applications in which a temperature difference exists between two surfaces or between a surface and the ambient temperature. The internal resistance (ESR) of most cells is in the range of 1Ω to 5Ω, allowing for reasonable power transfer. The curves in Figure 2 show the open-circuit output voltage and maximum power transfer for a typical Peltier cell (with an ESR of 2Ω) over a 20°C range of temperature differential.

TEG Load Matching

The LTC3108-1 was designed to present a minimum input resistance (load) in the range of 2Ω to 10Ω, depending on input voltage and transformer turns ratio (as shown in the Typical Performance Characteristics curves). For a given turns ratio, as the input voltage drops, the input resistance increases. This feature allows the LTC3108-1 to optimize power transfer from sources with a few ohms of source resistance, such as a typical TEG. Note that a lower source resistance will always provide more output current capability by providing a higher input voltage under load.

Peltier Cell (TEG) Suppliers

Peltier cells are available in a wide range of sizes and power capabilities, from less than 10mm square to over 50mm square. They are typically 2mm to 5mm in height. A list of Peltier cell manufacturers is given in Table 3.

Table 3. Peltier Cell Manufacturers

Fujitaka www.fujitaka.com/pub/peltier/english/thermoelectric_power.html
FerroTec www.ferrotec.com/products/thermal/modules
Laird Technologies www.lairdtech.com
Marlow Industries www.marlow.com
Micropelt www.micropelt.com
Nextreme www.nextreme.com
TE Technology www.tetech.com/Peltier-Thermoelectric-Cooler-Modules.html
Tellurex www.tellurex.com
Kryotherm www.kryothermusa.com

Table 4. Recommended TEG Part Numbers by Size

MANUFACTURER	15mm × 15mm	20mm × 20mm	30mm × 30mm	40mm × 40mm
CUI Inc. (Distributor)	CP60133	CP60233	CP60333	CP85438
Ferrotec	9501/031/030 B	9501/071/040 B	9500/097/090 B	9500/127/100 B
Fujitaka	FPH13106NC	FPH17106NC	FPH17108AC	FPH112708AC
Kryotherm			TGM-127-1.0-0.8	LCB-127-1.4-1.15
Laird Technology			PT6.7.F2.3030.W6	PT8.12.F2.4040.TA.W6
Marlow Industries		RC3-8-01	RC6-6-01	RC12-8-01LS
Tellurex	C2-15-0405	C2-20-0409	C2-30-1505	C2-40-1509
TE Technology	TE-31-1.0-1.3	TE-31-1.4-1.15	TE-71-1.4-1.15	TE-127-1.4-1.05

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Thermopile Generator

Thermopile generators (also called powerpile generators) are made up of a number of series-connected thermocouples enclosed in a metal tube. They are commonly used in gas burner applications to generate a DC output of hundreds of millivolts when exposed to the high temperature of a flame. Typical examples are the Honeywell CQ200 and Q313. These devices have an internal series resistance of less than 3Ω, and can generate as much as 750mV open-circuit at their highest rated temperature. For applications in which the temperature rise is too high for a solid-state thermoelectric device, a thermopile can be used as an energy source to power the LTC3108-1. Because of the higher output voltages possible with a thermopile generator, a lower transformer turns ratio can be used (typically 1:20, depending on the application).

Photovoltaic Cell

The LTC3108-1 converter can also operate from a single photovoltaic cell (also known as a PV or solar cell) at light levels too low for other low input voltage boost converters to operate. However, many variables will affect the performance in these applications. Light levels can vary over several orders of magnitude and depend on lighting conditions (the type of lighting and indoor versus outdoor). Different types of light (sunlight, incandescent, fluorescent) also have different color spectra, and will produce different output power levels depending on which type of photovoltaic cell is being used (monocrystalline, polycrystalline or thin-film). Therefore, the photovoltaic cell must be chosen for the type and amount of light available. Note that the short-circuit output current from the cell must be at least a few milliamps in order to power the LTC3108-1 converter

Non-Boost Applications

The LTC3108-1 can also be used as an energy harvester and power manager for input sources that do not require boosting. In these applications the step-up transformer can be eliminated.

Any source whose peak voltage exceeds 2.5V AC or 5V DC can be connected to the C1 input through a current-limiting resistor where it will be rectified/peak detected. In these applications the C2 and SW pins are not used and can be grounded or left open.

Examples of such input sources would be piezoelectric transducers, vibration energy harvesters, low current generators, a stack of low current solar cells or a 60Hz AC input.

A series resistance of at least 100Ω/V should be used to limit the maximum current into the VAUX shunt regulator.

COMPONENT SELECTION

Step-Up Transformer

The step-up transformer turns ratio will determine how low the input voltage can be for the converter to start. Using a 1:100 ratio can yield start-up voltages as low as 20mV. Other factors that affect performance are the DC resistance of the transformer windings and the inductance of the windings. Higher DC resistance will result in lower efficiency. The secondary winding inductance will determine the resonant frequency of the oscillator, according to the following formula.

$$\text{Frequency} = \frac{1}{2 \bullet \pi \bullet \sqrt{L(\text{sec}) \bullet C}} \text{ Hz}$$

Where L is the inductance of the transformer secondary winding and C is the load capacitance on the secondary winding. This is comprised of the input capacitance at pin C2, typically 30pF, in parallel with the transformer secondary winding's shunt capacitance. The recommended resonant frequency is in the range of 10kHz to 100kHz. See Table 5 for some recommended transformers.

Table 5. Recommended Transformers

VENDOR	PART NUMBER
Coilcraft www.coilcraft.com	LPR6235-752SML (1:100 Ratio) LPR6235-253PML (1:20 Ratio) LPR6235-123QML (1:50 Ratio)
Würth www.we-online	74488540070 (1:100 Ratio) 74488540120 (1:50 Ratio) 74488540250 (1:20 Ratio)

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C1 Capacitor

The charge pump capacitor that is connected from the transformer's secondary winding to the C1 pin has an effect on converter input resistance and maximum output current capability. Generally, a minimum value of 1nF is recommended when operating from very low input voltages using a transformer with a ratio of 1:100. Too large a capacitor value can compromise performance when operating at low input voltage or with high resistance sources. For higher input voltages and lower turns ratios, the value of the C1 capacitor can be increased for higher output current capability. Refer to the Typical Applications schematic examples for the recommended value for a given turns ratio.

Squegging

Certain types of oscillators, including transformer-coupled oscillators such as the resonant oscillator of the LTC3108-1, can exhibit a phenomenon called squegging. This term refers to a condition that can occur which blocks or stops the oscillation for a period of time much longer than the period of oscillation, resulting in bursts of oscillation. An example of this is the blocking oscillator, which is designed to squegg to produce bursts of oscillation. Squegging is also encountered in RF oscillators and regenerative receivers.

In the case of the LTC3108-1, squegging can occur when a charge builds up on the C2 gate coupling capacitor, such that the DC bias point shifts and oscillation is extinguished for a certain period of time, until the charge on the capacitor bleeds off, allowing oscillation to resume. It is difficult to predict when and if squegging will occur in a given application. While squegging is not harmful, it reduces the average output current capability of the LTC3108-1.

Squegging can easily be avoided by the addition of a bleeder resistor in parallel with the coupling capacitor on the C2 pin. Resistor values in the range of 100k to 1MΩ are sufficient to eliminate squegging without having any negative impact on performance. For the 330pF capacitor used for C2 in most applications, a 499k bleeder resistor is recommended. See the Typical Applications schematics for an example.

Using External Charge Pump Rectifiers

The synchronous charge pump rectifiers in the LTC3108-1 (connected to the C1 pin) are optimized for operation from very low input voltage sources, using typical transformer step-up ratios between 1:100 and 1:50, and typical C1 charge pump capacitor values less than 10nF.

Operation from higher input voltage sources (typically 250mV or greater, under load), allows the use of lower transformer step-up ratios (such as 1:20 and 1:10) and larger C1 capacitor values to provide higher output current capability from the LTC3108. However, due to the resulting increase in rectifier currents and resonant oscillator frequency in these applications, the use of external charge pump rectifiers is recommended for optimal performance.

In applications where the step-up ratio is 1:20 or less, and the C1 capacitor is 10nF or greater, the C1 pin should be grounded and two external rectifiers (such as 1N4148 or 1N914 diodes) should be used. These are available as dual diodes in a single package. Avoid the use of Schottky rectifiers, as their lower forward-voltage drop increases the minimum startup voltage. See the Typical Applications schematics for an example.

V_{OUT} and VSTORE Capacitor

For pulsed load applications, the V_{OUT} capacitor should be sized to provide the necessary current when the load is pulsed on. The capacitor value required will be dictated by the load current, the duration of the load pulse, and the amount of voltage droop the circuit can tolerate. The capacitor must be rated for whatever voltage has been selected for V_{OUT} by VS1 and VS2.

$$C_{OUT}(\mu F) \geq \frac{I_{LOAD}(mA) \bullet t_{PULSE}(ms)}{\Delta V_{OUT}\ (V)}$$

Note that there must be enough energy available from the input voltage source for V_{OUT} to recharge the capacitor during the interval between load pulses (to be discussed in the next example). Reducing the duty cycle of the load pulse will allow operation with less input energy.

The VSTORE capacitor may be of very large value (thousands of microfarads or even Farads), to provide holdup

APPLICATIONS INFORMATION

at times when the input power may be lost. Note that this capacitor can charge all the way to 5.25V (regardless of the settings for V_{OUT}), so ensure that the holdup capacitor has a working voltage rating of at least 5.5V at the temperature for which it will be used. The VSTORE capacitor can be sized using the following:

$$C_{STORE} \geq \frac{[6\mu A + I_Q + I_{LDO} + (I_{BURST} \bullet t \bullet f)] \bullet TSTORE}{5.25 - V_{OUT}}$$

Where 6µA is the quiescent current of the LTC3108-1, I_Q is the load on V_{OUT} in between bursts, I_{LDO} is the load on the LDO between bursts, I_{BURST} is the total load during the burst, t is the duration of the burst, f is the frequency of the bursts, TSTORE is the storage time required and V_{OUT} is the output voltage required.

To minimize losses and capacitor charge time, all capacitors used for V_{OUT} and VSTORE should be low leakage. See Table 6 for recommended storage capacitors.

Table 6. Recommended Storage Capacitors

VENDOR	PART NUMBER/SERIES
AVX www.avx.com	BestCap Series TAJ and TPS Series Tantalum
Cap-XX www.cap-xx.com	GZ Series
Cooper/Bussmann www.bussmann.com/3/PowerStor.html	KR Series P Series
Vishay/Sprague www.vishay.com/capacitors	Tantamount 592D 595D Tantalum 150CRZ/153CRV Aluminum 013 RLC (Low Leakage)

Storage capacitors requiring voltage balancing are not recommended due to the current draw of the balancing resistors.

PCB Layout Guidelines

Due to the rather low switching frequency of the resonant converter and the low power levels involved, PCB layout is not as critical as with many other DC/DC converters. There are, however, a number of things to consider.

Due to the very low input voltage the circuit may operate from, the connections to V_{IN}, the primary of the transformer and the SW and GND pins of the LTC3108-1 should be designed to minimize voltage drop from stray resistance and able to carry currents as high as 500mA. Any small voltage drop in the primary winding conduction path will lower efficiency and increase capacitor charge time.

Also, due to the low charge currents available at the outputs of the LTC3108-1, any sources of leakage current on the output voltage pins must be minimized. An example board layout is shown in Figure 3.

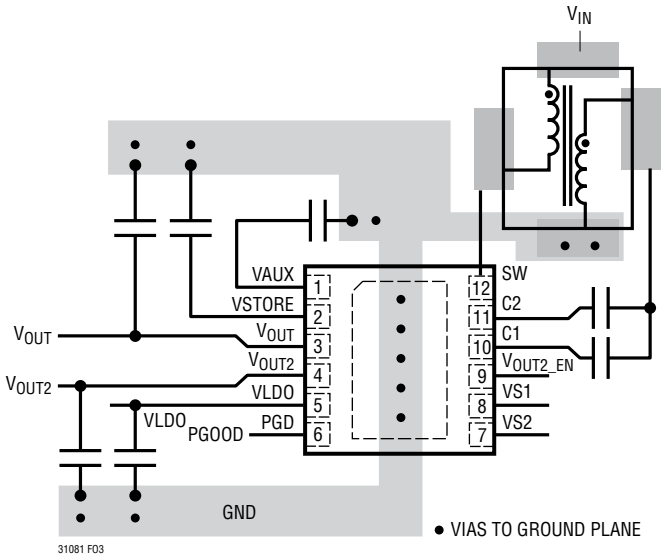


Figure 3. Example Component Placement for Two-Layer PC Board (DFN Package)

APPLICATIONS INFORMATION

Design Example 1

This design example will explain how to calculate the necessary storage capacitor value for V_{OUT} in pulsed load applications, such as a wireless sensor/transmitter. In these types of applications, the load is very small for a majority of the time (while the circuitry is in a low power sleep state), with bursts of load current occurring periodically during a transmit burst. The storage capacitor on V_{OUT} supports the load during the transmit burst, and the long sleep time between bursts allows the LTC3108-1 to recharge the capacitor. A method for calculating the maximum rate at which the load pulses can occur for a given output current from the LTC3108-1 will also be shown.

In this example, V_{OUT} is set to 3V, and the maximum allowed voltage droop during a transmit burst is 10%, or 0.3V. The duration of a transmit burst is 1ms, with a total average current requirement of 40mA during the burst. Given these factors, the minimum required capacitance on V_{OUT} is:

$$C_{OUT}(\mu F) \geq \frac{40mA \bullet 1ms}{0.3V} = 133\mu F$$

Note that this equation neglects the effect of capacitor ESR on output voltage droop. For most ceramic or low ESR tantalum capacitors, the ESR will have a negligible effect at these load currents.

A standard value of 150µF or larger could be used for C_{OUT} in this case. Note that the load current is the total current draw on V_{OUT}, V_{OUT2} and VLDO, since the current for all of these outputs must come from V_{OUT} during a burst. Current contribution from the holdup capacitor on VSTORE is not considered, since it may not be able to recharge between bursts. Also, it is assumed that the charge current from the LTC3108-1 is negligible compared to the magnitude of the load current during the burst.

To calculate the maximum rate at which load bursts can occur, determine how much charge current is available from the LTC3108-1 V_{OUT} pin given the input voltage source being used. This number is best found empirically, since there are many factors affecting the efficiency of the converter. Also determine what the total load current is on V_{OUT} during the sleep state (between bursts). Note that this must include any losses, such as storage capacitor leakage.

Assume, for instance, that the charge current from the LTC3108-1 is 50µA and the total current drawn on V_{OUT} in the sleep state is 17µA, including capacitor leakage. In addition, use the value of 150µF for the V_{OUT} capacitor. The maximum transmit rate (neglecting the duration of the transmit burst, which is typically very short) is then given by:

$$t = \frac{150\mu F \bullet 0.3V}{(50\mu A - 17\mu A)} = 1.36sec \text{ or } f_{MAX} = 0.73Hz$$

Therefore, in this application example, the circuit can support a 1ms transmit burst every 1.3 seconds.

It can be determined that for systems that only need to transmit every few seconds (or minutes or hours), the average charge current required is extremely small, as long as the sleep current is low. Even if the available charge current in the example above was only 10µA and the sleep current was only 5µA, it could still transmit a burst every 9 seconds.

The following formula enables the user to calculate the time it will take to charge the LDO output capacitor and the V_{OUT} capacitor the first time, from 0V. Here again, the charge current available from the LTC3108-1 must be known. For this calculation, it is assumed that the LDO output capacitor is 2.2µF.

$$t_{LDO} = \frac{2.2V \bullet 2.2\mu F}{I_{CHG} - I_{LDO}}$$

If there were 50µA of charge current available and a 5µA load on the LDO (when the processor is sleeping), the time for the LDO to reach regulation would be 107ms.

If V_{OUT} were programmed to 3V and the V_{OUT} capacitor was 150µF, the time for V_{OUT} to reach regulation would be:

$$t_{VOUT} = \frac{3V \bullet 150\mu F}{I_{CHG} - I_{VOUT} - I_{LDO}} + t_{LDO}$$

APPLICATIONS INFORMATION

If there were 50µA of charge current available and 5µA of load on V_{OUT}, the time for V_{OUT} to reach regulation after the initial application of power would be 11.35 seconds.

Design Example 2

In many pulsed load applications, the duration, magnitude and frequency of the load current bursts are known and fixed. In these cases, the average charge current required from the LTC3108-1 to support the average load must be calculated, which can be easily done by the following:

$$I_{CHG} \geq I_Q + \frac{I_{BURST} \bullet t}{T}$$

Where I_Q is the sleep current on V_{OUT} required by the external circuitry in between bursts (including cap leakage), I_{BURST} is the total load current during the burst, t is the duration of the burst and T is the period of the transmit burst rate (essentially the time between bursts).

In this example, I_Q = 5µA, I_{BURST} = 100mA, t = 5ms and T = one hour. The average charge current required from the LTC3108-1 would be:

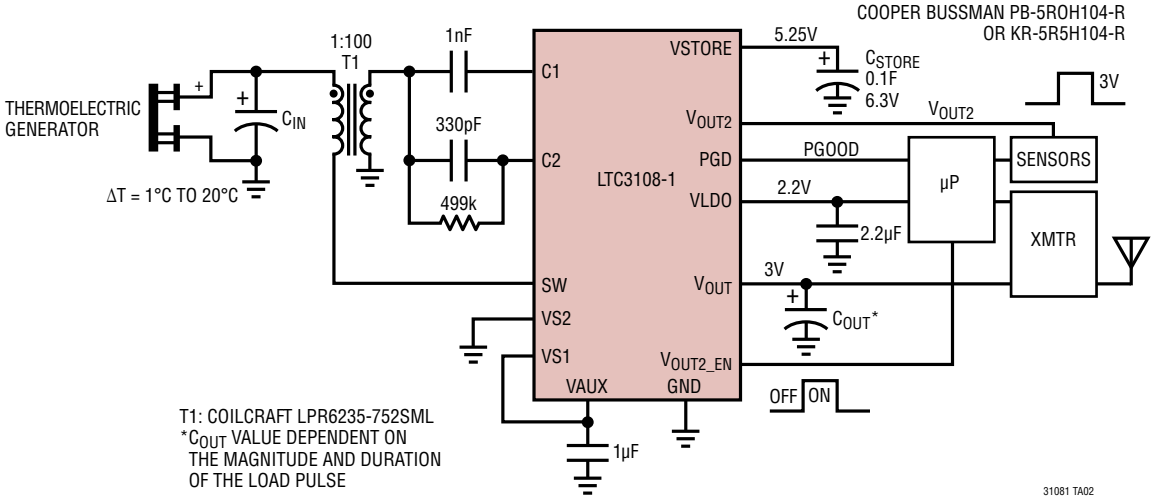
$$I_{CHG} \geq 5\mu A + \frac{100mA \bullet 0.005sec}{3600sec} = 5.14\mu A$$

Therefore, if the LTC3108-1 has an input voltage that allows it to supply a charge current greater than 5.14µA, the application can support 100mA bursts lasting 5ms every hour. It can be determined that the sleep current of 5µA is the dominant factor because the transmit duty cycle is so small (0.00014%). Note that for a V_{OUT} of 3V, the average power required by this application is only 15.4µW (not including converter losses).

Note that the charge current available from the LTC3108-1 has no effect on the sizing of the V_{OUT} capacitor (if it is assumed that the load current during a burst is much larger than the charge current), and the V_{OUT} capacitor has no effect on the maximum allowed burst rate.

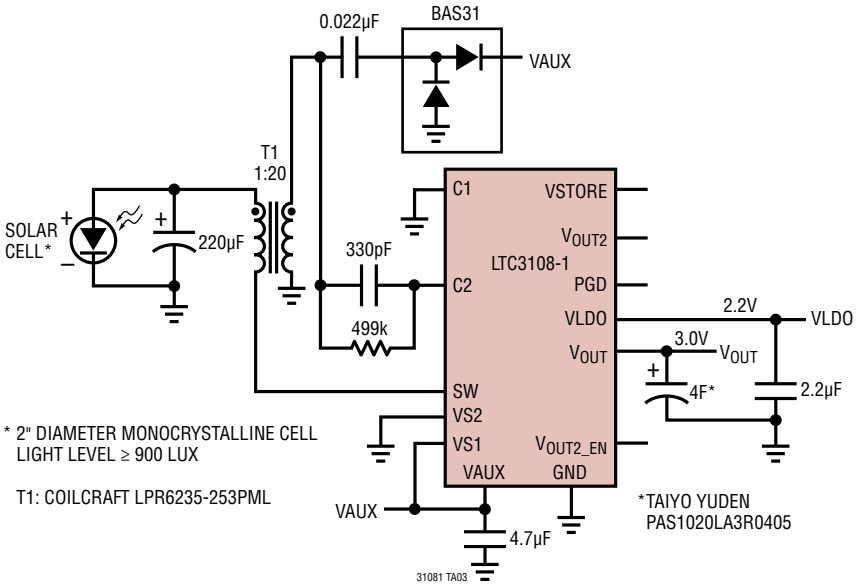
TYPICAL APPLICATIONS

Peltier-Powered Energy Harvester for Remote Sensor Applications

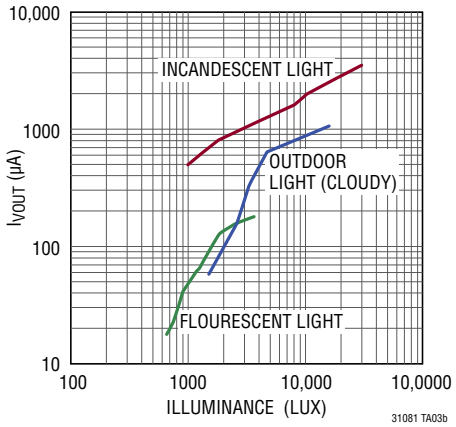


TYPICAL APPLICATIONS

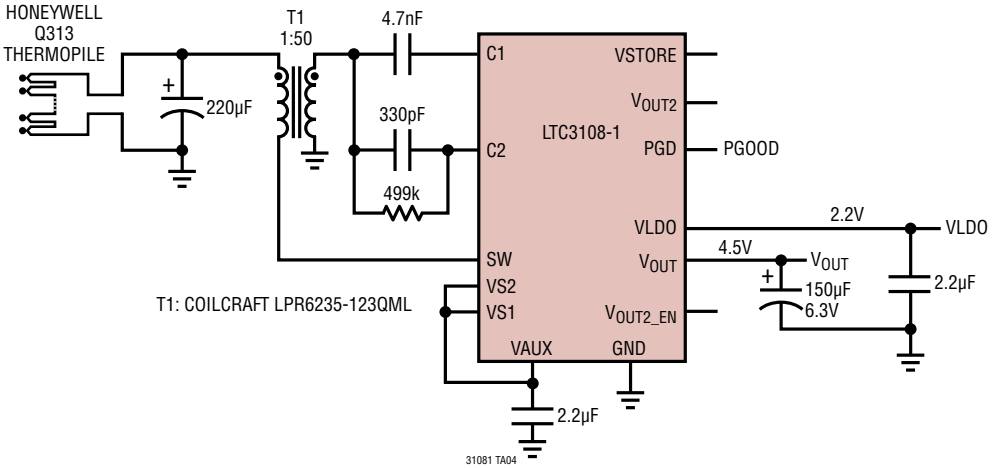
Supercapacitor Charger and LDO Powered by a Solar Cell (Uses External Charge Pump Rectifiers)



I_{VOUT} vs Illuminance (2" Diameter Monocrystalline Cell)

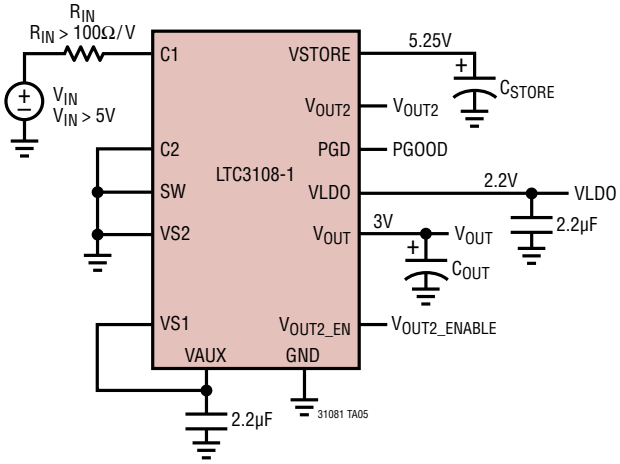


Dual Output Converter and LDO Powered by a Thermopile Generator

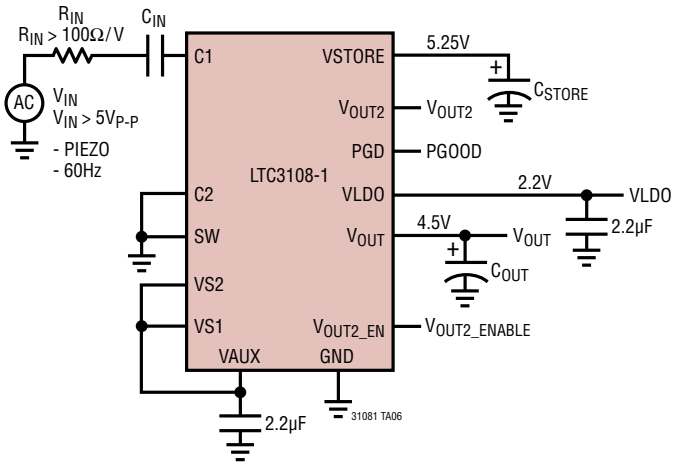


TYPICAL APPLICATIONS

DC Input Energy Harvester and Power Manager

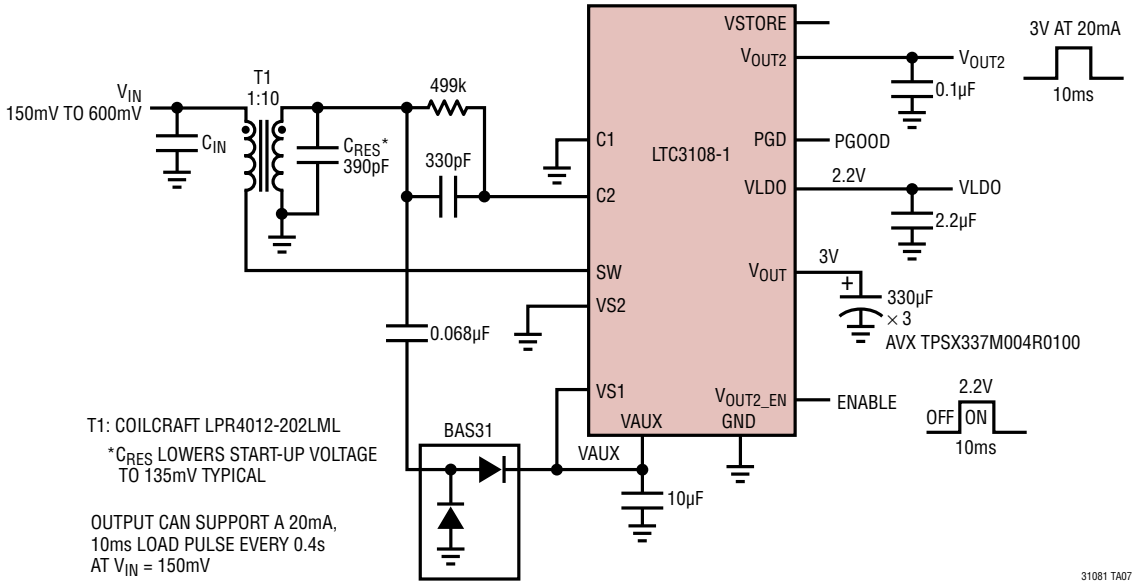


AC Input Energy Harvester and Power Manager

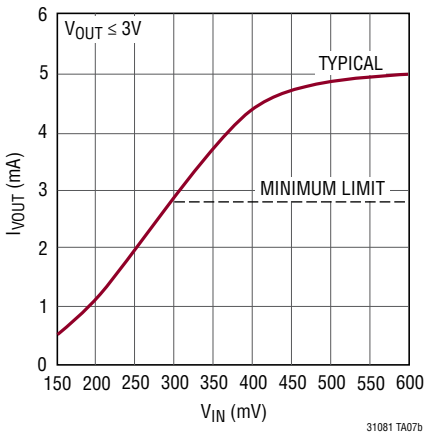


TYPICAL APPLICATIONS

Low Profile (1.5mm) Step-Up Converter/Harvester Using 1:10 Transformer



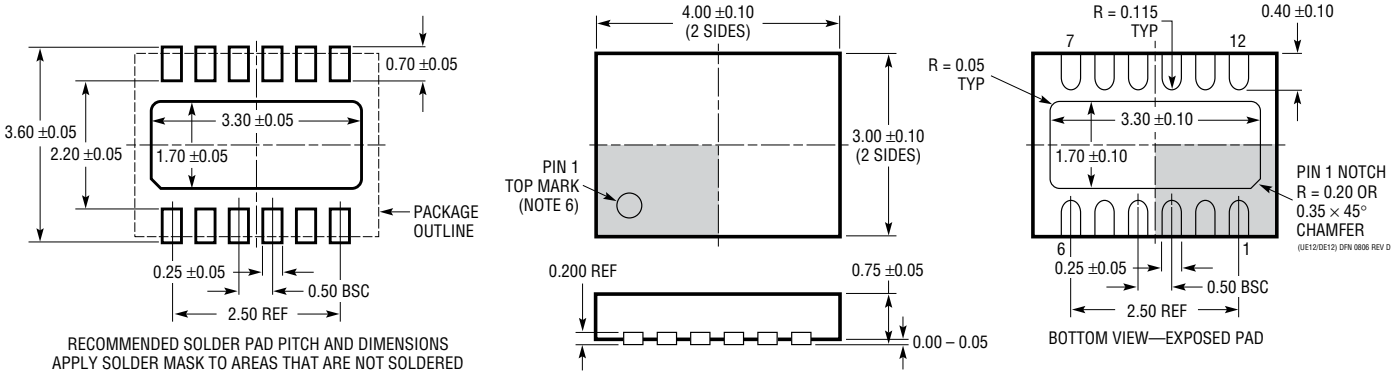
I_{VOUT} vs V_{IN} (Steady State)



PACKAGE DESCRIPTION

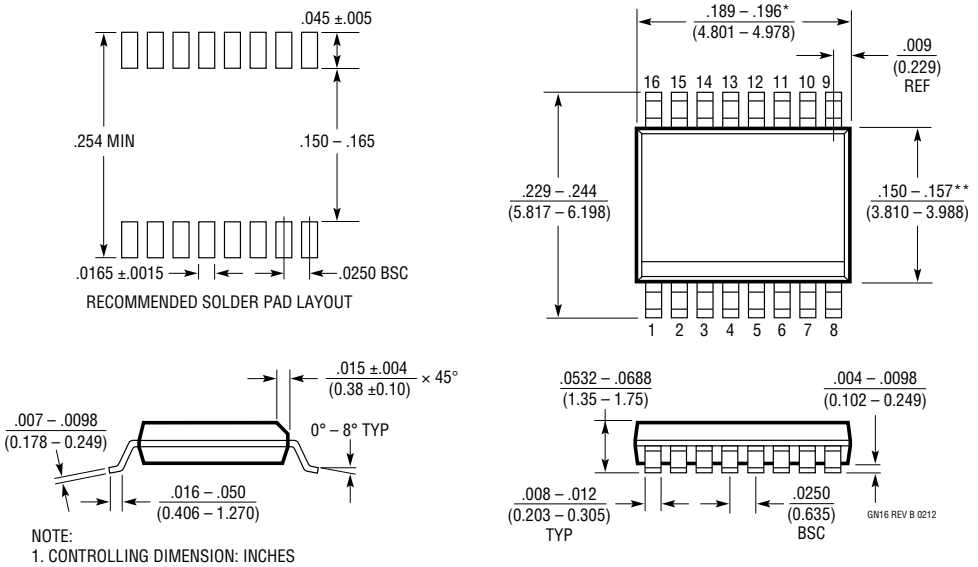
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/12	Added vendor information to Table 5	14
B	08/13	Changed Würth transformer part numbers	14