15V, 1.5A Synchronous Buck-Boost DC/DC Converter

FEATURES

- **Regulated Output with V_{IN} Above, Below or Equal to V_{OUT}**
- **2.5V to 15V Input and Output Voltage Range**
- **1.5A Continuous Output Current: $V_{IN} \geq 5V$, $V_{OUT} = 5V$, PWM Mode**
- **Single Inductor**
- **Accurate RUN Threshold**
- Up to 95% Efficiency
- 800kHz Switching Frequency, Synchronizable Between 600kHz and 1.5MHz
- 49µA No-Load Quiescent Current in Burst Mode® Operation
- Output Disconnect in Shutdown
- Shutdown Current < 1µA
- Internal Soft-Start
- Small, Thermally Enhanced 14-Lead (3mm × 4mm × 0.75mm) DFN and 16-Lead MSOP Packages

APPLICATIONS

- 3.3V or 5V from 1, 2 or 3 Li-Ion, Multiple-Cell Alkaline/NiMH Batteries
- RF Transmitters
- Military, Industrial Power Systems

DESCRIPTION

The LTC®3111 is a fixed frequency, synchronous buck-boost DC/DC converter with an extended input and output range. The unique 4-switch, single inductor architecture provides low noise and seamless operation from input voltages above, below or equal to the output voltage.

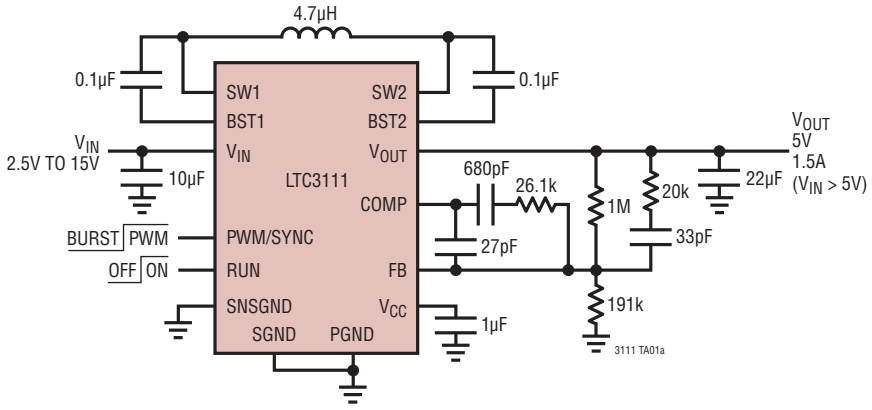
With an input and output range of 2.5V to 15V, the LTC3111 is well suited for a wide variety of single or multiple-cell batteries, back-up capacitor or wall adapter source applications. Low $R_{DS(ON)}$ internal N-channel MOSFET switches and selectable PWM or Burst Mode operation produce high efficiency over a wide range of operating conditions.

An accurate RUN pin allows the user to program the turn-on threshold voltage of the converter. Other features include: short-circuit protection, internal soft-start and thermal shutdown.

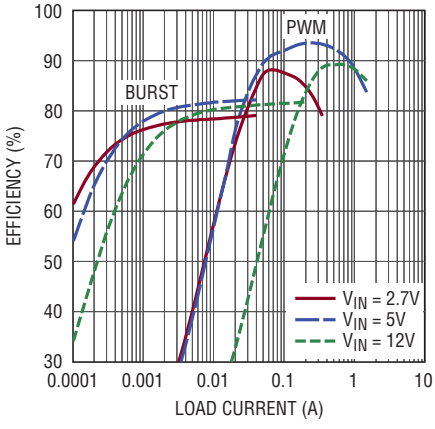
The LTC3111 is offered in both thermally enhanced 14-lead (3mm × 4mm × 0.75mm) DFN and 16-lead MSOP packages.

TYPICAL APPLICATION

5V, 800kHz Wide Input Voltage Buck-Boost Regulator



Efficiency at $5V_{OUT}$

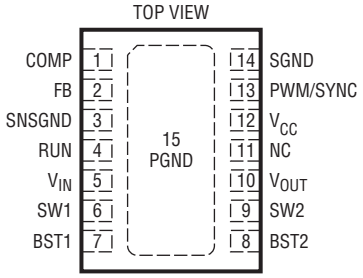


ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

V_{IN} Voltage ..... –0.3V to 16V
V_{OUT} Voltage ..... –0.3V to 16V
SW1 Voltage (Note 4) ..... –0.3V to (V_{IN} + 0.3V)
SW2 Voltage (Note 4) ..... –0.3V to (V_{OUT} + 0.3V)
BST1 Voltage ..... (V_{SW1} – 0.3V) to (V_{SW1} + 6V)
BST2 Voltage ..... (V_{SW2} – 0.3V) to (V_{SW2} + 6V)
RUN Voltage ..... –0.3V to 16V
PWM/SYNC, V_{CC} Voltage ..... –0.3V to 6V
FB, COMP, Voltage ..... –0.3V to 6V

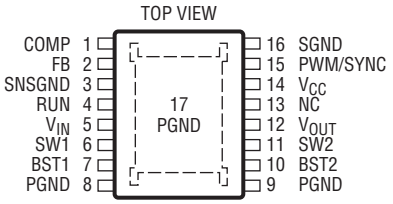
Operating Junction Temperature Range (Notes 2, 5)
LTC3111E, LTC3111I ..... –40°C to 125°C
LTC3111H ..... –40°C to 150°C
LTC3111MP ..... –55°C to 150°C
Maximum Junction Temperature (Note 3) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec)
MSOP ..... 300°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 15) IS PGND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3111EDE#PBF	LTC3111EDE#TRPBF	3111	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3111IDE#PBF	LTC3111IDE#TRPBF	3111	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3111HDE#PBF	LTC3111HDE#TRPBF	3111	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3111MPDE#PBF	LTC3111MPDE#TRPBF	3111	14-Lead (4mm × 3mm) Plastic DFN	–55°C to 150°C
LTC3111EMSE#PBF	LTC3111EMSE#TRPBF	3111	16-Lead Plastic MSOP	–40°C to 125°C
LTC3111IMSE#PBF	LTC3111IMSE#TRPBF	3111	16-Lead Plastic MSOP	–40°C to 125°C
LTC3111HMSE#PBF	LTC3111HMSE#TRPBF	3111	16-Lead Plastic MSOP	–40°C to 150°C
LTC3111MPMSE#PBF	LTC3111MPMSE#TRPBF	3111	16-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = PWM/SYNC = RUN = 5V unless otherwise noted.

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Input Operating Range		●	2.5		15	V
V_{IN} UVLO Threshold	Rising	●	1.9	2.1	2.3	V
V_{IN} UVLO Hysteresis				200		mV
V_{CC} UVLO Threshold	Rising	●	2.2	2.35	2.5	V
V_{CC} UVLO Hysteresis				190		mV
Output Voltage Adjust Range		●	2.5		15	V
$INTV_{CC}$ Clamp Voltage	V_{IN} = 5V or 15V	●	3.9	4.2	4.5	V
Quiescent Current—Burst Mode Operation	FB = 1V, PWM/SYNC = 0V			55	80	µA
Quiescent Current—Shutdown	RUN = V_{OUT} = V_{CC} = 0V, Not Including Switch Leakage			0	1	µA
Feedback Voltage	PWM Operation	●	0.78	0.8	0.82	V
Feedback Leakage	FB = 0.8V			0	50	nA
NMOS Switch Leakage	Switches A, B, C, D, V_{IN} = V_{OUT} = 15V			0.5	5	µA
NMOS Switch On-Resistance	Switch A			90		mΩ
	Switch B, C, D			105		mΩ
Input Current Limit		●	2.3	3	3.7	A
Peak Current Limit				5.8		A
Burst Current Limit	PWM/SYNC = 0V			0.8		A
Burst Zero Current Threshold	PWM/SYNC = 0V			0.1		A
Reverse Current Limit				–1		A
Maximum Duty Cycle	Percentage of the Period SW2 is Low in Boost Mode (Note 7)	●	85	90		%
Minimum Duty Cycle	Percentage of the Period SW1 is Low in Buck Mode (Note 7)	●			0	%
SW1, SW2 Minimum Low Time	(Note 7)			160		ns
Frequency	PWM/SYNC = 5V	●	700	800	900	kHz
SYNC Frequency Range	(Note 6)	●	600		1500	kHz
PWM/SYNC Threshold		●	0.5	0.9	1.5	V
RUN Threshold to Enable V_{CC}	Rising	●	0.35	0.8	1.15	V
RUN Threshold to Disable V_{CC}	Falling	●	0.3			V
RUN Threshold to Enable Switching	Rising	●	1.15	1.18	1.23	V
RUN Hysteresis				120		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetimes.

Note 2: The LTC3111 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3111E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3111I is guaranteed to meet performance specifications from –40°C to 125°C junction temperature, the LTC3111H is guaranteed to meet performance specifications from –40°C to 150°C junction temperature and the LTC3111MP is guaranteed and tested to meet performance specifications from –55°C to 150°C junction temperature. High junction temperatures degrade operating lifetimes: operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

ELECTRICAL CHARACTERISTICS

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Voltage transients on the switch pins beyond the DC limit specified in the Absolute Maximum Ratings, are non-disruptive to normal operation when using good layout practices, as shown on the demo board or described in the data sheet and application notes.

Note 5: The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

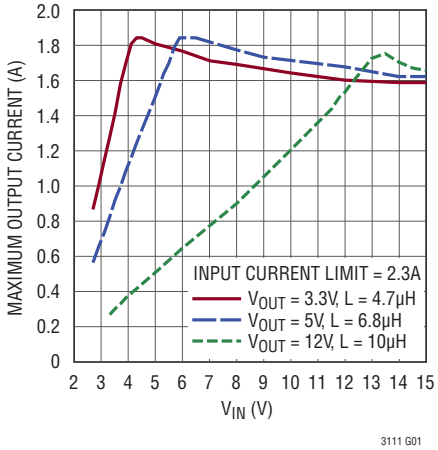
Note 6: SYNC frequency range is tested with a square wave. Operation with 100ns minimum high or low time is assured by design.

Note 7: Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during the non-overlap durations when the switch pin voltage is influenced by the magnitude and direction of the inductor current.

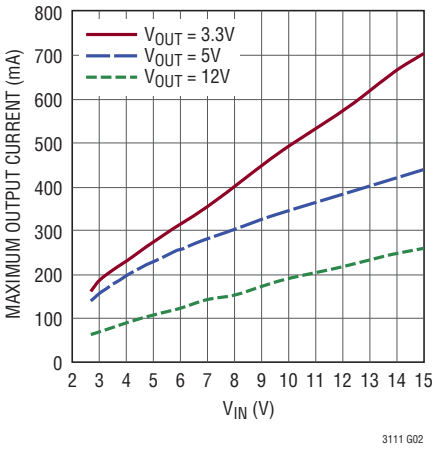
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, V_{OUT} = 5V, unless otherwise specified

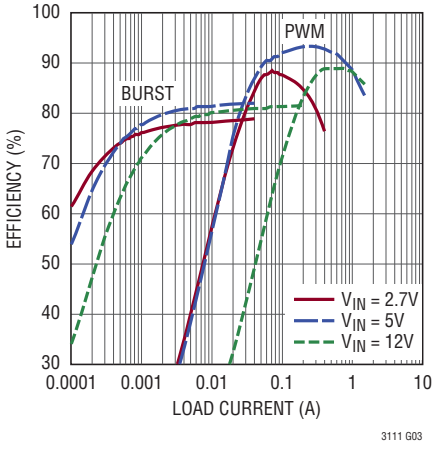
Maximum Output Current in PWM Mode vs V_{IN}



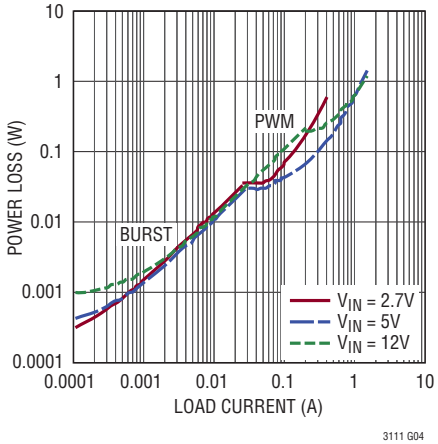
Maximum Load Current in Burst Mode Operation vs V_{IN}



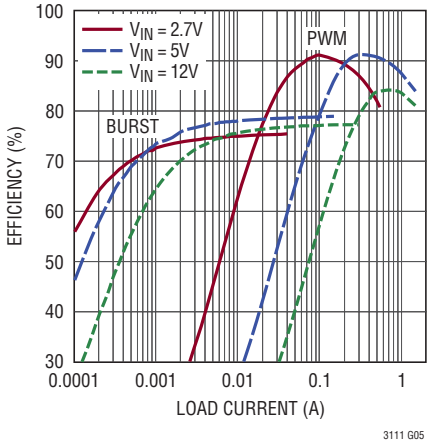
Wide V_{IN} to 5V_{OUT} Efficiency



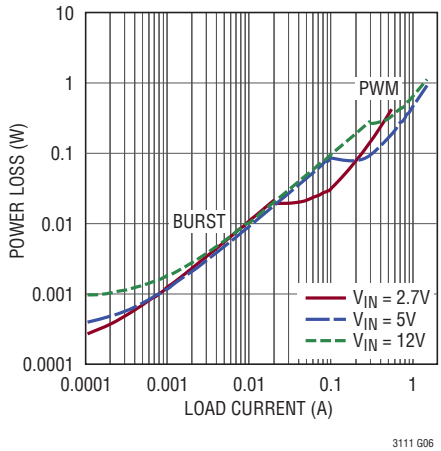
Wide V_{IN} to 5V_{OUT} Power Loss



Wide V_{IN} to 3.3V_{OUT} Efficiency



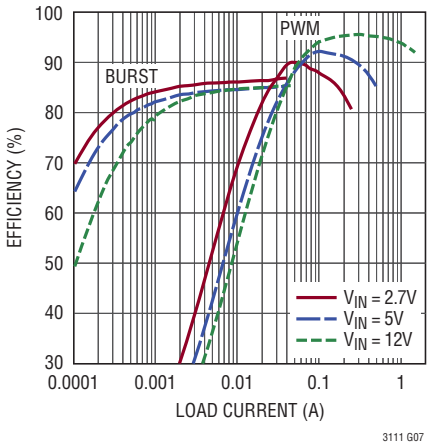
Wide V_{IN} to 3.3V_{OUT} Power Loss



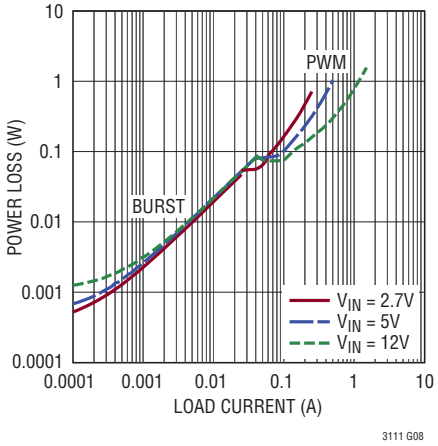
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, V_{OUT} = 5V, unless otherwise specified

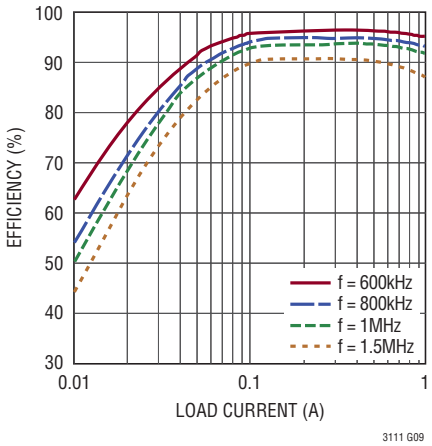
Wide V_{IN} to 12V_{OUT} Efficiency



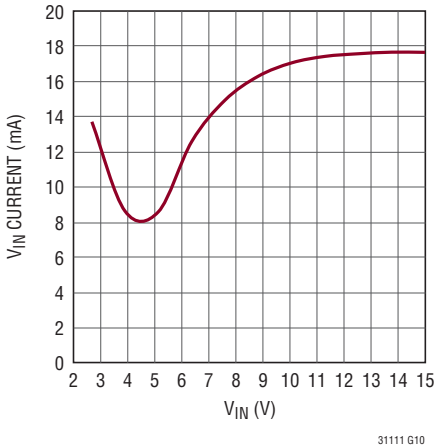
Wide V_{IN} to 12V_{OUT} Power Loss



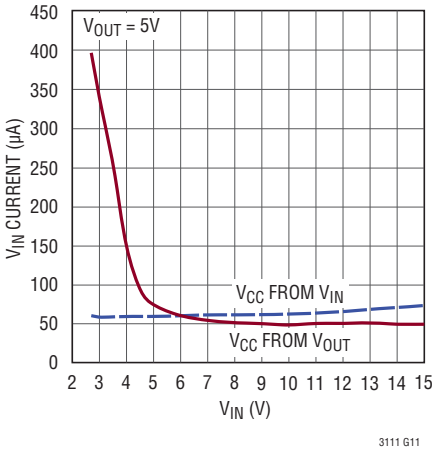
12V_{IN} to 12V_{OUT} Efficiency at f = 600kHz, 800kHz, 1MHz and 1.5MHz with L = 10µH



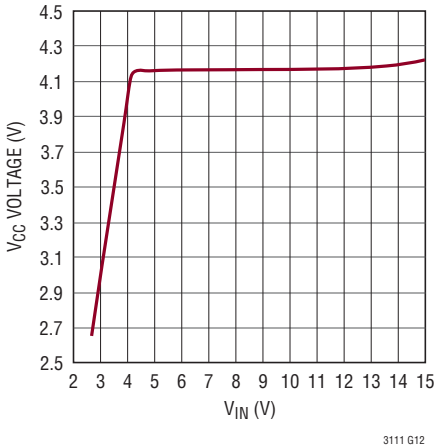
800kHz PWM Mode No-Load Input Current



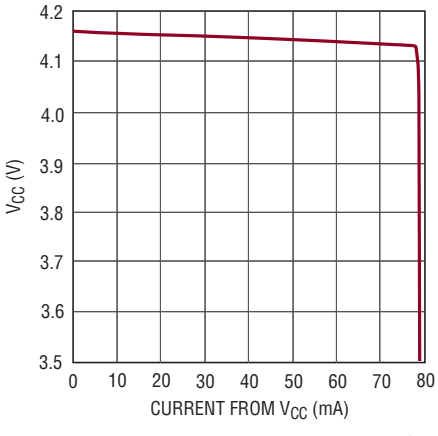
Burst Mode No-Load Current with V_{CC} from V_{IN} or Back-Fed from V_{OUT} with an Optional Diode



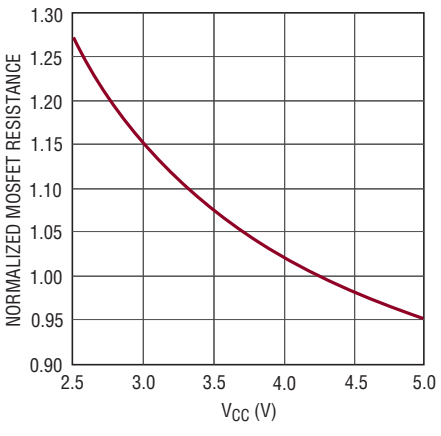
V_{CC} Voltage vs V_{IN} PWM Mode No Load



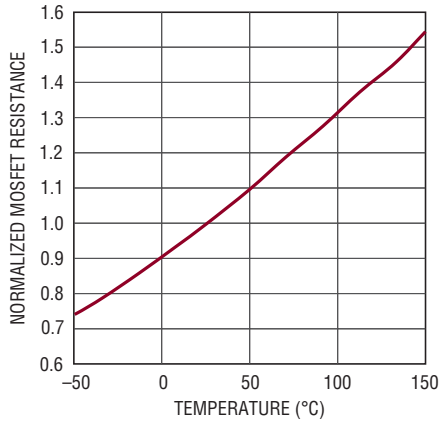
V_{CC} Voltage vs V_{CC} Current



Normalized N-Channel MOSFET Resistance vs V_{CC}



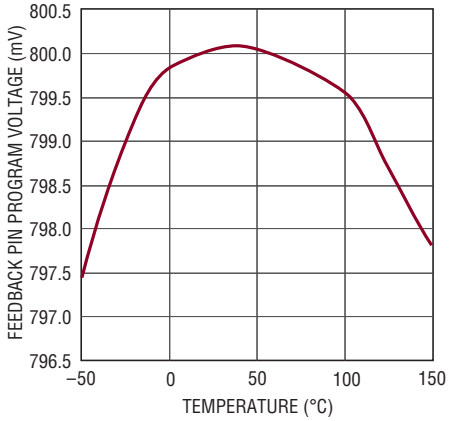
Normalized N-Channel MOSFET Resistance vs Temperature



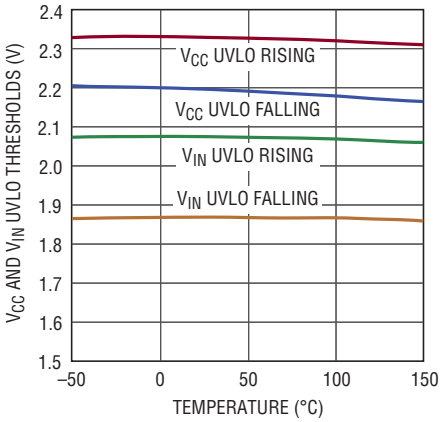
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, V_{OUT} = 5V, unless otherwise specified

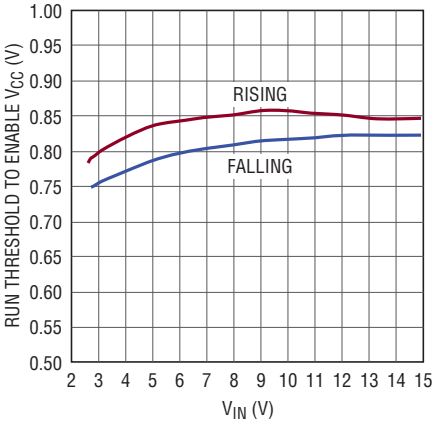
Feedback Pin Program Voltage vs Temperature



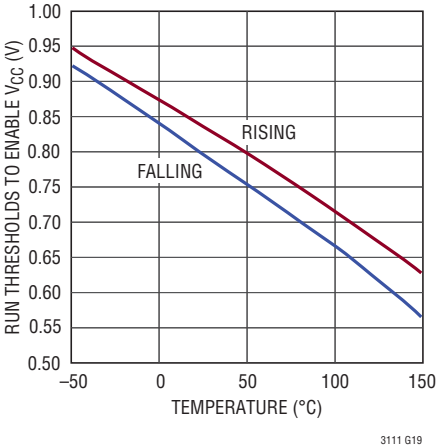
V_{CC} and V_{IN} UVLO Voltage Thresholds vs Temperature



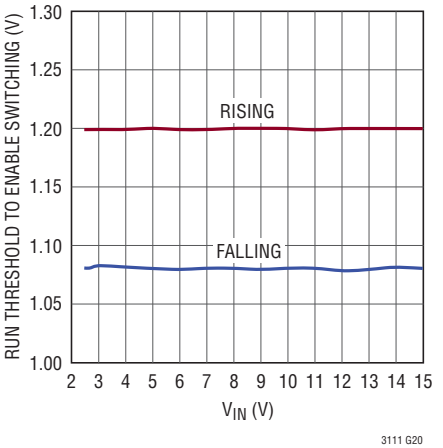
RUN Threshold to Enable/Disable V_{CC} vs V_{IN}



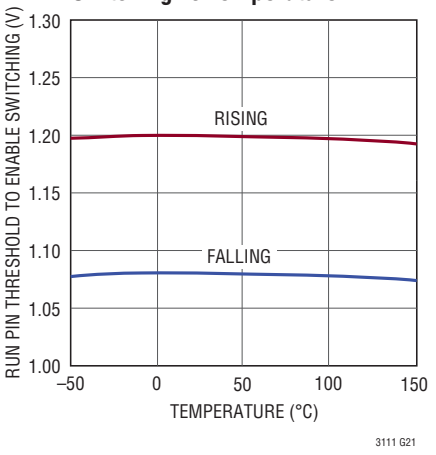
RUN Threshold to Enable/Disable V_{CC} vs Temperature



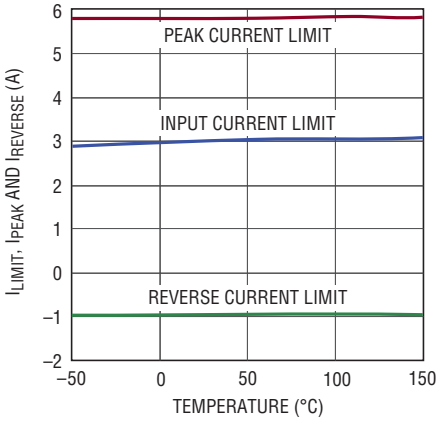
RUN Threshold to Enable/Disable Switching vs V_{IN}



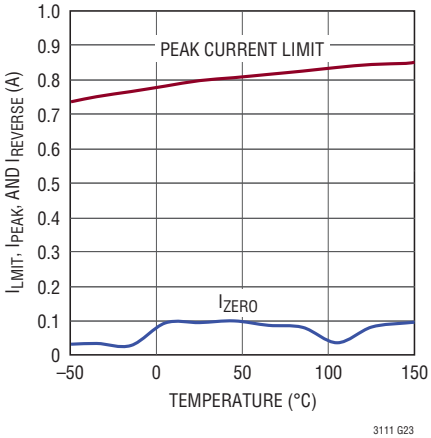
RUN Threshold to Enable/Disable Switching vs Temperature



PWM Mode Input, Peak and Reverse Current Limits vs Temperature



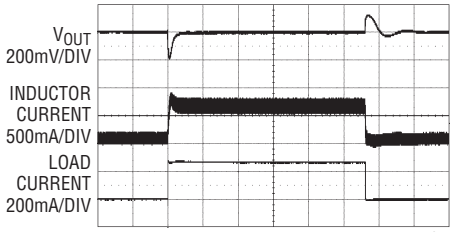
Burst Mode Peak Current, I_{ZERO} Limits vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

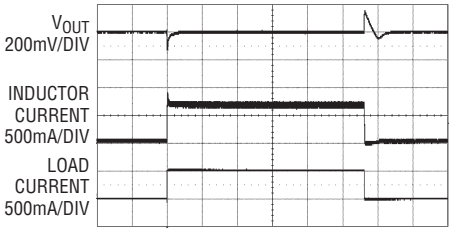
T_A = 25°C, V_{IN} = 5V, V_{OUT} = 5V, unless otherwise specified

3V_{IN} to 5V_{OUT} 0.05A to 0.25A Load Response



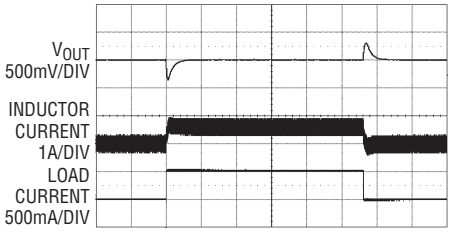
FRONT PAGE APPLICATION

5V_{IN} to 5V_{OUT} 0.05A to 0.5A Load Response



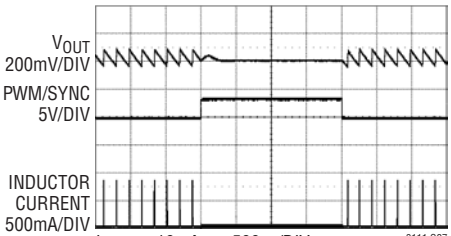
FRONT PAGE APPLICATION

12V_{IN} to 5V_{OUT} 0.05A to 0.5A Load Response

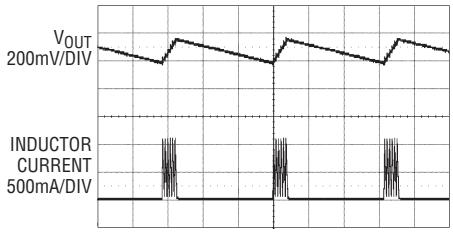


FRONT PAGE APPLICATION

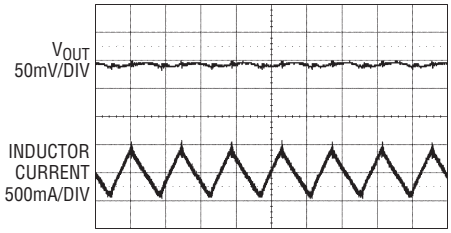
5V_{IN} to 5V_{OUT} Burst to PWM Response



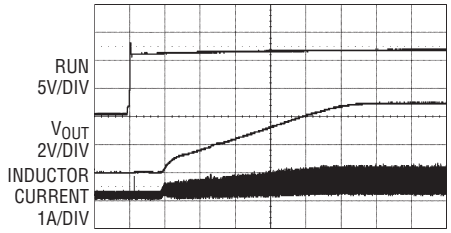
12V_{IN} to 5V_{OUT} Burst Mode V_{OUT} Ripple



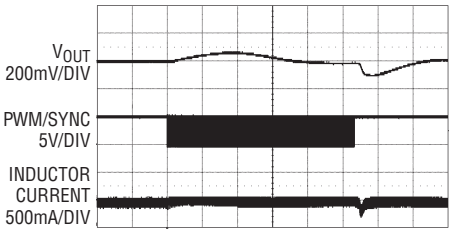
12V_{IN} to 5V_{OUT} PWM V_{OUT} Ripple



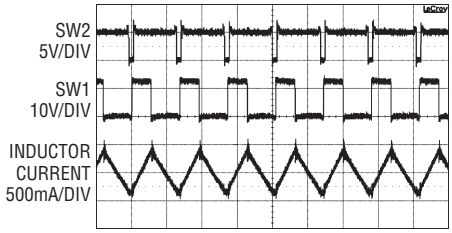
7.5V_{IN} to 5V_{OUT} Start-Up Response



1.5MHz SYNC Signal Capture and Release



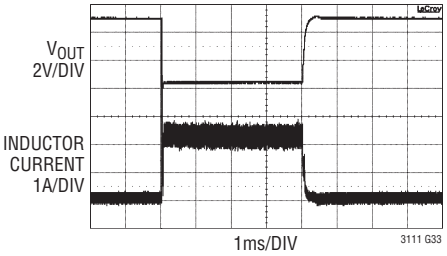
12V_{IN} to 5V_{OUT} SW1 and SW2 Waveforms



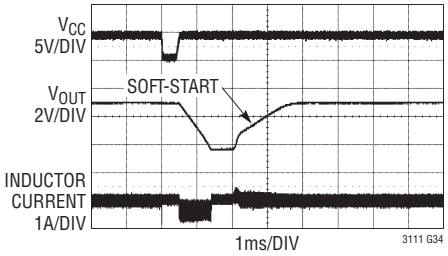
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, V_{OUT} = 5V, unless otherwise specified

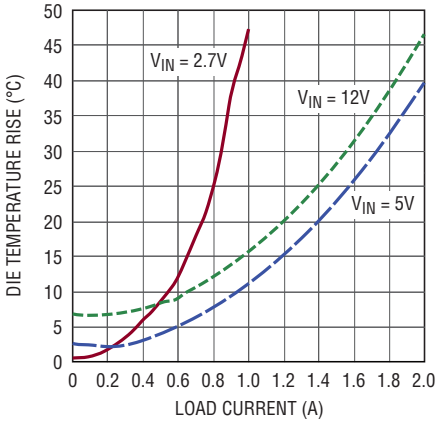
V_{OUT} Short-Circuit Response and Recovery



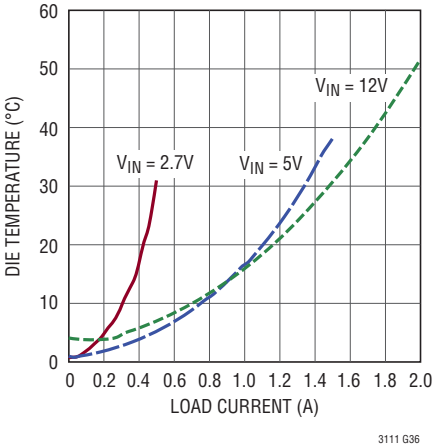
V_{CC} Short-Circuit Response and Recovery



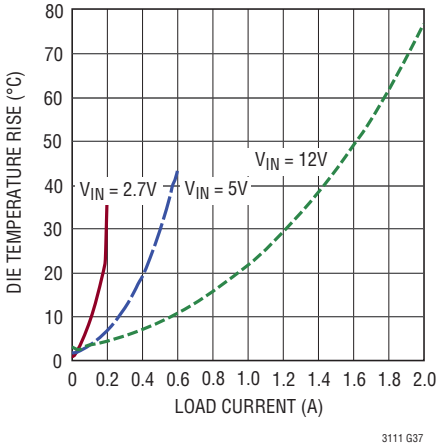
$3.3V_{OUT}$ Die Temperature Rise vs Continuous Load Current 4-Layer Demo Board at 25°C



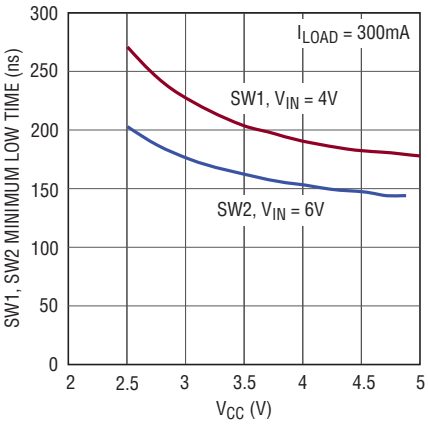
$5V_{OUT}$ Die Temperature Rise vs Continuous Load Current 4-Layer Demo Board at 25°C



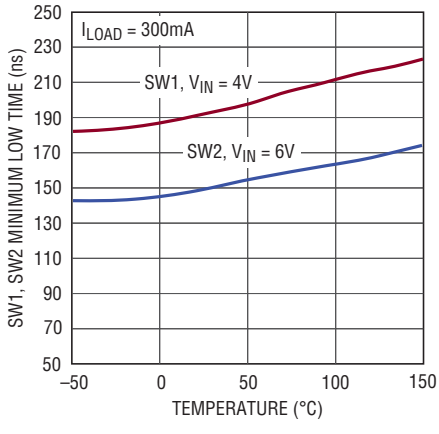
$12V_{OUT}$ Die Temperature Rise vs Continuous Load Current 4-Layer Demo Board at 25°C



SW1, SW2 Minimum Low Time vs V_{CC}



SW1, SW2 Minimum Low Time vs Temperature



PIN FUNCTIONS (DFN/MSOP)

COMP (Pin 1/Pin 1): Error Amp Output. An R-C network connected from this pin to FB sets the loop compensation for the voltage converter. Refer to the Applications Information section for component selection details.

FB (Pin 2/Pin 2): Feedback Voltage Input. Connect the V_{OUT} resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 15V by the following equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

where R1 is the resistor between V_{OUT} and FB and R2 is the resistor between FB and GND

SNSGND (Pin 3/Pin 3): This pin must be connected to ground.

RUN (Pin 4/Pin 4): Input to Enable or Disable the IC and Set Custom Input Undervoltage Lockout (UVLO) Thresholds. The RUN pin can be driven by an external logic signal to enable and disable the IC. In addition, the voltage on this pin can be set by a resistive voltage divider connected to the input supply in order to provide accurate turn-on and turn-off (UVLO) thresholds determined by:

$$V_{IN(RUN)} = 1.2V \bullet \left(1 + \frac{R5}{R6}\right)$$

The IC is enabled if RUN exceeds 1.2V nominally. Once enabled, the UVLO threshold has a built-in hysteresis of approximately 120mV, turn-off will occur when the voltage on RUN drops to below 1.08V nominally. To continuously enable the IC, RUN can be tied directly to the input voltage up to the absolute maximum rating. This pin should not be left unconnected.

V_{IN} (Pin 5/Pin 5): Input Supply Voltage. This pin should be bypassed to the ground plane with at least 10µF of low ESR, low ESL ceramic capacitance. Place this capacitor as close to the pin as possible and provide as short a return path to the ground plane as possible.

SW1 (Pin 6/Pin 6): The external inductor and internal switches A and B are connected here.

BST1 (Pin 7/Pin 7): Boosted Floating Driver Supply for A-Switch Driver. Connect a 0.1µF capacitor from this pin to SW1.

BST2 (Pin 8/Pin 10): Boosted Floating Driver Supply for D-Switch Driver. Connect a 0.1µF capacitor from this pin to SW2.

SW2 (Pin 9/Pin 11): The external inductor and internal switches C and D are connected here.

V_{OUT} (Pin 10/Pin 12): Regulated Output Voltage. This pin should be connected to a low ESR ceramic capacitor. The capacitor should be placed as close to the pin as possible and have a short return to the ground plane.

NC (Pin 11/Pin 13): Not Connected. This pin should be connected to ground.

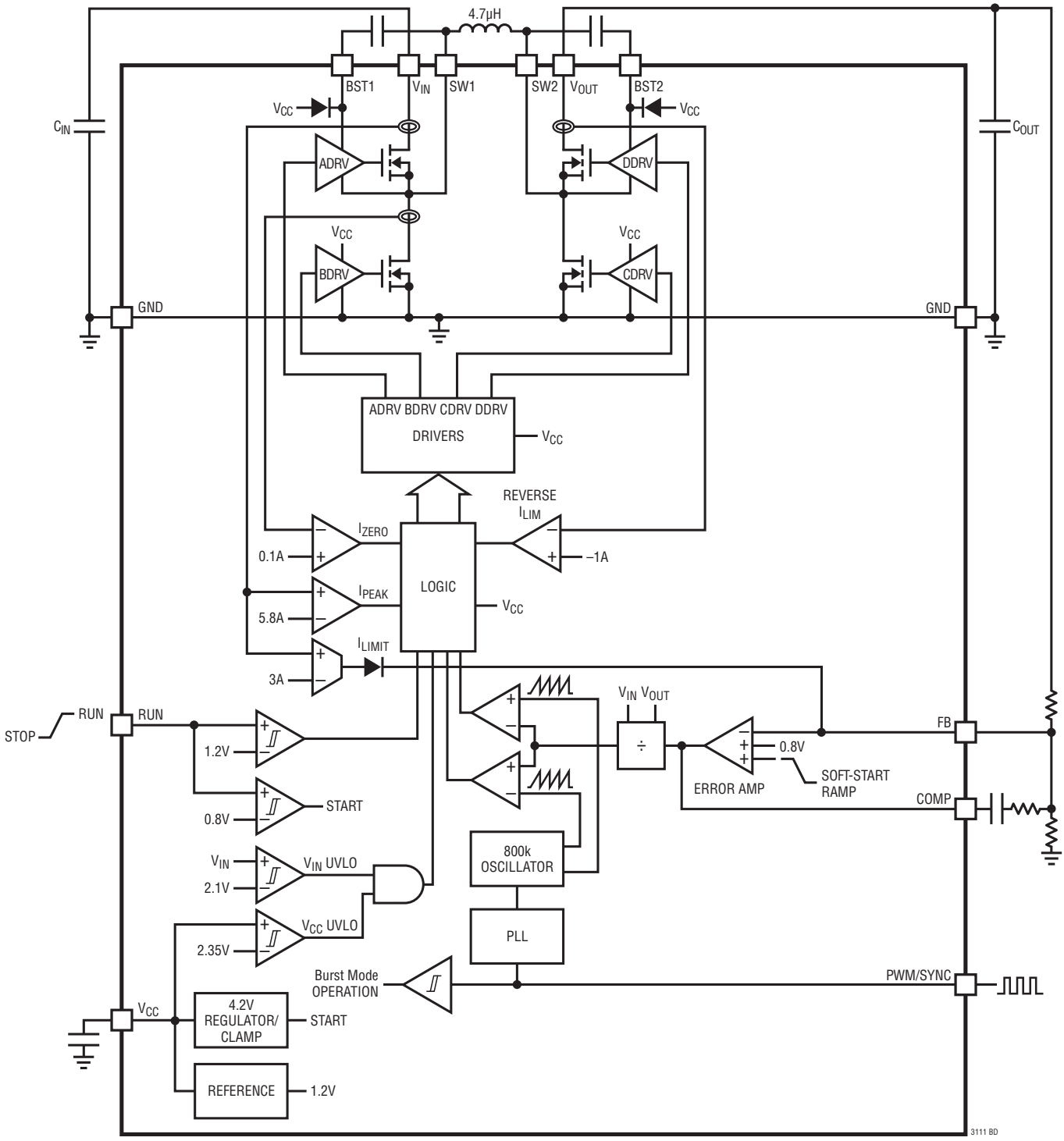
V_{CC} (Pin 12/Pin 14): External Capacitor Connection for the Regulated V_{CC} Supply. This supply is used to operate internal circuitry and switch drivers. V_{CC} will track V_{IN} up to 4.2V typical, but will maintain this voltage when V_{IN} > 4.2V. Connect a 1µF ceramic capacitor from this pin to GND. This pin can be tied to an external supply up to 5.5V. Refer to the Operation section of this data sheet under Power V_{CC} from an External Source for more details.

PWM/SYNC (Pin 13/Pin 15): Burst Mode Control and Synchronization Input. A DC voltage < 0.5V commands Burst Mode operation independent of load current, >1.5V commands 800kHz fixed frequency mode. A digital pulse train between 600kHz and 1.5MHz applied to this pin will override the internal oscillator and set the operating frequency. The pulse train should have a minimum high time or low time greater than 100ns (Note 6). Note the LTC3111 has reduced power capability when operating in Burst Mode operation. This pin should not be left unconnected.

SGND (Pin 14/Pin 16): Signal Ground. Terminate the RUN input voltage divider and output voltage divider to SGND.

PGND (Exposed Pad Pin 15/Pin 8, 9, Exposed Pad Pin 17) Power Ground. The exposed pad must be soldered to the PCB and electrically connected to ground through the shortest and lowest impedance connection possible.

SIMPLIFIED BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3111 is an extended input and output range, synchronous 1.5A buck-boost DC/DC converter optimized for a variety of applications. The LTC3111 utilizes a proprietary switching algorithm, which allows its output voltage to be regulated above, below or equal to the input voltage. The error amplifier output on COMP determines the output duty cycle of the switches. The low $R_{DS(ON)}$, low gate charge synchronous switches provide high efficiency pulse width modulation control. High efficiency is achieved at light loads when Burst Mode operation is commanded.

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator, Phase Lock Loop

An internal oscillator circuit sets the normal frequency of operation to 800kHz. A pulse train applied to the PWM/SYNC pin allows the operating frequency to be programmed between 600kHz to 1.5MHz via an internal phase-lock-loop circuit. The pulse train must have a minimum high or low state of at least 100ns to guarantee operation (see Note 6 of the Electrical Characteristics).

Error Amplifier

The LTC3111 contains a high gain operational amplifier which provides frequency compensation of the control loop to maintain output voltage regulation. To ensure loop stability, an external compensation network must be installed in the application circuit. A Type III compensation network, as shown in Figure 1, is recommended for most applications since it provides the flexibility to optimize the converter's transient response while simultaneously minimizing any DC error in the output voltage.

As shown in Figure 1, the error amplifier is followed by an internal analog divider which adjusts the loop gain by the reciprocal of the input voltage when the converter is in buck mode and by the output voltage when the converter is in boost mode which minimizes loop-gain variation over changes in the input voltage. This simplifies design of the compensation network and optimizes the transient response over the entire range of input voltages. Details

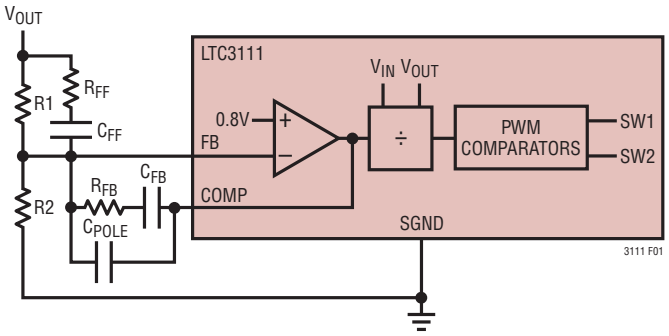


Figure 1. Error Amplifier and Compensation Network

on designing the compensation network for the LTC3111 applications can be found in the Applications Information section of this data sheet.

Current Limit Operation

The buck-boost converter has two current limit circuits. The input current limit sources current into the feedback divider network whenever the current in switch A exceeds 3A typical. Due to the high gain of the feedback loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The input current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A, the peak inductor current in current limit will have a dependency on the duty cycle (i.e., on the input and output voltages) in the overcurrent condition. For this current limit feature to be most effective, the Thevenin resistance from the FB to ground should exceed 100kΩ.

The speed of the input current limit circuit is limited by the dynamics of the converter loop. On a hard output short, it is possible for the inductor current to increase substantially beyond the input current limit before the input current limit circuit can react. For this reason, there is a peak current limit circuit which turns off switch A if the current in switch A exceeds approximately 190% of the input current limit value. This provides additional protection in the case of an instantaneous hard output short.

OPERATION

Should the output voltage become shorted, the input current limit is reduced to approximately one half of the normal operating current limit.

Reverse Current Limit

During fixed frequency operation, a reverse current comparator on switch D monitors the current entering the V_{OUT} pin. When this current exceeds 1A (typical) switch D will be turned off for the remainder of the switching cycle. This feature protects the buck-boost converter from excessive reverse current if the buck-boost output is held above the regulation voltage.

Internal Soft-Start

The LTC3111 buck-boost converter has an independent internal soft-start circuit with a nominal duration of 2ms. The converter remains in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load current during start-up. Soft-start is reset during a thermal shutdown.

THERMAL CONSIDERATIONS

For the LTC3111 to provide maximum output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct the heat away from the IC and into a copper plane with as much area as possible.

The efficiency and maximum output current capability of the LTC3111 will be reduced if the converter is required to continuously deliver large amounts of power or operate at high temperatures. The amount of output current derated is dependent upon factors such as board ground plane or heat sink area, ambient operating temperature and the input/output voltages of the application. A poor thermal design can cause excessive heating, resulting in impaired performance or reliability.

The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide to predict junction temperature rise from ambient. These curves were generated by mounting the LTC3111 to the 4-layer FR-4 demo printed circuit board layout shown in Figure 4. The curves were taken at room temperature, elevated ambient temperature will result in greater thermal rise rates due to increased $R_{DS(ON)}$ of the N-channel MOSFETs with temperature. The die temperature of the LTC3111 should be kept below the maximum junction rating of 125°C for E- and I-grades and 150°C for H- and MP-grades.

In the event that the junction temperature gets too high (approximately 170°C), the input current limit will be linearly decreased from its typical value. If the junction temperature continues to rise and exceeds approximately 175°C the LTC3111 will be disabled. All power devices are turned off and all switch nodes put to a high impedance state. The soft-start circuit for the converter is reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. When the die temperature drops to approximately 170°C the LTC3111 will restart.

UNDERVOLTAGE LOCKOUTS

The LTC3111 buck-boost converter is disabled and all power devices are turned off until the V_{CC} supply reaches 2.35V (typical). The soft-start circuit is reset during undervoltage lockout to provide a smooth restart once the input voltage rises above the undervoltage lockout threshold. A second UVLO circuit disables all power devices if V_{IN} is below 2.1V rising, 1.9V falling (typical). This can provide a lower V_{IN} operating range in applications where V_{CC} is powered from an alternate source or V_{OUT} after start-up.

INDUCTOR DAMPING

When the LTC3111 is disabled (RUN = 0V) or sleeping during Burst Mode operation (PWM/SYNC = 0V), active circuits "damp" the inductor voltage through 1kΩ (typical) impedance between SW1 and SW2 and GND to reduce ringing and EMI.

OPERATION

PWM MODE OPERATION

When the PWM/SYNC pin is held high, the LTC3111 buck-boost converter operates in a fixed-frequency pulse-width modulation (PWM) mode using voltage mode control. Full output current is only available in PWM mode. A proprietary switching algorithm allows the converter to transition between buck, buck-boost, and boost modes without discontinuity in inductor current. The switch topology for the buck-boost converter is shown in Figure 2.

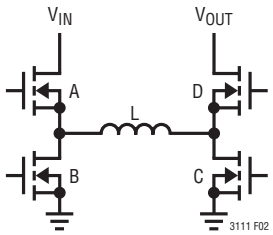


Figure 2. Buck-Boost Switch Topology

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on at maximum duty cycle and switch C turns on just long enough to refresh the voltage on the BST2 capacitor used to drive switch D. Switches A and B are pulse-width modulated to produce the required duty cycle to support the output regulation voltage.

As the input voltage nears the output voltage, switches A and D are on for a greater portion of the switching period, providing a direct current path from V_{IN} to V_{OUT}. Switches B and C are turned on only enough to ensure proper regulation and/or provide charging of the BST1 and BST2 capacitors. The internal control circuitry will determine the proper duty cycle in all modes of operation, which will vary with load current.

As the input voltage drops well below the output voltage, the converter operates solely in boost mode. Switch A turns on at maximum duty cycle and switch B turns on just long enough to refresh the voltage on the BST1 capacitor used to drive A. Switches C and D are pulse-width modulated to produce the required duty cycle to regulate the output voltage.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout the operational modes. These advantages result in increased efficiency and stability in comparison to the traditional 4-switch buck-boost converter.

OUTPUT VOLTAGE PROGRAMMING

The output voltage is set via the external resistor divider comprised of resistors R1 and R2 as show in Figures 1. The resistor divider values determine the output regulation voltage according to:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R1}{R2}\right)$$

In addition to setting the output voltage, the value of R1 is instrumental in controlling the dynamics of the compensation network. When changing the value of this resistor, care must be taken to understand the impact this will have on the compensation network.

In addition, the Thevenin equivalent resistance of the resistor divider controls the gain of the input current limit. To maintain sufficient gain in this loop, it is recommended that the Thevenin resistance be greater than 100kΩ.

RUN Comparator

In addition to serving as a logic-level input to enable the IC, the RUN pin includes an accurate internal comparator that allows it to be used to set custom rising and falling on/off thresholds with the addition of an external resistor divider. When RUN is driven above its logic threshold (0.8V typical), the LDO regulator is enabled, which provides power to the internal control circuitry of the IC. If the voltage on RUN is increased further so that it exceeds the RUN comparator accurate analog threshold (1.2V typical), all functions of the buck-boost converter will be enabled and a start-up sequence will ensue.

If RUN is brought below the accurate comparator threshold, the buck-boost converter will inhibit switching, but the

OPERATION

LDO regulator and control circuitry will remain powered unless RUN is brought below its logic threshold. Therefore, in order to completely shut down the IC, it is necessary to ensure that RUN is brought below its worst-case low logic threshold of 0.3V. RUN is a high voltage input and can be tied directly to V_{IN} to continuously enable the IC when the input supply is present. The RUN pin can be driven above V_{IN} or V_{OUT} as long as it stays within the operating range of 15V.

With the addition of an optional resistor divider as shown in Figure 3, the RUN pin can be used to establish a user-programmable turn on and turn off threshold.

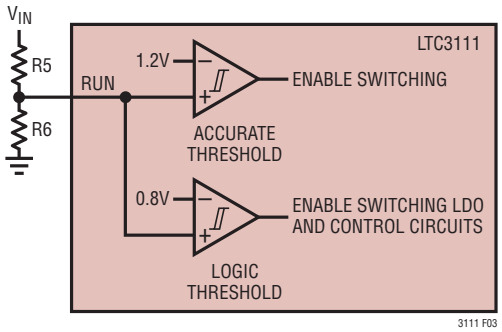


Figure 3. Accurate RUN Comparator

The buck-boost converter is enabled when the voltage on RUN reaches 1.2V (nominal). Therefore, the turn-on voltage threshold on V_{IN} is given by:

$$V_{IN(RUN)} = 1.2V \bullet \left(1 + \frac{R5}{R6}\right)$$

Once the converter is enabled, the RUN comparator includes a built-in hysteresis of approximately 120mV, so that the turn-off threshold will be approximately 10% lower than the turn-on threshold. Put another way, the internal threshold level for the RUN comparator looks like 1.08V after the IC is enabled.

The RUN comparator is relatively noise insensitive, but there may be cases due to PCB layout, very large value resistors for R5 and R6 or proximity to noisy components where noise pickup is unavoidable and may cause the turn-on or turn-off of the IC to be intermittent. In these cases, a filter capacitor can be added across R6 to ensure proper operation.

Powering V_{CC} from an External Source

The LTC3111's V_{CC} regulator can be powered or back-fed from an external source up to 5.5V. The advantage of back feeding V_{CC} from a voltage above 4.2V is higher efficiency. For $5V_{OUT}$ applications, V_{CC} can be easily powered from V_{OUT} using an external low current Schottky as shown in several applications circuits in the Typical Applications section.

Back feeding V_{CC} also improves a light load PWM mode output voltage ripple that occurs when the inductor passes through zero current by reducing the switch pin anti-cross conduction times. A disadvantage of powering V_{CC} from V_{OUT} is that no-load quiescent current increases at lower input voltage in Burst Mode operation as shown in the Typical Performance Characteristics (compared to V_{CC} powered from V_{IN}).

Burst Mode OPERATION

When the PWM/SYNC pin is held low, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light load and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses and as a result only a fraction of the maximum output current can be delivered when in Burst Mode operation.

These current pulses are repeated as often as necessary to maintain the output regulation voltage. The maximum output current, I_{MAX}, which can be supplied in Burst Mode operation is dependent upon the input and output voltage as approximated by the following formula:

$$I_{MAX} = \frac{I_{PK}}{2} \bullet \eta \bullet \left(\frac{V_{IN}}{V_{IN} + V_{OUT}}\right) A$$

where I_{PK} is the Burst Mode peak current limit (0.8A typical) in amps and η is the efficiency.

If the buck-boost load exceeds the maximum Burst Mode current capability, the output rail will lose regulation. In Burst Mode operation, the error amplifier is configured for low power operation and used to hold the compensation pin, COMP, to reduce transients that may occur during transitions from and to burst and PWM mode operation.

APPLICATIONS INFORMATION

The basic LTC3111 application circuit is shown on the front page of this data sheet. The external component selection is dependent upon the required performance of the IC in each particular application given trade-offs such as PCB area, output voltages, output currents, ripple voltages, and efficiency. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the application circuit.

Inductor Selection

To achieve high efficiency, a low ESR inductor should be utilized for the buck-boost converter. In addition, the buck-boost inductor must have a saturation current rating that is greater than the worst-case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple for buck or boost mode operation can be calculated from the following formulas:

$$\Delta I_{L(P\text{-}P\_BUCK)} = \frac{V_{OUT}}{L} \bullet \left(\frac{V_{IN} - V_{OUT}}{V_{IN}} \right) \bullet \left(\frac{1}{f} - t_{LOW} \right)$$

$$\Delta I_{L(P\text{-}P\_BOOST)} = \frac{V_{IN}}{L} \bullet \left(\frac{V_{OUT} - V_{IN}}{V_{OUT}} \right) \bullet \left(\frac{1}{f} - t_{LOW} \right)$$

where f is the frequency in Hz and L is the inductance in Henries and t_{LOW} is the switch pin minimum low time in seconds, which is typically 160ns.

In addition to affecting output current ripple, the inductor value can also impact the stability of the feedback loop. In boost mode, the converter transfer function has a right-half-plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductance can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop. It is recommended that the inductor value be chosen less than 15µH if the converter is to be used in the boost region. For 800kHz operation, a 4.7µH inductor is recommended for $5V_{OUT}$ and 10µH for $12V_{OUT}$.

The inductor DC resistance can impact the efficiency of the buck-boost converter as well as the maximum output current capability at low input voltage. In buck mode, the output current is limited only by the inductor current reaching the current limit value. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These include switch resistances, inductor resistance, and PCB trace resistance. Use of an inductor with high DC resistance can degrade the output current capability from that shown in the graph in the Typical Performance Characteristics section of this data sheet.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3111 buck-boost converter applications. Within each family (i.e., at a fixed size), the DC resistance generally increases and the maximum current generally decreases with increased inductance.

Table 1. Representative Buck-Boost Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft				
LPS6225	4.7	65	3.2	6.2 × 6.2 × 2.5
LPS6235	6.8	75	2.8	6.2 × 6.2 × 3.5
Cooper-Bussmann				
FP3-8R2-R	8.2	74	3.4	7.3 × 6.7 × 3.0
CD1-150-R	15	50	3.6	10.5 × 10.4 × 4.0
Sumida				
CDRH8D28/HP	10	78	3.0	8.3 × 8.3 × 3.0
CDRH8D28NP	4.7	24.7	3.4	8.3 × 8.3 × 3.0
TOKO				
B1047AS-6R8N	6.8	36	2.9	7.6 × 7.6 × 5.0
B1179BS-150M	15	56	2.7	12.0 × 12.0 × 6.0
Würth				
7447789004	4.7	33	2.9	7.3 × 7.3 × 3.2
744311470	4.7	19.5	6	6.9 × 6.9 × 3.8

Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer X5R and X7R dielectric ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be

APPLICATIONS INFORMATION

chosen large enough to reduce the output voltage ripple to acceptable levels. The minimum output capacitor needed for a given output voltage ripple (neglecting the capacitor ESR and ESL) can be calculated by the following formulas:

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} \bullet t_{LOW}}{C_{OUT}}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}}{f \bullet C_{OUT}} \bullet \left(\frac{V_{OUT} - V_{IN} + t_{LOW} \bullet f \bullet V_{IN}}{V_{OUT}} \right)$$

where f is the frequency in Hz, C_{OUT} is the output capacitance in µF, I_{LOAD} is the output current in amps and t_{LOW} is the switch pin minimum low time in seconds, which is typically 160ns.

In addition to output ripple generated across the output capacitor, there is also output ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by the following expression:

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD} \bullet R_{ESR}}{1 - t_{LOW} \bullet f} \cong I_{LOAD} \bullet R_{ESR}$$

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD} \bullet R_{ESR} \bullet V_{OUT}}{V_{IN}\left(1 - t_{LOW} \bullet f\right)} \cong \frac{I_{LOAD} \bullet R_{ESR} \bullet V_{OUT}}{V_{IN}}$$

where R_{ESR} is the series resistor of the output capacitor and all other terms are as previously defined.

Input Capacitor Selection

It is recommended that a low ESR ceramic capacitor with a value of at least 10µF be located as close to the V_{IN} pin as possible. In addition, the return trace from the pin to the ground plane should be made as short as possible. It is important to minimize any stray resistance from the converter to the battery or power source. If cabling is required to connect the LTC3111 to the battery or power supply, a higher ESR capacitor or a series resistor with a low ESR capacitor in parallel with the low ESR capacitor may be required to damp out ringing caused by the cable inductance.

Capacitor Vendor Information

Both the input bypass capacitors and output capacitors used with the LTC3111 must be low ESR and designed to handle the large AC currents generated by switching converters. This is important to maintain proper functioning of the IC and to reduce input/output ripple. Many modern low voltage ceramic capacitors experience significant loss in capacitance from their rated value with increased DC bias voltages. For example, it is not uncommon for a small surface mount ceramic capacitor to lose more than 50% of its rated capacitance when operated near its rated voltage. As a result, it is sometimes necessary to use a larger value capacitance or a capacitor with a larger case size than required in order to actually realize the intended capacitance at the full operating voltage. For details, consult the capacitor vendor's curve of capacitance versus DC bias voltage.

The capacitors listed in Table 2 provide a sampling of small surface mount ceramic capacitors that are well suited to LTC3111 application circuits. All listed capacitors are either X5R or X7R dielectric in order to ensure that capacitance loss over temperature is minimized.

Table 2. Representative Bypass and Output Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	SIZE (mm) L × W × H (FOOTPRINT)
AVX			
12103D226MAT2A	22	25	3.2 × 2.5 × 2.79 X5R Ceramic
Kemet			
C220X226K3RACTU	22	25	5.7 × 5.0 × 2.4 X7R Ceramic
A700D226M016ATE030	22	16	7.3 × 4.3 × 2.8 Al Poly, 25mΩ
Murata			
GRM32ER71E226KE15L	22	25	3.2 × 2.5 × 2.5 X7R Ceramic
Panasonic			
ECJ-4YB1E226M	22	25	3.2 × 2.5 × 2.5 X5R Ceramic
Sanyo			
25SVPF47M	47	25	6.6 × 6.6 × 5.9 OS-CON, 30mΩ
Vishay			
94SVPD476X0035F12	47	35	10.3 × 10.3 × 12.6 OS-CON, 30mΩ

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PCB Layout Considerations

The LTC3111 switches large currents at high frequencies. Special attention should be paid to the PCB layout to ensure a stable, noise-free and efficient application circuit. Figure 4 presents a representative PCB layout to outline some of the primary considerations. A few key guidelines are outlined below:

1. All circulating high current paths should be kept as short as possible. This can be accomplished by keeping the routes to all circled components in the figure below as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on V_{IN} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The exposed pad is the power ground connection for the LTC3111. Multiple vias should connect the back pad directly to the ground plane. In addition maximization of the metallization connected to the back pad will improve the thermal environment and improve the power handling capabilities of the IC.
3. The circled components and their connections should all be placed over a complete ground plane to minimize loop cross-sectional areas. This minimizes EMI and reduces inductive drops.
4. Connections to all of the circled components should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.

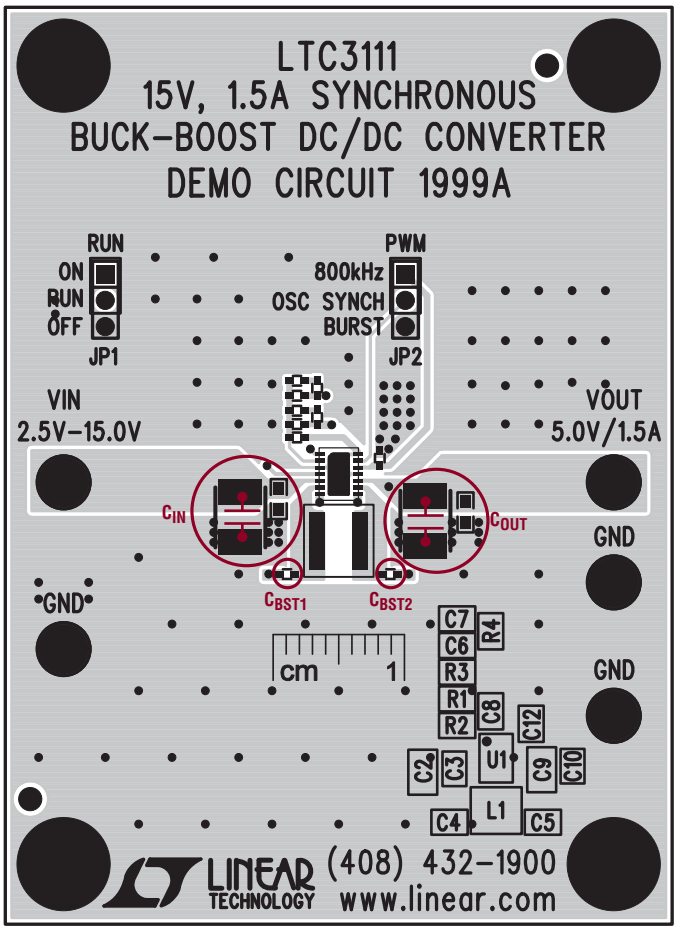

Figure 4a. Top and Fabrication Layer of Example PCB

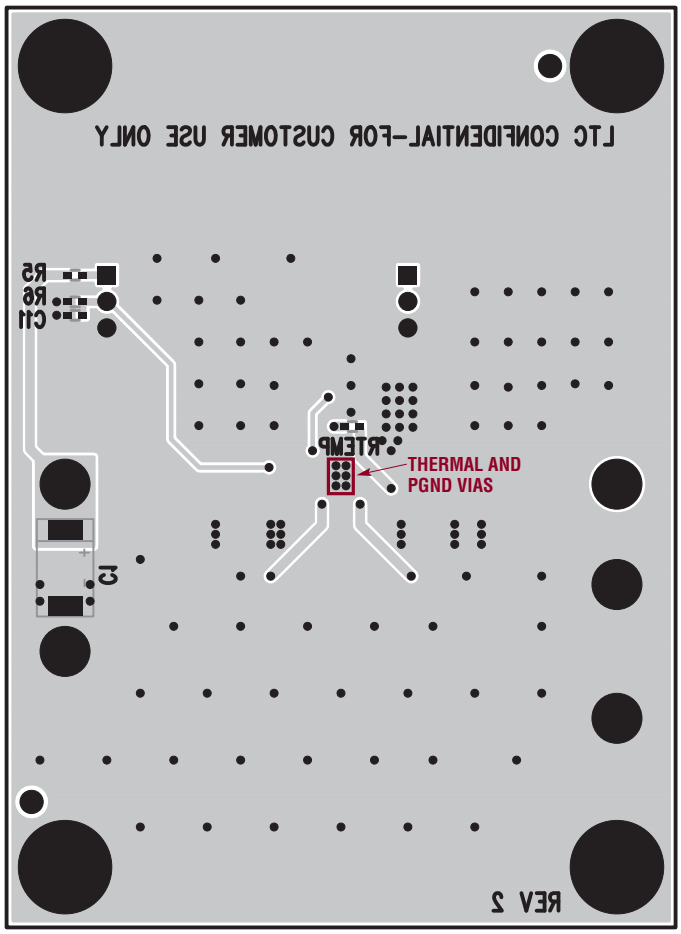

Figure 4b. Bottom and Fabrication Layer of Example PCB

APPLICATIONS INFORMATION

5. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned to the ground plane using a via placed close to the IC and away from the power connections.
6. Keep the connection from the resistor dividers to the feedback pins (FB pin) as short as possible and away from the switch pin connections.
7. Crossover connections should be made on inner copper layers if available. If it is necessary to place these on the ground plane, make the trace on the ground plane as short as possible to minimize the disruption to the ground plane.

Buck Mode Small-Signal Model

The LTC3111 uses a voltage mode control loop to maintain regulation of the output voltage. An externally compensated error amplifier drives the COMP pin to generate the appropriate duty cycle of the power switches. Use of an external compensation network provides the flexibility for optimization of closed-loop performance over the wide variety of output voltages, switching frequencies, and external component values supported by the LTC3111.

The small-signal transfer function of the buck-boost converter is different in the buck and boost modes of operation and care must be taken to ensure stability in both operating regions. When stepping down from a higher input voltage to a lower output voltage, the converter will operate in buck mode and the small-signal transfer function from the error amplifier output COMP, to the converter output voltage is given by the following equation:

$$\left.\frac{V_O}{V_{COMP}}\right|_{BUCK} = G_{BUCK}\,\frac{1+\frac{s}{2\bullet\pi\bullet f_Z}}{1+\frac{s}{2\bullet\pi\bullet f_0\bullet Q}+\left(\frac{s}{2\bullet\pi\bullet f_0}\right)^2}$$

The gain term, G_{BUCK}, is comprised of three different components: the gain of the analog divider, the gain of the pulse-width modulator, and the gain of the power stage as given by the following expressions where V_{IN} is the input voltage to the converter, f is the switching frequency, R is the load resistance, and t_{LOW} is the switch pin minimum low time, which is typically 160ns. The parameter R_S represents the average series resistance of the power stage and can be approximated as twice the average power switch resistance plus the DC resistance of the inductor.

$$G_{BUCK} = G_{DIVIDER}\bullet G_{PWM}\bullet G_{POWER}$$

$$G_{DIVIDER} = \frac{18}{V_{IN}}$$

$$G_{PWM} = 2.5\bullet\left(1-t_{LOW}\bullet f\right)$$

$$G_{POWER} = \frac{V_{IN}\bullet R}{\left(1-t_{LOW}\bullet f\right)\bullet\left(R+R_S\right)}$$

Notice that the gain of the analog divider cancels the input voltage dependence of the power stage. As a result, the buck mode gain is approximated by a constant as given by the following equation:

$$G_{BUCK} = 45\bullet\frac{R}{R+R_S} \cong 45 = 33dB$$

The buck mode transfer function has a single zero which is generated by the ESR of the output capacitor. The zero frequency, f_Z, is given by the following expression where R_C and C_O are the ESR and value of the output filter capacitor respectively.

$$f_Z = \frac{1}{2\bullet\pi\bullet R_C\bullet C_O}$$

In most applications, an output capacitor with a very low ESR is utilized in order to reduce the output voltage ripple to acceptable levels. Such low values of capacitor ESR result in a very high frequency zero and as a result the zero is commonly too high in frequency to significantly impact compensation of the feedback loop. The denominator of the buck mode transfer function exhibits a pair of resonant poles generated by the LC filtering of the power stage. The resonant frequency of the power stage, f_O, is given by the following expression where L is the value of the inductor:

$$f_O = \frac{1}{2\bullet\pi}\bullet\sqrt{\frac{R+R_S}{L\bullet C_O\left(R+R_C\right)}} \cong \frac{1}{2\bullet\pi\bullet\sqrt{L\bullet C_O}}$$

APPLICATIONS INFORMATION

The quality factor, Q, has a significant impact on compensation of the voltage loop since a higher Q factor produces a sharper loss of phase near the resonant frequency. The quality factor is inversely related to the amount of damping in the power stage and is substantially influenced by the average series resistance of the power stage, R_S. Lower values of R_S will increase the Q and result in a sharper loss of phase near the resonant frequency and will require more phase boost or lower bandwidth to maintain an adequate phase margin.

$$Q = \frac{\sqrt{L \bullet C_O \left(R + R_C\right) \bullet \left(R + R_S\right)}}{R \bullet R_C \bullet C_O + L + C_O \bullet R_S \bullet \left(R + R_C\right)}$$

$$\cong \frac{\sqrt{L \bullet C_O}}{\frac{L}{R} + C_O \bullet R_S}$$

Boost Mode Small-Signal Model

When stepping up from a lower input voltage to a higher output voltage, the buck-boost converter will operate in boost mode where the small-signal transfer function from control voltage, V_{COMP}, to the output voltage is given by the following expression:

$$\left.\frac{V_O}{V_{COMP}}\right|_{BOOST} = G_{BOOST} \frac{\left(1 + \frac{s}{2 \bullet \pi \bullet f_Z}\right) \bullet \left(1 - \frac{s}{2 \bullet \pi \bullet f_{RHPZ}}\right)}{1 + \frac{s}{2 \bullet \pi \bullet f_O \bullet Q} + \left(\frac{s}{2 \bullet \pi \bullet f_O}\right)^2}$$

In boost mode operation, the transfer function is characterized by a pair of resonant poles and a zero generated by the ESR of the output capacitor as in buck mode. However, in addition there is a right-half-plane zero which generates increasing gain and decreasing phase at higher frequencies. As a result, the crossover frequency in boost mode operation generally must be set lower than in buck mode in order to maintain sufficient phase margin.

The boost mode gain, G_{BOOST}, is comprised of three components: the analog divider, the pulse width modulator and the power stage. The gain of the PWM remains the same as in buck mode operation, but the gain of the analog divider and power stage in boost mode are given by the following equation:

$$G_{DIVIDER} = \frac{18}{V_{OUT}}$$

$$G_{POWER} = \frac{V_{OUT}^2}{\left(1 - t_{LOW} \bullet f\right) \bullet V_{IN}}$$

By combining the individual terms, the total gain in boost mode can be reduced to the following expression. Notice that unlike in buck mode, the gain in boost mode is a function of both the input and output voltage:

$$G_{BOOST} = 45 \bullet \frac{V_{OUT}}{V_{IN}}$$

In boost mode operation, the frequency of the right-half-plane zero, f_{RHPZ}, is given by the following expression. The frequency of the right-half-plane zero decreases at higher loads and with larger inductors:

$$f_{RHPZ} - \frac{R \bullet \left(1 - t_{LOW} \bullet f\right)^2 \bullet V_{IN}^2}{2 \bullet \pi \bullet L \bullet V_{OUT}^2}$$

In boost mode, the resonant frequency of the power stage has a dependence on the input and outputvoltage as shown by the following equation:

$$f_O = \frac{1}{2 \bullet \pi} \bullet \sqrt{\frac{R_S + \frac{R \bullet V_{IN}^2}{V_{OUT}^2}}{L \bullet C_O \bullet \left(R + R_C\right)}} \cong \frac{1}{2 \bullet \pi} \bullet \frac{V_{IN}}{V_{OUT}} \bullet \sqrt{\frac{1}{L \bullet C_O}}$$

Finally, the magnitude of the quality factor of the power stage in boost mode operation is given by the following expression:

$$Q = \frac{\sqrt{L \bullet C_O \bullet R \bullet \left(R_S + \frac{R \bullet V_{IN}^2}{V_{OUT}^2}\right)}}{L + C_O \bullet R_S \bullet R}$$

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Compensation Of The Voltage Loop

The small-signal models of the LTC3111 reveal that the transfer function from the error amplifier output, COMP, to the output voltage is characterized by a set of resonant poles and a possible zero generated by the ESR of the output capacitor as shown in the Bode plot of Figure 5. In boost mode operation, there is an additional right-half-plane zero that produces phase lag and increasing gain at higher frequencies. Typically, the compensation network is designed to ensure that the loop crossover frequency is low enough that the phase loss from the right-half-plane zero is minimized. The low frequency gain in buck mode is a constant, but varies with both V_{IN} and V_{OUT} in boost mode.

For charging or other applications that do not require an optimized output voltage transient response, a simple Type I compensation network as shown in Figure 6 can be used to stabilize the voltage loop. To ensure sufficient phase margin, the gain of the error amplifier must be low enough that the resultant crossover frequency of the control loop is well below the resonant frequency.

In most applications, the low bandwidth of the Type I compensated loop will not provide sufficient transient response performance. To obtain a wider bandwidth feedback loop, optimize the transient response, and minimize the size of the output capacitor, a Type III compensation network as shown in Figure 7 is required.

A Bode plot of the typical Type III compensation network is shown in Figure 8. The Type III compensation network provides a pole near the origin which produces a very high loop gain at DC to minimize any steady-state error in the regulation voltage. Two zeros located at f_{ZERO1} and f_{ZERO2} provide sufficient phase boost to allow the loop crossover frequency to be set above the resonant frequency, f_O, of the power stage. The Type III compensation network also introduces a second and third pole. The second pole, at frequency f_{POLE2}, reduces the error amplifier gain to a zero slope to prevent the loop crossover from extending

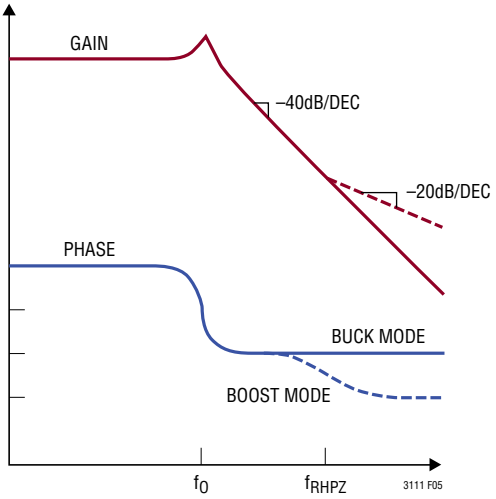

Figure 5: Buck-Boost Converter Bode Plot

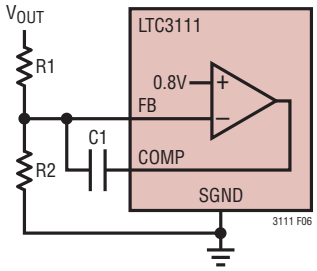

Figure 6: Error Amplifier with Type I Compensation

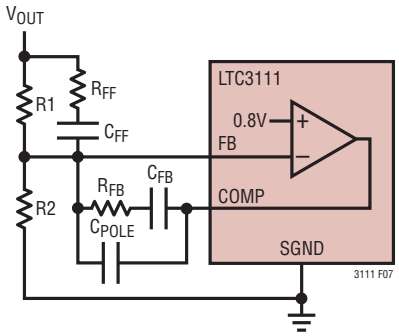

Figure 7: Error Amplifier with Type III Compensation

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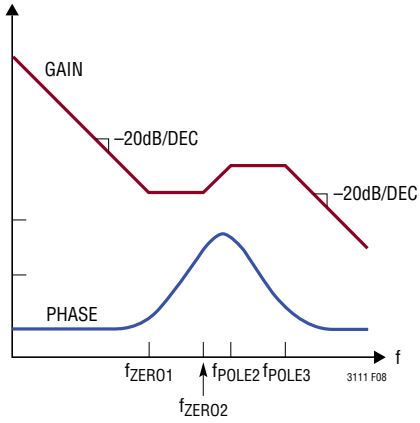

Figure 8: Type III Compensation Bode Plot

too high in frequency. The third pole at frequency f_{POLE3} provides attenuation of high frequency switching noise.

The transfer function of the compensated Type III error amplifier from the input of the resistor divider to the output of the error amplifier, COMP, is:

$$\frac{V_{COMP}}{V_O} = G_{COMP} \bullet \frac{\left(1+\frac{s}{2\bullet\pi\bullet f_{ZERO1}}\right)\bullet\left(1+\frac{s}{2\bullet\pi\bullet f_{ZERO2}}\right)}{s\bullet\left(1+\frac{s}{2\bullet\pi\bullet f_{POLE2}}\right)\bullet\left(1+\frac{s}{2\bullet\pi\bullet f_{POLE3}}\right)}$$

The compensation gain is given by the following equation. The simpler approximate value is sufficiently accurate in most cases since C_{FB} is typically much larger in value than C_{POLE}.

$$G_{COMP} \cong \frac{1}{R1\bullet\left(C_{FB}+C_{POLE}\right)} \cong \frac{1}{R1\bullet C_{FB}}$$

The pole and zero frequencies of the Type III compensation network can be calculated from the following equations where all frequencies are in Hz, resistances are in ohms, and capacitances are in farads.

$$f_{ZERO1} = \frac{1}{2\bullet\pi\bullet R_{FB}\bullet C_{FB}}$$

$$f_{ZERO2} = \frac{1}{2\bullet\pi\left(R1+R_{FF}\right)\bullet C_{FF}} \cong \frac{1}{2\bullet\pi\bullet R1\bullet C_{FF}}$$

$$f_{POLE2} = \frac{1}{2\bullet\pi\bullet\frac{C_{FB}\bullet C_{POLE}}{C_{FB}+C_{POLE}}\bullet R_{FB}} \cong \frac{1}{2\bullet\pi\bullet R_{FB}\bullet C_{POLE}}$$

$$f_{POLE3} = \frac{1}{2\bullet\pi\bullet R_{FF}\bullet C_{FF}}$$

In most applications the compensation network is designed so that the loop crossover frequency is above the resonant frequency of the power stage, but sufficiently below the boost mode right-half-plane zero to minimize the additional phase loss. Once the crossover frequency is decided upon, the phase boost provided by the compensation network is centered at that point in order to maximize the phase margin. A larger separation in frequency between the zeros and higher order poles will provide a higher peak phase boost but may also increase the gain of the error amplifier which can push out the loop crossover to a higher frequency.

The Q of the power stage can have a significant influence on the design of the compensation network because it determines how rapidly the 180° of phase loss in the power stage occurs. For very low values of series resistance, R_S, the Q will be higher and the phase loss will occur sharply. In such cases, the phase of the power stage will fall rapidly to –180° above the resonant frequency and the total phase margin must be provided by the compensation network.

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However, with higher losses in the power stage (larger R_S) the Q factor will be lower and the phase loss will occur more gradually. As a result, the power stage phase will not be as close to –180° at the crossover frequency and less phase boost is required of the compensation network.

The LTC3111 error amplifier is designed to have a fixed maximum bandwidth in order to provide rejection of switching noise to prevent it from interfering with the control loop. From a frequency domain perspective, this can be viewed as an additional single pole as illustrated in Figure 9. The nominal frequency of this pole is 400kHz. For typical loop crossover frequencies below about 60kHz the phase contributed by this additional pole is negligible. However, for loops with higher crossover frequencies this additional phase loss should be taken into account when designing the compensation network.

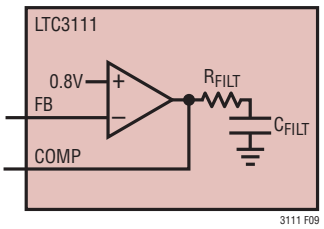

Figure 9. Internal Loop Filter

Loop Compensation Example

This section provides an example illustrating the design of a compensation network for a typical LTC3111 application circuit. In this example a 5V regulated output voltage is generated with the ability to supply a 500mA load from an input power source ranging from 3.5V to 15V. To reduce switching losses a 800kHz switching frequency has been chosen for this example. In this application the maximum inductor current ripple will occur at the highest input voltage. An inductor value of 4.7µH has been chosen to limit the worst-case inductor current ripple to less than 1A peak to peak. A low ESR output capacitor with a value of 22µF is specified to yield a worst-case output voltage ripple (occurring at the worst-case step-up ratio and maximum load current) of approximately 20mV. In summary, the key power stage specifications for this LTC3111 example application are given below.

$f = 0.8MHz$, $t_{LOW} = 160ns$

$V_{IN} = 3.5V$ to $15V$

$V_{OUT} = 5V$ at $R = 10\Omega$

$C_{OUT} = 22\mu F$, $R_C = 10m\Omega$

$L = 4.7\mu H$, $R_L = 25m\Omega$

$R_S = 200m\Omega$

With the power stage parameters specified, the compensation network can be designed. In most applications, the most challenging compensation corner is boost mode operation at the greatest step-up ratio and highest load current since this generates the lowest frequency right-half-plane zero and results in the greatest phase loss. Therefore, a reasonable approach is to design the compensation network at this worst-case corner and then verify that sufficient phase margin exists across all other operating conditions. In this example application, at V_{IN} = 3.5V and the full 500mA load current, the right-half-plane zero will be located at 136kHz and this will be a dominant factor in determining the bandwidth of the control loop.

The first step in designing the compensation network is to determine the target crossover frequency for the compensated loop. A reasonable starting point is to assume that the compensation network will generate a peak phase boost of approximately 60°. Therefore, in order to obtain a phase margin of 60°, the loop crossover frequency, f_C, should be selected as the frequency at which the phase

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of the buck-boost converter reaches –180°. As a result, at the loop crossover frequency the total phase will be simply the 60° of phase provided by the error amplifier as shown:

$$\text{Phase Margin} = \varphi_{\text{BUCK-BOOST}} + \varphi_{\text{ERRORAMPLIFIER}} + 180°$$
$$= -180° + 60° + 180° = 60°$$

Similarly, if a phase margin of 45° is required, the target crossover frequency should be picked as the frequency at which the buck-boost converter phase reaches –195° so that the combined phase at the crossover frequency yields the desired 45° of phase margin.

This example will be designed for a 60° phase margin to ensure adequate performance over parametric variations and varying operating conditions. As a result, the target crossover frequency, f_C, will be the point at which the phase of the buck-boost converter reaches –180°. It is generally difficult to determine this frequency analytically given that it is significantly impacted by the Q factor of the resonance in the power stage. As a result, it is best determined from a Bode plot of the buck-boost converter as shown in Figure 10. This Bode plot is for the LTC3111 buck-boost converter using the previously specified power stage parameters and was generated from the small-signal model equations using LTspice® software. In this case, the phase reaches –180° at 40kHz making f_C = 40kHz the target crossover frequency for the compensated loop.

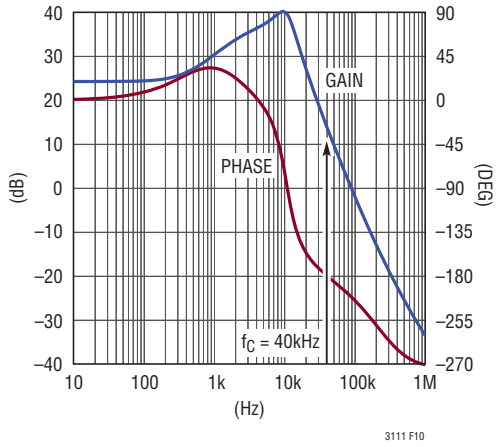

Figure 10. Converter Bode Plot V_{IN} = 3.5V, V_{OUT} = 5V, R = 10Ω

From the Bode plot of Figure 10 the gain of the power stage at the target crossover frequency is 13.5dB. Therefore, in order to make this frequency the crossover frequency in the compensated loop, the total loop gain at f_C must be adjusted to 0dB. To achieve this, the gain of the compensation network must be designed to be –13.5dB at the crossover frequency.

At this point in the design process, there are three constraints that have been established for the compensation network. It must have –13.5dB of gain at f_C = 40kHz, a peak phase boost of 60° that is centered at f_C = 40kHz. One way to design a compensation network to meet these targets is to simulate the compensation error amplifier Bode plot in LTspice for the typical compensation network shown on the front page of this data sheet. Then, the gain, pole and zero frequencies can be iteratively adjusted until the required constraints are met. Alternatively, an analytical approach can be used to design a compensation network with the desired phase boost, center frequency and gain. In general, this procedure can be cumbersome due to the large number of degrees of freedom in the Type III compensation network. However the design process can be simplified by assuming that both the compensation zeros occur at the same frequency, f_Z, and both higher order poles (f_{POLE2} and f_{POLE3}) occur at the common frequency, f_P. In most cases this is a reasonable assumption since the zeros are typically located between 1kHz and 10kHz and the poles are typically located near each other at much higher frequencies. Given this assumption, the maximum phase boost, provided by the compensation error amplifier is determined simply by the amount of separation between the poles and zeros as shown by the following equation:

$$\phi_{MAX} = 4 \bullet \arctan\left(\sqrt{\frac{f_P}{f_Z}}\right) - 270°$$

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A reasonable choice is to pick the frequency of the poles, f_P, to be 50 times higher than the frequency of the zeros, f_Z, which provides a peak phase boost of approximately 60° as was assumed previously. Next, the phase boost must be centered so that the peak phase occurs at the target crossover frequency. The frequency of the maximum phase boost, f_{CENTER}, is the geometric mean of the pole and zero frequency as:

$$f_{CENTER} = \sqrt{f_P \bullet f_Z} = \sqrt{50} \bullet f_Z \cong 7 \bullet f_Z$$

Therefore, in order to center the phase boost given a factor of 50 separation between the pole and zero frequencies, the zero should be located at one-seventh of the crossover frequency and the poles should be located at seventh times the crossover frequency as given by the following equation:

$$f_Z = \frac{f_C}{7} = \frac{40kHz}{7} = 5.71kHz$$

$$f_P = 7 \bullet f_C = 7 \bullet 40kHz = 280kHz$$

This placement of the poles and zeros will yield a peak phase boost of 60° that is centered at the crossover frequency, f_C. Next, in order to produce the desired target crossover frequency, the gain of the compensation network at the point of maximum phase boost, G_{CENTER}, must be set to –13.5dB. The gain of the compensated error amplifier at the point of the phase gain is given by:

$$G_{CENTER} = 10 \bullet \log\left[\frac{2 \bullet \pi \bullet f_P}{(2 \bullet \pi \bullet f_Z)^3 \bullet (R1 \bullet C_{FB})^2}\right] dB$$

Assuming a multiple of 50 separation between the pole and zero frequencies this can be simplified to the following expression:

$$G_{CENTER} = 20 \bullet \log\left(\frac{50}{2 \bullet \pi \bullet f_C \bullet R1 \bullet C_{FB}}\right) dB$$

This equation completes the set of constraints needed to determine the compensation component values. Specifically, the two zeros, f_{ZERO1} and f_{ZERO2}, should be located near 5.71kHz. The two poles, f_{POLE2} and f_{POLE3}, should be located near 280kHz and the gain should be set to provide a gain at the crossover frequency of G_{CENTER} = –13.5dB.

The first step in defining the compensation component values is to pick a value for R1 that provides an acceptably low quiescent current through the resistor divider. A value of R1 = 1MΩ is a reasonable choice. Next, the value of C_{FB} can be found in order to set the error amplifier gain at the crossover frequency to –13.5dB as follows:

$$G_{CENTER} = -13.5dB = 20 \bullet \log\left[\frac{50}{2 \bullet \pi \bullet 40kHz \bullet 1M\Omega \bullet C_{FB}}\right]$$

$$C_{FB} = \frac{50}{2 \bullet \pi \bullet 40kHz \bullet 1M\Omega \bullet 10^{-\frac{13.5}{20}}} \cong 1000pF$$

The compensation poles can be set at 280kHz and the zeros at 5.71kHz by using the expressions for the pole and zero frequencies given in the previous sections. Setting the frequency of the first zero, f_{ZERO1}, to 5.71kHz results in the following value for R_{FB}:

$$R_{FB} = \frac{1}{2 \bullet \pi \bullet 5.71kHz \bullet 1000pF} \cong 28.0k\Omega$$

This leaves the free parameter, C_{POLE}, to set frequency f_{POLE1} to the common pole frequency of 280kHz as given:

$$C_{POLE} = \frac{1}{2 \bullet \pi \bullet 280kHz \bullet 28k\Omega} \cong 22pF$$

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Next, C_{FF} can be chosen to set the second zero, f_{ZERO2}, to the common zero frequency of 5.71kHz.

$$C_{FF} = \frac{1}{2 \bullet \pi \bullet 5.71kHz \bullet 1M\Omega} \cong 27pF$$

Finally, the resistor value R_{FF} can be chosen to place the second pole at 280kHz.

$$R_{FF} = \frac{1}{2 \bullet \pi \bullet 280kHz \bullet 27pF} \cong 20k\Omega$$

Now that the pole frequencies, zero frequencies and gain of the compensation network have been established, the next step is to generate a Bode plot for the compensated error amplifier to confirm its gain and phase properties. A Bode plot of the error amplifier with the designed compensation component values is shown in Figure 11. The Bode plot confirms that the peak phase occurs at 40kHz and the phase boost at that point is 57°. In addition, the gain at the peak phase frequency is –14dB which is close to the design target.

The final step in the design process is to compute the Bode plot for the entire designed compensation network and confirm its phase margin and crossover frequency. The complete loop Bode plot for this example is shown in Figure 12. The loop crossover frequency is 40kHz and the phase margin is approximately 59°.

The Bode plot for the complete loop should be checked over all operating conditions and for variations in component values to ensure that sufficient phase margin exist in all cases. The stability of the loop should also be confirmed via time domain simulation and by the transient response of the converter in the actual circuit.

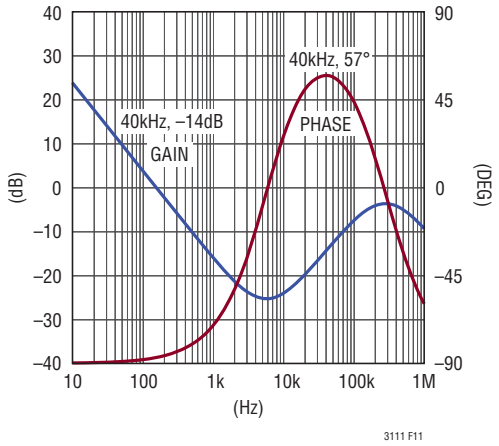


Figure 11: Compensation Error Amplifier Bode Plot

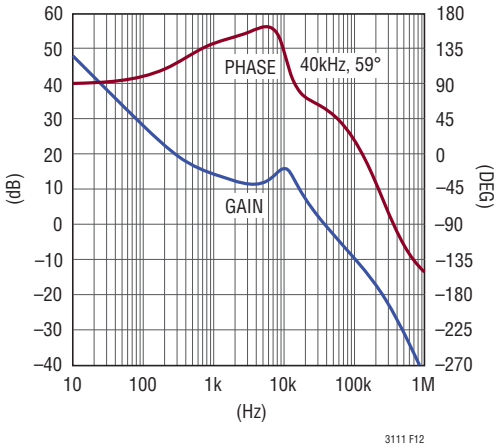
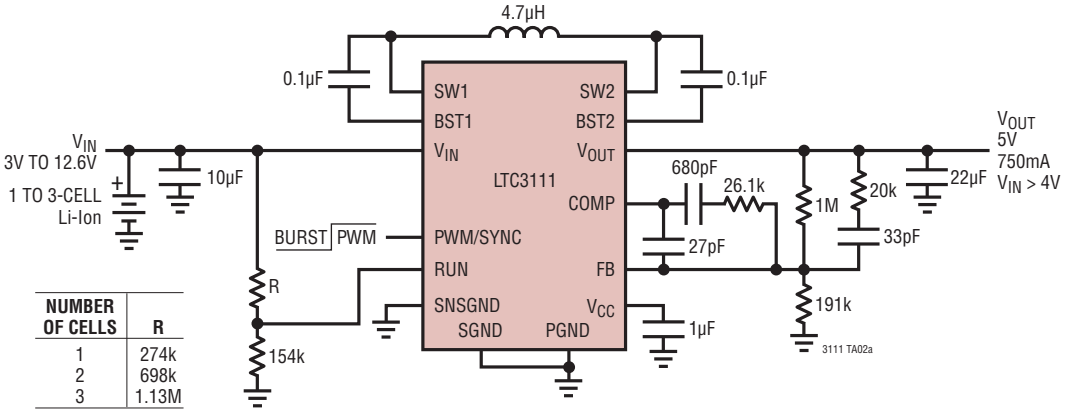


Figure 12: Complete Loop Bode Plot

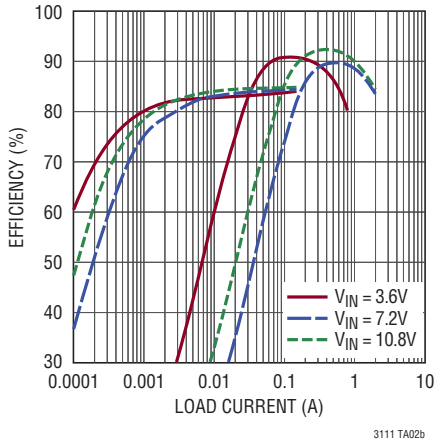
TYPICAL APPLICATIONS

1, 2, 3 Li-Ion to 5V



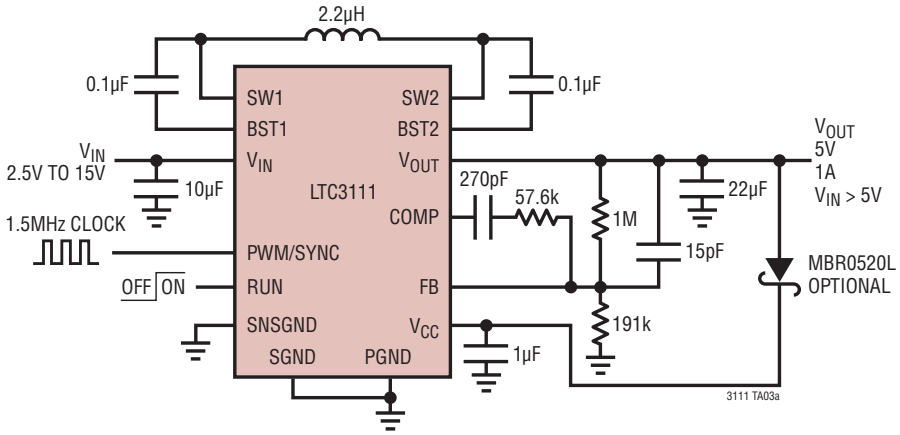
NUMBER OF CELLS	R
1	274k
2	698k
3	1.13M

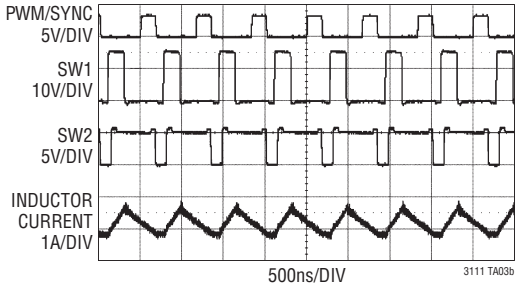
Wide V_{IN} to $5V_{OUT}$ Efficiency



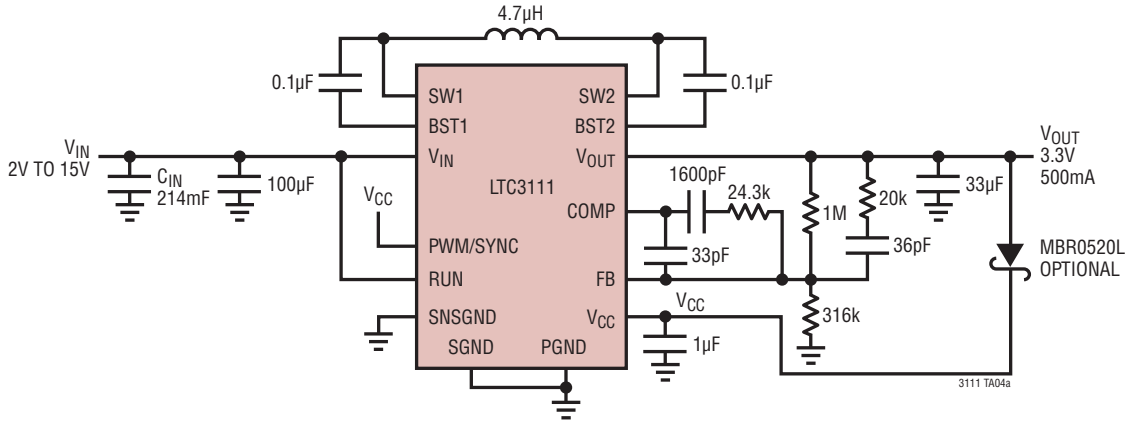
TYPICAL APPLICATIONS

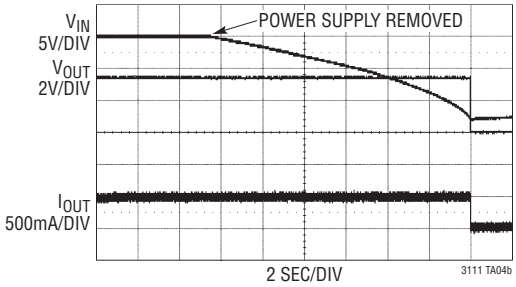
LTC3111 Synchronized to a 1.5MHz Clock, 5V/1A Output





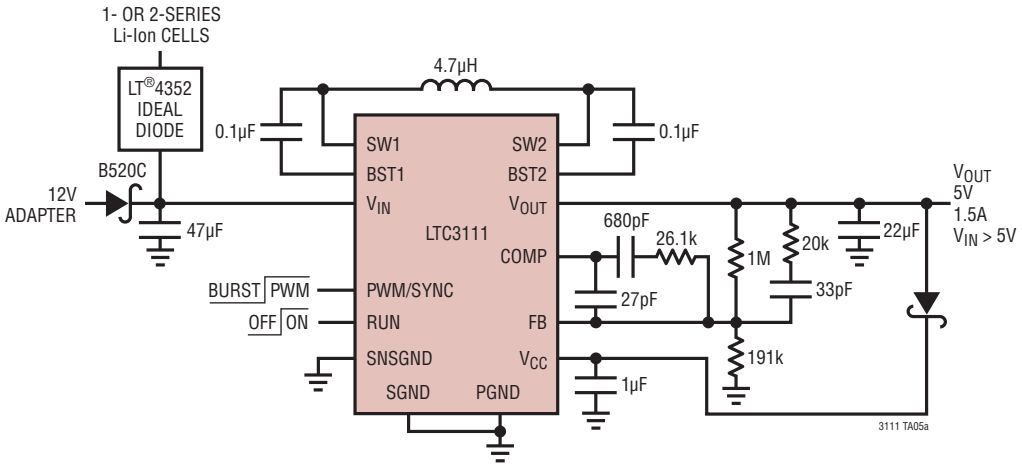
3.3V Backup from a High Voltage Capacitor Bank Runs Down to V_{IN} = 2V with 500mA Load

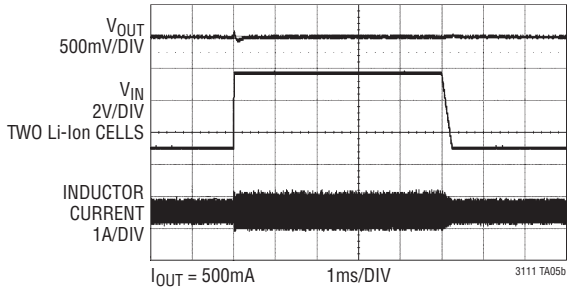




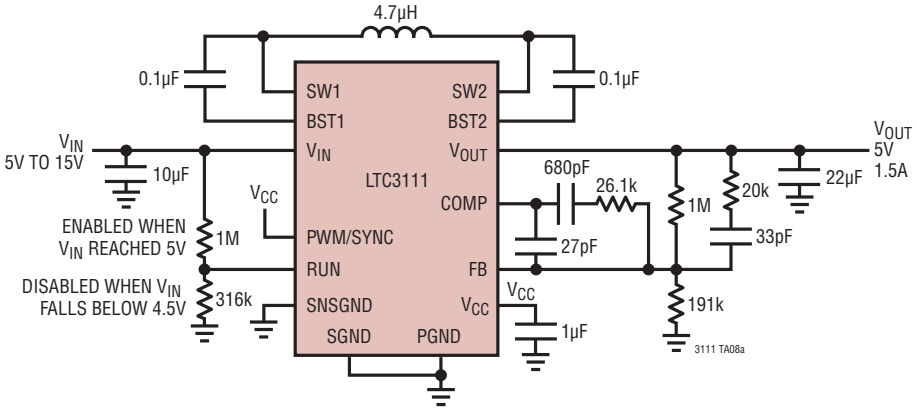
TYPICAL APPLICATIONS

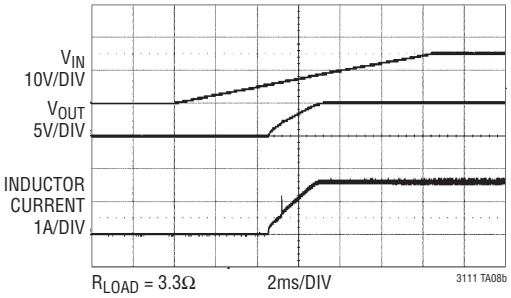
Stepped Response from 1 or 2 Li-Ion to 12V Adapter Source V_{OUT} = 5V

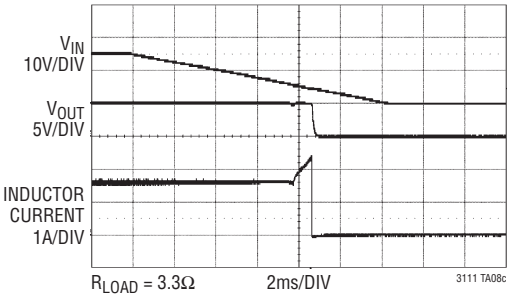




Custom Input Undervoltage Lockout Thresholds



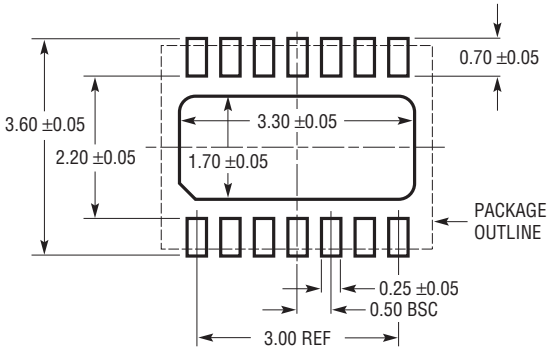




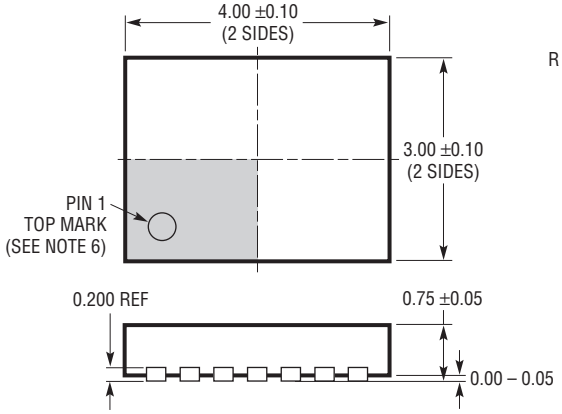
PACKAGE DESCRIPTION

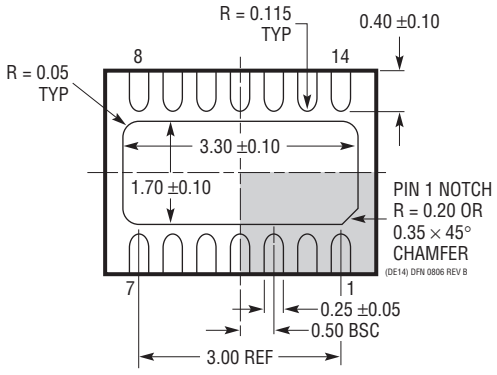
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





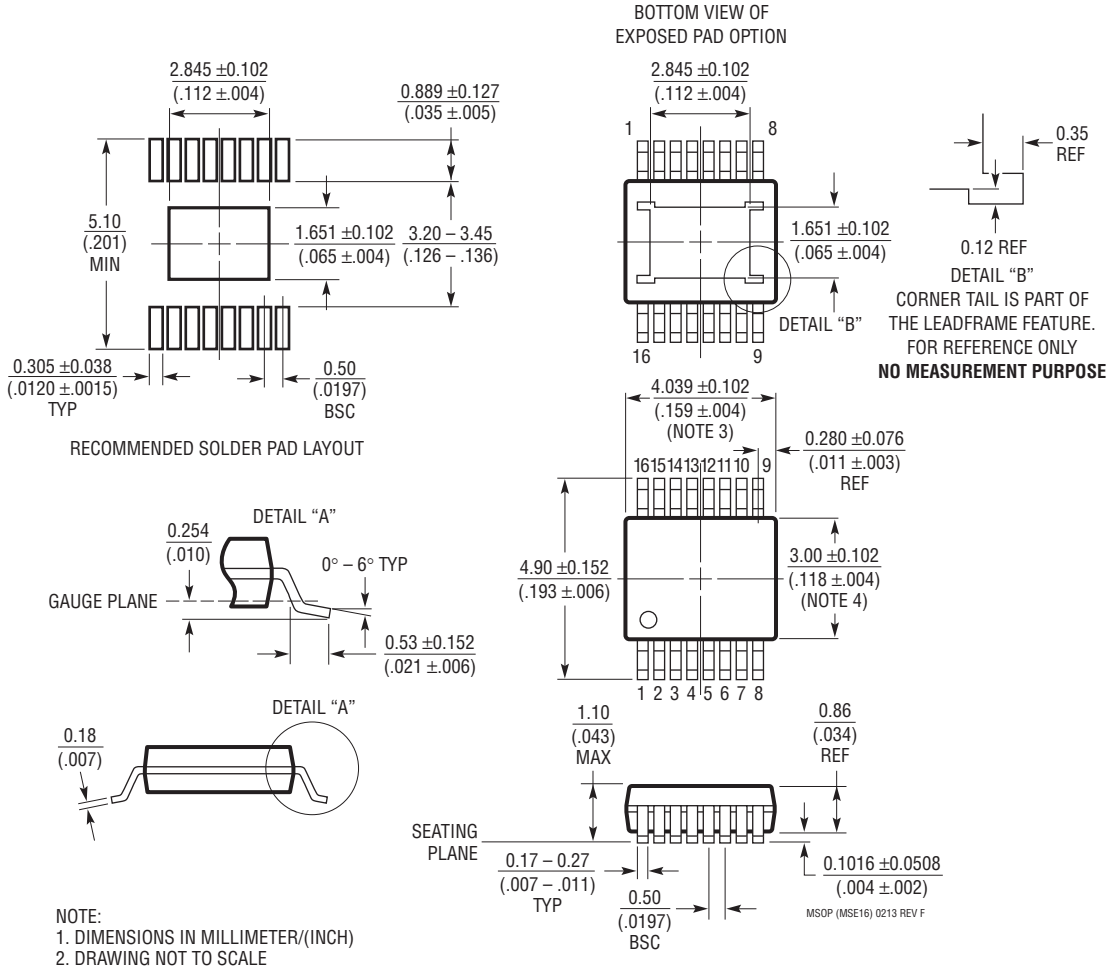
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/14	Clarified graphs	1, 4, 5, 6