18V, 2A Buck-Boost DC/DC Converter with Low Loss Dual Input PowerPath

FEATURES

- **Integrated High Efficiency Dual Input PowerPath™ Plus Buck-Boost DC/DC Converter**
- **Ideal Diode or Priority V_{IN} Select Modes**
- **V_{IN1} and V_{IN2} Range: 2.2V to 18V**
- **V_{OUT} Range: 2V to 18V**
- **Either V_{IN} Can Be Above, Below or Equal to V_{OUT}**
- **Generates 5V at 2A for V_{IN} > 6V**
- **1.2MHz Low Noise Fixed Frequency Operation**
- **Current Mode Control**
- All Internal N-Channel MOSFETs
- Pin-Selectable PWM or Burst Mode® Operation
- Accurate, Independent RUN Pin Thresholds
- Up to 94% Efficiency
- V_{IN} and V_{OUT} Power Good Indicators
- I_Q of 50µA in Sleep, 2µA in Shutdown
- 4mm × 5mm 24-Lead QFN or 28-Lead TSSOP Packages

APPLICATIONS

- Systems with Multiple Input Sources
- Back Up Power Systems
- Wall Adapter or Li-Ion(s) Input to 5V_{OUT}
- Battery or Super Capacitor Input for Reserve Power
- Replace Diode-OR Designs with Higher Efficiency, Flexibility and Performance

DESCRIPTION

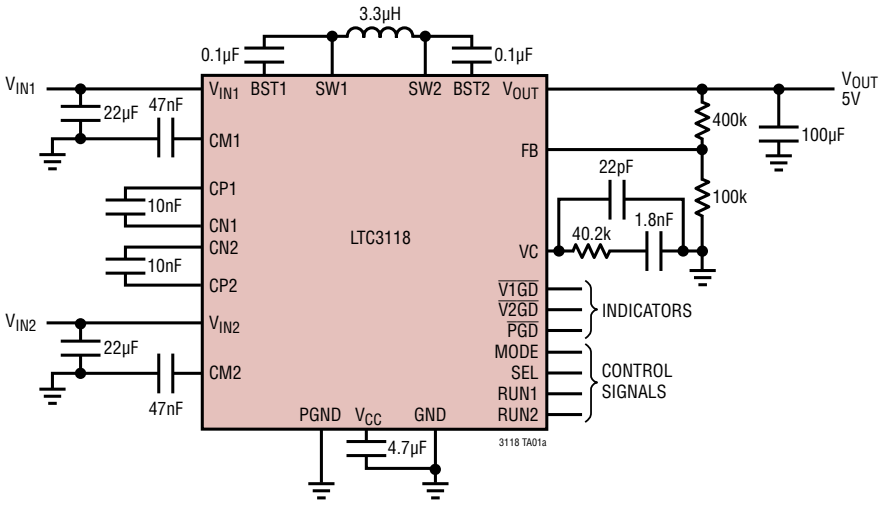
The LTC®3118 is a dual-input, wide voltage range synchronous buck-boost DC/DC converter with an intelligent, integrated, low loss PowerPath control. The unique power switch architecture provides efficient operation from either input source to a programmable output voltage above, below or equal to the input. Voltage capability of up to 18V provides flexibility and voltage margin for a wide variety of applications and power sources.

The LTC3118 uses a low noise, current mode architecture with a fixed 1.2MHz PWM mode frequency that minimizes the solution footprint. For high efficiency at light loads, automatic Burst Mode operation can be selected consuming only 50µA of quiescent current in sleep.

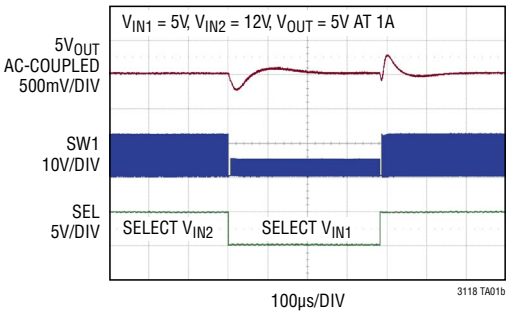
System level features include ideal diode or V_{IN} priority modes, V_{IN} and V_{OUT} power good indicators, accurate RUN comparators to program independent UVLO thresholds, and output disconnect in shutdown. Other features include 2µA shutdown current, short-circuit protection, soft-start, current limit and thermal overload protection.

The LTC3118 is offered in thermally enhanced 24-lead 4mm × 5mm QFN and 28-lead TSSOP packages.

TYPICAL APPLICATION



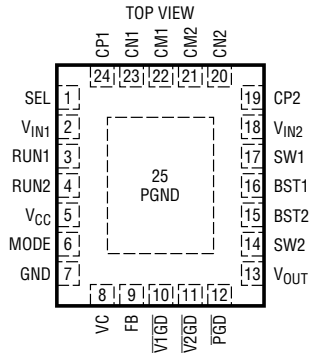
Input Switchover Response



ABSOLUTE MAXIMUM RATINGS (Note 1)

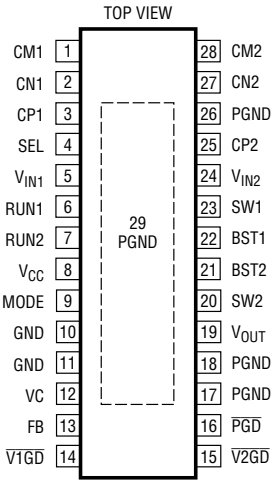
V_{IN1}, V_{IN2} Voltage ..... –0.3V to 20V
V_{OUT} Voltage ..... –0.3V to 20V
SW1 DC Voltage (Note 4) ..... –0.3V to (V_{IN1} + 0.3V) or (V_{IN2} + 0.3V)
SW2 DC Voltage (Note 4) ..... –0.3V to (V_{OUT} + 0.3V)
BST1 Voltage ..... (SW1 – 0.3V) to (SW1 + 6V)
BST2 Voltage ..... (SW2 – 0.3V) to (SW2 + 6V)
RUN1, RUN2 Voltage ..... –0.3V to 20V
$\overline{PGD}$, $\overline{V1GD}$, $\overline{V2GD}$ Voltage ..... –0.3V to 20V
CM1, CM2 Voltage ..... –0.3 to 20V
CP1 Voltage ..... (V_{IN1} – 0.3V) to (V_{IN1} + 6V)
CP2 Voltage ..... (V_{IN2} – 0.3V) to (V_{IN2} + 6V)
V_{CC}, CN1, CN2 Voltage ..... –0.3 to 6V
MODE, SEL, FB, VC Voltage ..... –0.3 to 6V
Operating Junction Temperature Range (Notes 2, 3)
LTC3118E/LTC3118I ..... –40°C to 125°C
LTC3118H ..... –40°C to 150°C
LTC3118MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) TSSOP ..... 300°C

PIN CONFIGURATION



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 3.4°C/W, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 25) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
28-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JC} = 5°C/W, θ_{JA} = 30°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3118EUFD#PBF	LTC3118EUFD#TRPBF	3118	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3118IUFD#PBF	LTC3118IUFD#TRPBF	3118	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3118HUFD#PBF	LTC3118HUFD#TRPBF	3118	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
LTC3118MPUFD#PBF	LTC3118MPUFD#TRPBF	3118	24-Lead (4mm × 5mm) Plastic QFN	–55°C to 150°C
LTC3118EFE#PBF	LTC3118EFE#TRPBF	3118FE	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3118IFE#PBF	LTC3118IFE#TRPBF	3118FE	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3118HFE#PBF	LTC3118HFE#TRPBF	3118FE	28-Lead Plastic TSSOP	–40°C to 150°C
LTC3118MPFE#PBF	LTC3118MPFE#TRPBF	3118FE	28-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_J \approx T_A = 25°C$ (Note 2). Unless otherwise noted, V_{IN1} or $V_{IN2} = 5V$, $V_{OUT} = 5V$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Operating Voltage Range	V_{IN1} or V_{IN2}, $V_{CC} \geq 2.5V$	●	2.2		18	V
Output Operating Voltage		●	2		18	V
Undervoltage Lockout Threshold on V_{CC}	V_{CC} Rising, $V_{IN} = 2.5V$	●	2.2	2.35	2.5	V
Minimum V_{IN} Start-Up Voltage	V_{CC} Powered from V_{IN1} or V_{IN2} ($I_{VCC} = 10mA$)	●	2.2	2.5	2.65	V
Input Quiescent Current in Shutdown	RUN1 and RUN2 < 0.2V			2		µA
Input Quiescent Current in Burst Mode Operation	Active V_{IN1} or V_{IN2}, FB = 1.2V			50		µA
	Inactive V_{IN1} or V_{IN2}, FB = 1.2V			5		µA
Input Quiescent Current in PWM Mode Operation	Active V_{IN1} or V_{IN2}, FB = 0.8V			12		mA
Output Quiescent Current in Burst Mode Operation				1		µA
Oscillator Frequency		●	1000	1200	1400	kHz
Oscillator Frequency Variation	Active V_{IN} = 3V to 18V			0.1		%/V
Feedback Voltage		●	0.98	1.0	1.02	V
Feedback Voltage Line Regulation	Active V_{IN} = 3V to 18V			0.2		%
Error Amplifier Transconductance	VC Current = ±4µA			80		µS
Feedback Pin Input Current	FB = 1V			0	50	nA
VC Source Current	VC = 0.5V, FB = 0.8V			–14		µA
VC Sink Current	VC = 0.5V, FB = 1.2V			14		µA
RUN Pin Threshold: Accurate	RUN1 or RUN2 Rising	●	1.17	1.22	1.27	V
RUN Pin Hysteresis: Accurate	Accurate RUN (Rising – Falling)			170		mV
RUN Pin Logic Threshold for V_{CC} Enable/Shutdown		●	0.2	0.65	1.15	V
RUN Pin Leakage Current	RUN1 or RUN2 = 4V				0.2	µA
V_{CC} Output Voltage	$I_{VCC} = 1mA$	●	3.5	3.8	4.1	V
V_{CC} Load Regulation	I_{VCC} = 1mA to 10mA			–1		%
V_{CC} Line Regulation	$I_{VCC} = 1mA$, V_{IN} = 5V to 18V			0.5		%
V_{CC} Current Limit	$V_{IN} > 6V$			60		mA
Average Inductor Current Limit (Note 5)		●	3.0	3.6	5.2	A
Overload Current Limit (Note 5)	Current from V_{IN1} or V_{IN2}			6		A
Reverse Inductor Current Limit (Note 5)	PWM Mode			–200		mA
Maximum Duty Cycle	Percentage of Period SW2 Is Low in Boost Mode	●	90	95		%
	Percentage of Period SW1 Is High in Boost Mode	●	83	88		%
Minimum Duty Cycle	Percentage of Period SW1 Is High in Buck Mode	●			0	%
SW1 and SW2 Forced Low Time	BST1 or BST2 Capacitor Charge Time			100		ns
N-Channel Switch Resistance	Switch A1 (From V_{IN1} to SW1)			80		mΩ
	Switch A2 (From V_{IN2} to SW1)			120		mΩ
	Switch B (From SW1 to PGND)			80		mΩ
	Switch C (From SW2 to PGND)			80		mΩ
	Switch D (From PV_{OUT} to SW2)			80		mΩ
N-Channel Switch Leakage	V_{IN2}, V_{IN2} or $V_{OUT} = 18V$			0.1	10	µA
Soft-Start Time				1		ms
MODE and SEL Threshold Voltage		●	0.3	0.75	1.2	V
MODE and SEL Leakage	Pin = 5V			0	0.5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_J \approx T_A = 25°C$ (Note 2). Unless otherwise noted, V_{IN1} or $V_{IN2} = 5V$, $V_{OUT} = 5V$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1} Becomes Active Input in Ideal Diode Mode	V_{IN2} = SEL = 5V Rising Falling		 5 4.2	 5.4 4.6	 5.8 5	 V V
$\overline{PGD}$ Threshold	Percent of FB Voltage Rising		90	94	98	%
$\overline{PGD}$ Hysteresis	Percent of FB Voltage Falling			–2		%
$\overline{V1GD}$, $\overline{V2GD}$, $\overline{PGD}$ Low Voltage	I_{SINK} = 5mA			300		mV
$\overline{V1GD}$, $\overline{V2GD}$, $\overline{PGD}$ Leakage	Pin = 18V				1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3118 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3112E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3118I is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature, the LTC3118H is guaranteed to meet specifications over the –40°C to 150°C operating junction temperature range and the LTC3118MP is guaranteed and tested to meet specifications over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for temperatures greater than 125°C.

The maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD in Watts) according to the following formula:
$T_J = T_A + (PD \bullet \theta_{JA})$ where θ_{JA} is the thermal impedance of the package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

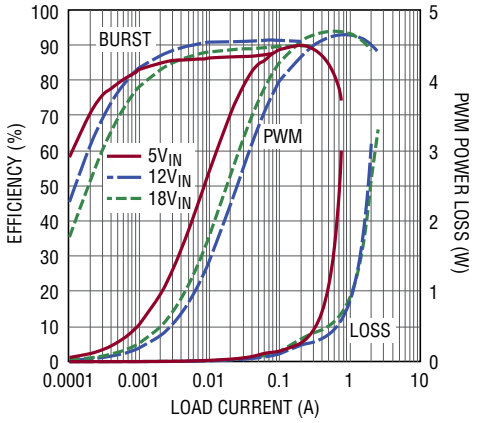
Note 4: Voltage transients on the switch pins beyond the DC limit specified in the Absolute Maximum Ratings, are non disruptive to normal operation when using good layout practices, as shown on the demo board or described in the data sheet and application notes.

Note 5: Current measurements are performed when the LTC3118 is not switching. The current limit values measured in operation will be somewhat higher, while the reverse current thresholds may be lower due to the propagation delay of the comparators and inductor value.

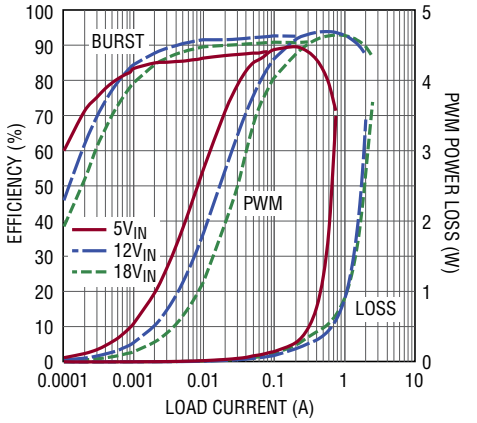
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

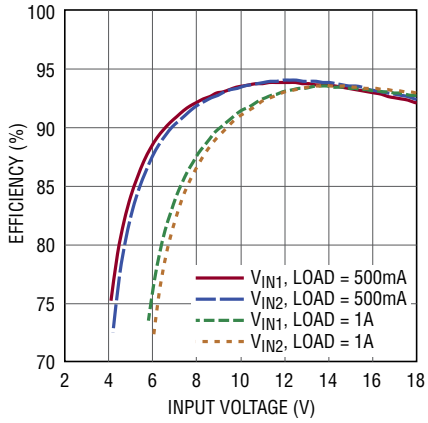
V_{OUT} = 12V, Efficiency and Power Loss vs Load Current from V_{IN1}



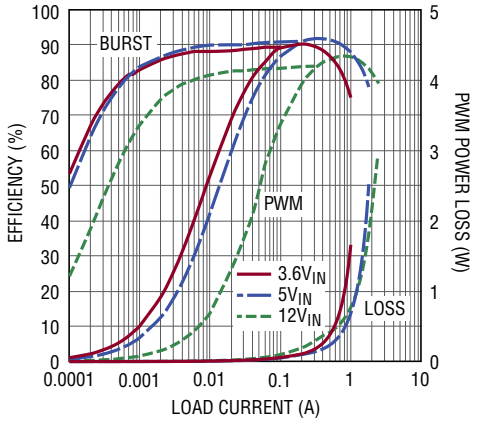
V_{OUT} = 12V, Efficiency and Power Loss vs Load Current from V_{IN2}



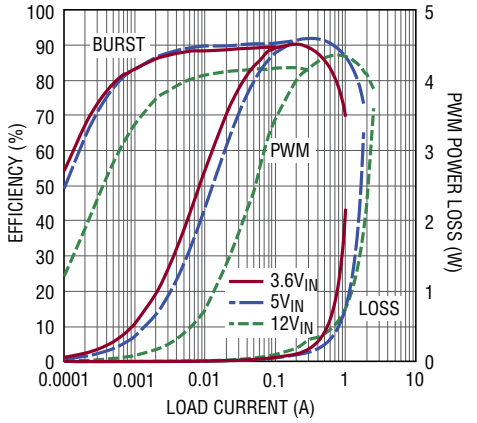
$12V_{OUT}$ Efficiency vs V_{IN1} or V_{IN2} Voltage with 500mA and 1A Load Current



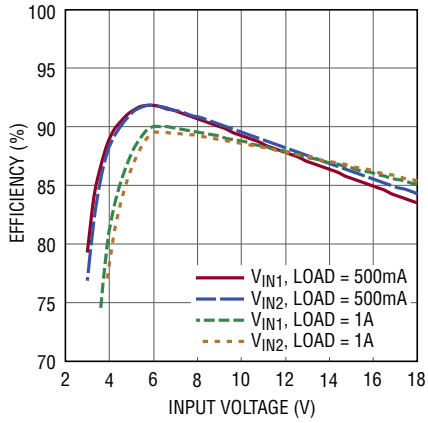
V_{OUT} = 5V, Efficiency and Power Loss vs Load Current from V_{IN1}



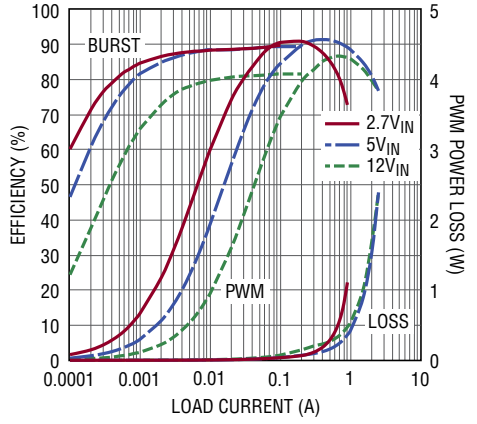
V_{OUT} = 5V, Efficiency and Power Loss vs Load Current from V_{IN2}



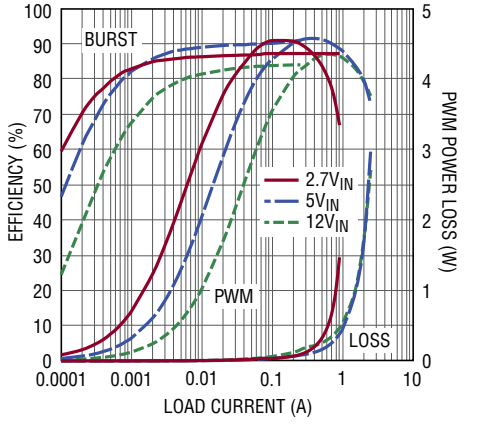
$5V_{OUT}$ Efficiency vs V_{IN1} or V_{IN2} Voltage with 500mA and 1A Load Current



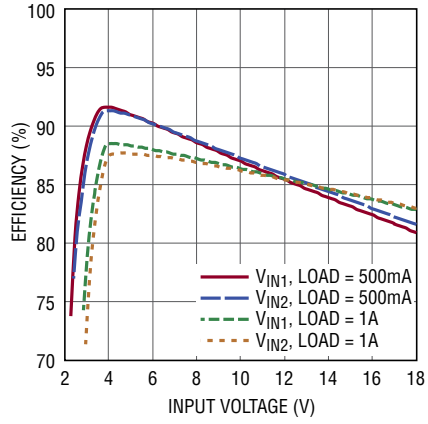
V_{OUT} = 3.3V Efficiency and Power Loss vs Load Current from V_{IN1}



V_{OUT} = 3.3V Efficiency and Power Loss vs Load Current from V_{IN2}

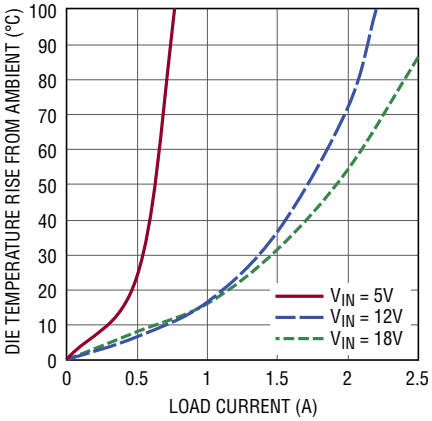


$3.3V_{OUT}$ Efficiency vs V_{IN1} or V_{IN2} Voltage with 500mA and 1A Load Current

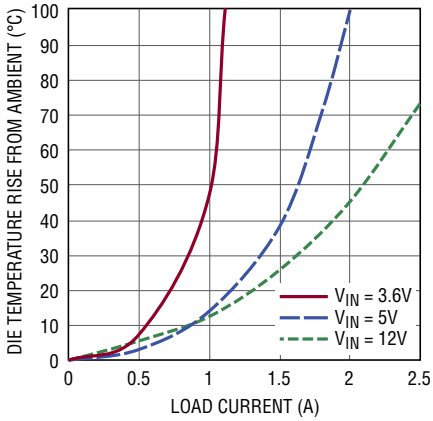


TYPICAL PERFORMANCE CHARACTERISTICS

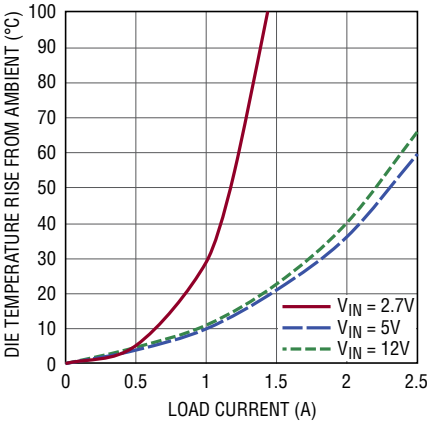
Die Temperature Rise vs Load Current, V_{OUT} = 12V, 4-Layer LTC3118 Demo Board



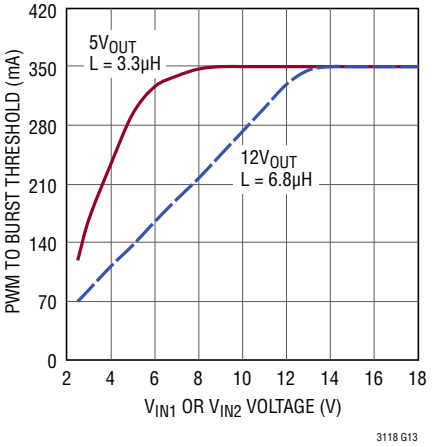
Die Temperature Rise vs Load Current, V_{OUT} = 5V, 4-Layer LTC3118 Demo Board



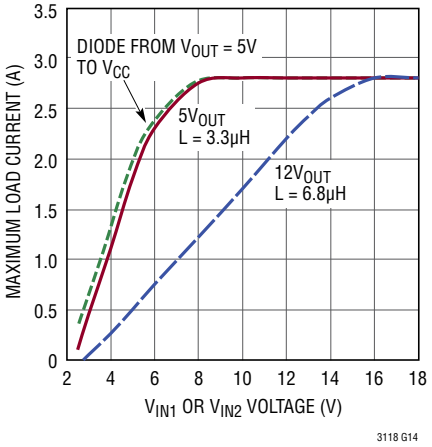
Die Temperature Rise vs Load Current, V_{OUT} = 3.3V, 4-Layer LTC3118 Demo Board



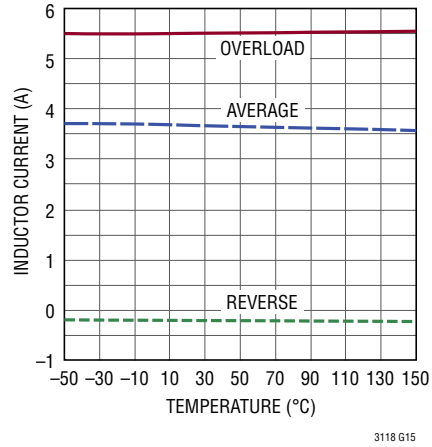
PWM to Burst Mode Thresholds vs V_{IN}



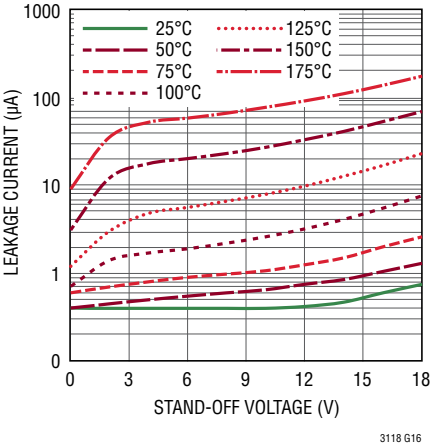
Maximum Load Current vs V_{IN} in PWM Mode



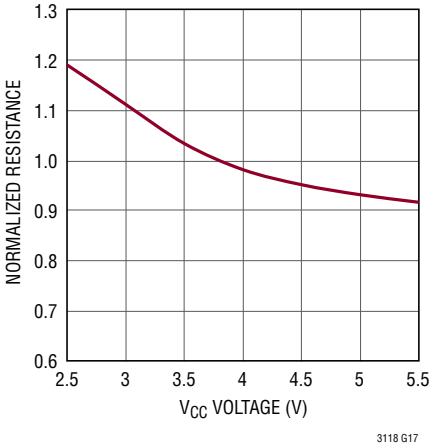
Inductor Overload, Average and Reverse Current Limits vs Temperature



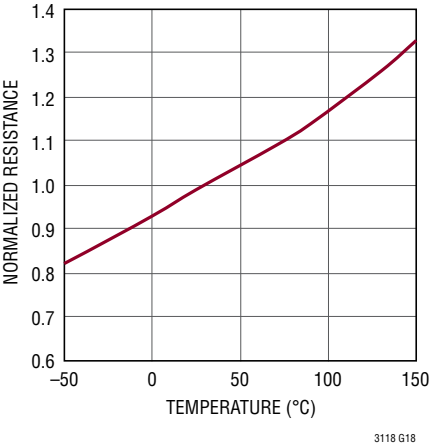
N-Channel MOSFET Leakage vs Die Temperature and Stand-Off Voltage



Normalized N-MOSFET Resistance vs V_{CC}

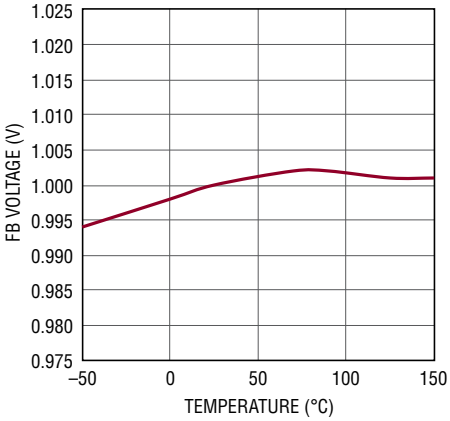


Normalized N-Channel MOSFET Resistance vs Die Temperature

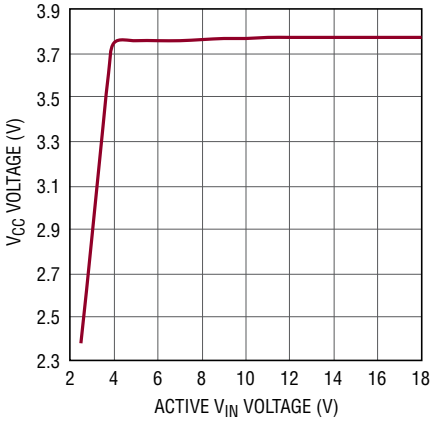


TYPICAL PERFORMANCE CHARACTERISTICS

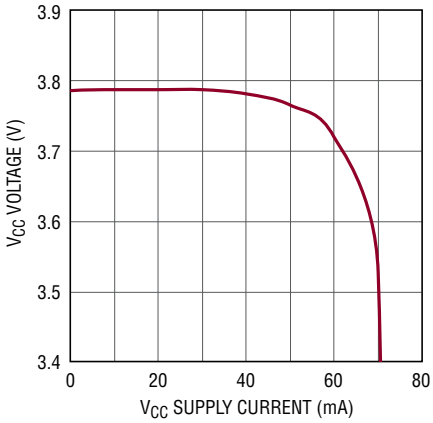
FB Program Voltage vs Temperature



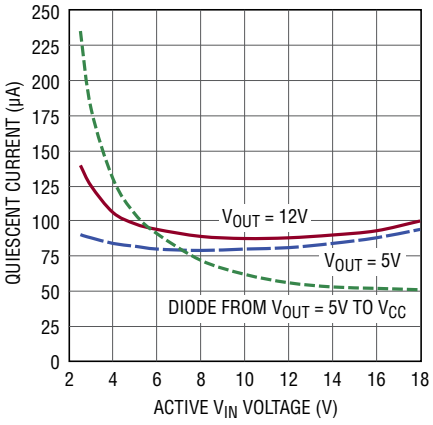
V_{CC} vs Active V_{IN}



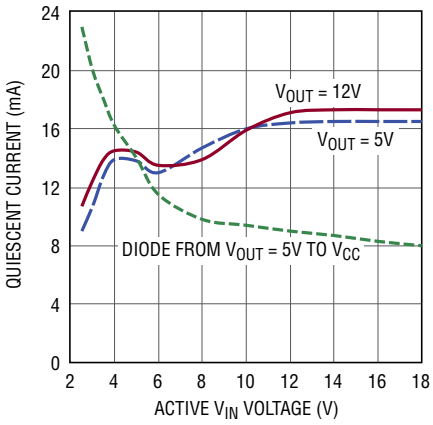
V_{CC} vs Supply Current (V_{IN} > 5V) Showing Current Limit



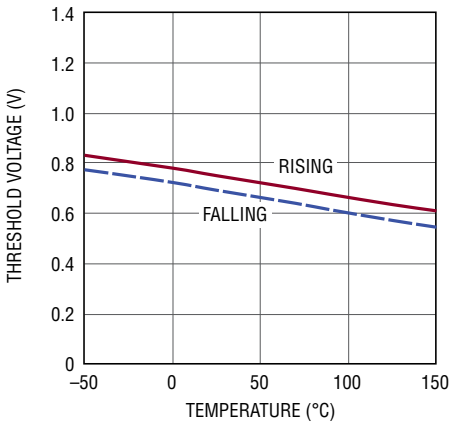
No-Load Active V_{IN} Current in Burst Mode



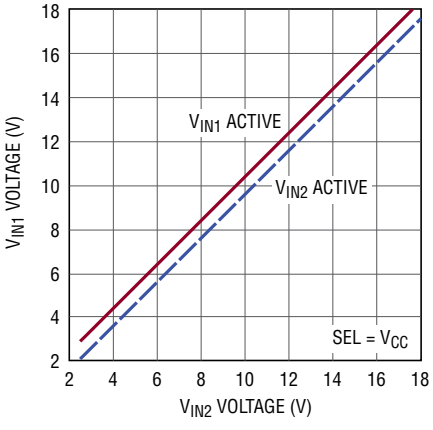
No-Load Active V_{IN} Current in PWM



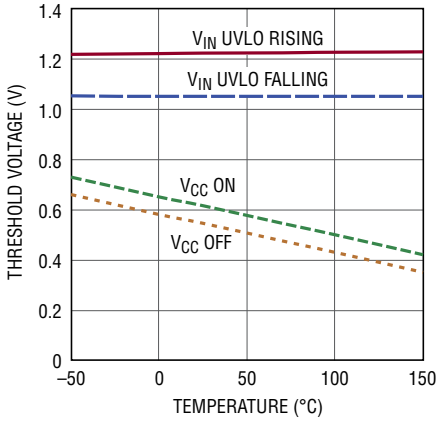
MODE and SEL Logic Thresholds



Active V_{IN} in Ideal Diode Mode with Hysteresis



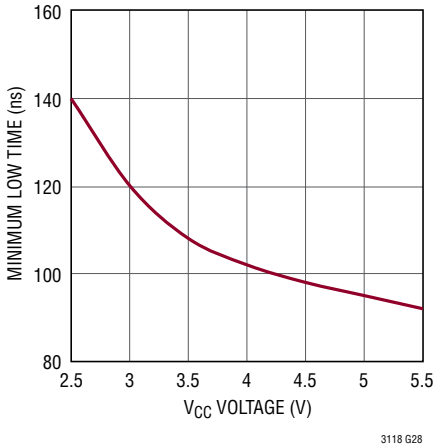
RUN1 and RUN2 Thresholds for V_{IN} UVLO and V_{CC} Enable



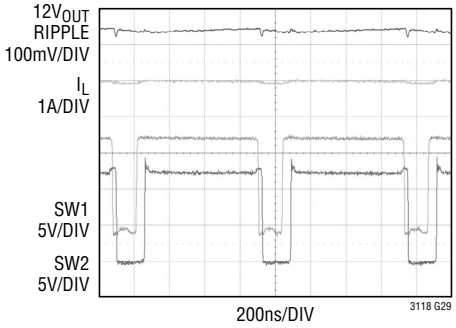
RUN1 and RUN2 Current vs Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

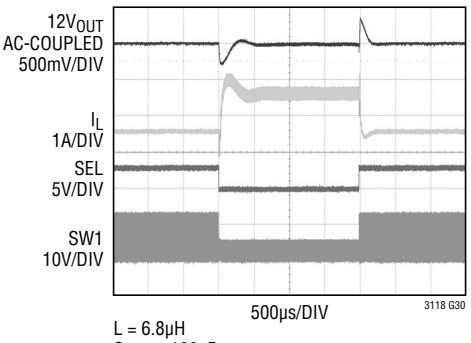
SW1, SW2 Minimum Low Time vs V_{CC}



Switch and V_{OUT} Waveforms ($12V_{IN}$, $12V_{OUT}$)

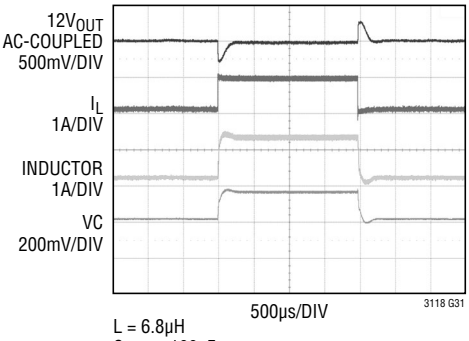


$12V_{IN2}$ to $5V_{IN1}$ Switchover Waveforms, V_{OUT} = 12V 500mA Load



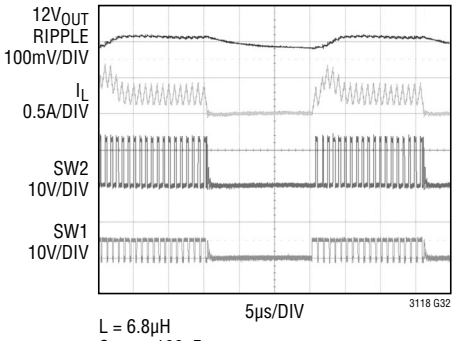
L = 6.8µH
C_{OUT} = 100µF

100mA to 1A Load Step PWM Mode ($12V_{IN}$, $12V_{OUT}$)



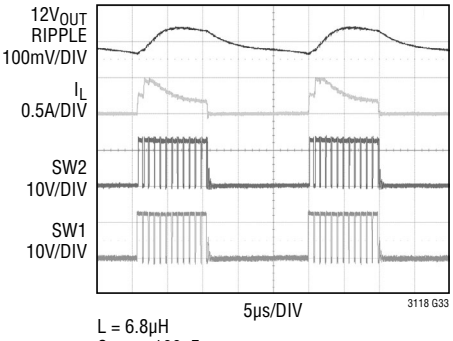
L = 6.8µH
C_{OUT} = 100µF

$5V_{IN}$ Burst Mode Waveforms $12V_{OUT}$, 50mA



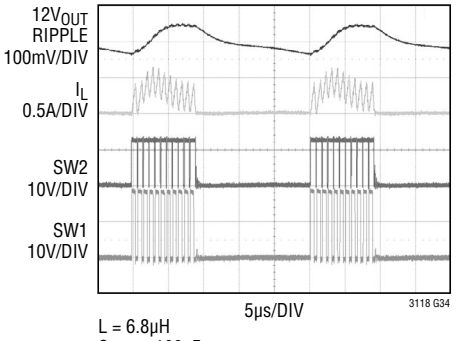
L = 6.8µH
C_{OUT} = 100µF

$12V_{IN}$ Burst Mode Waveforms $12V_{OUT}$, 100mA



L = 6.8µH
C_{OUT} = 100µF

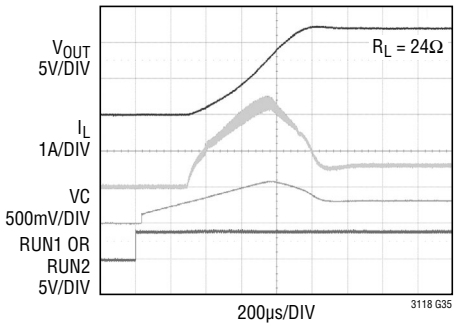
$18V_{IN}$ Burst Mode Waveforms $12V_{OUT}$, 100mA



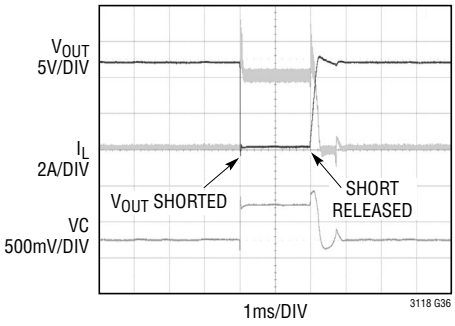
L = 6.8µH
C_{OUT} = 100µF

TYPICAL PERFORMANCE CHARACTERISTICS

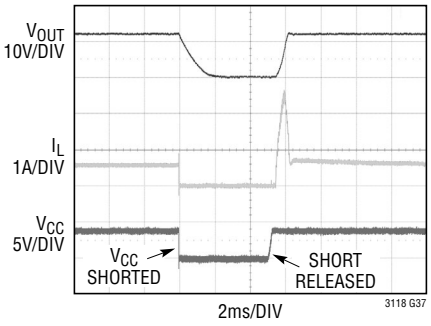
Soft-Start Waveforms with 500mA Load ($12V_{IN}$, $12V_{OUT}$)



V_{OUT} Short-Circuit Waveforms Response and Recovery ($12V_{IN}$, $12V_{OUT}$)



V_{CC} Short-Circuit Waveforms Response and Recovery ($12V_{IN}$, $12V_{OUT}$, 500mA Load)



PIN FUNCTIONS (QFN/TSSOP)

SEL (Pin 1/Pin 4): Input Select Pin.

SEL = Logic Low (ground): V_{IN1} priority mode, the converter will operate from V_{IN1} if RUN1 and V_{IN1} voltages are above their respective thresholds. If these conditions are not met, the converter will operate from V_{IN2} as long as RUN2 and V_{IN2} voltages are above their thresholds.

SEL = Logic High (connect to V_{CC}): Ideal diode mode, the converter will operate from the higher voltage of V_{IN1} or V_{IN2}.

V_{IN1} (Pin 2/Pin 5): The first input voltage source for the converter. Connect a minimum of 22µF ceramic decoupling capacitor from this pin to ground, as close to the IC as possible. In ideal diode mode (SEL = 1), this input will be selected if $V_{IN1} > V_{IN2}$, V_{IN1} is above its internal UVLO threshold, and RUN1 > 1.22V. In priority mode (SEL = 0), this input will be selected if V_{IN1} is above its internal UVLO threshold and RUN1 > 1.22V.

Since this input has lower $R_{DS(ON)}$ MOSFETs between V_{IN1} and SW1, it should be considered for use with the source where high efficiency is more critical.

RUN1 (Pin 3/Pin 6): Input to enable and disable the IC and program the UVLO threshold for V_{IN1}. Pull RUN1 above 1.22V to enable the converter. Connecting this pin to a resistor divider from V_{IN1} to ground allows programming of V_{IN1}'s UVLO threshold above 2.2V. Pulling both RUN1 and RUN2 to logic low states will put the IC in a low current shutdown state.

RUN2 (Pin 4/Pin 7): Input to enable and disable the IC and program the UVLO threshold for V_{IN2}. Pull RUN2 above 1.22V to enable the converter. Connecting this pin to a resistor divider from V_{IN2} to ground allows programming of V_{IN2}'s UVLO threshold above 2.2V. Pulling both RUN1 and RUN2 to logic low states will put the IC in a low current shutdown state.

V_{CC} (Pin 5/Pin 8): Output voltage of the internal V_{CC} regulator. This is the supply pin for the internal driver circuitry. Bypass this output with a 4.7µF ceramic capacitor. This pin may be back driven by an external supply, up to 5.5V. V_{CC} will be generated from either V_{IN1} or V_{IN2} depending upon which input the converter is operating from.

MODE (Pin 6/Pin 9): PWM or Auto Burst Mode Select Pin.

MODE = Logic Low (ground): Enables automatic Burst Mode operation.

MODE = Logic High (connect to V_{CC}): Forces PWM mode operation.

GND (Pin 7/Pins 10, 11): Signal Ground for the IC. Provide a short direct PCB path from this pin to the ground plane.

VC (Pin 8/Pin 12): Output of the voltage error amplifier used to program average inductor current. An RC from this pin to ground sets the voltage loop compensation. The average current loop is internally compensated.

FB (Pin 9/Pin 13): Feedback input to the voltage error amplifier. Connect to a resistor divider from V_{OUT} to ground. The output voltage can be adjusted from 2V to 18V by: $V_{OUT} = 1 + (R1/R2)$.

$\overline{V1GD}$ (Pin 10/Pin 14): Open-drain indicator that pulls to ground when both V_{IN1} and RUN1 are above their respective thresholds. Connect a pull-up resistor from this pin to a positive supply.

$\overline{V2GD}$ (Pin 11/Pin 15): Open-drain indicator that pulls to ground when both V_{IN2} and RUN2 are above their respective thresholds. Connect a pull-up resistor from this pin to a positive supply.

$\overline{PGD}$ (Pin 12/Pin 16): Open-drain output that pulls to ground when V_{OUT} is greater than 92% of the programmed output voltage. Connect a pull-up resistor from this pin to a positive supply.

V_{OUT} (Pin 13/Pin 19): Regulated Output Voltage. Connect a minimum of 47µF ceramic or low ESR decoupling capacitor from this pin to ground. The capacitor should be placed as close to the IC as possible with short, wide traces to V_{OUT} and GND.

SW2 (Pin 14/Pin 20): Switch Pin. Connect to the other side of the inductor. Keep PCB trace lengths as short and wide as possible to reduce EMI.

BST2 (Pin 15/Pin 21): Bootstrapped floating supply for high side N-channel MOSFET gate drive. Connect to SW2 through a 0.1µF capacitor, as close to the part as possible.

PIN FUNCTIONS (QFN/TSSOP)

BST1 (Pin 16/Pin 22): Bootstrapped floating supply for high side N-channel MOSFET gate drive for V_{IN1} or V_{IN2}. Connect to SW1 through a 0.1µF capacitor, as close to the part as possible. This capacitor provides gate drive for the N-channel MOSFETs connected between SW1 and either V_{IN1} or V_{IN2}.

SW1 (Pin 17/Pin 23): Switch Pin. Connect to one side of the inductor. Keep PCB trace lengths as short and wide as possible to reduce EMI.

V_{IN2} (Pin 18/Pin 24): The second input voltage source for the converter. Connect a minimum of 22µF ceramic decoupling capacitor from this pin to ground, as close to the IC as possible. In ideal diode mode (SEL = 1), this input will be selected if $V_{IN2} > V_{IN1}$, V_{IN2} is above its internal UVLO threshold, and RUN2 > 1.22V. In priority mode (SEL = 0), this input will only be selected if V_{IN1} is below its internal UVLO threshold or RUN1 < 1.05V.

Since this input has the higher $R_{DS(ON)}$ MOSFETs between V_{IN2} and SW1, it should be considered for use with the source where slightly lower conversion efficiency is acceptable.

CP2 (Pin 19/Pin 25): Positive pin for the V_{IN2} top N-channel MOSFET charge-pump capacitor. This pin toggles between V_{IN2} and $V_{IN2} + V_{CC}$ when V_{IN2} is active.

CN2 (Pin 20/Pin 27): Negative pin for the V_{IN2} top N-channel MOSFET charge-pump capacitor. This pin is driven between V_{CC} and GND when V_{IN2} is active. Connect a 10nF ceramic capacitor between CN2 and CP2. This pin can be monitored to indicate operation from V_{IN2}.

CM2 (Pin 21/Pin 28): Filter pin for the common connection of V_{IN2} to SW1 N-channel MOSFETs. Connect a 47nF capacitor from this pin to the ground plane.

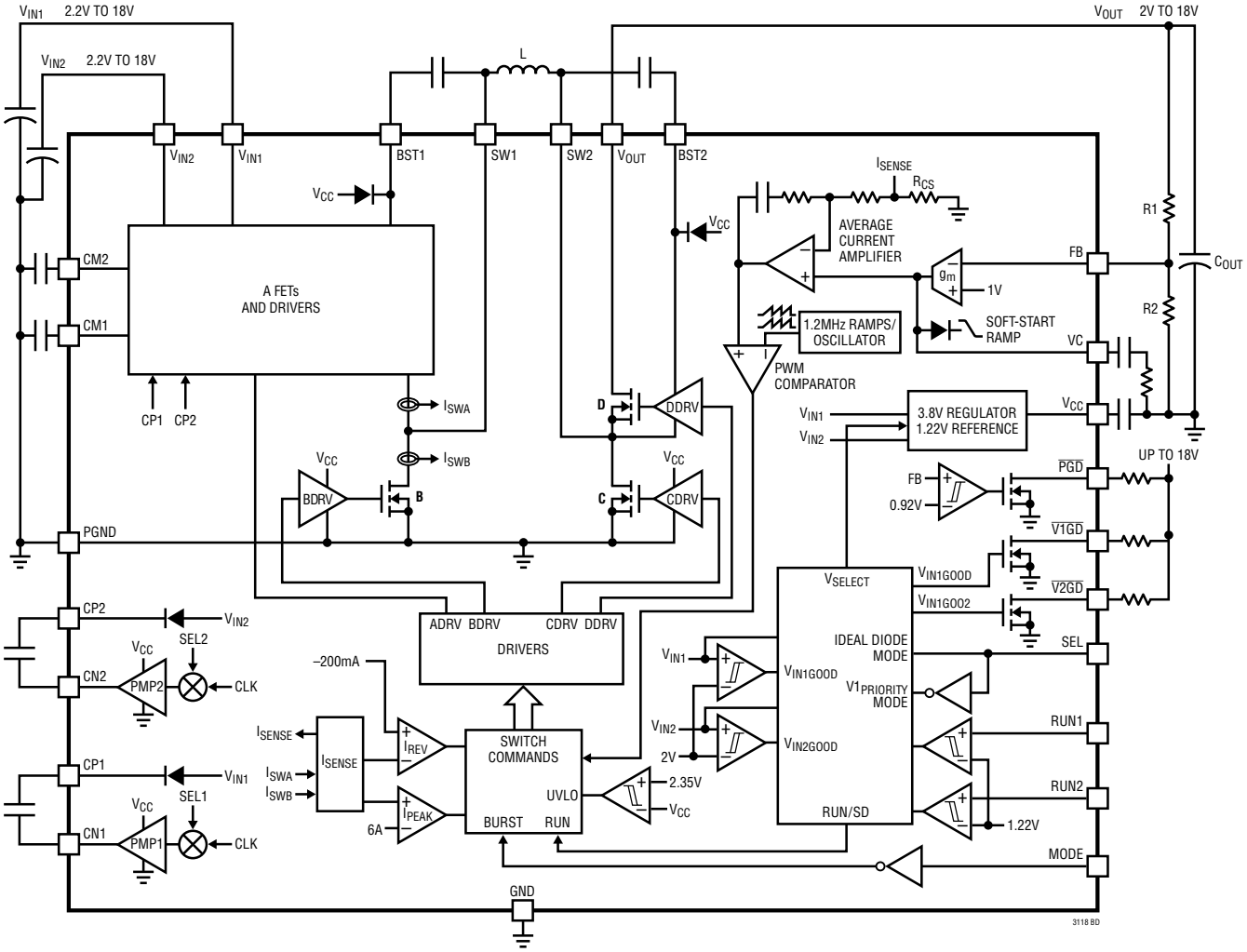
CM1 (Pin 22/Pin 1): Filter pin for the common connection of V_{IN1} to SW1 N-channel MOSFETs. Connect a 47nF capacitor from this pin to the ground plane.

CN1 (Pin 23/Pin 2): Negative pin for the V_{IN1} top N-channel MOSFET charge-pump capacitor. This pin is driven between V_{CC} and GND when V_{IN1} is active. Connect a 10nF ceramic capacitor between CN1 and CP1. This pin can be monitored to indicate operation from V_{IN1}.

CP1 (Pin 24/Pin 3): Positive pin for the V_{IN1} top N-channel MOSFET charge-pump capacitor. This pin toggles between V_{IN1} and $V_{IN1} + V_{CC}$ when V_{IN1} is active.

PGND (Exposed Pad Pin 25/Pins 17, 18, 26, Exposed Pad Pin 29): Power Ground for the IC. **The exposed pad must be soldered to the PCB ground plane.** It serves as the power ground connection, and as a means of conducting heat away from the die.

BLOCK DIAGRAM



OPERATION

Introduction

The LTC3118 is a dual-input, current mode, monolithic buck-boost DC/DC converter that can operate over a wide input voltage range of 2.2V to 18V. The output voltage can be programmed between 2V to 18V and deliver more than 2A of load current. The LTC3118 operates from either V_{IN1} or V_{IN2} depending on the state of the SEL pin. If SEL is commanded to be a logic high, V_{OUT} will be powered from the highest valid input voltage. If SEL is a logic low, V_{OUT} will be powered from V_{IN1} (priority mode) assuming sufficient input voltage is present. Internal, low $R_{DS(ON)}$ N-channel power switches reduce the solution complexity and maximize efficiency.

A proprietary switch algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between the step-up or step-down operating modes are seamless and free of transients and subharmonic switching, making this product ideal for noise sensitive applications. The LTC3118 operates at a fixed nominal switching frequency of 1.2MHz, which provides an ideal trade-off between small solution size and high efficiency. Current mode control provides inherent input line voltage rejection, simplified compensation and rapid response to load transients. Burst Mode operation capability is also included in the LTC3118 and is user-selected via the MODE input pin. In Burst Mode operation, the LTC3118 provides exceptional efficiency at light output loads by operating the converter only when necessary to maintain voltage regulation. At higher loads, the LTC3118 automatically transitions to fixed frequency PWM mode when Burst Mode operation is selected.

For 5V V_{OUT} applications, the input quiescent currents in Burst Mode operation can be reduced with the internal LDO regulator bootstrapped to the output voltage. If the application requires extremely low noise, continuous PWM operation can also be selected via the MODE pin. The LTC3118 also features accurate, resistor programmable RUN comparator thresholds with hysteresis for each V_{IN}. This allows the buck-boost DC/DC converter to turn on and off at user-selected voltage thresholds depending on the power source for each V_{IN}. With a wide voltage range and high efficiency, the LTC3118 is well suited for many demanding power systems.

Power Stage Topology

Figure 1 shows the topology of the dual-input LTC3118 power stage switches and their associated gate drivers. The LTC3118 integrates independent switch paths from V_{IN1} to SW1 and V_{IN2} to SW1 to provide isolation between the selected input and the inactive input. This configuration allows conversion from either input source, regardless of their respective voltage levels, enabling ideal diode or V_{IN1} priority modes (see SEL pin description).

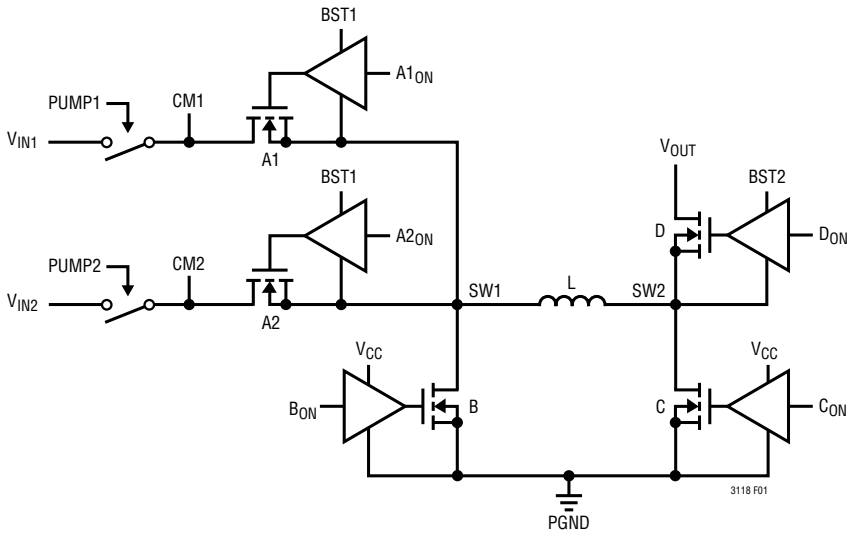


Figure 1. LTC3118 Dual-Input Power Stage

OPERATION

If operation from V_{IN1} is selected, PUMP1 connects the low R_{DSON} static switch between V_{IN1} and CM1 as shown. Switch A1 is then driven on for a portion of each switching cycle, as commanded by the PWM circuitry and powered by the flying capacitor between BST1 and SW1. When operating from V_{IN1}, PUMP2 and A2 are disabled.

Operation from V_{IN2} is accomplished in a similar manner, except that PUMP2 connects V_{IN2} to CM2 and A2 is commanded on by the PWM. With operation from V_{IN2}, PUMP1 and A1 are disabled providing isolation from V_{IN1}.

PWM Mode Operation

If the MODE pin is high, or if the load current on the converter is high enough to force PWM mode operation, the LTC3118 operates at a fixed 1.2MHz frequency using a current mode control loop. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability and lower output voltage ripple. In PWM mode operation, both SW1 and SW2 transition on every cycle independent of the input and output voltages. In response to the internal control loop command, an internal pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

When stepping down from a high input voltage to a lower output voltage, the converter operates in buck mode and switch D remains on for the entire switching cycle except for a minimum SW2 low duration (typically 100ns). During the switch low duration, switch C is turned on which forces SW2 low and charges the flying capacitor between BST2 and SW2. This ensures that the switch D gate driver power supply rail on BST2 is maintained. The duty cycle of switch A1 (or A2) and switch B are adjusted by the PWM circuit to maintain output voltage regulation in buck mode.

If the input voltage is lower than the output voltage, the converter operates in boost mode. Switch A1 (or A2) remains on for the entire switching cycle except for the minimum switch low duration (typically 100ns). During the switch low duration, switch B is turned on which forces SW1 low and charges the flying capacitor between BST1 and SW1. This ensures that switch A1 (or A2) gate driver power supply rail on BST1 is maintained. The duty cycle of switch C and switch D are adjusted by the PWM circuit to maintain output voltage regulation in boost mode.

Oscillator

The LTC3118 operates from an internal oscillator with a nominal fixed frequency of 1.2MHz. This allows the DC/DC converter efficiency to be maximized while still using small external components.

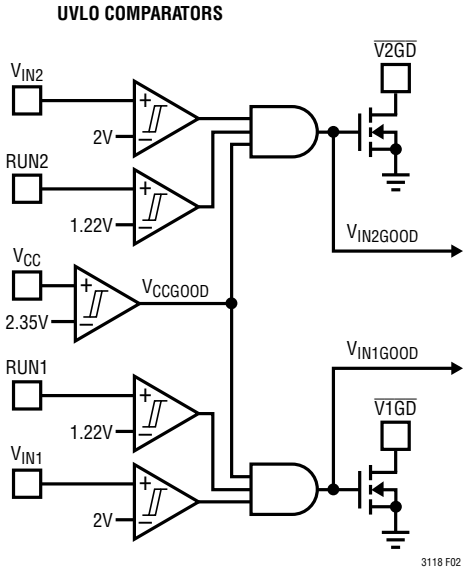
Input Select Logic and V_{IN} Power Good Indicators

A simplified schematic diagram of the LTC3118's input select circuitry is shown in Figure 2. UVLO comparators on V_{IN1}, V_{IN2} and V_{CC} set minimum operating voltages to ensure proper operation. V_{CC} must be greater than 2.35V before operation is allowed from either input. Once V_{CC} is valid, one of the inputs must be greater than 2V typical before the LTC3118 enables switching. Finally, the RUN pin voltage for the particular input must be greater than 1.22V to enable operation. This condition will be met if the appropriate RUN pin is connected to its own V_{IN}, RUN1 to V_{IN1} for example, but may not be met if a resistor divider is used to program the accurate RUN pin higher than the V_{IN} UVLO minimum. Detailed discussions of V_{CC}, V_{IN} and RUN pin UVLOs are presented in later sections.

Once the UVLO conditions are satisfied, internal $V_{IN1GOOD}$ and/or $V_{IN2GOOD}$ will assert and the LTC3118 is allowed to operate. The state of each V_{INGOOD} signal and the SEL pin are decoded in logic to determine which input source is selected, as shown on the table in Figure 2.

Open-drain indicator pins $\overline{V1GD}$ and $\overline{V2GD}$ are driven by their respective internal V_{INGOOD} signals and can be used to alert the system of undervoltage conditions on the inputs. External pull-up resistors can be connected between these pins and any supply voltage up to 18V. Since these pins pull low with valid input voltages, even in Burst Mode operation, high value resistors are recommended for applications where minimal no-load quiescent current is critical.

OPERATION



INPUT VOLTAGE SELECT LOGIC			
SEL PIN	**$V_{IN1GOOD}$**	**$V_{IN2GOOD}$**	**SELECTED V_{IN}**
1 IDEAL DIODE MODE	1	1	Highest V_{IN}
	1	0	V_{IN1}
	0	1	V_{IN2}
	0	0	No Switching
0 PRIORITY MODE	1	1	V_{IN1}
	1	0	V_{IN1}
	0	1	V_{IN2}
	0	0	No Switching

Figure 2. Simplified Input Select Logic and V_{IN} Power Good Indicators

If SEL is a logic low, the LTC3118 operates in V_{IN1} priority mode where V_{IN1} is selected for operation if conditions are met for $V_{IN1GOOD}$ to be high. If $V_{IN1GOOD}$ is low in priority mode, the LTC3118 will revert to V_{IN2} operation if $V_{IN2(GOOD)}$ is asserted, keeping V_{OUT} powered.

If SEL is a logic high, the LTC3118 operates in ideal diode mode, where V_{OUT} is powered from the highest input voltage source with a high V_{INGOOD} signal. An internal comparator with 400mV hysteresis monitors the input voltages to determine which is higher. If the state of this comparator changes during PWM operation, switching will be suspended for six clock cycles before resuming from the other input source. An approximate 250µs filter/time constant prevents rapid transitions between inputs.

As with priority mode, if one of the V_{INGOOD} signals is low the LTC3118 will operate from the other input in order to keep the output powered. If both V_{INGOOD} signals are low in either mode, the LTC3118 will not deliver power to V_{OUT}.

V_{OUT} Power Good Indicator

The V_{OUT} power good indicator is an open-drain output pin similar to the $\overline{V1GD}$ and $\overline{V2GD}$ pins shown in Figure 2. $\overline{PGD}$ is driven by an internal comparator that monitors the FB pin. If FB is below 0.92V (V_{OUT} is 8% low) $\overline{PGD}$ will open circuit, allowing an external resistor to pull high indicating the output voltage is not in regulation. The power good comparator has internal filtering for glitch suppression.

OPERATION

Current Mode Control

The LTC3118 utilizes average current mode control for the pulse width modulator, as shown in Figure 3. Current mode control, both average and the better known peak method, enjoy some benefits compared to other control methods, including: simplified loop compensation, rapid response to load transients and inherent line voltage rejection.

Referring to Figure 3, an internal high gain transconductance error amplifier, labeled V_{AMP}, monitors V_{OUT} through a voltage divider connected to the FB pin and provides an output, VC, used by the current mode control loop to command the appropriate inductor current level. To ensure stability, external frequency compensation components (R_Z, C_{P1} and C_{P2}) must be installed between VC and GND. The procedure for determining these components is provided in the Applications Information section of this data sheet. VC is internally connected to the noninverting input of a high gain, integrating, operational amplifier, referred to in Figure 3 as I_{AMP}. The inverting input of the average current amplifier is connected to the inductor current sense resistor R_{CS} through a gain-setting resistor R_{A1} and to its output (I_{COMP}) through an internal frequency compensation network comprised of R_{A2} and C_A. The average current amplifier's output provides the cycle-by-cycle duty cycle command into the buck-boost PWM circuitry.

The non-inverting reference level input to the average current amplifier is VC and the feedback or inverting input is driven from the inductor current sensing circuitry. The inductor current sensing circuitry alternately measures the current through switches A1 (or A2) and B. The output of the sensing circuitry produces a voltage across resistor R_{CS} that resembles the inductor current waveform transformed to a voltage. If there is an increase in the power converter load on V_{OUT}, the instantaneous level of V_{OUT} will drop slightly, which will increase the voltage level on VC by the inverting action of the voltage error amplifier. When the increase on VC first occurs, the output of the current averaging amplifier, I_{COMP}, will increase momentarily to command a larger duty cycle. This duty cycle increase will result in a higher inductor current level, ultimately raising the average voltage across R_{CS}. Once the average

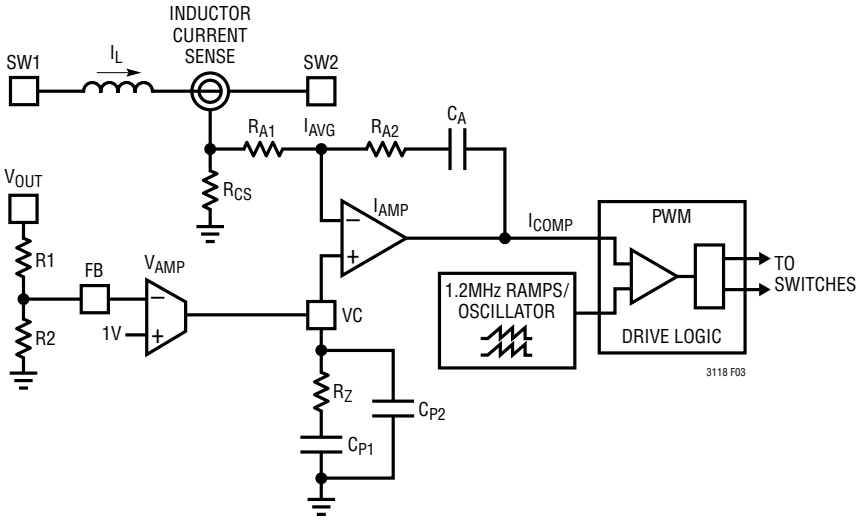


Figure 3. Average Current Mode Control Loop

OPERATION

value of the voltage on R_{CS} is equivalent to the VC level, the voltage on I_{COMP} will revert very closely to its previous level into the PWM, and force the correct duty cycle to maintain voltage regulation at this new higher inductor current level. The average current amplifier is configured as an integrator, so in steady state, the average value of the voltage applied to its inverting input (voltage across R_{CS}) will be equivalent to the voltage on its noninverting input VC. As a result, the average value of the inductor current is controlled in order to maintain voltage regulation. The entire current amplifier and PWM can be simplified as a voltage controlled current source, with the driving voltage coming from VC. VC is commonly referred to as the current command for this reason, and the voltage on VC is directly proportional to average inductor current, which can prove useful for many applications.

The voltage error amplifier monitors V_{OUT} through a voltage divider and makes adjustments to the current command as necessary to maintain regulation. The voltage error amplifier therefore controls the outer voltage regulation loop. The average current amplifier makes adjustments to the inductor current as directed by the voltage error amplifier output via VC and is commonly referred to as the inner current loop amplifier. The average current mode control technique is similar to peak current mode control except that the average current amplifier, by virtue of its configuration as an integrator, controls average current instead of the peak current. This difference eliminates the peak-to-average current error inherent to peak current mode control, while maintaining most of the advantages inherent to peak current mode control.

Average current mode control requires appropriate compensation for the inner current loop, unlike peak current mode control. The compensation network must have high DC gain to minimize V_{OUT} regulation errors and high bandwidth to quickly change the commanded current level following transient load steps. The inner loop compensation components are fixed internally on the LTC3118. External compensation of the voltage loop is detailed in the Applications Information section and is similar to techniques used for peak current mode control.

Inductor Current Sense and Maximum Output Current

As part of the current control loop, the LTC3118 has current sense circuitry that measures the inductor current of the buck-boost converter, as shown in Figure 3. This circuitry measures the current through switches A1 (or A2) and B separately and produces proportional output currents that are summed at the current sense resistor R_{CS}. Sensed A and B switch currents form a voltage replica of the inductor current at R_{CS}, which is used by the average current amplifier, as described in the previous section.

The voltage amplifier output, VC, is internally clamped to a nominal value of 1V. Since the average inductor current is proportional to VC, the 1V clamp sets the maximum average inductor current that can be programmed by the inner current loop. Taking into account the current sense amplifier's gain, and the value of R_{CS}, the maximum average inductor current is 3.6A typical. In buck mode, the output current is approximately equal to the inductor current I_L.

$$I_{OUT(BUCK)} \approx I_L \bullet 0.85$$

The 100ns SW1/SW2 forced low time on each switching cycle briefly disconnects the inductor from V_{OUT} and V_{IN}, resulting in slightly less output current in either buck or boost mode for a given inductor current. In boost mode, the output current is related to average inductor current and duty cycle by:

$$I_{OUT(BOOST)} \approx I_L \bullet (1 - D)$$

where D is the converter duty cycle.

Since the output current in boost mode is reduced by the duty cycle (D), the output current rating in buck mode is always greater than in boost mode. Also, because boost mode operation requires a higher inductor current for a given output current compared to buck mode, the efficiency in boost mode will be lower due to higher conduction ($I_L^2 \bullet R_{DS(ON)}$) losses in the power switches. This will further reduce the output current capability in boost mode. In either operating mode, however, the inductor peak-to-peak ripple current does not play a major role in determining the output current capability.

OPERATION

The maximum load current capability in PWM mode curves in the Typical Performance Characteristics section show the relationship of input voltage and the ability to deliver load current at V_{OUT} = 5V and 12V. When the input voltage is a volt or more above V_{OUT} in buck mode, the LTC3118 is capable of providing more than 2A of load current. In boost mode, the output current capability is further reduced by the boost ratio or duty cycle (D) as described in the preceding equation.

Overload Current Limit and Reverse Current Comparators

The internal current sense waveforms are used by the peak overload current (I_{PEAK}) and reverse current (I_{REV}) comparators. The I_{PEAK} current comparator monitors I_{SENSE} and interrupts normal PWM operation if the inductor current level exceeds its maximum internal threshold. This threshold is approximately 60% above the maximum average current level of the current control loop. If the internal current sense waveform rises above this level, the LTC3118 will disconnect the inductor from V_{IN} by shutting off switch A1 (or A2) to prevent higher current in the inductor. The I_{PEAK} circuitry is reset by the oscillator clock at the end of each switching cycle. In the event that the overload comparator is tripped as the result of an output short-circuit condition, where V_{OUT} is discharged below approximately 1V, the LTC3118 will initiate a soft-start event keeping the on-chip power dissipation to low levels. Once the short circuit is removed, the LTC3118 will restart in the normal fashion. If the average current loop is able to prevent inductor current from reaching I_{PEAK} during a short-circuit event, soft-start will not be initiated, but the maximum current capability of the current loop will be reduced by 40% to reduce power dissipation.

The LTC3118 contains a reverse current comparator set to a nominal value of –200mA. If the internal current sense waveform transitions below the internally set reverse current threshold, the LTC3118 will disconnect the inductor from V_{OUT} by shutting off switch D, to prevent rapid discharge of the output capacitor. The I_{REV} circuitry is reset by the oscillator clock at the end of the switching cycle.

Burst Mode Operation

When the MODE pin is held low, the LTC3118 is configured for automatic Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with normal continuous PWM switching above a predetermined average inductor current and will automatically transition to power saving Burst Mode operation below this level. Refer to the Typical Performance Characteristics section of this data sheet to determine the Burst Mode transition threshold for various combinations of V_{IN} and V_{OUT}.

With MODE held low at light output loads, the LTC3118 will go into a standby or sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all nonessential functions of the IC, significantly reducing the quiescent current of the LTC3118. This greatly improves overall power conversion efficiency when the output load is light. Since the converter does not operate in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, the LTC3118 will wake up and resume normal PWM switching operation until the voltage on V_{OUT} is restored to the previous level. If the load is very light, the LTC3118 may only need to switch for a few cycles to restore V_{OUT}, and may sleep for extended periods of time, significantly improving conversion efficiency.

OPERATION

Soft-Start

The LTC3118 soft-start circuit minimizes inrush current and output voltage overshoot on initial power up. The required timing components for soft-start are internal to the LTC3118 and produce typical soft-start durations of approximately 1ms. The internal soft-start circuit slowly ramps the error amplifier output at VC. In doing so, the current command of the IC is slowly increased, starting from zero. After initial power-up, soft-start can be reset by UVLO on V_{CC}, both $V_{IN1GOOD}$ and $V_{IN2GOOD}$ de-asserting, thermal shutdown, or a V_{OUT} short circuit.

V_{CC} Regulator

An internal low dropout regulator (LDO) generates a nominal 3.8V rail from the active input V_{IN1} or V_{IN2}. The V_{CC} rail powers the internal control circuitry and power device gate drivers of the LTC3118, including the BST pin capacitors. The V_{CC} regulator is disabled in shutdown to reduce quiescent current and is enabled by forcing one RUN pin above its logic threshold. The V_{CC} regulator includes current-limit protection to safeguard against accidental short-circuiting of the LDO rail. In 5V V_{OUT} applications, V_{CC} can be powered by V_{OUT} through an external Schottky diode. This technique is commonly referred to as bootstrapping. Bootstrapping can provide a significant efficiency improvement, particularly when the active V_{IN} is high, and also allows operation to the minimum rated input voltage of 2V. For more information see Bootstrapping the V_{CC} Regulator with 5V V_{OUT} or External Supply, in the Applications Information section.

Undervoltage Lockouts

The LTC3118 undervoltage lockout (UVLO) circuits disable operation of the internal power switches if both V_{IN1} and V_{IN2} or the V_{CC} voltages are below their respective UVLO thresholds (see Figure 2). There are three UVLO circuits, one for each V_{IN} and another that monitors V_{CC}. The V_{IN} UVLO comparators have a falling voltage threshold of 1.8V (typical at room temperature). If both input voltages fall below this level, switching is disabled until one V_{IN} rises above 2V, as long as V_{CC} is above its UVLO threshold. The V_{CC} UVLO has a falling voltage threshold of 2.2V (typical). If V_{CC} falls below this threshold, IC operation is disabled until V_{CC} rises above 2.35V as long as one V_{IN} is above its UVLO threshold level.

Depending on the particular application, any of these UVLO thresholds could be the limiting factor affecting the minimum input voltage required for operation. The LTC3118 V_{CC} regulator uses V_{IN1} or V_{IN2} for its power input, whichever is active (see the Input Select Logic and V_{IN} Power Good Indicators section). If V_{CC} is not bootstrapped, there exists a voltage drop between the active V_{IN} and V_{CC}. The dropout voltage is proportional to the loading on V_{CC} due to the gate charge to the internal power switches. The Typical Performance Characteristics section of this data sheet provides information on the dropout voltage between V_{IN1} (or V_{IN2}) and V_{CC}.

In applications where V_{CC} is bootstrapped (powered by V_{OUT} through a Schottky diode or auxiliary power rail), the minimum input voltage for operation (after start-up) will be limited only by the V_{IN} UVLO thresholds (1.8V typical). **Please note: If the bootstrap voltage is derived from the LTC3118 V_{OUT} and not an independent power rail, then the minimum input voltages required for *initial start-up* are still limited by the minimum V_{CC} voltage (2.35V typical).**

OPERATION

RUN1 and RUN2 Pin Comparators

Forcing both RUN1 and RUN2 to a logic low places the LTC3118 in a low current shutdown state. When the voltage on either pin is brought above a 0.65V logic threshold, certain IC functions are enabled as shown in Figure 4a. The RUN1 and RUN2 pins also include accurate internal comparators that allow them to be used to set custom rising and falling ON/OFF thresholds for V_{IN1} and V_{IN2}, respectively, with the addition of external resistor dividers. If either RUN pin voltage is increased to exceed its accurate comparator threshold (1.22V nominal), all functions of the buck-boost converter will be enabled and switching will commence, assuming the respective V_{IN} and V_{CC} UVLO circuits are cleared (see Figure 2).

If both RUN1 and RUN2 are brought below the accurate comparator threshold, the buck-boost converter will inhibit switching, but the V_{CC} regulator and control circuitry will remain powered unless both RUN pins are brought below the logic threshold. Therefore, in order to completely shut down the IC and reduce the V_{IN} currents to < 2µA (typical), it is necessary to ensure that both RUN pins are brought below the worst-case low logic threshold of 0.2V. RUN1 and RUN2 are high voltage capable inputs but must be connected to their respective V_{IN1} and V_{IN2} supplies **through a high value resistor greater than 200k to prevent a potential latch condition at the pin.** The RUN pins can be driven above V_{IN} or V_{OUT} within their specified voltage ratings. If either RUN pin is forced above 5V, it will sink a small current, as given by the following equation:

$$I_{RUN} \approx \frac{V_{RUN} - 5V}{3M\Omega}$$

With the addition of optional resistor divider(s), as shown in Figure 4a, the RUN pin(s) can be used to establish a user-programmable turn-on and turn-off threshold.

The buck-boost converter is enabled when the voltage on either RUN pin reaches 1.22V. Therefore, the turn-on voltage threshold on V_{IN} is given by:

$$V_{TURNON} = 1.22V\left(1+\frac{R_T}{R_B}\right)$$

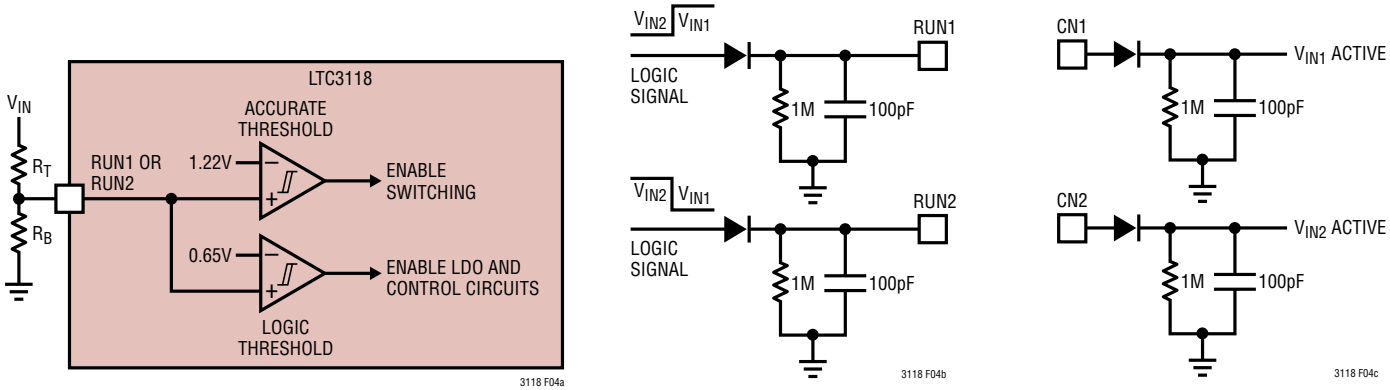


Figure 4. (a) Accurate RUN1 or RUN2 Pin Comparators, (b) Manual V_{IN} Select with Overlap Timing, (c) Active V_{IN} Indicators

OPERATION

The RUN comparators include a built-in hysteresis of approximately 170mV, so that the turn-off threshold will be approximately 15% lower than the turn-on threshold. Put another way, the internal threshold levels for the RUN comparators to disable switching from a particular input is 1.05V.

$$V_{TURNOFF} = 1.05V\left(1+\frac{R_T}{R_B}\right)$$

The RUN comparator is relatively noise insensitive, but there may be cases due to PCB layout, very large value resistors for R_T and R_B (Figure 4a), or proximity to noisy components where noise pickup is unavoidable and may cause the turn-on or turn-off levels to be intermittent. In these cases, a small value filter capacitor can be added across R_B to ensure proper operation.

Selecting Priority or Ideal Diode Mode Operation

Priority Mode (SEL=0)

Priority mode operation is suggested for most applications, since powering from one of the sources is typically preferred. In priority mode, the primary input is connected to V_{IN1} and the auxiliary input is connected to V_{IN2}. The LTC3118 will maintain operation from V_{IN1} until either the RUN1 or minimum V_{IN1} UVLO circuits transition the LTC3118 to V_{IN2} operation if valid. **It is important that the RUN1 turn-off threshold programs the minimum V_{IN1} above 2.5V in Priority Mode** unless V_{CC} is back-fed and held above 2.5V. This prevents an unintended soft-start cycle from occurring if V_{CC} hits its UVLO threshold when the V_{IN1} source is removed, before transitioning to V_{IN2} operation.

Depending on the maximum load current of the application, the RUN1 and RUN2 minimum V_{IN} turn-off thresholds may need to set well above 2.5V to prevent V_{OUT} from losing regulation, especially in step-up mode. Please refer to Maximum Load Current vs V_{IN} curves found in the Typical Performance Characteristics. Maximum load current capability when V_{IN1} or V_{IN2} is less than 3.8V can be improved if V_{CC} is boot-strapped to 5V as shown in Figure 7.

Ideal Diode Mode (SEL=1)

Ideal Diode mode operation is available on the LTC3118 for systems with low ESR sources or where the programmed operating range of the two inputs can be separated as will be discussed. In Ideal Diode mode, an internal comparator monitors the voltage on both V_{IN1} and V_{IN2} to determine which input is higher. The comparator has approximately 800mV of hysteresis to help prevent the part from switching between the two inputs if the source voltages are equal. The comparator has an approximate 250µs filter delay to prevent rapid switching between inputs and erratic operation. When the LTC3118 switches between inputs, current supplied from one source is suspended before transitioning to the other source. Depending on the impedance of each source and the amount of input current required to support the load on V_{OUT}, it is possible for the voltage ripple on one or both inputs to exceed this comparator's hysteresis.

As an example, if both input sources have 300mΩ of impedance and 2A of current is being drawn from the active source, a 600mV step will occur on the inputs during switchover, approaching the comparator's 800mV of typical hysteresis. When the input voltages are equal, the LTC3118 could toggle between V_{IN1} and V_{IN2} operation at high load currents. For such systems, operation in Priority mode is recommended, unless the RUN pins can be programmed such that the minimum operating voltage of one input is set above the maximum source voltage of the other input. As with priority mode, the minimum V_{IN} operating voltages should be set by their RUN pins above V_{CC} UVLO and higher if needed to support maximum load current. Low ESR 100µF to 220µF aluminum electrolytic capacitors close to both input pins help to reduce resonant ringing during V_{IN} switchover, due to cable inductances found in some applications and bench evaluation set-ups.

OPERATION

Manual V_{IN} Select Circuits

The SEL pin can be used to manually switch between V_{IN1} and V_{IN2}, if V_{IN2} is connected to a voltage greater than V_{IN1}. In this case, both RUN pins must remain asserted above their 1.22V thresholds. The LTC3118 will run off V_{IN1} when SEL is low and the higher V_{IN2} source when SEL is high.

For systems requiring manual V_{IN} selection where the relative voltages are unknown, the RUN pins can be used with a few precautions. Each RUN pin contains internal filtering to reduce the chance of unintended turn-on or turn-off due to noise events. The turn-on delay is typically 50µs in order to manage inductive ringing during supply plug in. Accordingly, a >100µs overlap time of asserted RUN1 and RUN2 signals is recommended to prevent a momentary shutdown of the IC and a subsequent soft-start cycle.

If this overlap timing cannot be provided by the system micro-controller, an external circuit similar to Figure 4b can be added to each RUN pin. With the added circuit, V_{IN1} and V_{IN2} can be driven alternately off and on as shown. The diode provides a faster turn-on path, where the RC delay to GND is set to ~100µs in order to prevent V_{OUT} from drooping during switch-over.

Active V_{IN} Indicator

The $\overline{V1GD}$ and $\overline{V2GD}$ indicators can be monitored to determine if V_{IN1} or V_{IN2} have sufficient voltage based on internal UVLO circuits and the RUN pin divider networks as previously discussed. Some applications may require an additional indication of which V_{IN} is active and which is inactive. This indication can be implemented with the CN1 and CN2 charge-pump pins and an external circuit similar to Figure 4c. The diode and RC network provide peak detection and filtering of the active CN pin which is switching in PWM mode and held high in sleep. The CN pin for the inactive V_{IN} is held low.

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Thermal Considerations

The power switches of the LTC3118 are designed to operate continuously with currents up to the internal current limit thresholds. However, when operating at high current levels, there may be significant heat generated within the IC. In addition, the V_{CC} regulator can generate a significant amount of heat when the active V_{IN} is high. This adds to the total power dissipation of the IC. As described elsewhere in this data sheet, bootstrapping of V_{CC} for 5V output applications can essentially eliminate this power dissipation term and significantly improve efficiency.

Careful consideration must be given to the thermal environment of the IC in order to provide a means to remove heat from the IC and ensure that the LTC3118 is able to provide its full rated output current. Specifically, the exposed die attach pad of both the QFN and FE packages must be soldered to a copper layer on the PCB to maximize the conduction of heat out of the IC package. This can be accomplished by utilizing multiple vias from the die attach pad connection underneath the IC package to other PCB layer(s) containing large copper planes. A recommended board layout incorporating these concepts is shown in Figure 5. Typical temperature rise versus load current curves using the PCB in Figure 5 are given in the Typical Performance Characteristics section.

If the IC die temperature exceeds approximately 165°C, thermal shutdown will be invoked and all switching will be inhibited. The part will remain disabled until the die temperature cools by approximately 10°C, at which time a soft-start is initiated to provide a smooth recovery.

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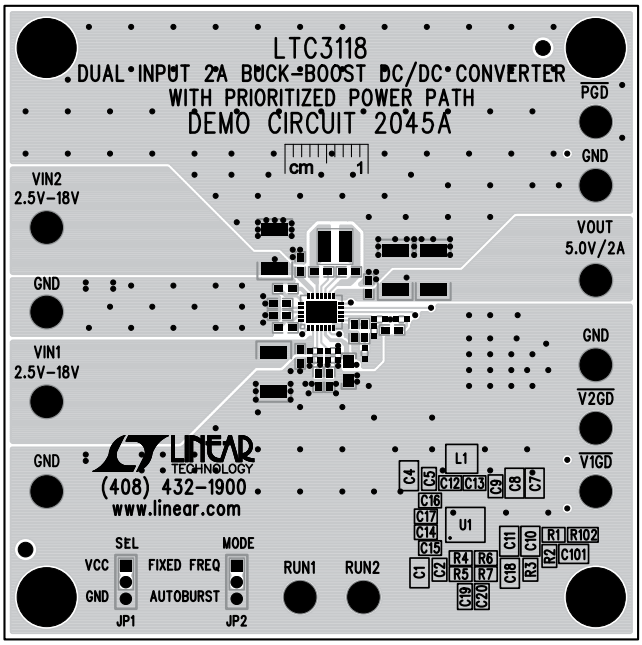
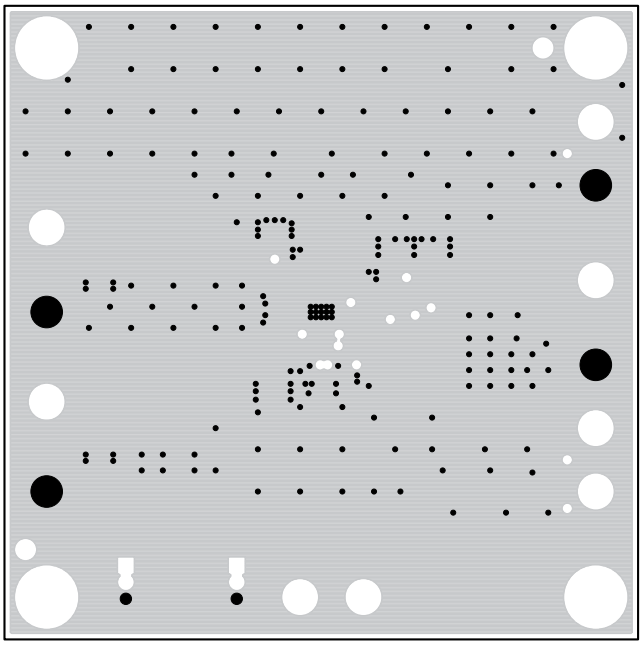
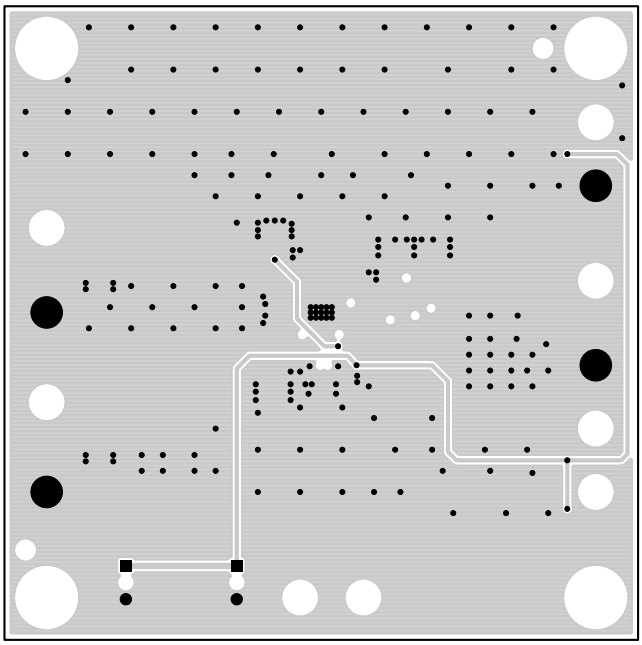
Top Layer



2nd Layer



3rd Layer



Bottom Layer (Top View)

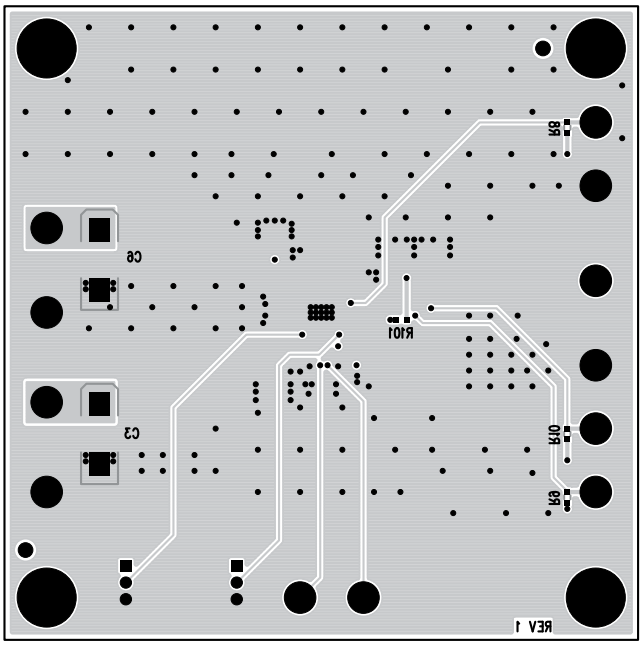


Figure 5. Typical 4-Layer PC Board Layout

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Inactive V_{IN} Leakage Currents

The inactive input (V_{IN1} or V_{IN2}) consumes a small amount of bias current and will exhibit some amount of leakage current, through the disabled switches, depending on the temperature of the die and the average DC voltage between the inactive V_{IN} and SW1 (stand-off voltage). Please refer to the Die Temperature Rise and N-Channel MOSFET leakage curves in the Typical Performance Characteristics of the data sheet. The stand-off voltage can be positive or negative depending on the V_{IN1} and V_{IN2} voltages and varies with SW1 duty cycle. Figure 6 shows typical currents into the inactive input as a function of its voltage at various levels of inductor current as the LTC3118 operates in PWM mode from an active 12V input and 12V output. Higher inductor currents generally translate to higher leakage currents due to power dissipation, resulting in a die temperature rise.

Referring to the curves in Figure 6, leakage currents are generally supplied from the inactive source into its respective V_{IN} pin above a few volts. At lower voltages, it is possible to get reverse current back-fed into the source, causing a depleted battery or unplugged input to slowly charge. In some cases, a dummy load resistor across the inactive input may be needed to prevent that input from rising above its UVLO causing a momentary turn-on. A good thermal design will help to reduce unwanted leakage currents into or out of the inactive input, especially at high switch currents where die temperatures increase. A tight board layout near the V_{IN1}/CM1 and V_{IN2}/CM2 pins to ground is advised to reduce leakage that may occur due to SW1 edge rates and parasitic inductances in the traces.

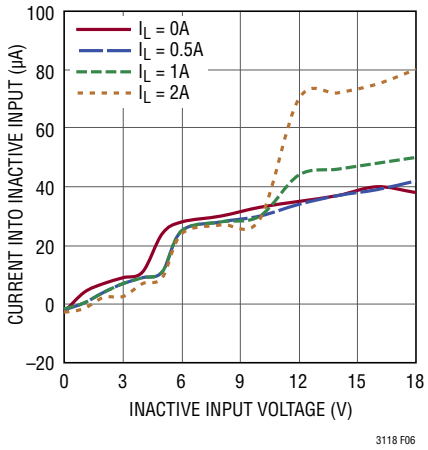

Figure 6. Inactive V_{IN} Current vs Voltage and Inductor Current (I_L)
Active V_{IN} = V_{OUT} = 12V in PWM Mode

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A standard application circuit for the LTC3118 is shown on the front page of this data sheet. The appropriate selection of external components is dependent upon the required performance of the IC in each particular application, given considerations and trade-offs such as PCB area, input and output voltage range, output voltage ripple, required efficiency, thermal considerations and cost. This section of the data sheet provides some basic guidelines and considerations to aid in the selection of external components and the design of the applications circuit.

V_{CC} Capacitor Selection

V_{CC} is generated by a low dropout linear regulator from either V_{IN1} or V_{IN2}, whichever is selected. Both V_{CC} regulators have been designed for stable operation with a wide range of output capacitors. For most applications, a low ESR capacitor of 4.7µF should be used. The capacitor should be located as close to V_{CC} as possible and connected to ground through the shortest trace possible. If the connecting trace cannot be made short, an additional 0.1µF bypass capacitor should be connected between V_{CC} and ground, as close to the package pins as possible.

Bootstrapping the V_{CC} Regulator with 5V V_{OUT} or External Supply

The high and low side gate drivers are powered by V_{CC}, which is generated from the selected V_{IN} through an internal linear regulator. In some applications, especially at high input voltages, the power dissipation in the linear regulator can become a significant contributor to thermal heating of the IC. The Typical Performance Characteristics section of this data sheet provides data on V_{CC} current in PWM operation, which is supplied by V_{IN}. A significant performance advantage can be attained in applications where V_{OUT} is programmed to 5V, if V_{CC} is powered by V_{OUT} rather than the selected V_{IN}. This can be done by connecting a Schottky diode from V_{OUT} to V_{CC}, as shown in Figure 7. With the bootstrap diode installed, the gate driver currents are supplied by the buck-boost converter at high efficiency rather than through the less efficient internal linear regulator. The internal linear regulator contains reverse blocking circuitry that allows V_{CC} to be driven slightly above their nominal regulation level with only a slight amount of reverse current. Please note that the bootstrapping supply (either V_{OUT} or a separate regulator) must limit V_{CC} to less than 6V.

BST, Charge Pump and CM Capacitor Selection

Small ceramic capacitors are needed to provide a sufficient amount of charge to the high side switches. As shown in the applications circuits and the front page of this data sheet, small capacitors are required from BST1 to SW1, BST2 to SW2, CN1 to CP1, CN2 to CP2, CM1 to GND and CM2 to GND. Recommended initial values for the BST to SW capacitors are 0.1µF with > 5V rating, CN to CP capacitors are 10nF with > 20V rating, and CM to GND capacitors are 47nF with > 20V rating.

Inductor Selection

The choice of inductor used in LTC3118 applications influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance and high output

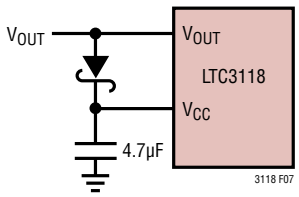

Figure 7. Bootstrapping V_{CC}

APPLICATIONS INFORMATION

current capability or efficiency will be compromised. Larger inductor values reduce inductor current ripple, but will not increase output current capability as is the case with peak current mode control, as described in the Inductor Current Sense and Maximum Output Current section of this data sheet. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance also lower the right half plane (RHP) zero frequency when operating in boost mode, requiring the converter bandwidth to be set lower in frequency, thereby slowing the converter's load transient response. Most LTC3118 application circuits deliver the best performance with an inductor value between 3.3µH and 10µH. In general, a 3.3µH inductor is recommended for V_{OUT} up to 5V, 6.8µH for V_{OUT} = 12V and 10µH for V_{OUT} = 18V. Inductor values for other output voltages can be scaled accordingly.

Regardless of inductor value, the saturation current rating should be such that it is greater than the worst-case average inductor current plus half of the ripple current. The peak-to-peak inductor current ripple for each operational mode can be calculated from the following formula, where f is the switching frequency (1.2MHz), L is the inductance in µH, and t_{LOW} is the switch pin minimum low time in µs. The switch pin minimum low time is typically 0.1µs.

$$\Delta I_{L(P-P)BUCK} =$$

$$\frac{V_{OUT}}{L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}-t_{LOW}\right)\text{Amps}$$

$$\Delta I_{L(P-P)BOOST} =$$

$$\frac{V_{IN}}{L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)\left(\frac{1}{f}-t_{LOW}\right)\text{Amps}$$

It should be noted that the worst-case inductor peak-to-peak inductor ripple current occurs when the duty cycle in buck mode is maximum (highest V_{IN}), and in boost mode when the duty cycle is 50% ($V_{OUT} = 2 \bullet V_{IN}$). As an example, if V_{IN} (minimum) = 2.7V and V_{IN} (maximum) = 18V, V_{OUT} = 5V and L = 3.3µH, the peak-to-peak inductor ripples at the voltage extremes (18V V_{IN} for buck and 2.7V V_{IN} for boost) are:

Buck = 600mA peak-to-peak

Boost = 200mA peak-to-peak

One-half of this inductor ripple current must be added to the highest expected average inductor current in order to select the proper saturation current rating for the inductor (about 4A).

In addition to its influence on power conversion efficiency, the inductor DC resistance can also impact the maximum output current capability of the buck-boost converter particularly at low input voltages. In buck mode, the output current of the buck-boost converter is primarily limited by the inductor current reaching the average current limit threshold defined by VC. However, in boost mode, especially at large step-up ratios, the output current capability can also be limited by the total resistive losses in the power stage. These losses include switch resistances, inductor DC resistance and PCB trace resistance. Avoid inductors with a high DC resistance (DCR), as they can degrade the maximum output current capability from what is shown in the Typical Performance Characteristics section. As a guideline, the inductor DCR should be significantly less than the typical power switch resistance of 100mΩ. The only exceptions are applications that have a maximum output current much less than what the LTC3118 is capable of delivering.

Different inductor core materials and styles have an impact on the size and price of an inductor at any given current rating. Shielded construction is generally preferred as it minimizes the chances of interference with other circuitry. The choice of inductor style depends upon the price, sizing and EMI requirements of a particular application. Table 1 provides a small sampling of inductors that are well suited to many LTC3118 applications.

Output Capacitor Selection

A low effective series resistance (ESR) output capacitor should be connected at the output of the buck-boost converter in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor

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Table 1. Representative Buck-Boost Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (mΩ)	MAX DC CURRENT (A)	SIZE (W × L × H) mm	MANUFACTURER
MSS7341T	3.3	18	3.7	7 × 7 × 4	Coilcraft
XAL7030	6.8	42	4.4	8 × 8 × 3	www.coilcraft.com
SD8328	3.3	14	4.0	8 × 8 × 3	Coiltronics
	4.7	19	3.6	8 × 8 × 3	www.coiltronics.com
LQH88PN	3.3	16	5	8 × 8 × 4	Murata
LQH88PN	4.7	22	4.2	8 × 8 × 4	www.murata.com
LQH88PN	6.8	28	3.8	8 × 8 × 4	
CDRH8D28NP	3.3	18	4	8 × 8 × 3	Sumida
	4.7	25	3.4	8 × 8 × 3	www.sumida.com
VLP840	3.3	15	5.2	8 × 8 × 4	TDK Electronics
	6.8	24	3.6	8 × 8 × 4	www.tdk.co.jp
FDSD0603	3.3	23	5.6	7 × 7 × 3	Toko
	6.8	51	3.7	7 × 7 × 3	www.toko.co.jp
7447789003	3.3	30	4.2	7 × 7 × 3	Würth Elektronik
7447789004	4.7	35	3.9	7 × 7 × 3	www.we-online.com
7447779006	6.8	35	3.3	7 × 7 × 4.5	

value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor's ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formula, where f is the frequency in MHz (1.2MHz), C_{OUT} is the capacitance in µF, t_{LOW} is the switch pin minimum low time in µs (0.1µs) and I_{LOAD} is the output current in Amps.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD}\ t_{LOW}}{C_{OUT}} \text{Volts}$$

$$\Delta V_{P-P(BOOST)} =$$

$$\frac{I_{LOAD}}{fC_{OUT}}\left(\frac{V_{OUT} - V_{IN} + t_{LOW}\ fV_{IN}}{V_{OUT}}\right)\text{Volts}$$

Examining the previous equations reveals that the output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. Note that these equations only take into account the voltage ripple that occurs from the inductor current to the output being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where the output voltage ripple is dominated by the inductor current ripple.

In addition to the output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor, and is given by the following expressions where R_{ESR} is the series resistance of the output capacitor and all other terms as previously defined.

$$\Delta V_{P-P(BUCK)} = \frac{I_{LOAD}\ R_{ESR}}{1 - t_{LOW}\ f} \cong I_{LOAD}\ R_{ESR} \text{Volts}$$

$$\Delta V_{P-P(BOOST)} =$$

$$\frac{I_{LOAD}\ R_{ESR}\ V_{OUT}}{V_{IN}\ (1 - t_{LOW}\ f)} \cong I_{LOAD}\ R_{ESR}\left(\frac{V_{OUT}}{V_{IN}}\right)\text{Volts}$$

In most LTC3118 applications, an output capacitor between 47µF and 100µF will work well.

Input Capacitor Selection

The V_{IN1} or V_{IN2} pin carries the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 10µF should be located as close to the pin as possible.

APPLICATIONS INFORMATION

The traces connecting this capacitor to V_{IN1} or V_{IN2} and the ground plane should be made as short as possible.

When powered through long leads or from a high ESR power source, a larger value bulk input capacitor may be required. In such applications, a 47µF to 100µF electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution. In ideal diode mode, the voltage ripple on each input must be kept below the V_{IN} comparator's 800mV hysteresis to prevent repetitive switching between V_{IN1} and V_{IN2} operation when the input voltages are similar.

Recommended Input and Output Capacitors

The capacitors used to filter the input and output of the LTC3118 must have low ESR and must be rated to handle the large AC currents generated by the switching converters. This is important to maintain proper functioning of the IC and to reduce output voltage ripple. There are many capacitor types that are well suited to these applications including multilayer ceramic, low ESR tantalum, OS-CON and POSCAP technologies. In addition, there are certain types of electrolytic capacitors, such as solid aluminum organic polymer capacitors, that are designed for low ESR and high AC currents and these are also well suited to some LTC3118 applications. Table 2 provides a partial listing of appropriate capacitors to use. The choice of capacitor technology is primarily dictated by a trade-off between size, leakage current and cost. In backup power applications, the input or output capacitor might be a super or ultra capacitor with a capacitance value measuring in the Farad range. The selection criteria in these applications are generally similar except that voltage ripple is generally not a concern. Some capacitors exhibit a high DC leakage current which may preclude their consideration for applications that require a very low quiescent current in Burst Mode operation.

Table 2. Representative Bypass and Output Capacitors

PART NUMBER	VALUE (µF)	VOLTAGE (V)	CAPACITOR TYPE ESR (mΩ)	SIZE (W × L × H) mm	MANUFACTURER
12103D226MAT2A	22	25	X5R Ceramic	3.2 × 2.5 × 2.8	AVX www. avx.com
C2220X226K3RACTU A700D226M016ATE030	22 22	25 16	X7R Ceramic, Aluminum Polymer 30mΩ	5.7 × 5 × 2.4 7.3 × 4.3 × 2.8	Kemet www.kemet.com
GRM32ER71E226KE15L	22	25	X7R Ceramic	3.2 × 2.5 × 2.5	Murata www.murata.com
PLV1E121MDL1	82	25	Aluminum Polymer, 25mΩ	8 × 8 × 3	Nichicon www.nichicon.com
ECJ-4YB1E226M	22	25	X5R Ceramic	3.2 × 2.5 × 2.5	Panasonic www.panasonic.com
25TQC22MV 16TQC100M 25SVPF47M	22 100 47	25 16 25	POSCAP, 50mΩ POSCAP, 45mΩ OS-CON, 30mΩ	7.3 × 4.3 × 1.9 7.3 × 4.3 × 3.1 6.6 × 6.6 × 5.9	Sanyo www.sanyo.com
TMK325BJ226MM-T	22	25	X5R Ceramic	3.2 × 2.5 × 2.5	Taiyo Yuden www.t-yuden.com
CKG57NX5R1E476M	47	25	X5R Ceramic	6.5 × 5.5 × 5.5	TDK www.tdk.com

APPLICATIONS INFORMATION

Ceramic capacitors are often utilized in switching converter applications due to their small size, low ESR and low leakage currents. However, many ceramic capacitors intended for power applications experience a significant loss in capacitance from their rated value as the DC bias voltage on the capacitor increases. It is not uncommon for a small surface mount capacitor to lose more than 50% of its rated capacitance when operated near its maximum rated voltage. This effect is generally reduced as the case size is increased for the same nominal value capacitor. As a result, it is often necessary to use a larger value capacitance or a higher voltage rated capacitor than would ordinarily be required to actually realize the intended capacitance at the operating voltage of the application. X5R and X7R dielectric types are recommended as they exhibit the best performance over the wide operating range and temperature of the LTC3118. To verify that the intended capacitance is achieved in the application circuit, be sure to consult the capacitor vendor's curve of capacitance versus DC bias voltage.

Compensation of the Buck-Boost Converter

The LTC3118 utilizes an average current architecture to regulate the output voltage. Average current mode control has two loops that require frequency compensation, the inner average current loop and the outer voltage loop. The compensation for the inner average current loop is fixed within the LTC3118 to simplify the loop design and provide the highest possible bandwidth over a wide operating range. The outer voltage loop does require external compensation components, allowing the overall loop characteristics to be customized for the application.

The average current mode control used in the LTC3118 can be conceptualized as a voltage-controlled current source (V_{CCS}), driving the output load formed primarily by R_{LOAD} and C_{OUT}, as shown in Figure 8.

The voltage error amplifier output (VC), provides a command input to the V_{CCS}. The full-scale range of VC is 0.6V (200mV to 800mV). With a full-scale command on VC,

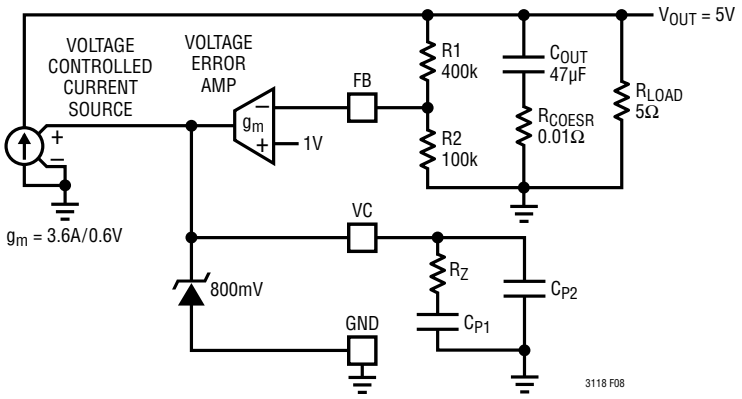

Figure 8. Simplified Representation of Average Current Mode Control Loop

APPLICATIONS INFORMATION

the LTC3118 buck-boost converter will generate an average 3.6A of inductor current (typical) from the converter making the transconductance gain 6A/V. As with peak current mode control, the inner average current control loop effectively turns the inductor into a current source over the frequency range of interest, resulting in a frequency response from the power stage that exhibits a single pole (–20dB / decade) roll-off. The output capacitor (C_{OUT}) and load resistance (R_{LOAD}) form a dominant low frequency pole, where the effective series resistance of the output capacitor and its capacitance form a zero, usually at a high enough frequency to be ignored.

A potentially troublesome right half plane zero (RHPZ) is also encountered if the converter is operated in boost mode. The RHPZ causes an increase in gain, like a zero, but a decrease in phase, like a pole. This can ultimately limit the maximum converter bandwidth that can be achieved with the LTC3118. The RHPZ is not present when operating in buck mode.

The overall open loop gain at DC is the product of the following terms:

Voltage Error Amp Gain:

$$g_m \bullet R_{EA} = 80\mu S \bullet 5M\Omega = \frac{400V}{V} \text{ (fixed)}$$

Voltage Divider Gain:

$$\frac{V_{FB}}{V_{OUT}} = \frac{1V}{V_{OUT}}$$

Current Loop Transconductance:

$$g_c = \frac{6A}{V} \text{ (fixed)}$$

Load Resistance:

$$R_{LOAD} = \frac{V_{OUT}}{I_{LOAD}}$$

The frequency dependent terms that affect the loop gain include:

Output Load Pole (P1):

$$\frac{1}{2\pi \bullet R_{LOAD} \bullet C_{OUT}} \text{ (application dependent)}$$

Right Half Plane Zero (RHPZ):

$$\frac{V_{IN}^{\,2} \bullet R_L}{V_{OUT}^{\,2} \bullet 2\pi \bullet L} \text{ (application dependent)}$$

Voltage Error Amplifier Compensation: 2 poles and 1 zero (application dependent)

The voltage amplifier's frequency response is designed to optimize the response for the overall loop. Measurement of the power stage gain over line, load, component variation and frequency is strongly recommended prior to loop design. The design parameters for compensation design will focus on the series resistor and capacitors connected from VC to ground (R_Z, C_{P1} and C_{P2}). Being a buck-boost converter, the target loop crossover frequency for the compensation design will be dictated by the highest boost ratio and load current that is expected, as this will result in the lowest RHPZ frequency. The general goal is to set the crossover frequency and provide sufficient phase boost using the external compensation network.

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Compensation Example

This section will demonstrate how to derive and select the compensation components for a typical LTC3118 application. Designing compensation for other applications is a matter of substituting different values in the equations provided based on the power stage bode plots. Since the compensation design procedure uses a simplified model of the LTC3118, the results from the following compensation design should always be verified with time domain step load response tests to validate the effectiveness of the compensation design. It is assumed that the value and type of output capacitor will be selected based on the guidelines provided elsewhere in this data sheet. Particular attention needs to be paid to the voltage bias effect on ceramic capacitors typically used for output bypassing. Similarly, it is assumed that the inductor value and current rating has been selected as well, based on the application requirements.

Example Application Details:

V_{IN} = 3V to 15V

V_{OUT} = 5V

Maximum I_{OUT} (boost mode) = 1A, R_{LOAD} = 5Ω

Maximum I_{OUT} (buck mode) = 1A, R_{LOAD} = 5Ω (could supply 2A if V_{IN} > 5V)

C_{OUT} = 100µF but use 66µF in calculations to account for DC voltage bias effects.

L = 3.3µH

Since this application includes boost mode operation, the first step is to calculate the worst-case RHPZ frequency as this will dictate the maximum loop bandwidth for the converter.

$$RHPZ(f) = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} =$$

$$\frac{3V^2 \bullet 5\Omega}{5V^2 \bullet 2\pi \bullet 3.3\mu H} = 87kHz$$

In order to account for internal IC component variations, it is a good practice to set the converter bandwidth, or crossover frequency, at least 4 to 5 times lower than the RHPZ frequency, to avoid excessive phase loss from the RHPZ when operating in boost mode. In some instances such as higher output voltage applications, an even greater separation between the loop crossover frequency and the RHPZ frequency may be necessary. In this example design, we'll plan to achieve a loop bandwidth (f_{CC}) of 20kHz, well below the RHPZ frequency. The 5V, 1A design example bode plots are shown in Figure 9. The top curve set shows the power stage gain (and phase) in buck (> $5V_{IN}$) and $3V_{IN}$ boost mode operation. The DC gain in buck mode is simply the current loop transconductance (6A/V) multiplied by the load resistance (5Ω). The V_{OUT} resistor divider will be accounted for in voltage amplifier network.

Buck DC Gain:

$$20\log(6A/V \bullet 5\Omega) = 29dB$$

In boost mode the gain is reduced by V_{IN}/V_{OUT}.

Boost DC Gain at $3V_{IN}$:

$$20\log\left(\frac{6A/V \bullet 3V \bullet 5\Omega}{5V}\right) = 25dB$$

The output load pole will move depending on the output load resistance. The power stage poles at full load are shown in the top set of curves in Figure 9.

Output Load Pole:

$$\frac{1}{2\pi \bullet R_{LOAD} \bullet C_{OUT}} = \frac{1}{2\pi \bullet 5\Omega \bullet 66\mu F} = 480Hz$$

APPLICATIONS INFORMATION

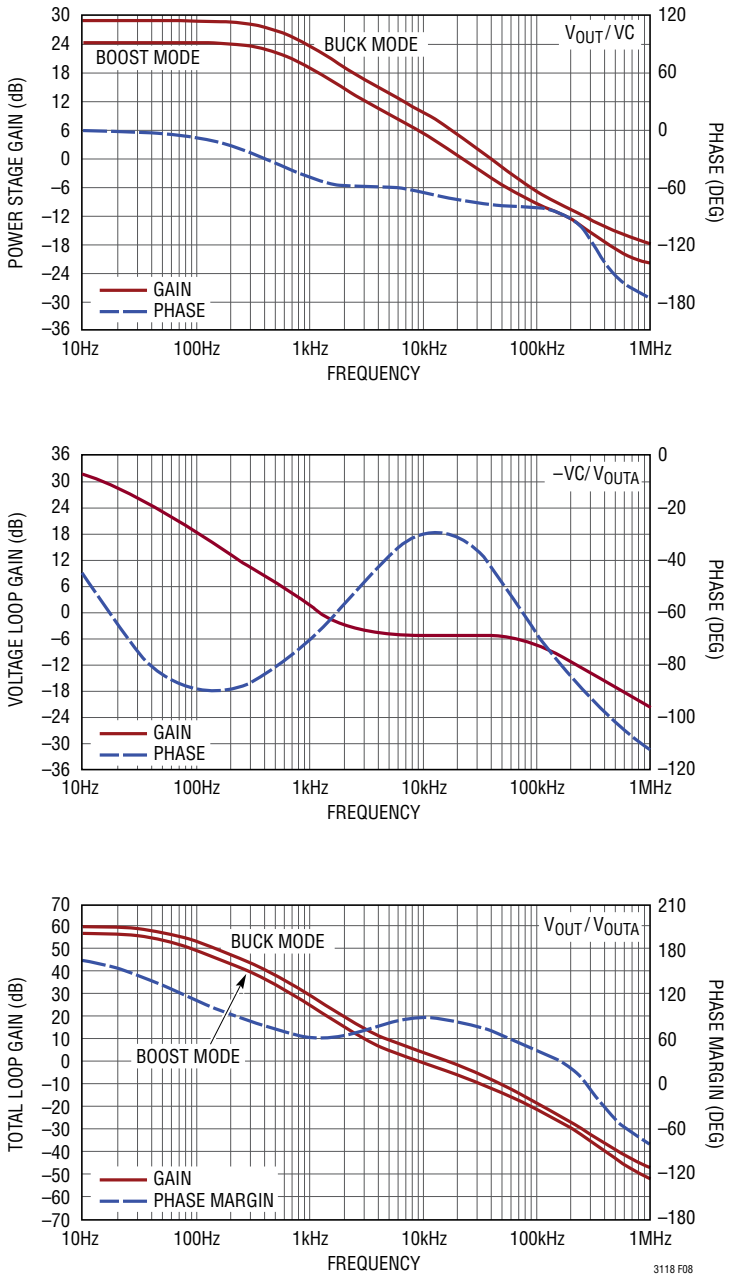


Figure 9. Bode Plot Showing Power Stage Gain (Top), V_A Loop (Center), and Total Loop Gain vs Frequency

These values were verified in the top set of curves in Figure 9. The resulting power stage crossover frequency is around 40kHz in buck mode (V_{IN} > 5V), 20kHz in boost mode at $3.5V_{IN}$.

The uncompensated power stage crossover frequency is higher than the goal of 20kHz. More importantly, the uncompensated power stage DC gain is low, especially in boost mode. A pole-zero-pole network will now be added to the voltage amplifier to increase the DC gain, reduce the crossover frequency and reduce the overall gain at high frequencies:

$$V_A \text{ Pole 1} = \frac{1}{2\pi R_{EA} C_{P1}}$$

APPLICATIONS INFORMATION

this pole is close to DC, R_{EA} = Voltage Error Amp output resistance, which is approximately 5MΩ. This pole is mentioned for completeness, but has no effect on the overall loop design:

$$V_A \text{ Zero 1} = \frac{1}{2\pi R_Z C_{P1}}$$

this zero is placed below the crossover frequency to flatten the V_A gain at the crossover to improve phase margin:

$$V_A \text{ Pole 2} = \frac{1}{2\pi R_Z C_{P2}}$$

This pole is placed above the crossover frequency to reduce the gain to suppress noise and mitigate any RHPZ effects.

Referring to the power stage gain curves in Figure 9, the loop gain needs to be reduced by 4dB to achieve a total loop crossover frequency of 20kHz. Assuming Zero 1 is placed well below the crossover frequency and Pole 2 is placed well above the crossover frequency, the voltage amplifiers gain at crossover is given by:

V_A gain at crossover:

$$20\log\left(\frac{V_{FB} \bullet g_m \bullet R_Z}{V_{OUT}}\right) =$$

$$20\log\left(\frac{1V \bullet 80\mu A/V \bullet 40k}{5V}\right) = -4dB$$

Where g_m is the V_A transconductance, V_{FB}/V_{OUT} is the feedback divider gain, and R_Z is the external zero resistor.

As shown, a 40kΩ value for R_Z will provide –4db of gain at crossover. With R_Z selected, C_{P1}'s value is determined by setting the Zero 1 frequency at one-tenth the crossover frequency, or 2kHz.

$$C_{P1} = \frac{1}{2\pi \bullet R_Z \bullet f_{ZERO1}} =$$

$$\frac{1}{2\pi \bullet 40k\Omega \bullet 2kHz} \cong 1.8nF$$

Finally, the high frequency Pole 2 is set at 10 times the crossover frequency to provide a high frequency pole at 200kHz.

$$C_{P2} = \frac{1}{2\pi \bullet R_Z \bullet f_{POLE2}} =$$

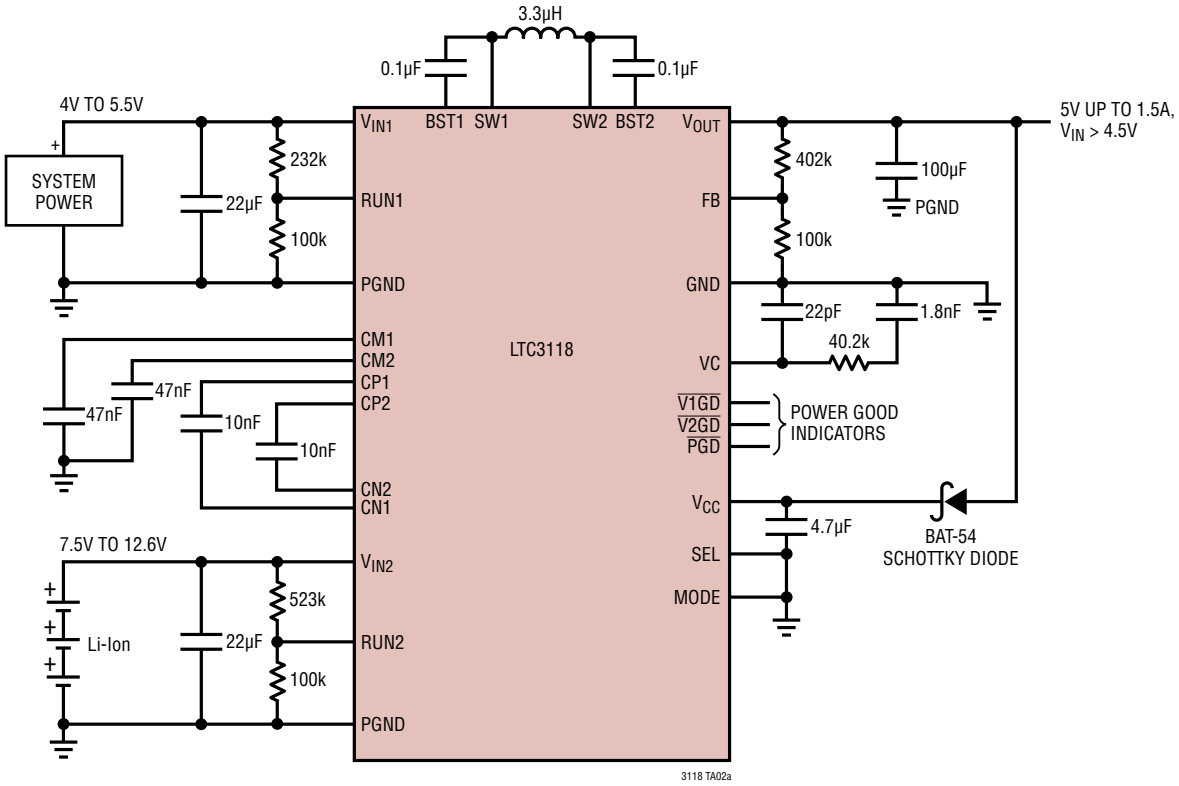
$$\frac{1}{2\pi \bullet 40k\Omega \bullet 200kHz} \cong 22pF$$

The second set of curves in Figure 9 show the resulting V_A response to the selected values. Notice that the separation between Zero 1 and Pole 2 provides 60 degrees phase bump near the crossover frequency.

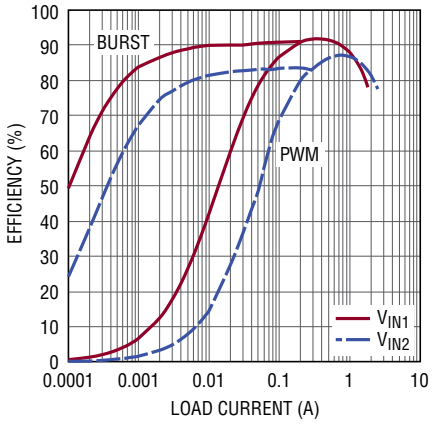
Combining the power stage and V_A frequency responses, the measured overall loop gains are shown in the bottom set of curves of Figure 9. As shown, the crossover frequency was reduced to 20kHz in buck mode, 10kHz in boost. The phase margin at crossover is around 70 degrees. The V_A design provided the additional benefits of high gain (>50dB) at DC and gain attenuation above the crossover frequency to prevent RHPZ issues.

TYPICAL APPLICATIONS

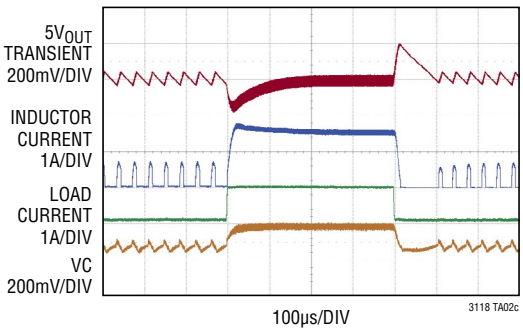
System Power (Priority) or 3-Cell Li-Ion to 5V V_{OUT} Regulator with Automatic Burst Mode Operation



Efficiency vs Load Current: V_{IN1} = 5V, V_{IN2} = 10.8V, V_{OUT} = 5V

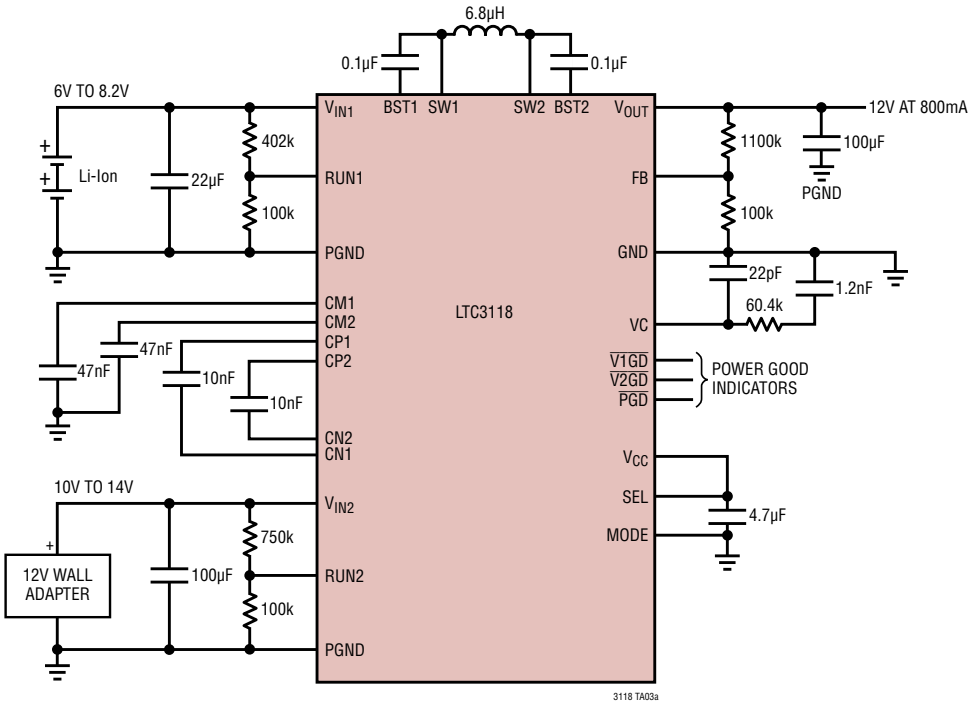


100mA to 1A Load Step, V_{IN1} = 5V, V_{OUT} = 5V, Auto Burst Mode

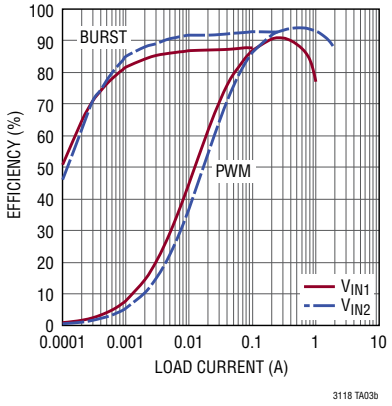


TYPICAL APPLICATIONS

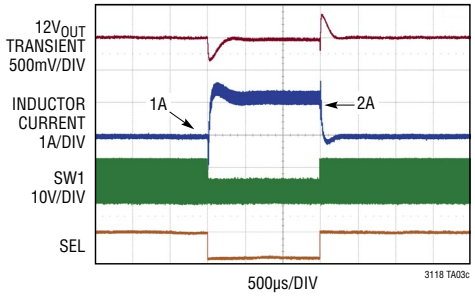
12V Wall Adapter (When Present) or 2-Cell Li-Ion to 12V V_{OUT} Regulator with Automatic Burst Mode Operation



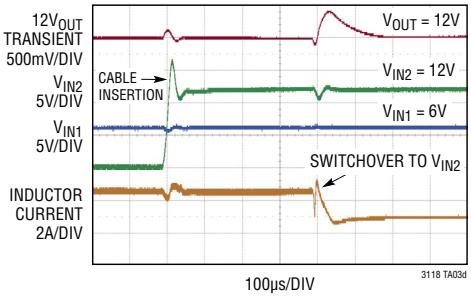
Efficiency vs Load Current: V_{IN1} = 7V, V_{IN2} = 12V, V_{OUT} = 12V



$12V_{IN2}$ to $6V_{IN1}$ SEL Pin Switchover with V_{OUT} = 12V and 800mA Load

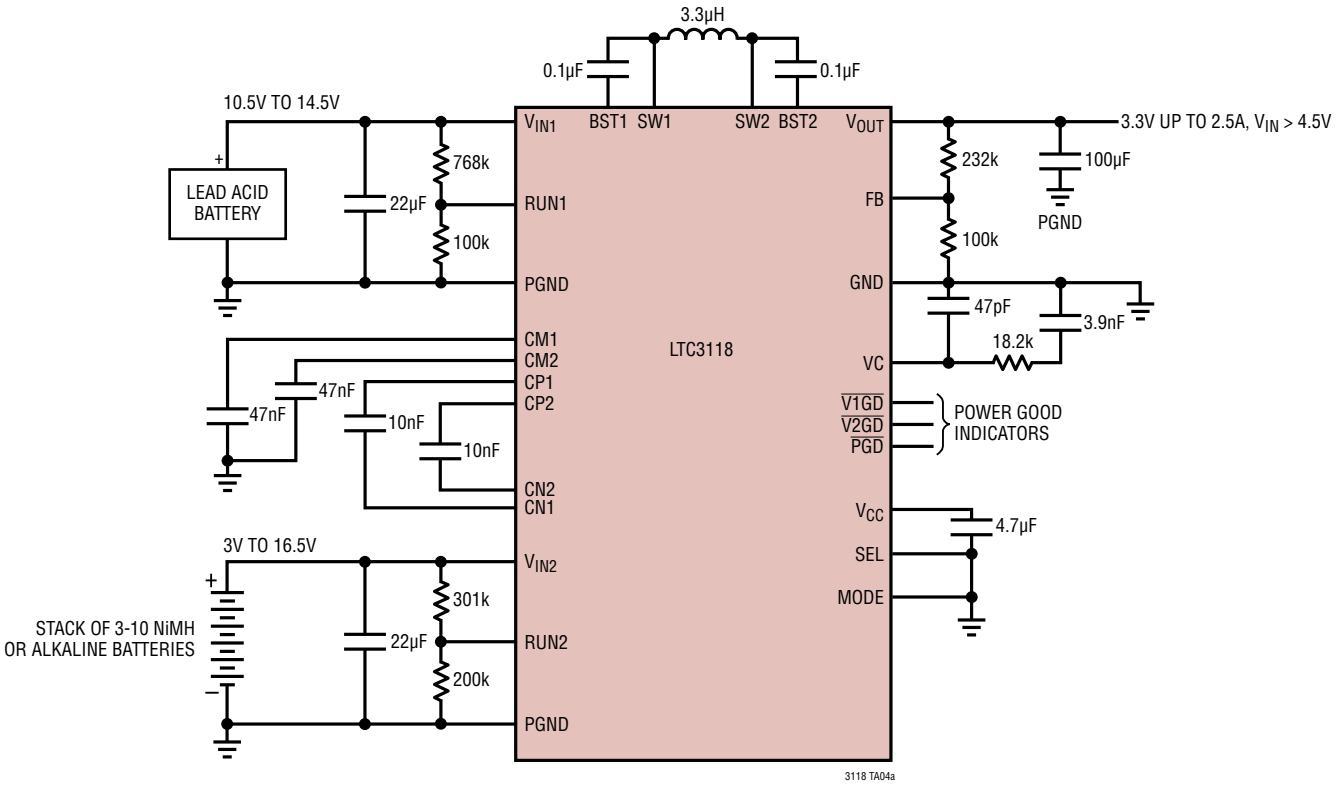


$12V_{IN2}$ Inductive Cable Insertion with V_{OUT} = 12V and 800mA Load

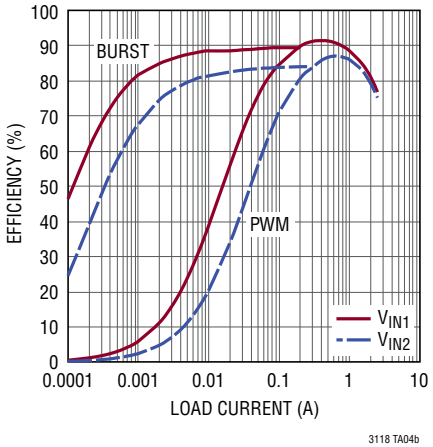


TYPICAL APPLICATIONS

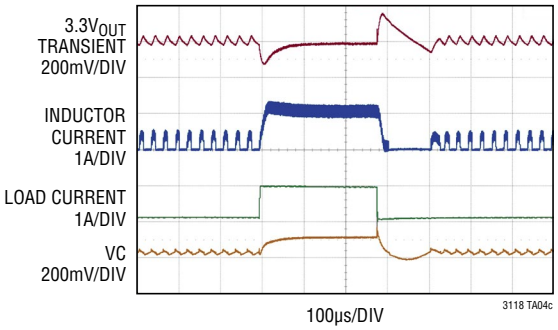
Dual Battery System to 3.3V V_{OUT}, Runs from Lead Acid (Priority) When Present Automatic Burst Mode Operation



Efficiency vs Load Current: V_{IN1} = 5V, V_{IN2} = 12V, V_{OUT} = 3.3V



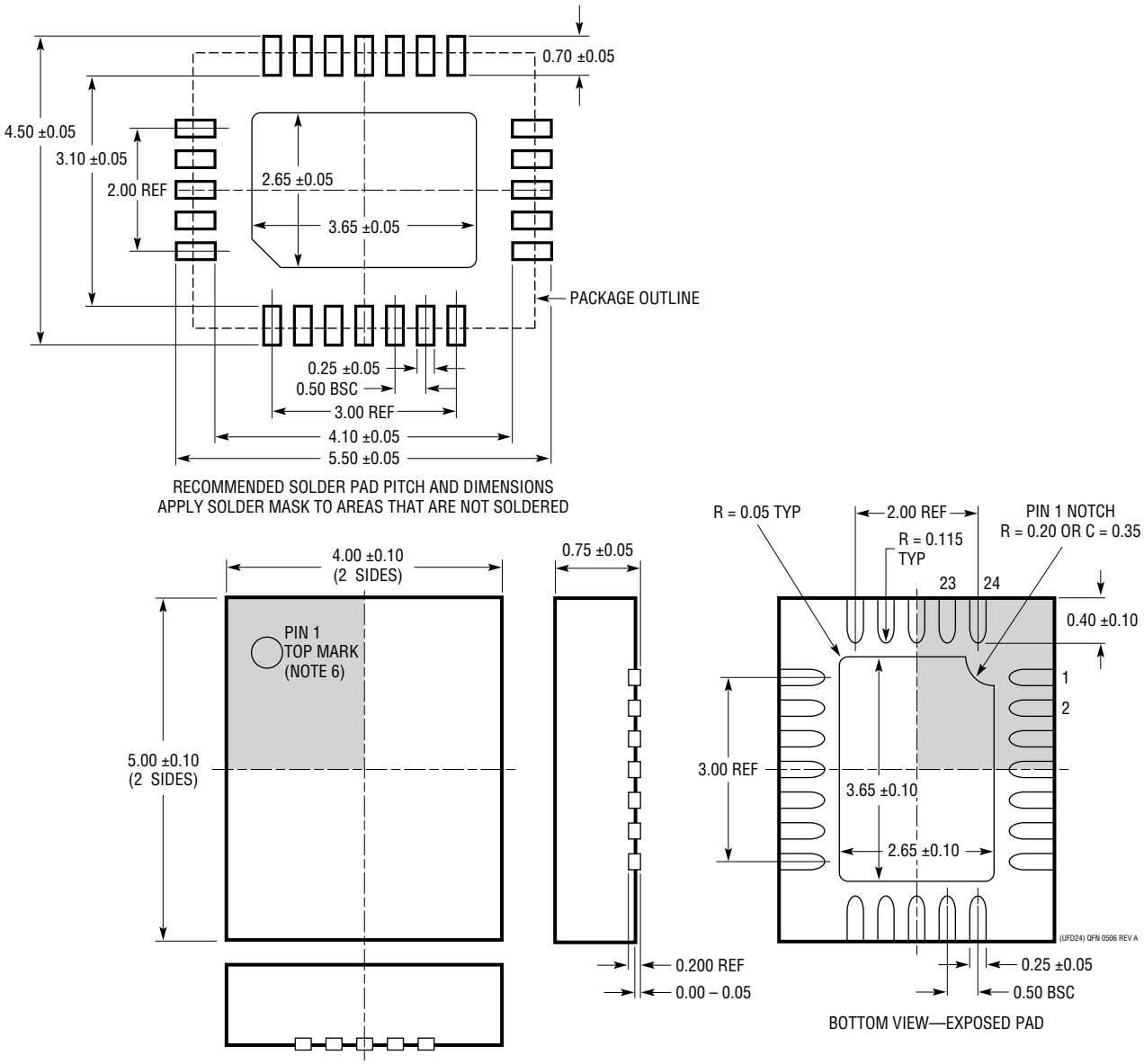
100mA to 1A Load Step, V_{IN} = 12V, V_{OUT} = 3.3V, Auto Burst Mode



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)

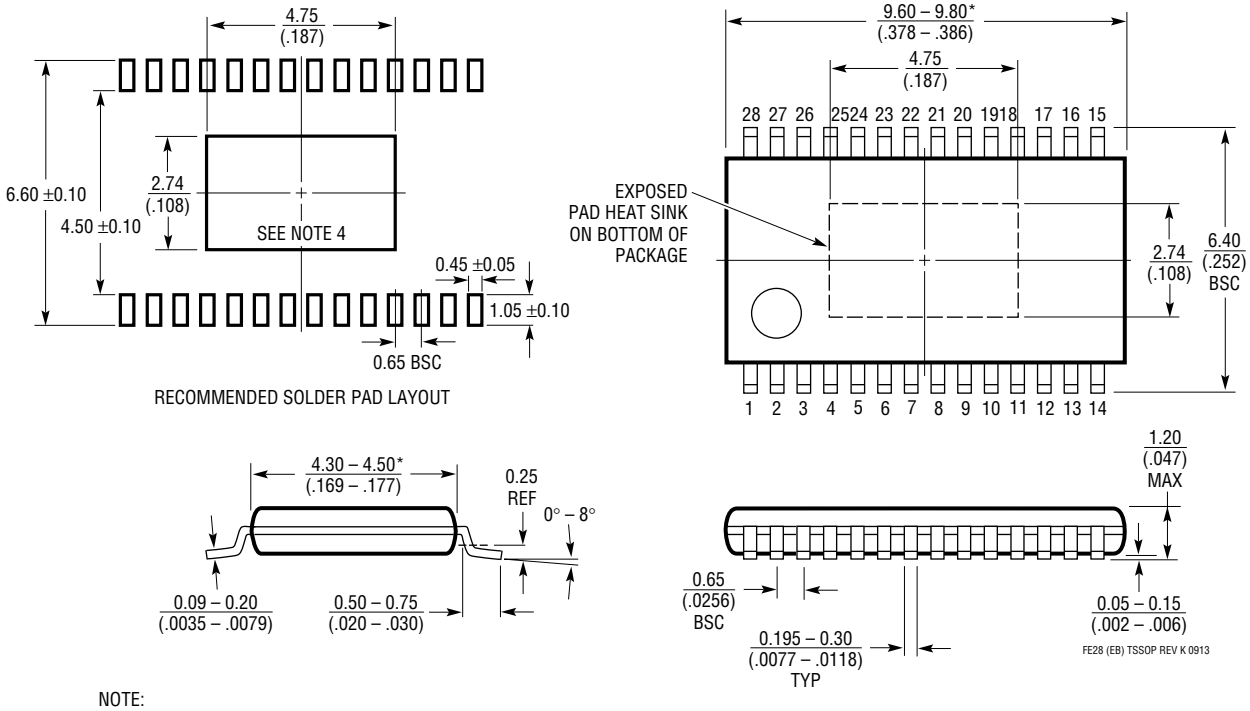


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/15	Text clarification	1
		Pin name corrections for SW1, SW2, BST1 and BST2	34, 35