LTC3204-3.3/LTC3204-5/ LTC3204B-3.3/LTC3204B-5

Low Noise Regulated Charge Pump in 2 × 2 DFN

FEATURES

- **Fixed 3.3V or 5V Outputs**
- **V_{IN} Range:**
  1.8V to 4.5V (LTC3204-3.3/LTC3204B-3.3)
  2.7V to 5.5V (LTC3204-5/LTC3204B-5)
- **Output Current:**
  Up to 150mA (LTC3204-5/LTC3204B-5)
  Up to 50mA (LTC3204-3.3/LTC3204B-3.3)
- **Automatic Burst Mode® Operation with I_Q = 48µA (LTC3204-3.3/LTC3204-5)**
- **Constant Frequency Operation at All Loads (LTC3204B-3.3/LTC3204B-5)**
- Low Noise Constant Frequency (1.2MHz) Operation*
- Built-In Soft-Start Reduces Inrush Current
- Shutdown Disconnects Load from Input
- Shutdown Current <1µA
- Short-Circuit/Thermal Protection
- Available in Low Profile 6-Lead DFN Package

APPLICATIONS

- 2 AA Cell to 3.3V
- Li-Ion to 5V
- USB On-The-Go Devices
- White LED Drivers
- Handheld Devices

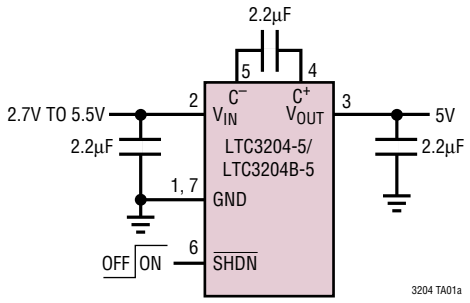
DESCRIPTION

The LTC®3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 are low noise, constant frequency (1.2MHz) switched capacitor voltage doublers. The LTC3204-3.3/LTC3204B-3.3 can produce a regulated output voltage of 3.3V from a minimum input voltage of 1.8V (2 alkaline cells) whereas the LTC3204-5/LTC3204B-5 can produce 5V from a minimum of 2.7V (Li-Ion battery) input.

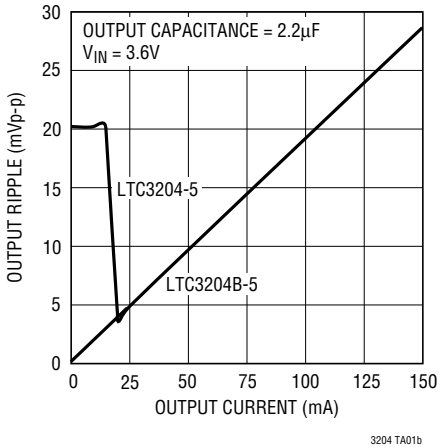
LTC3204-3.3/LTC3204-5 feature automatic Burst Mode® operation at light loads to maintain low supply current whereas LTC3204B-3.3/LTC3204B-5 feature constant frequency operation at any load. Built-in soft-start circuitry prevents excessive inrush current during start-up. Thermal shutdown and current-limit circuitry allow the parts to survive a continuous short-circuit from V_{OUT} to GND.

High switching frequency minimizes overall solution footprint by allowing the use of tiny ceramic capacitors. In shutdown, the load is disconnected from the input and the quiescent current is reduced to <1µA. The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 are available in a low profile (0.75mm) 6-lead 2mm × 2mm DFN package.

TYPICAL APPLICATION



Output Ripple vs Load Current

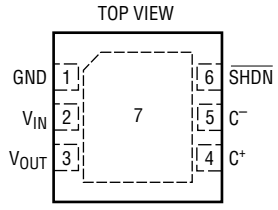


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} to GND ..... –0.3V to 6V
V_{OUT} to GND ..... –0.3V to 5.5V
$\overline{SHDN}$ to GND ..... –0.3V to 6V
V_{OUT} Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Maximum Junction Temperature ..... 125°C

PACKAGE/ORDER INFORMATION



DC PACKAGE
6-LEAD (2mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 80°C/W
EXPOSED PAD IS GND (PIN 7)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3204EDC-3.3 LTC3204EDC-5 LTC3204BEDC-3.3 LTC3204BEDC-5
DC PART MARKING
LBJV LBNK LBVF LBVG

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range. Specifications are at T_A = 25°C, V_{IN} = 2.4V (LTC3204-3.3/LTC3204B-3.3) or 3.6V (LTC3204-5/LTC3204B-5), $\overline{SHDN}$ = V_{IN}, C_{FLY} = 2.2µF, C_{IN} = 2.2µF, C_{OUT} = 2.2µF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(LTC3204-3.3/LTC3204B-3.3) (LTC3204-5/LTC3204B-5)	● ●	1.8 2.7		4.5 5.5	V V
V_{OUT}	Output Voltage Range	1.8V < V_{IN} < 4.5V, I_{OUT} < 40mA 1.9V < V_{IN} < 4.5V, I_{OUT} < 50mA (LTC3204-3.3/LTC3204B-3.3)	 ●	 3.168	 3.3	 3.432	 V
		2.7V < V_{IN} < 5.5V, I_{OUT} < 65mA 3.1V < V_{IN} < 5.5V, I_{OUT} < 150mA (LTC3204-5/LTC3204B-5)	 ●	 4.8	 5	 5.2	 V
I_{IN}	No Load Input Current	I_{OUT} = 0 (LTC3204-3.3) I_{OUT} = 0 (LTC3204-5) I_{OUT} = 0 (LTC3204B-3.3) I_{OUT} = 0 (LTC3204B-5)			48 60 1.25 3.6		µA µA mA mA
$I_{\overline{SHDN}}$	Shutdown Current	$\overline{SHDN}$ = 0V, V_{OUT} = 0V				1	µA
I_{BURST}	Burst Mode Threshold	(LTC3204-3.3) (LTC3204-5)			15 20		mA mA
V_R	Output Ripple	I_{OUT} = 100mA			20		mV_{P-P}
η	Efficiency	V_{IN} = 3V, I_{OUT} = 100mA (LTC3204-5/LTC3204B-5)			82		%
f_{OSC}	Switching Frequency		●	0.6	1.2	1.8	MHz
V_{IH}	$\overline{SHDN}$ Input Threshold		●	1.3			V
V_{IL}	$\overline{SHDN}$ Input Threshold		●			0.4	V
I_{IH}	$\overline{SHDN}$ Input Current		●	–1		1	µA
I_{IL}	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 0V	●	–1		1	µA
R_{OL}	Effective Open-Loop Output Resistance (Note 3)	V_{IN} = 1.8V, V_{OUT} = 3V (LTC3204-3.3/LTC3204B-3.3) V_{IN} = 2.7V, V_{OUT} = 4.5V (LTC3204-5/LTC3204B-5)			7 6		Ω Ω
I_{LIM}	Output Current Limit	V_{OUT} = 0V			300		mA
T_{SS}	Soft-Start Time	From the Rising Edge of $\overline{SHDN}$ to 90% of V_{OUT}			0.75		ms

Note 1: Absolute Maximum Ratings are those beyond which the life of a device may be impaired.

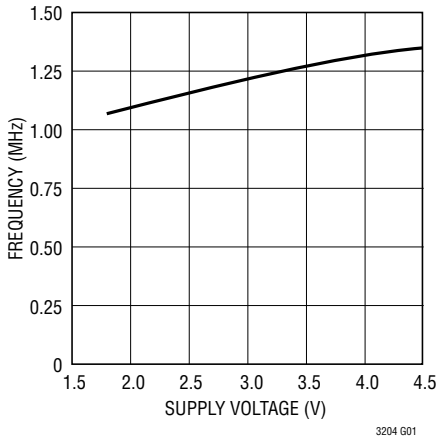
Note 2: The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: $R_{OL} \equiv (2V_{IN} – V_{OUT})/I_{OUT}$

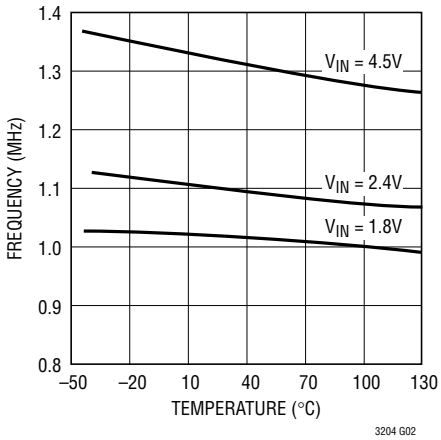
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, C_{FLY} = C_{IN} = C_{OUT} = 2.2µF unless otherwise specified)

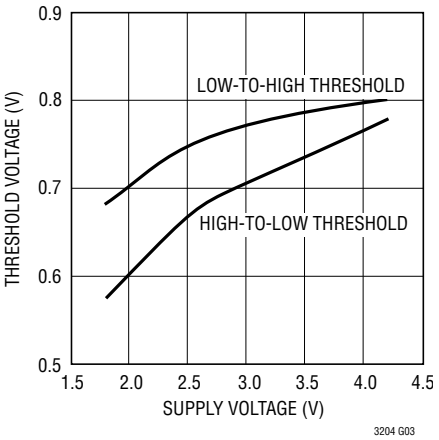
Oscillator Frequency vs Supply Voltage



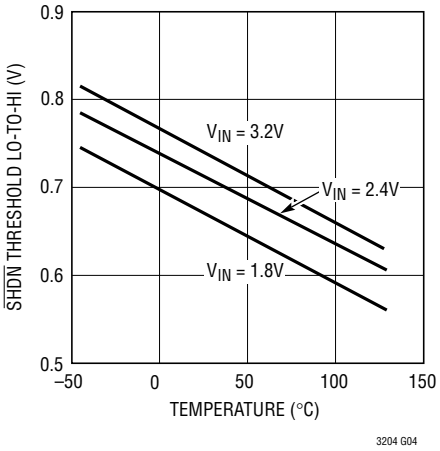
Oscillator Frequency vs Temperature



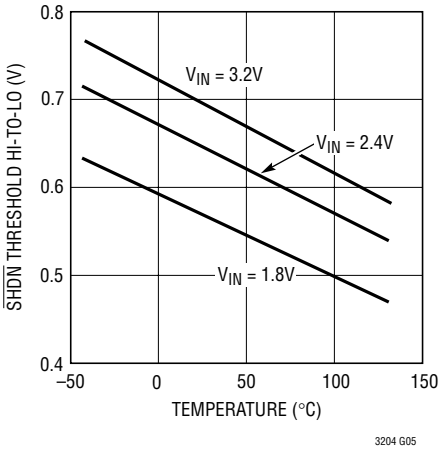
$\overline{SHDN}$ Threshold Voltage vs Supply Voltage



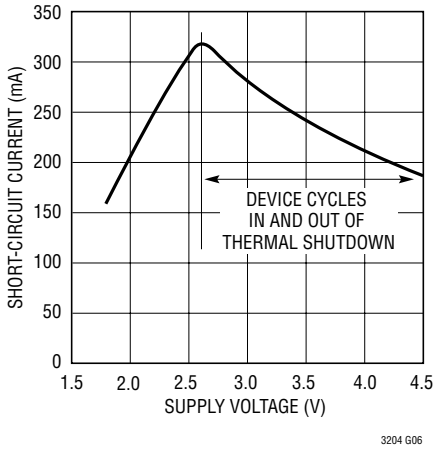
$\overline{SHDN}$ LO-to-HI Threshold vs Temperature



$\overline{SHDN}$ HI-to-LO Threshold vs Temperature



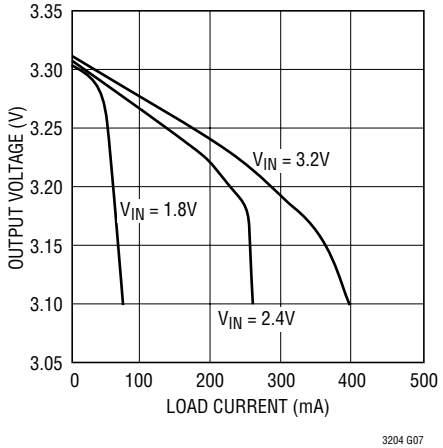
Short-Circuit Current vs Supply



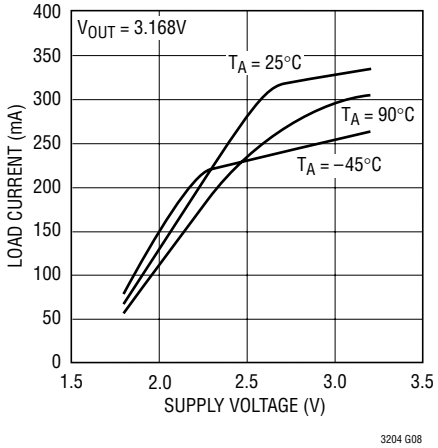
TYPICAL PERFORMANCE CHARACTERISTICS (LTC3204-3.3/LTC3204B-3.3 ONLY)

(T_A = 25°C, C_{FLY} = C_{IN} = C_{OUT} = 2.2µF unless otherwise specified)

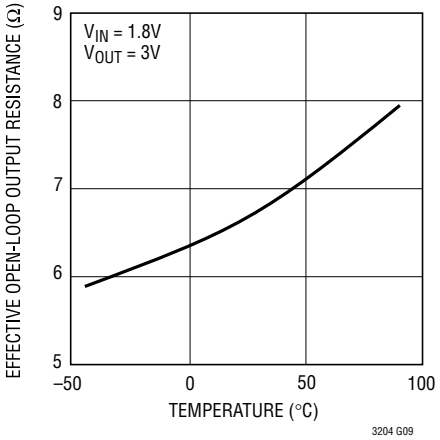
Load Regulation



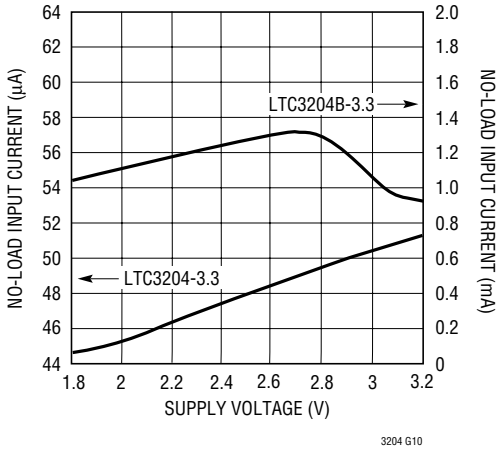
Output Load Capability at 4% Below Regulation



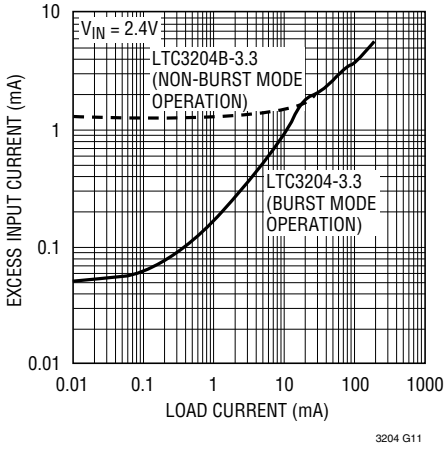
Effective Open-Loop Output Resistance vs Temperature



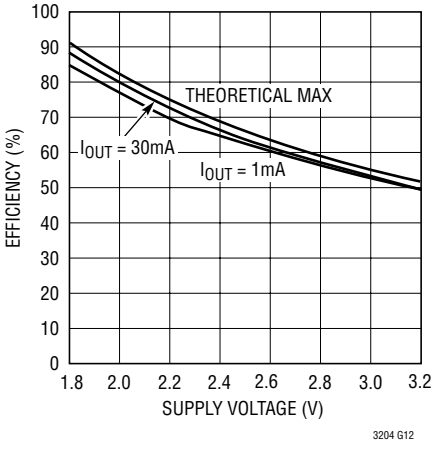
No-Load Input Current vs Supply Voltage



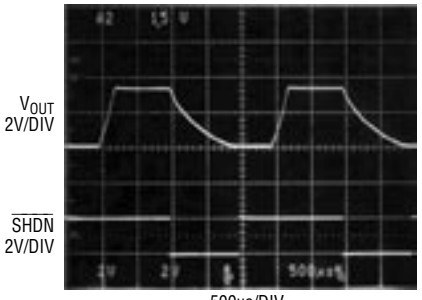
Extra Input Current vs Load Current (I_{IN}-2I_{LOAD})



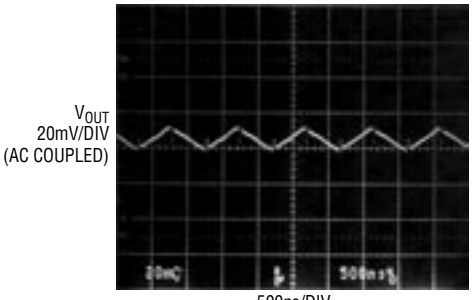
Efficiency vs Supply Voltage



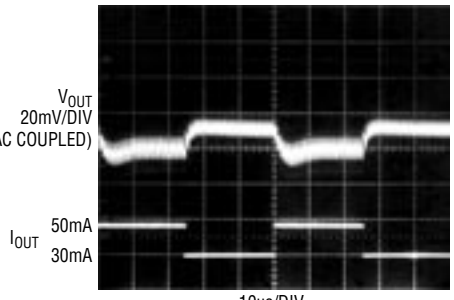
V_{OUT} Soft-Start Response



Output Ripple



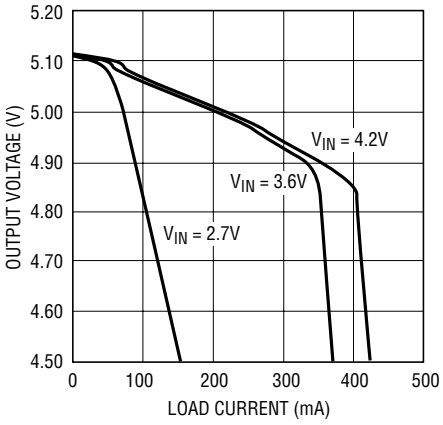
Load Transient Response



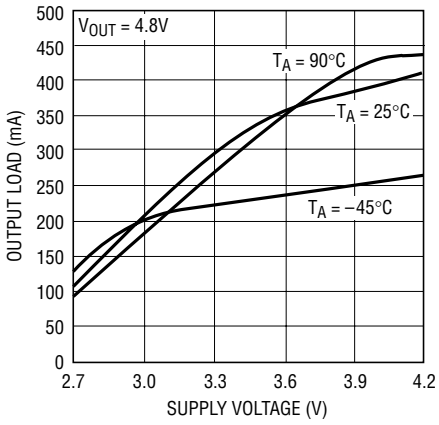
TYPICAL PERFORMANCE CHARACTERISTICS (LTC3204-5/LTC3204B-5 ONLY)

(T_A = 25°C, C_{FLY} = C_{IN} = C_{OUT} = 2.2µF unless otherwise specified)

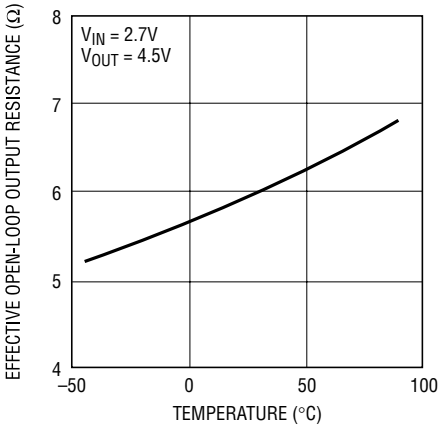
Load Regulation



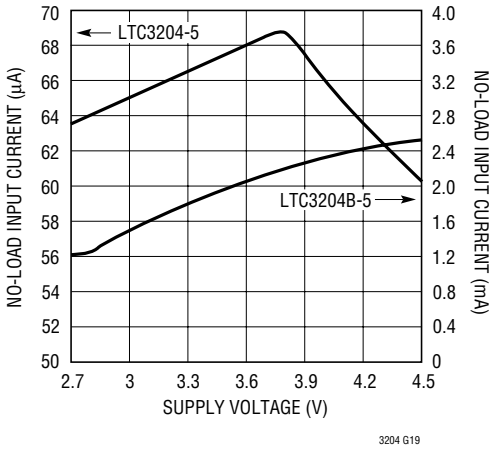
Output Load Capability at 4% Below Regulation



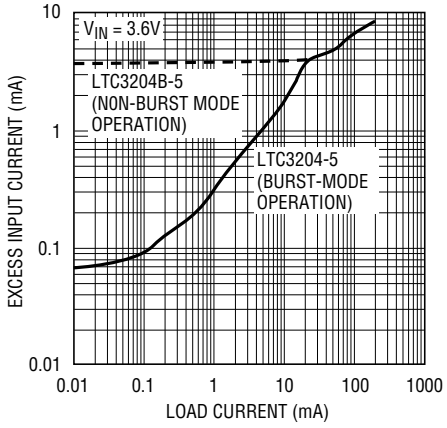
Effective Open-Loop Output Resistance vs Temperature



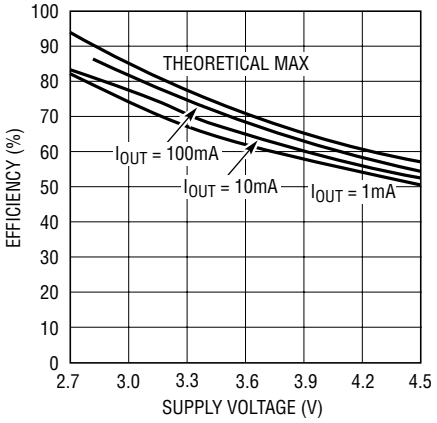
No-Load Input Current vs Supply Voltage



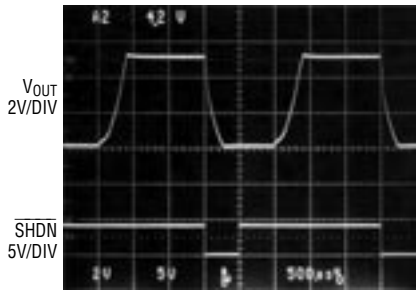
Extra Input Current vs Load Current (I_{IN}-2I_{LOAD})



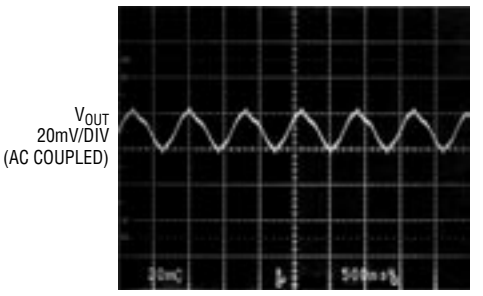
Efficiency vs Supply Voltage



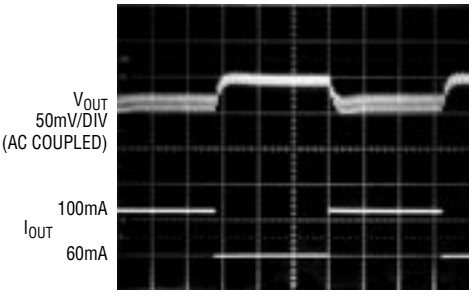
V_{OUT} Soft-Start



Output Ripple



Load Transient Response



PIN FUNCTIONS

GND (Pin 1, 7): Ground. These pins should be tied to a ground plane for best performance. The exposed pad must be soldered to PCB ground to provide electrical contact and optimum thermal performance.

V_{IN} (Pin 2): Input Supply Voltage. V_{IN} should be bypassed with a 1µF to 4.7µF low ESR ceramic capacitor.

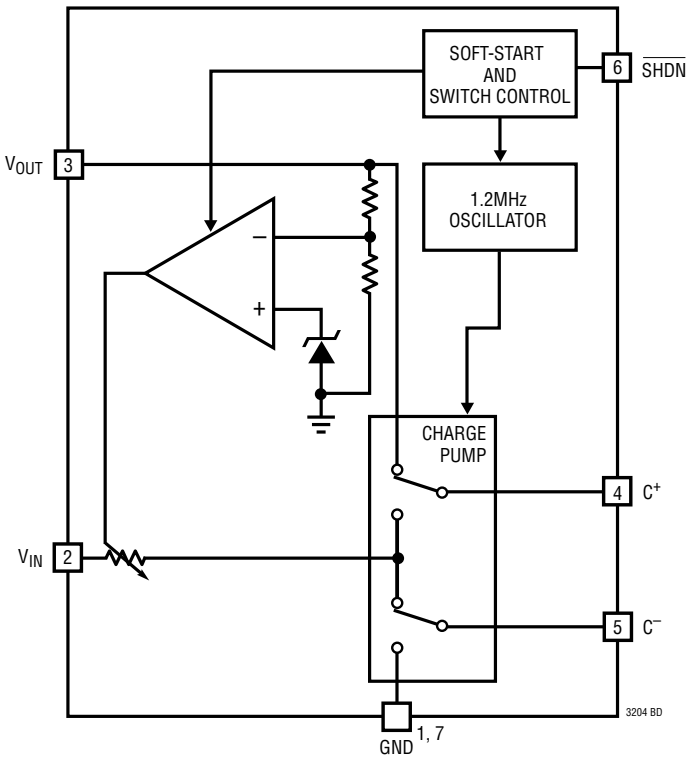
V_{OUT} (Pin 3): Regulated Output Voltage. V_{OUT} should be bypassed with a low ESR ceramic capacitor providing at least 2µF of capacitance as close to the pin as possible for best performance.

C^+ (Pin 4): Flying Capacitor Positive Terminal.

C^- (Pin 5): Flying Capacitor Negative Terminal.

$\overline{SHDN}$ (Pin 6): Active Low Shutdown Input. A low on $\overline{SHDN}$ disables the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5. This pin must not be allowed to float.

BLOCK DIAGRAM



OPERATION (Refer to the Block Diagram)

The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 use a switched capacitor charge pump to boost V_{IN} to a regulated output voltage. Regulation is achieved by sensing the output voltage through an internal resistor divider and modulating the charge pump output current based on the error signal. A 2-phase nonoverlapping clock activates the charge pump switches. The flying capacitor is charged from V_{IN} on the first phase of the clock. On the second phase of the clock it is stacked in series with V_{IN} and connected to V_{OUT}. This sequence of charging and discharging the flying capacitor continues at a free running frequency of 1.2MHz (typ).

Shutdown Mode

In shutdown mode, all circuitry is turned off and the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 draws only leakage current from the V_{IN} supply. Furthermore, V_{OUT} is disconnected from V_{IN}. The $\overline{SHDN}$ pin is a CMOS input with a threshold voltage of approximately 0.7V. The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 are in shutdown when a logic low is applied to the $\overline{SHDN}$ pin. Since the $\overline{SHDN}$ pin is a very high impedance CMOS input, it should never be allowed to float. To ensure that its state is defined, it must always be driven with a valid logic level.

Since the output voltages of these devices can go above the input voltage, special circuitry is required to control the internal logic. Detection logic will draw an input current of 5µA when the devices are in shutdown. However, this current will be eliminated if the output voltage (V_{OUT}) is less than approximately 0.8V.

Burst Mode Operation

The LTC3204-3.3/LTC3204-5 provide automatic Burst Mode operation to reduce supply current at light loads. Burst Mode operation is initiated if the output load current falls below an internally programmed threshold. Once Burst Mode operation is initiated, the part shuts down the internal oscillator to reduce the switching losses and goes into a low current state. This state is referred to as the sleep state in which the IC consumes only about 40µA from the input. When the output voltage droops enough to overcome the burst comparator hysteresis, the part wakes up and commences normal fixed frequency operation. The output capacitor recharges and causes the part to reenter the sleep state if the output load still remains less than the Burst Mode threshold. This Burst Mode threshold varies with V_{IN}, V_{OUT} and the choice of output storage capacitor.

Soft-Start

The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 have built-in soft-start circuitry to prevent excessive current flow during start-up. The soft-start is achieved by charging an internal capacitor with a very weak current source. The voltage on this capacitor, in turn, slowly ramps the amount of current available to the output storage capacitor from zero to a value of 300mA over a period of approximately 0.75ms. The soft-start circuit is reset in the event of a commanded shutdown or thermal shutdown.

Short-Circuit/Thermal Protection

The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 have built-in short-circuit current limit as well as over-temperature protection. During a short-circuit condition, they will automatically limit their output current to approximately 300mA. At higher temperatures, or if the input voltage is high enough to cause excessive self-heating of the part, the thermal shutdown circuitry will shutdown the charge pump once the junction temperature exceeds approximately 160°C. It will enable the charge pump once the junction temperature drops back to approximately 150°C. The LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 will cycle in and out of thermal shutdown indefinitely without latchup or damage until the short-circuit condition on V_{OUT} is removed.

APPLICATIONS INFORMATION

Power Efficiency

The power efficiency (η) of the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 is similar to that of a linear regulator with an effective input voltage of twice the actual input voltage. This occurs because the input current for a voltage doubling charge pump is approximately twice the output current. In an ideal regulating voltage doubler the power efficiency would be given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet 2I_{OUT}} = \frac{V_{OUT}}{2V_{IN}}$$

At moderate to high output power, the switching losses and the quiescent current of the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 are negligible and the expression above is valid. For example, with V_{IN} = 3V, I_{OUT} = 100mA and V_{OUT} regulating to 5V, the measured efficiency is 81.8% which is in close agreement with the theoretical 83.3% calculation.

Maximum Available Output Current

For the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5,the maximum available output current and voltage can be calculated from the effective open-loop output resistance, R_{OL}, and the effective input voltage, $2V_{IN(MIN)}$.

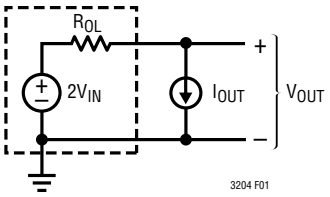


Figure 1. Equivalent Open-Loop Circuit

From Fig. 1, the available current is given by:

$$I_{OUT} = \frac{2V_{IN} - V_{OUT}}{R_{OL}}$$

Effective Open Loop Output Resistance (R_{OL})

The effective open loop output resistance (R_{OL}) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator frequency (f_{OSC}), value of the flying capacitor (C_{FLY}), the nonoverlap time, the internal switch resistances (R_S), and the ESR of the external capacitors. A first order approximation for R_{OL} is given below:

$$R_{OL} \cong 2\sum_{S=1\ TO\ 4} R_S + \frac{1}{f_{OSC} \bullet C_{FLY}}$$

Typical R_{OL} values as a function of temperature are shown in Figure 2.

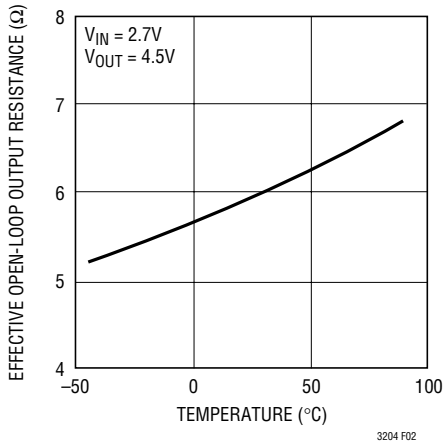


Figure 2. Typical R_{OL} vs Temperature

V_{IN}, V_{OUT} Capacitor Selection

The style and value of capacitors used with the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low ESR (<0.1Ω) ceramic capacitors be used for both C_{IN} and C_{OUT}. These capacitors should be 1µF or greater. Tantalum and aluminum capacitors are not recommended because of their high ESR.

The value of C_{OUT} directly controls the amount of output ripple for a given load current. Increasing the size of C_{OUT} will reduce the output ripple at the expense of higher minimum turn-on time. The peak-to-peak output ripple is approximately given by the expression:

$$V_{RIPPLE(P-P)} \cong \frac{I_{OUT}}{2f_{OSC} \bullet C_{OUT}}$$

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where f_{OSC} is the oscillator frequency (typically 1.2MHz) and C_{OUT} is the value of output charge storage capacitor.

Also, the value and style of the output capacitor can significantly affect the stability of the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5. As shown in the Block Diagram, the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 use a linear control loop to adjust the strength of the charge pump to match the current required at the output. The error signal of this loop is stored directly on the output storage capacitor. This output capacitor also serves to form the dominant pole of the control loop. To prevent ringing or instability on the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5, it is important to maintain at least 1µF of capacitance over all conditions.

Excessive ESR on the output capacitor can degrade the loop stability of the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5. The closed loop output resistance of the LTC3204-5 is designed to be 0.5Ω. For a 100mA load current change, the output voltage will change by about 50mV. If the output capacitor has 0.5Ω or more of ESR, the closed loop frequency response will cease to roll off in a simple one-pole fashion and poor load transient response or instability could result. Ceramic capacitors typically have exceptional ESR performance and combined with a good board layout should yield very good stability and load transient performance.

As the value of C_{OUT} controls the amount of output ripple, the value of C_{IN} controls the amount of ripple present at the input pin (V_{IN}). The input current to the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 will be relatively constant during the input charging phase or the output charging phase but will drop to zero during the nonoverlap times. Since the nonoverlap time is small (~25ns), these missing notches will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the voltage drop in the ESR. Therefore, ceramic capacitors are again recommended for their exceptional ESR performance.

Further input noise reduction can be achieved by powering the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 through a very small series inductor as shown in Figure 3. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

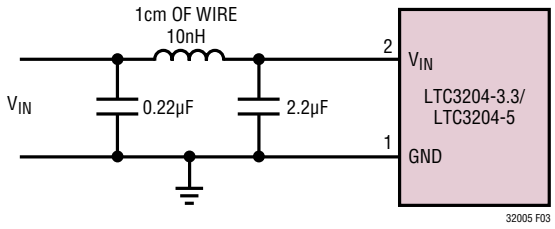

Figure 3. 10nH Inductor Used for Additional Input Noise Reduction

Flying Capacitor Selection

Warning: A polarized capacitor such as tantalum or aluminum should never be used for the flying capacitor since its voltage can reverse upon start-up of the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5. Low ESR ceramic capacitors should always be used for the flying capacitor.

The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary to have at least 1µF of capacitance for the flying capacitor.

For very light load applications, the flying capacitor may be reduced to save space or cost. From the first order approximation of R_{OL} in the section "Effective Open-Loop Output Resistance," the theoretical minimum output resistance of a voltage doubling charge pump can be expressed by the following equation:

$$R_{OL(MIN)} = \frac{2V_{IN} - V_{OUT}}{I_{OUT}} \cong \frac{1}{f_{OSC} \bullet C_{FLY}}$$

where f_{OSC} is the switching frequency (1.2MHz) and C_{FLY} is the value of the flying capacitor. The charge pump will typically be weaker than the theoretical limit due to additional switch resistance. However, for very light load applications, the above expression can be used as a guideline in determining a starting capacitor value.

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Ceramic Capacitors

Ceramic capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1µF 10V Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF 10V X7R capacitor available in the same 0603 case. In fact, for most LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 applications, these capacitors can be considered roughly equivalent. The capacitor manufacturer's data sheet should be consulted to ensure the desired capacitance at all temperatures and voltages.

Below is a list of ceramic capacitor manufacturers and how to contact them:

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com
TDK	www.component.tdk.com

Layout Considerations

Due to the high switching frequency and high transient currents produced by LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5, careful board layout is necessary for optimum performance. A true ground plane and short connections to all the external capacitors will improve performance and ensure proper regulation under all conditions. Figure 4 shows an example layout for the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5.

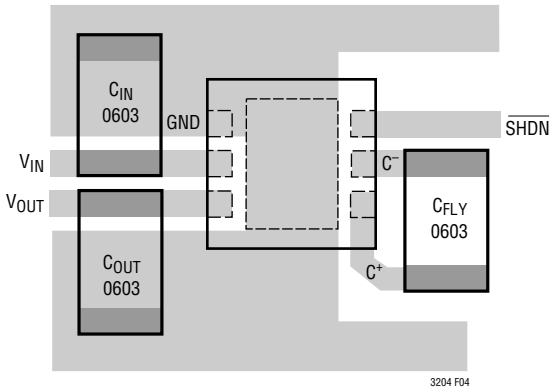

Figure 4. Recommended Layout

Thermal Management

For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5. If the junction temperature increases above approximately 160°C, the thermal shutdown circuitry will automatically deactivate the output. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the GND pin (Pin 1) and the exposed pad of the DFN package (Pin 7) to a ground plane under the device on two layers of the PC board can reduce the thermal resistance of the package and PC board considerably.

Derating Power at High Temperatures

To prevent an overtemperature condition in high power applications, Figure 5 should be used to determine the maximum combination of ambient temperature and power dissipation.

The power dissipated in the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 should always fall under the line shown for a given ambient temperature. The power dissipation in the LTC3204-3.3/LTC3204-5/LTC3204B-3.3/LTC3204B-5 is given by the expression:

$$P_D = (2V_{IN} - V_{OUT}) \bullet I_{OUT}$$

This derating curve assumes a maximum thermal resistance, θ_{JA}, of 80°C/W for the 2mm × 2mm DFN package.

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This can be achieved from a printed circuit board layout with a solid ground plane and a good connection to the ground pins of LTC3204-3.3/LTC3204-5/LTC3204B-3.3/ LTC3204B-5 and the exposed pad of the DFN package. Operation out of this curve will cause the junction temperature to exceed 160°C which may trigger the thermal shutdown.

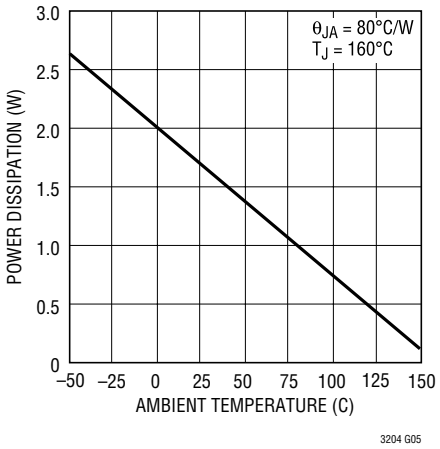
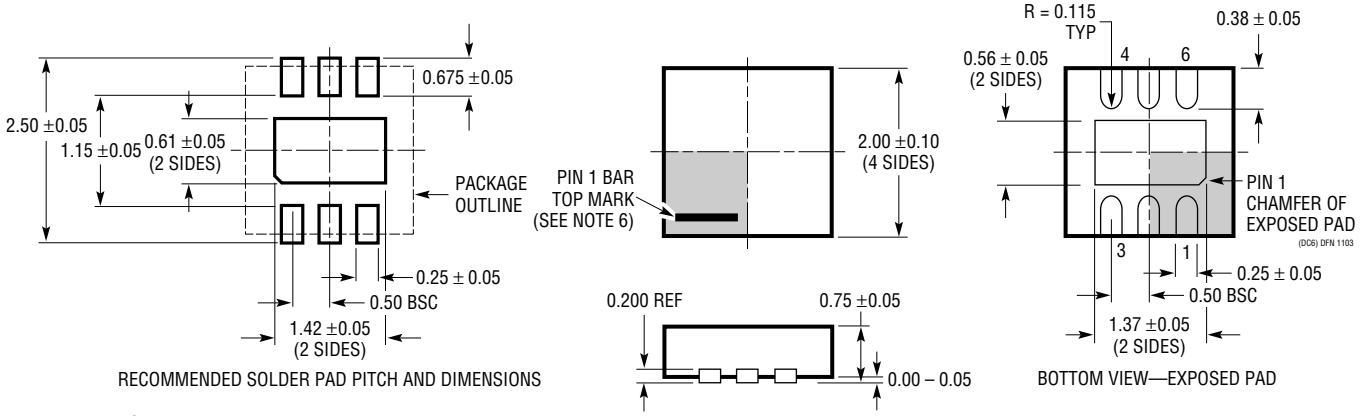


Figure 5. Maximum Power Dissipation vs Ambient Temperature

PACKAGE DESCRIPTION

DC Package
6-Lead Plastic DFN (2mm × 2mm)
(Reference LTC DWG # 05-08-1703)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WCCD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE