600mA Universal Multi-Output LED/CAM Driver

FEATURES

- **Low Noise, Multi-Mode Charge Pump (1x, 1.5x, 2x) Provides Up to 91% Efficiency**
- **Slew Limited Switching Reduces Conducted and Radiated Noise (EMI)**
- **Up to 600mA Total Output Current**
- **Twelve 28mA Universal Current Sources with 64-Step Linear Brightness Control**
- **425mA CAM LED Current Source with 16-Step Linear Brightness Control and 2-Second High Current Safety Timer**
- **Independent On/Off, Brightness Level, Blinking and Gradation Control for Each Current Source Using 2-Wire I²C™ Interface**
- **Internal Current Reference**
- **Two I²C Addresses are Available (LTC3207 00110110, LTC3207-1 00110100)**
- Configurable ENU Pin for Asynchronous LED On/Off Control
- Automatic or Forced Mode Switching
- Internal Soft-Start Limits Inrush Current
- Short-Circuit/Thermal Protection
- 4mm × 4mm 24-Pin QFN Plastic Package

APPLICATIONS

- Video Phones with QVGA+ Displays

DESCRIPTION

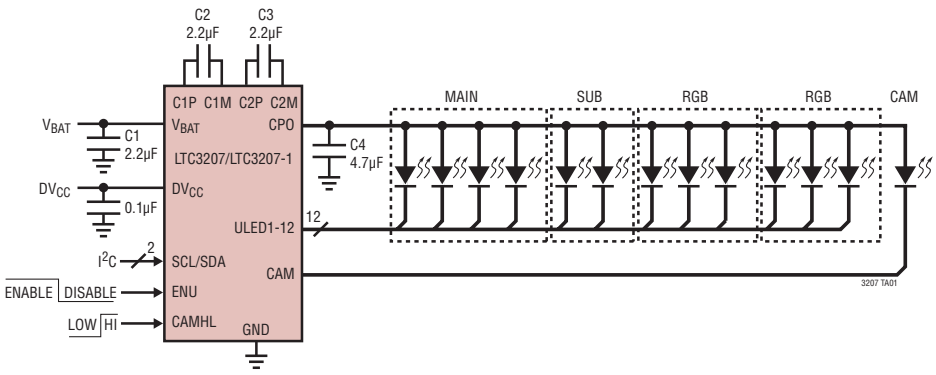
The LTC®3207/LTC3207-1 are highly integrated multi-display LED drivers. The device contains a high-efficiency, low-noise charge pump to provide power to 12 universal LED current sources and one camera LED current source. The LTC3207/LTC3207-1 require only five small ceramic capacitors to form a complete LED power supply and current controller. In addition there are two I²C addresses available.

The display currents are set by an internal precision current reference. Independent dimming, On/Off, blinking and gradation control for all universal current sources is achieved via the I²C serial interface. 6-bit linear DACs are available for adjusting brightness levels for each universal LED current source. The CAM current source has a 4-bit linear DAC to adjust brightness.

The LTC3207/LTC3207-1 charge pumps optimize efficiency based on the voltage across the LED current sources. The device powers-up in 1x mode and will automatically switch to boost mode whenever any enabled LED current source begins to enter dropout. The first dropout switches the IC into 1.5x mode and a subsequent dropout switches the LTC3207/LTC3207-1 into 2x mode. The device resets to 1x mode whenever a data register is updated via the I²C port.

TYPICAL APPLICATION

4-LED MAIN, 2-LED SUB, Dual RGB and Camera Light

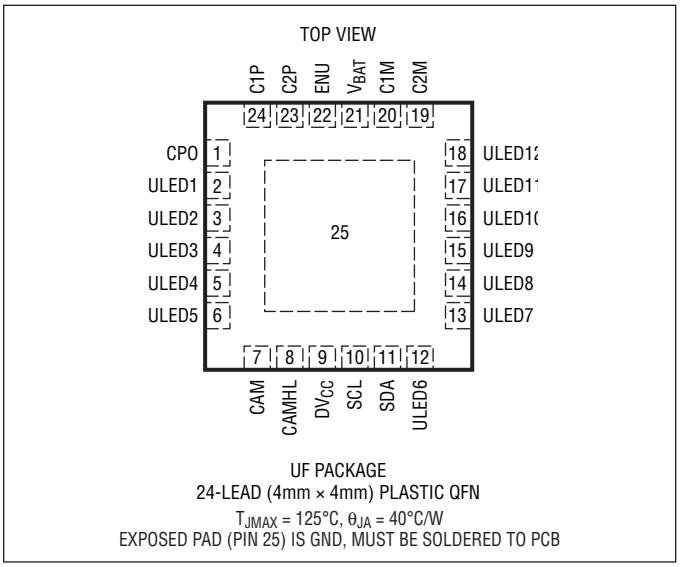


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 4)

V_{BAT}, DV_{CC}, CPO ..... –0.3V to 6V
ULED1 to ULED12, CAM ..... –0.3V to 6V
SDA, SCL, ENU, CAMHL .....–0.3V to (DV_{CC} + 0.3V)
I_{CPO}
  Continuous (Note 3) 350mA
  Pulsed at 10% Duty Cycle.....600mA
I_{CAM}
  Continuous (Note 3) 300mA
  Pulsed at 10% Duty Cycle.....460mA
CPO Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2).... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3207EUF#PBF	LTC3207EUF#TRPBF	3207	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC3207EUF-1#PBF	LTC3207EUF-1#TRPBF	32071	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BAT} = 3.6V, DV_{CC} = 3V, ENU = Hi, CAMHL = LO, C1 = C2 = C3 = 2.2µF, C4 = 4.7µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT} Operating Voltage		●	2.9		5.5	V
I_{VBAT} Operating Current	I_{CPO} = 0, 1x Mode I_{CPO} = 0, 1.5x Mode I_{CPO} = 0, 2x Mode			0.5 2.9 4.1		mA mA mA
DV_{CC} UVLO Threshold				1		V
DV_{CC} Operating Voltage		●	1.5		5.5	V
V_{BAT} UVLO Threshold				1.5		V
V_{BAT} Shutdown Current		●		3.2	7	µA
DV_{CC} Shutdown Current		●			1	µA
Universal LED Current, 6-Bit Linear DACs, ULED = 1V						
Full-Scale LED Current		●	24.2	27.5	31	mA
Minimum (1LSB) LED Current				0.436		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BAT} = 3.6V, DV_{CC} = 3V, ENU = Hi, CAMHL = LO, C1 = C2 = C3 = 2.2µF, C4 = 4.7µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LED Current Matching	Any Two Outputs, 50% of FS			2		%
LED Dropout Voltage	I_{LED} = FS			180		mV
Blink Rate Period	REG15, D6 and D7			1.25 2.5		s s
ULED Up/Down Gradation Times	REG15, D4 and D5			0.24		s
		●			0.45	s
				0.48		s
		●			0.9	s
				0.96		s
		●			1.8	s
V_{OL} General Purpose Output Mode (GPO)	I_{OUT} = 1mA, Single Output Enabled			7		mV
CAM LED Current, 4-Bit Linear DAC, CAM = 1V						
Full-Scale LED Current				425		mA
Minimum (1LSB) LED Current				29		mA
LED Dropout Voltage	I_{LED} = FS			450		mV
High Current Safety Timer	High Current Mode			2.1		s
Charge Pump (CPO)						
1x Mode Output Impedance				0.6		Ω
1.5x Mode Output Impedance	V_{BAT} = 3V, V_{CPO} = 4.2V (Note 5)			3.6		Ω
2x Mode Output Impedance	V_{BAT} = 3V, V_{CPO} = 4.8V (Note 5)			4.1		Ω
CPO Regulation Voltage	1.5x Mode, I_{CPO} = 20mA 2x Mode, I_{CPO} = 20mA			4.55 5.05		V V
CLOCK Frequency		●	0.65	0.85	1.05	MHz
SDA, SCL, ENU, CAMHL						
V_{IL}		●			0.3 • DV_{CC}	V
V_{IH}		●	0.7 • DV_{CC}			V
I_{IH}	SDA, SCL, ENU, CAMHL = DV_{CC}	●	–1		1	µA
I_{IL}	SDA, SCL, ENU, CAMHL = 0V	●	–1		1	µA
V_{OL} Digital Output Low (SDA)	I_{PULLUP} = 3mA	●		0.12	0.4	V
Serial Port Timing (Notes 6, 7)						
t_{SCL}	Clock Operating Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition		0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		0.6			µs
$t_{HD,DAT(OUT)}$	Output Data Hold Time		0		900	ns
$t_{HD,DAT(IN)}$	Input Data Hold Time		0			ns
$t_{SU,DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_f	Clock Data Fall Time		20		300	ns
t_r	Clock Data Rise Time		20		300	ns
t_{SP}	Spike Suppression Time		50			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3207E/LTC3207E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C ambient operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Based on long term current density limitations. Assumes operating duty cycle of <10% under absolute maximum conditions for durations less than 10 seconds.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 5: 1.5x mode output impedance is defined as $(1.5V_{BAT} – V_{CPO})/I_{OUT}$. 2x mode output impedance is defined as $(2V_{BAT} – V_{CPO})/I_{OUT}$.

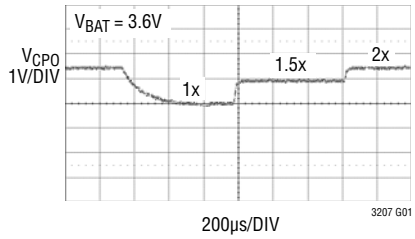
Note 6: All values are referenced to V_{IH} and V_{IL} levels.

Note 7: Guaranteed by design.

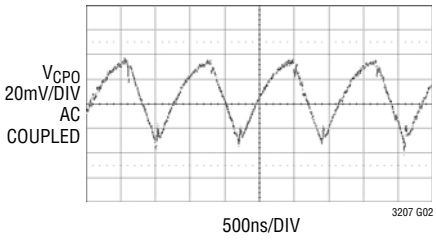
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted

Mode Switch Dropout Times

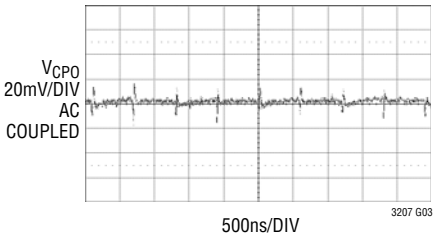


1.5x Mode CPO Ripple



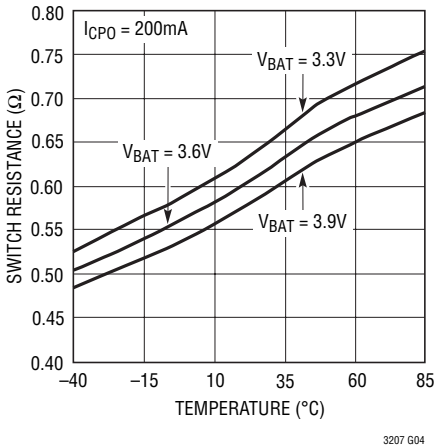
V_{BAT} = 3.6V
I_{CPO} = 200mA
C_{CPO} = 4.7µF

2x Mode CPO Ripple

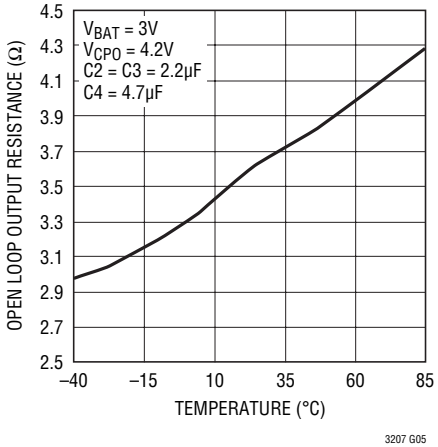


V_{BAT} = 3.6V
I_{VCPO} = 200mA
C_{CPO} = 4.7µF

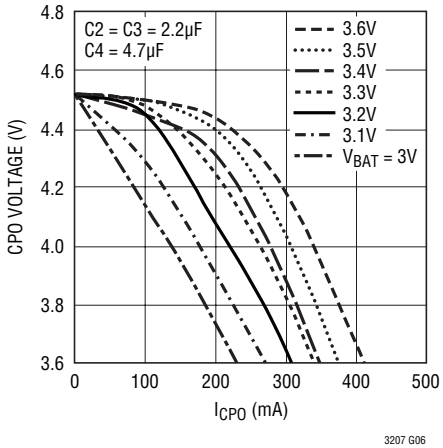
1x Mode Switch Resistance vs Temperature



1.5x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(1.5V_{BAT}-V_{CPO})/I_{CPO}$



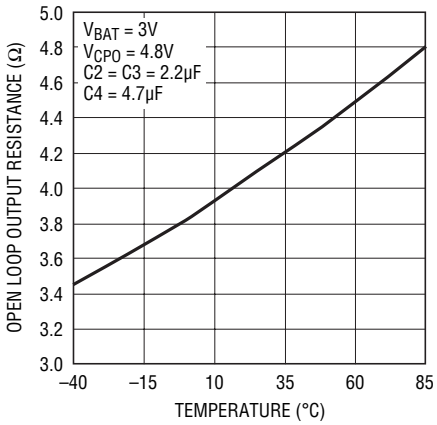
1.5x Mode CPO Voltage vs I_{CPO}



TYPICAL PERFORMANCE CHARACTERISTICS

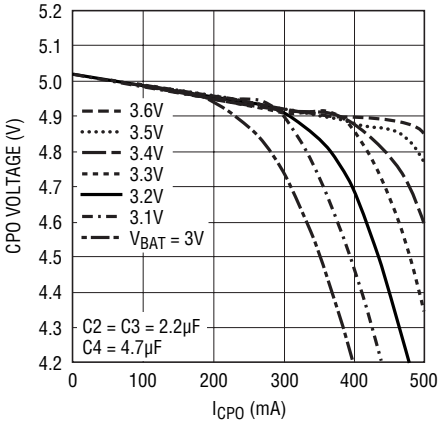
T_A = 25°C unless otherwise noted

2x Mode Charge Pump Open-Loop Output Resistance vs Temperature ($2V_{BAT}-V_{CPO})/I_{CPO}$



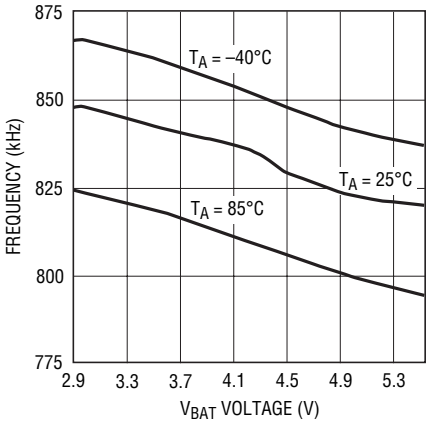
3207 G07

2x Mode CPO Voltage vs I_{CPO}



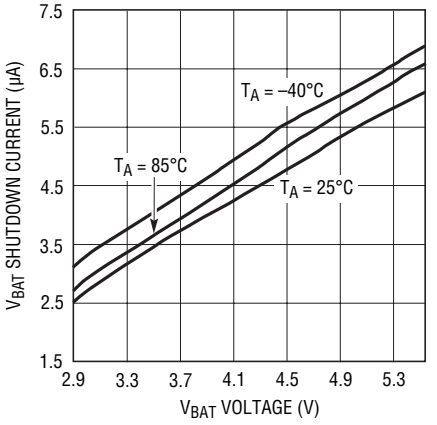
3207 G08

Oscillator Frequency vs V_{BAT} Voltage



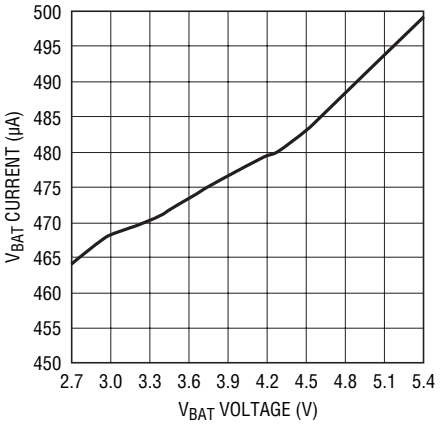
3207 G09

V_{BAT} Shutdown Current vs V_{BAT} Voltage



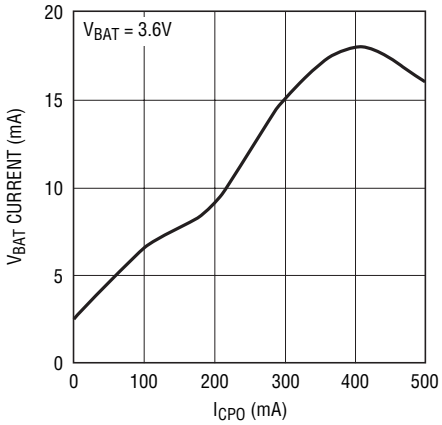
3207 G10

1x Mode No Load V_{BAT} Current vs V_{BAT} Voltage



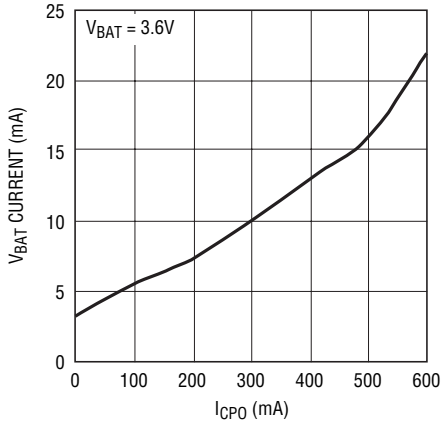
3207 G11

1.5x Mode V_{BAT} Current vs I_{CPO} ($IV_{BAT}-1.5I_{CPO}$)



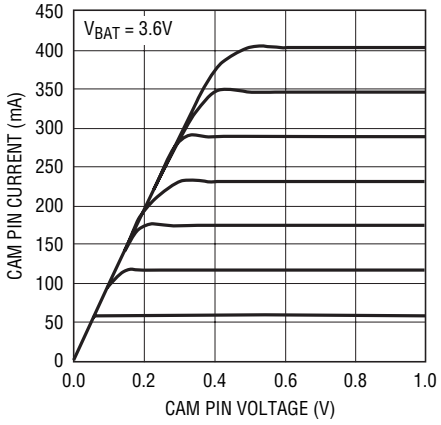
3207 G12

2x Mode V_{BAT} Current vs I_{CPO} ($IV_{BAT}-2I_{CPO}$)



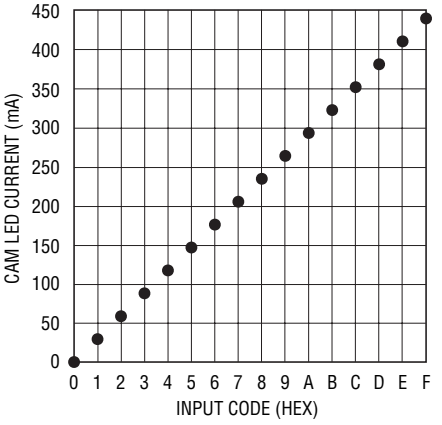
3207 G13

CAM Pin Current vs CAM Pin Voltage



3207 G14

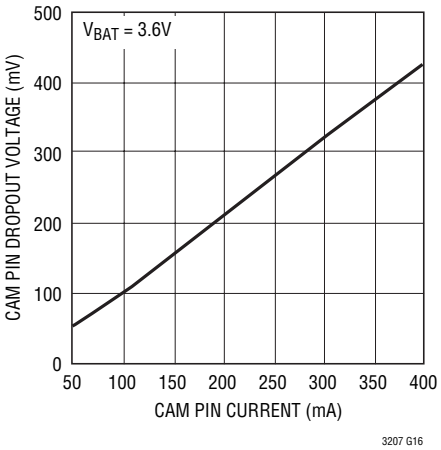
CAM LED Current vs Input Code



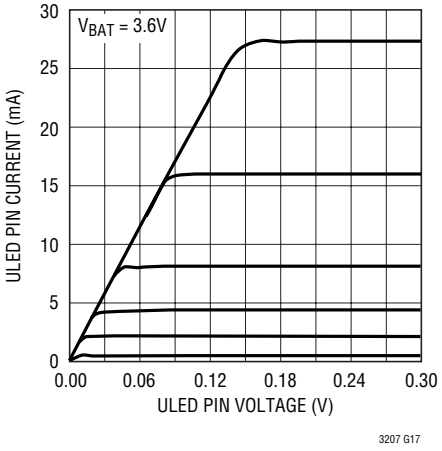
3207 G15

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

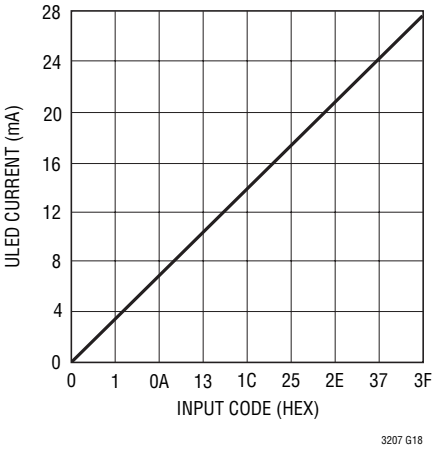
CAM Pin Dropout Voltage vs CAM Pin Current



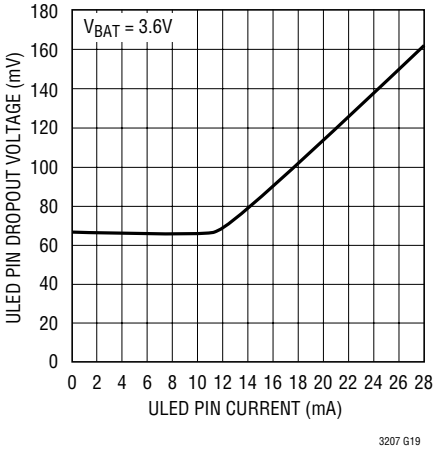
ULED Pin Current vs ULED Pin Voltage



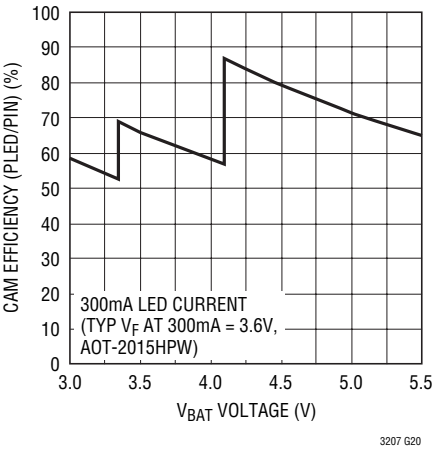
ULED Current vs Input Code



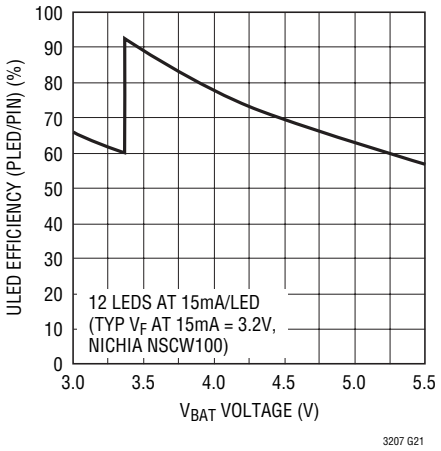
ULED Pin Dropout Voltage vs ULED Pin Current



CAM Efficiency vs V_{BAT} Voltage



12-LED ULED Display Efficiency vs V_{BAT} Voltage



PIN FUNCTIONS

CPO (Pin 1): Output of the Charge Pump. Used to power all LEDs. A 4.7µF X5R or X7R ceramic capacitor should be connected to ground.

ULED1-ULED12 (Pins 2-6, 12-18): Current Source Outputs for Driving LEDs. The LED current can be set from 0mA to 27.5mA in 64 steps via software control and internal 6-bit linear DAC. Each output can be disabled by setting the associated data register REG1 to REG12 low. ULED1 to ULED12 can also be used as I^2C controlled open-drain general purpose outputs. Connect unused outputs to ground.

CAM (Pin 7): Current Source Output for the CAM Display White LED. The LED on the CAM display can be set from 0mA to 425mA in 16 steps via software control and internal 4-bit linear DAC. Two 4-bit registers are available. One is used to program the high camera current and the second the low camera current. These registers can be selected via the serial port or the CAMHL pin. The output can be disabled by setting data in REG13 low. A safety timer will disable the output after two seconds whenever the high camera current mode is selected (see Applications Information).

PIN FUNCTIONS

CAMHL (Pin 8): Selects CAM high register when asserted high and CAM low register when low. The high to low transition automatically resets the charge pump mode to 1x. The logic level for CAMHL is referenced to DV_{CC}. If unused, the pin should be connected to ground.

DV_{CC} (Pin 9): Supply Voltage for All Digital I/O Lines. This pin sets the logic reference level of the device. DV_{CC} will reset the data registers when set below the undervoltage lockout threshold which is the recommended method for resetting the part after power up. A 0.1µF X5R or X7R ceramic capacitor should be connected to ground.

SCL (Pin 10): I^2C Clock Input. The logic-level for SCL is referenced to DV_{CC}.

SDA (Pin 11): Input Data for the Serial Port. Serial data is shifted in one bit per clock to control the device. The logic-level is referenced to DV_{CC}.

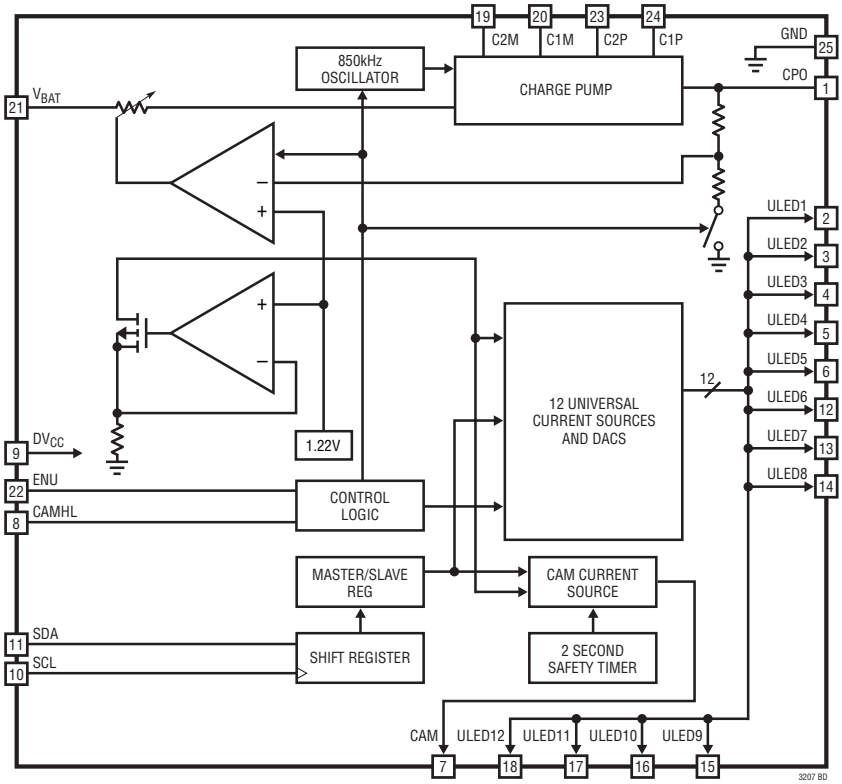
C1P, C2P, C1M, C2M (Pin 24, 23, 20, 19): Charge Pump Flying Capacitor Pins. A 2.2µF X7R or X5R ceramic capacitor should be connected from C1P to C1M and C2P to C2M.

V_{BAT} (Pin 21): Supply Voltage for the Entire Device. This pin must be bypassed with a single 2.2µF low ESR ceramic capacitor.

ENU (Pin 22): Input. Used to enable or disable the preselected ULED outputs. When the pin is toggled from low (disable) to high (enable), the device illuminates the preselected LEDs. When ENU is controlling selected outputs and other outputs have been enabled the charge pump mode will be reset to 1x on the falling edge of ENU. When ENU is controlling selected outputs and no other outputs are active the part will go from enabled to shutdown. The ENU logic-level is referenced to DV_{CC}. This pin is connected to ground if unused.

Exposed Pad (Pin 25): Ground. The Exposed Pad must be soldered to PCB ground.

BLOCK DIAGRAM



OPERATION

Power Management

The LTC3207/LTC3207-1 use a switched capacitor charge pump to boost CPO to as much as two times the input voltage up to 5.05V. The part starts up in 1x mode. In this mode, V_{BAT} is connected directly to CPO. This mode provides maximum efficiency and minimum noise. The LTC3207/LTC3207-1 will remain in 1x mode until an LED current source drops out. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. When dropout is detected, the LTC3207/LTC3207-1 will switch into 1.5x mode. The CPO voltage will then start to increase and will attempt to reach 1.5x V_{BAT} up to 4.55V. Any subsequent dropout will cause the part to enter the 2x mode. The CPO voltage will attempt to reach 2x V_{BAT} up to 5.05V.

A 2-phase non-overlapping clock activates the charge pump switches. In the 2x mode, the flying capacitors are charged on alternate clock phases from V_{BAT} to minimize CPO voltage ripple. In 1.5x mode the flying capacitors are charged in series during the first clock phase and stacked in parallel on V_{BAT} during the second phase. This sequence of charging and discharging the flying capacitors continues at a constant-frequency of 850kHz.

The current delivered by each LED current source is controlled by an associated DAC. Each DAC is programmed via the I^2C port.

Soft-Start

Initially, when the part is in shutdown, a weak switch connects V_{BAT} to CPO. This allows V_{BAT} to slowly charge the CPO output capacitor and to prevent large charging currents from occurring.

The LTC3207/LTC3207-1 also employ a soft-start feature on its charge pump to prevent excessive inrush current and supply droop when switching into the step-up modes. The current available to the CPO pin is increased linearly over a typical period of 125µs. Soft-start occurs at the start of both 1.5x and 2x mode changes.

Charge Pump Strength

When the LTC3207/LTC3207-1 operate in either 1.5x mode or 2x mode, the charge pump can be modeled as a Thevenin-equivalent circuit to determine the amount of current available from the effective input voltage and effective open-loop output resistance, R_{OL} (Figure 1).

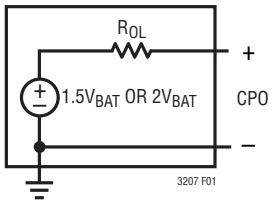


Figure 1. Equivalent Open-Loop

R_{OL} is dependent on a number of factors, including the switching term, $1/(2f_{OSC} \bullet C_{FLY})$, internal switch resistances and the non-overlap period of the switching circuit. However, for a given R_{OL}, the amount of current available will be directly proportional to the advantage voltage of $1.5V_{BAT} - CPO$ for 1.5x mode and $2V_{BAT} - CPO$ for 2x mode. Consider the example of driving LEDs from a 3.1V supply. If the LED forward voltage is 3.8V and the current sources require 100mV, the advantage voltage for 1.5x mode is 3.1V • 1.5 – 3.8V – 0.1V or 750mV. Notice that if the input voltage is raised to 3.2V, the advantage voltage jumps to 900mV, a 20% improvement in available strength.

From Figure 1, for 1.5x mode the available current is given by:

$$I_{OUT} = \frac{1.5V_{BAT} - V_{CPO}}{R_{OL}} \quad (1)$$

For 2x mode, the available current is given by:

$$I_{OUT} = \frac{2V_{BAT} - V_{CPO}}{R_{OL}} \quad (2)$$

Notice that the advantage voltage in this case is 3.1V • 2 – 3.8V – 0.1V = 2.3V. R_{OL} is higher in 2x mode but a significant overall increase in available current is achieved.

OPERATION

Mode Switching

The LTC3207/LTC3207-1 will automatically switch from 1x mode to 1.5x mode and subsequently to 2x mode whenever a dropout condition is detected at an LED pin. Dropout occurs when an active current source voltage becomes too low for the programmed current to be supplied. The mode change will not occur unless dropout has existed for approximately 400µs. This delay will allow the LEDs to warm up and achieve the final LED forward voltage value.

The mode will automatically switch back to 1x whenever a register is updated via the I^2C port, when gradation completes ramping down, on the falling edge of either ENU or CAMHL and after each blink period.

The part can be forced to operate in 1x, 1.5x or 2x mode by writing the appropriate bits into REG0. This feature may be used for powering loads from CPO.

Nonprogrammed current sources do not affect dropout. In addition, ENU controlled current sources do not affect dropout when ENU is low.

Universal Current Sources (ULED1 to ULED12)

There are twelve universal 27.5mA current sources. Each current source has a 6-bit linear DAC for current control. The output current range is 0 to full-scale in 64 steps.

Each current source is disabled when an all zero data word is written. The supply current for that source is reduced to zero. Connect unused outputs to ground.

ULED1 to ULED12 can also be used as general purpose outputs (GPO). Current sources in the GPO mode can be used as I^2C controlled open-drain drivers. The GPO mode is selected by programming REG1 to REG12, Bit 6 and Bit 7 to a logic one. In the GPO mode dropout detection is disabled, output swings to ground will not cause mode switching.

Camera Current Source

There is one CAM current source. This current source has a 4-bit linear DAC for current control. The output current range is 0mA to 425mA in 16 steps.

The current source is disabled when this section receives an all zero data word. The supply current for the current source is reduced to zero.

CAMHL

The CAMHL pin quickly selects the camera high register for flash applications without re-accessing the I^2C port. When low, the CAM current range will be controlled by the camera low 4-bit register. When CAMHL is asserted high, the current range will be set by the camera high 4-bit register. The charge pump mode will be reset to 1x on the falling edge of CAMHL.

A safety timer will disable the CAM output after two seconds whenever the high current mode is selected. To reset the safety timer, the CAMHL signal from the external pin or through the I^2C port is set low. Alternatively the CAM register can be written to all zeroes. If unused, the pin should be connected to ground.

Blinking

Each universal output (ULED1 to ULED12) can be set to blink 0.156s or 0.625s with a period of 1.25s or 2.5s via the I^2C port. The blinking rate is selected via REG15 and ULED outputs are selected via REG1 to REG12. Blinking and gradation rates are independent. Blink resets the charge pump to 1x mode after each period. Please refer to Application Note 108 for detailed information and examples on programming blinking.

Gradation

Universal LED outputs ULED1 to ULED12 can be set to have the current ramp up and down at 0.24s, 0.48s and 0.96s rates via the I^2C port. The total gradation period is longer than the ramp time since there is a region at the start and end where the ULED current does not change. A new gradation period cannot be started until after the previous gradation period has ended. Each of these outputs can have either blinking or gradation enabled. The gradation time is set via REG15 and ULED outputs are selected via REG1 to REG12. The ramp direction is controlled via REG0. Setting the UP bit high causes gradation to ramp up; setting this bit low causes gradation to ramp down. Please refer to Application Note 108 for detailed information and examples on programming gradation.

OPERATION

When gradation is disabled the LED output current remains at the programmed value. The gradation enable bit must be cleared when the gradation timer is disabled.

The charge pump mode is reset to 1x after gradation completes ramping down.

External Enable Control (ENU)

The ENU pin can be used to enable or disable the LTC3207/LTC3207-1 without reaccessing the I^2C port. This might be useful to indicate an incoming phone call without waking the micro-controller. ENU can be programmed to independently control all preselected displays. LED displays are controlled with ENU by setting the appropriate data bits in REG1 to REG12 and control bits in REG14 and REG15.

To use the ENU pin, the I^2C port must first be configured to select the desired LED outputs. When ENU is high, the selected displays will be enabled as per the REG14 and REG15 settings. When ENU is low, the selected displays will be off. If no other displays are programmed to be enabled, the chip will be in shutdown.

Gradation can also be preprogrammed for control by the ENU pin. The registers are written as required per the gradation description and the UP bit is ignored. The registers are programmed when ENU is low. When ENU is set high the part will become enabled and the selected LED outputs will ramp up. When ENU is set low the selected LED outputs will ramp low to zero current and then the part will shut down. The charge pump must be in auto mode if shutdown is required.

If the ENU pin is not used, it is connected to ground. If ENU is used and other ULED outputs are active then ENU will reset the charge pump mode to 1x on the falling edge. Please refer to Application Note 108 for detailed information and examples on programming ENU control.

Shutdown Current

Shutdown occurs when all the current source data bits have been written to zero, when DV_{CC} is set below the undervoltage lockout voltage or when ENU switches low (all other outputs disabled). The charge pump must also be in auto mode.

Although the LTC3207/LTC3207-1 are designed to have very low shutdown current, they will draw about 3.5µA from V_{BAT} when in shutdown. Internal logic ensures that the device is in shutdown when DV_{CC} is low. Note, however, that all of the logic signals that are referenced to DV_{CC} (SCL, SDA, ENU and CAMHL) will need to be at DV_{CC} or below (i.e., ground) to avoid violation of the absolute maximum specifications on these pins.

EMI Reduction

The flying capacitor pins C1M, C1P, C2M and C2P have controlled slew rates, in the 5ns to 10ns range, to reduce conducted and radiated noise.

Serial Port

The microcontroller-compatible I^2C serial port provides all of the command and control inputs for the LTC3207/LTC3207-1. Data on the SDA input is loaded on the rising edge of SCL. D7 is loaded first and D0 last. There are 16 data registers, one address register and one sub-address register. Once all address bits have been clocked into the address register, acknowledge occurs. The sub-address register is then written, followed by writing the data register. Each data register has a sub-address. After the data register has been written, a load pulse is created after the stop bit. The load pulse transfers all of the data held in the data registers to the DAC registers. The stop bit can be delayed until all of the data master registers have been written. At this point the LED current will be changed to the new settings. The serial port uses static logic registers so there is no minimum speed at which it can be operated.

I^2C Interface

The LTC3207/LTC3207-1 communicate with a host (master) using the standard I^2C 2-wire interface. The Timing Diagram (Figure 3) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus Accelerator, are required on these lines.

OPERATION

The LTC3207/LTC3207-1 are receive-only (slave) devices.

There are two I²C addresses available. The LTC3207 I²C address is 00110110 and the LTC3207-1 I²C address is 00110100. The I²C address is the only difference between the LTC3207 and the LTC3207-1.

Write Word Protocol Used by the LTC3207/LTC3207-1

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	*Sub-Address	A	Data Byte	A	P**

S = Start Condition, Wr = Write Bit = 0, A = Acknowledge,
P = Stop Condition
*The sub-address uses only the first four bits, D0, D1, D2 and D3
**Stop can be delayed until all of the data registers have been written

Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupt.

Sub-Address Byte

MSB							LSB		
7	6	5	4	3	2	1	0	Register	Function
X	X	X	X	0	0	0	0	REG0	COMMAND
X	X	X	X	0	0	0	1	REG1	ULED1
X	X	X	X	0	0	1	0	REG2	ULED2
X	X	X	X	0	0	1	1	REG3	ULED3
X	X	X	X	0	1	0	0	REG4	ULED4
X	X	X	X	0	1	0	1	REG5	ULED5
X	X	X	X	0	1	1	0	REG6	ULED6
X	X	X	X	0	1	1	1	REG7	ULED7
X	X	X	X	1	0	0	0	REG8	ULED8
X	X	X	X	1	0	0	1	REG9	ULED9
X	X	X	X	1	0	1	0	REG10	ULED10
X	X	X	X	1	0	1	1	REG11	ULED11
X	X	X	X	1	1	0	0	REG12	ULED12
X	X	X	X	1	1	0	1	REG13	CAM
X	X	X	X	1	1	1	0	REG14	ENU
X	X	X	X	1	1	1	1	REG15	G/B/ENU

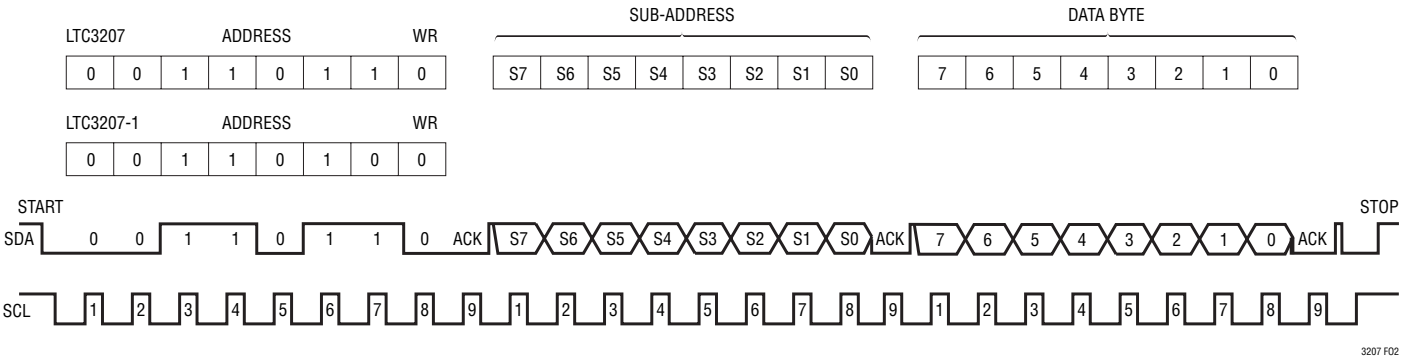


Figure 2. Bit Assignments

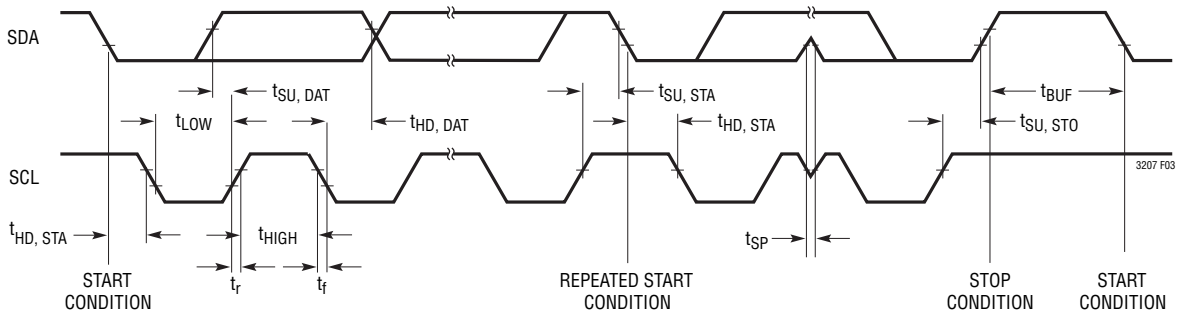


Figure 3. Timing Parameters

OPERATION

REG0, Command Byte.

Register Sub-Address = 0000

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
CAMHL	Reserved	Reserved	Reserved	Force2x	Force1p5	Quick write	UP

UP	0 1	Gradation counts down Gradation counts up
Quick write	0 1	Normal write to each register Quick write, REG1 data is written to all twelve universal registers
Force1p5	1 0	Forces charge pump into 1.5x mode Enables mode logic to control mode charges based on dropout signal
Force2x	1 0	Forces charge pump into 2x mode. Enables mode logic to control mode changes based on dropout signal
Force1x		D2 (Force1p5x) = 1 D3 (Force2x) = 1 } Forces Charge Pump Into 1x Mode
Reserved	X	
Reserved	X	
Reserved	X	
CAMHL	0 1	External control of CAM I^2C control of CAM

Data Bytes

REG1 to REG12, Universal LED 6-bit linear DAC data with blink/gradation.

Sub-Address 0001 TO 1100 per Sub-Address Table Above

ULED Mode Enable Bits			LED Current Data					
	MSB							LSB
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal	0	0	D5	D4	D3	D2	D1	D0
Blink Enabled	0	1	D5	D4	D3	D2	D1	D0
Gradation Enabled	1	0	D5	D4	D3	D2	D1	D0
GPO Mode (Gradation/Blink/Dropout Off)	1	1	D5	D4	D3	D2	D1	D0

OPERATION

REG13, Camera

LED 4-bit high and 4-bit low DAC data.

Register Sub-Address = 1101

MSB	HIGH BITS		LSB	MSB	LOW BITS		LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D3	D2	D1	D0	D3	D2	D1	D0

REG14, ENU

Setting bit high selects the outputs to be controlled by ENU.

Register Sub-Address = 1110

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ULED8	ULED7	ULED6	ULED5	ULED4	ULED3	ULED2	ULED1

REG15, ENU, Gradation and Blink Times

Setting bits 0 high to 3 high selects the outputs to be controlled by ENU. Bits 4 to 7 control gradation and blink times.

Register Sub-Address = 1111

ENU Output Selection			LSB
3	2	1	0
ULED12	ULED11	ULED10	ULED9

Sub-Address = 1111

Blink Times and Period				Gradation Ramp Times and Period			
D7	D6	Blink	Period	D5	D4	Ramp	Period
0	0	0.625s	1.25s	0	0	Disabled	Disabled
0	1	0.156s	1.25s	0	1	0.24s	0.45s
1	0	0.625s	2.5s	1	0	0.48s	0.9s
1	1	0.156s	2.5s	1	1	0.96s	1.8s

START and STOP Conditions

A bus-master signals the beginning of a communication to a slave device by transmitting a START condition.

A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Byte Format

Each byte sent to the LTC3207/LTC3207-1 must be 8 bits long followed by an extra clock cycle for the Acknowledge bit to be returned by the LTC3207/LTC3207-1. The data should be sent to the device most significant bit (MSB) first.

OPERATION

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave (LTC3207/LTC3207-1) lets the master know that the latest byte of information was received. The Acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock cycle. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse.

Slave Address

The LTC3207 responds to only one 7-bit address which has been factory programmed to 0011011. The LTC3207-1 responds to only one 7-bit address which has been factory programmed to 0011010. The eighth bit of the address byte (R/W) must be 0 for the LTC3207/LTC3207-1 to recognize the address since it is a write-only device. This effectively forces the address to be 8 bits long where the least significant bit of the address is 0. If the correct seven bit address is given but the R/W bit is 1, the LTC3207/LTC3207-1 will not respond.

Bus Write Operation

The master initiates communication with the LTC3207/LTC3207-1 with a START condition and a 7-bit address followed by the write bit R/W = 0. If the address matches that of the LTC3207/LTC3207-1, the device returns an Acknowledge. The master should then deliver the most significant sub-address byte for the data register to be written. Again, the LTC3207/LTC3207-1 acknowledge and then the data is delivered starting with the most significant bit. This cycle is repeated until all of the required data registers have been written. Any number of data registers can be written. Each data byte is transferred to an internal holding latch upon the return of an Acknowledge. After all data bytes have been transferred to the LTC3207/LTC3207-1, the master may terminate the communication with a STOP condition. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I^2C bus can be addressed. This cycle can continue indefinitely and the LTC3207/LTC3207-1 will remember the last input of valid data that they receive. Once all chips on the bus have been addressed and sent valid data, a global STOP condition can be sent and the LTC3207/LTC3207-1 will update all registers with the data that it had received.

In certain circumstances the data on the I^2C bus may become corrupt. In these cases the LTC3207/LTC3207-1 respond appropriately by preserving only the last set of complete data that they have received. For example, assume the LTC3207/LTC3207-1 have been successfully addressed and are receiving data when a STOP condition mistakenly occurs. The LTC3207/LTC3207-1 will ignore this stop condition and will not respond until a new START condition, correct address, sub-address and new set of data and STOP condition are transmitted.

Likewise, if the LTC3207/LTC3207-1 were previously addressed and sent valid data but not updated with a STOP, they will respond to any STOP that appears on the bus with only one exception, independent of the number of REPEAT-STARTs that have occurred. If a REPEAT-START is given and the LTC3207/LTC3207-1 successfully acknowledge their address and first byte, they will not respond to a STOP until all bytes of the new data have been received and acknowledged.

Quick Write

Registers REG1 to REG12 can be written in parallel by setting Bit 1 of REG0 high. When this bit is set high the next write sequence to REG1 will write the data to REG1 through REG12 which is all of the universal LED registers.

APPLICATIONS INFORMATION

V_{BAT}, CPO Capacitor Selection

The style and value of the capacitors used with the LTC3207/LTC3207-1 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) ceramic capacitors are used for both C_{VBAT} and C_{CPO}. Tantalum and aluminum capacitors are not recommended due to high ESR.

The value of C_{CPO} directly controls the amount of output ripple for a given load current. Increasing the size of C_{CPO} will reduce output ripple at the expense of higher start-up current. The peak-to-peak output ripple of the 1.5x mode is approximately given by the expression:

$$V_{RIPPLEp-p} = \frac{I_{OUT}}{3f_{OSC} \bullet C_{CPO}}$$

Where f_{OSC} is the LTC3207/LTC3207-1's oscillator frequency, or typically 850kHz, and C_{CPO} is the output storage capacitor.

The output ripple in 2x mode is very small due to the fact that load current is supplied on both cycles of the clock.

Both style and value of the output capacitor can significantly affect the stability of the LTC3207/LTC3207-1. As shown in the Block Diagram, the device uses a control loop to adjust the strength of the charge pump to match the required output current. The error signal of the loop is stored directly on the output capacitor. The output capacitor also serves as the dominant pole for the control loop. To prevent ringing or instability, it is important for the output capacitor to maintain at least 3.2µF of capacitance over all conditions and the ESR should be less than 80mΩ.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout will result in very good stability. As the value of C_{CPO} controls the amount of output ripple, the value of C_{VBAT} controls the amount of ripple present at the input pin(V_{BAT}). The LTC3207/LTC3207-1's input current will be relatively constant while the charge pump is either in the input charging phase or the output charging phase but will drop to zero during the clock nonoverlap times. Since the nonoverlap time is small (~25ns), these missing "notches" will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the higher ESR. Therefore, ceramic capacitors are recommended for low ESR. Input noise can be further reduced by powering the LTC3207/LTC3207-1 through a very small series inductor as shown in Figure 4. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant-current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

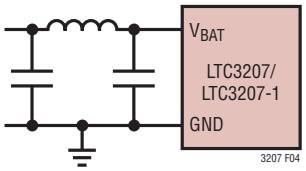


Figure 4. 10nH Inductor Used for Input Noise Reduction (Approximately 1cm of Board Trace)

APPLICATIONS INFORMATION

Flying Capacitor Selection

Warning: Polarized capacitors, such as tantalum or aluminum, should never be used for the flying capacitors since their voltage can reverse upon start-up of the LTC3207/LTC3207-1. Ceramic capacitors should always be used for the flying capacitors.

The flying capacitors control the strength of the charge pump. In order to achieve the rated output current it is necessary to have at least 1.6µF of capacitance for each of the flying capacitors. Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a very poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, overrated voltage and temperature conditions, a 1µF, 10V, Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF, 10V, X7R available in the same case. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitances at all temperatures and voltages.

Table 1 shows a list of ceramic capacitor manufacturers and how to contact them:

Table 1. Recommended Capacitor Vendors

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com

Layout Considerations and Noise

The LTC3207/LTC3207-1 have been designed to minimize EMI. However due to the high switching frequency and the transient currents produced by the LTC3207/LTC3207-1, careful board layout is necessary. A true ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions.

The flying capacitor pins, C1P, C2P, C1M and C2M, will have 5ns to 10ns edge-rate waveforms. The large dv/dt on these pins can couple energy capacitively to adjacent PCB runs. Magnetic fields can also be generated if the flying capacitors are not close to the LTC3207/LTC3207-1 (i.e., the loop area is large). To decouple capacitive energy transfer, a Faraday shield may be used. This is a grounded PCB trace between the sensitive node and the LTC3207/LTC3207-1 pins. For a high quality AC ground, it should be returned to a solid ground plane that extends all the way to the LTC3207/LTC3207-1.

APPLICATIONS INFORMATION

Power Efficiency

To calculate the power efficiency (η) of an LED driver chip, the LED power should be compared to the input power. The difference between these two numbers represents lost power whether it is in the charge pump or the current sources. Stated mathematically, the power efficiency is given by:

$$\eta = \frac{P_{LED}}{P_{IN}}$$

The efficiency of the LTC3207/LTC3207-1 depends upon the mode in which they are operating. Recall that the LTC3207/LTC3207-1 operate as pass switches, connecting V_{BAT} to CPO, until dropout is detected at the I_{LED} pin. This feature provides the optimum efficiency available for a given input voltage and LED forward voltage. When it is operating as a switch, the efficiency is approximated by:

$$\eta = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet I_{BAT}} = \frac{V_{LED}}{V_{BAT}}$$

since the input current will be very close to the sum of the LED currents.

At moderate to high output power, the quiescent current of the LTC3207/LTC3207-1 is negligible and the expression above is valid.

Once dropout is detected at any the LED pin, the LTC3207/LTC3207-1 enable the charge pump in 1.5x mode.

In 1.5x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 1.5 times the actual input voltage. This is because the input current for a 1.5x charge pump is approximately 1.5 times the load current. In an ideal 1.5x charge pump, the power efficiency would be given by:

$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet 1.5 \bullet I_{LED}} = \frac{V_{LED}}{1.5 \bullet V_{BAT}}$$

Similarly, in 2x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 2x the actual input voltage. In an ideal 2x charge pump, the power efficiency would be given by:

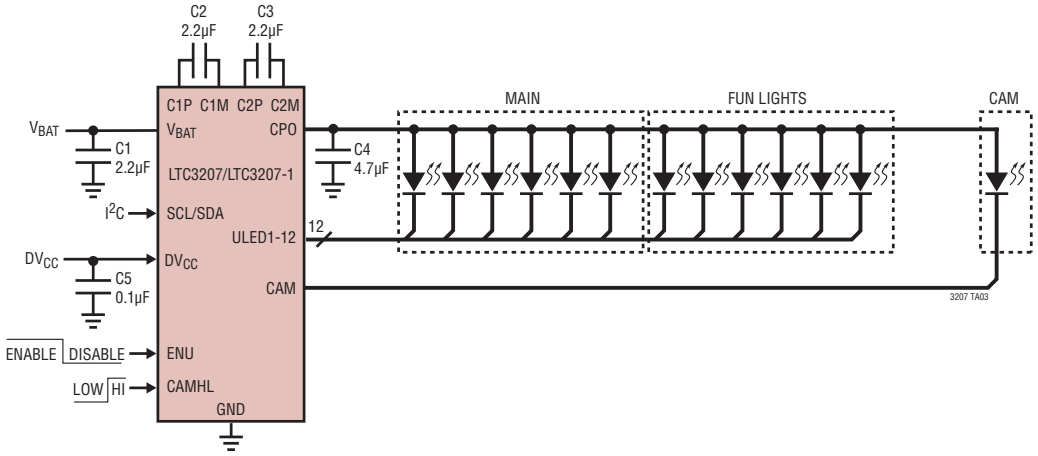
$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet 2 \bullet I_{LED}} = \frac{V_{LED}}{2 \bullet V_{BAT}}$$

Thermal Management

For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3207/LTC3207-1. If the junction temperature increases above approximately 150°C the thermal shutdown circuitry will automatically deactivate the output current sources and charge pump. To reduce maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the Exposed Pad to a ground plane and maintaining a solid ground plane under the device will reduce the thermal resistance of the package and PC board considerably.

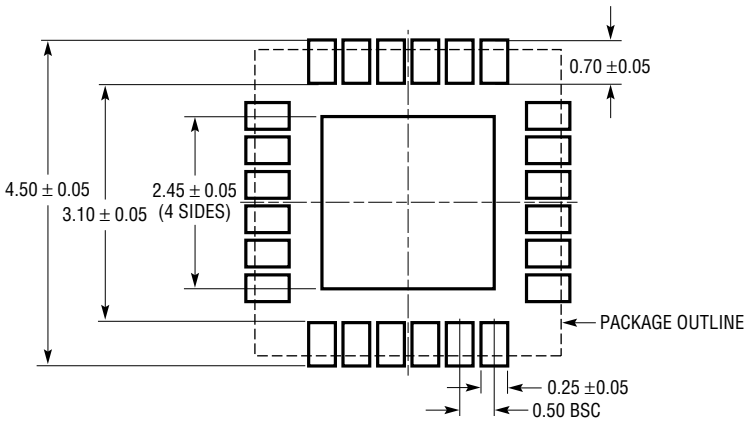
TYPICAL APPLICATIONS

6-LED MAIN, 6-LED Fun Lights Plus Low/High Camera Light

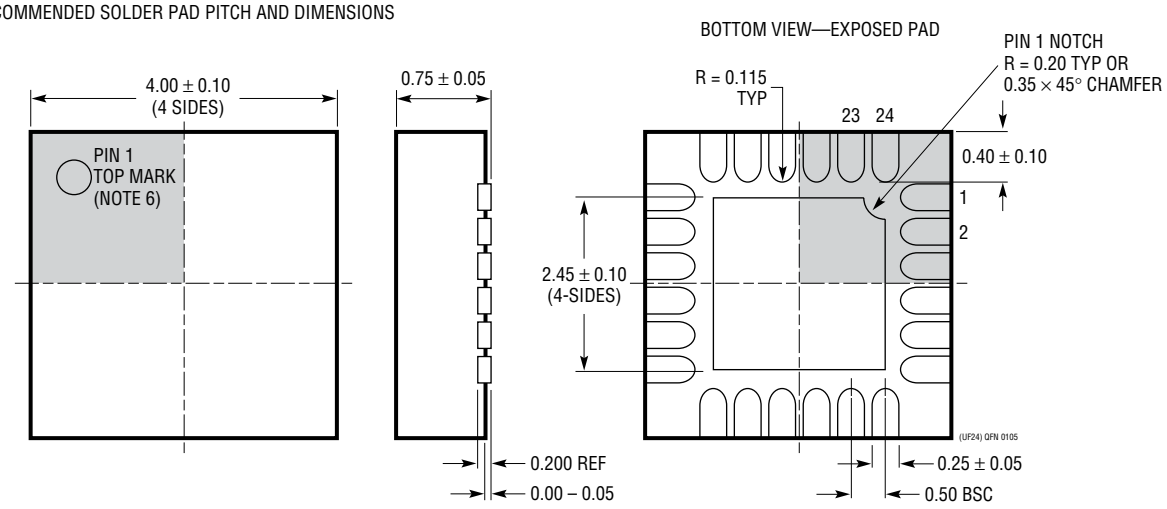


PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE