High Current Software Configurable Multidisplay LED Controller

FEATURES

- **1x/1.5x/2x Charge Pump Provides Up to 95% Efficiency**
- **Up to 1A Total Output Current**
- **17 Current Sources Available as MAIN, SUB, RGB, CAM and AUX LED Drivers**
- **LED ON/OFF, Brightness Level and Display Configuration Programmable Using 2-Wire I²C™ Interface**
- Low Noise Constant Frequency Operation with Flying Capacitor Edge Rate Control
- Automatic Charge Pump Mode Switching
- Internal Soft-Start Limits Inrush Current During Startup and Mode Switching
- Open/Shorted LED Protection
- Short-Circuit/Thermal Protection
- 256 Brightness States for MAIN and SUB Displays
- 4096 Color Combinations for the RGB Display
- 5mm × 5mm 32-Lead QFN Plastic Package

APPLICATIONS

- Video/Camera Phones with QVGA + Displays

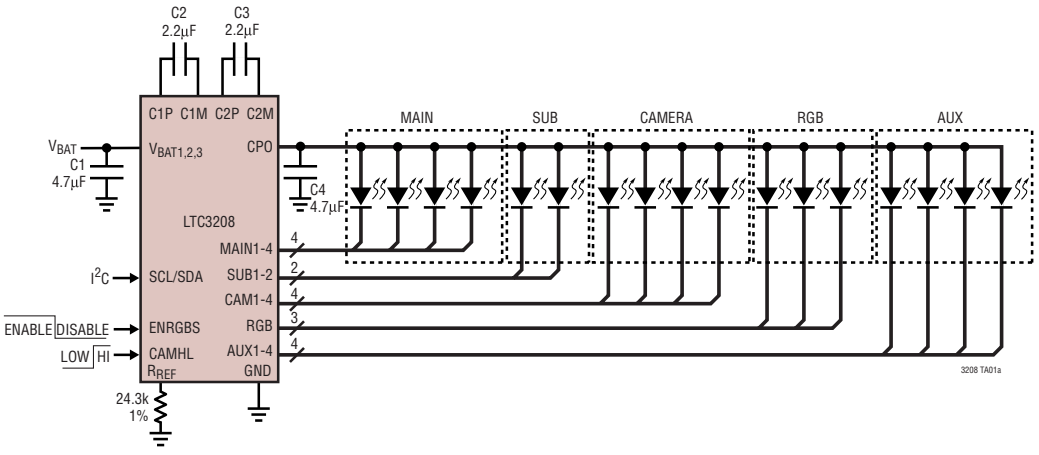
DESCRIPTION

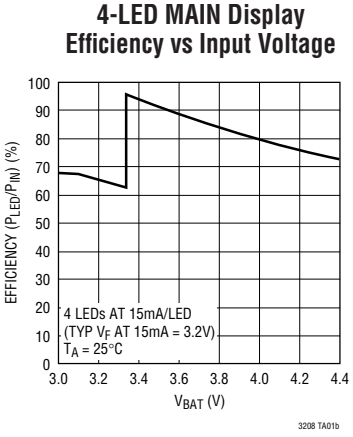
The LTC®3208 is a highly integrated multidisplay LED controller. The part contains a 1A high efficiency, low noise charge pump to provide power to the MAIN, SUB, RGB, CAM and AUX LED displays. The LTC3208 requires only small ceramic capacitors and one current set resistor to form a complete LED power supply and current controller.

The maximum display currents are set by a single external resistor. Current for each LED is controlled by a precision internal current source. Dimming and On/Off for all displays is achieved via the I²C serial interface. 256 brightness levels are available for the MAIN and SUB displays. 16 levels are available for the RGB and CAM displays. Four AUX current sources can be independently assigned via the I²C port to the CAM, SUB, MAIN or AUX DAC controlled displays.

The LTC3208 charge pump optimizes efficiency based on the voltage across the LED current sources. The part powers up in 1x mode and will automatically switch to boost mode whenever any enabled LED current source begins to enter dropout. The first dropout switches the part into 1.5x mode and a subsequent dropout switches the LTC3208 into 2x mode. The part is available in a small 5mm × 5mm 32-lead QFN package.

TYPICAL APPLICATION



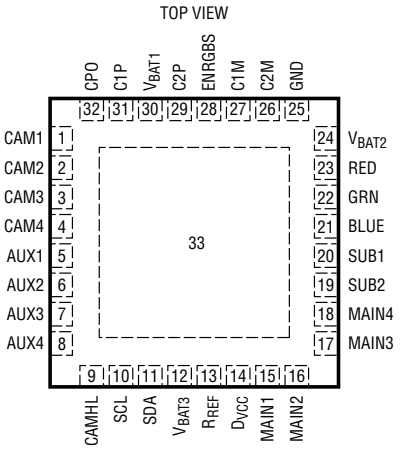


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BAT}, DV_{CC}, CPO to GND ..... – 0.3 to 6V
SDA, SCL, ENRGBS, CAMHL ..... – 0.3V to (DV_{CC} + 0.3V)
I_{CPO} (Note 2) 1.3A
$I_{MAIN1-4}$, I_{SUB1-2} (Note 3) 33mA
I_{RED}, I_{GRN}, I_{BLUE} (Note 3) 33mA
I_{CAM1-4}, I_{AUX1-4} (Note 3) 120mA
CPO, R_{REF} Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 4) .. – 40°C to 85°C
Storage Temperature Range..... – 65°C to 125°C

PACKAGE/ORDER INFORMATION



UH PACKAGE
32-LEAD (5mm × 5mm) QFN
EXPOSED PAD IS GND (PIN 33)
MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 34°C/W

ORDER PART NUMBER	UH PART MARKING
LTC3208EUH	3208

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BAT} = 3.6V, DV_{CC} = 3V, ENRGBS = Hi, R_{REF} = 24k, C2 = C3 = 2.2µF, C1 = C4 = 4.7µF, unless otherwise noted.

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT} Operating Voltage		●	2.9		4.5	V
I_{VBAT} Operating Current	I_{CPO} = 0, 1x Mode, LEDs Disabled I_{CPO} = 0, 1.5x Mode I_{CPO} = 0, 2x Mode			280 4.7 7		µA mA mA
DV_{CC} Operating Voltage		●	1.5		5.5	V
DV_{CC} Operating Current	DV_{CC} = 1.8V, Serial Port Idle	●			1	µA
V_{BAT} UVLO Threshold				1.5		V
DV_{CC} UVLO Threshold				1		V
V_{BAT} Shutdown Current	DV_{CC} = 1.8V			3.2		µA
R_{REF}						
VR_{REF}		●	1.195	1.215	1.235	V
RR_{REF}	Reference Resistor Range	●	22		30	k
White LED Current (MAIN1-4, SUB1-2), 8-Bit Linear DACs						
Full-Scale LED Current	MAIN, SUB = 1V	●	25.3	27.5	29.7	mA
Minimum (1LSB) LED Current	MAIN, SUB = 1V			108		µA
LED Current Matching	Any Two MAIN or SUB Outputs, 50% FS			1		%
LED Dropout Voltage	I_{LED} = FS			180		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BAT} = 3.6V, DV_{CC} = 3V, ENRGBS = Hi, R_{REF} = 24k, C2 = C3 = 2.2µF, C1 = C4 = 4.7µF, unless otherwise noted.

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
White LED Current (CAM1-4), 4-Bit Linear DAC						
Full-Scale LED Current	CAM = 1V	●	92.5	102.5	112.5	mA
Minimum (1LSB) LED Current	CAM = 1V			6.96		mA
LED Current Matching	Any Two CAM Outputs, 50% FS			1		%
LED Dropout Voltage	I_{LED} = FS			540		mV
White LED Current (AUX1-4, AUX Outputs Assigned to AUX DAC), 4-Bit Linear DAC						
Full-Scale LED Current	AUX = 1V	●	23	26	28.5	mA
Minimum (1LSB) LED Current	AUX = 1V			1.73		mA
LED Current Matching	Two AUX Outputs, 50% FS			1		%
LED Dropout Voltage	I_{LED} = FS			140		mV
Full-Scale AUX LED Current Full-Scale AUX LED Current	AUX Connected to CAM DAC, AUX = 1V AUX Connected to SUB or MAIN DAC, AUX = 1V			104.9 28.1		mA mA
RGB LED Current (RED, GREEN, BLUE), 4-Bit Exponential DAC						
DAC Code 0001	RED, GREEN, BLUE = 1V			0.24		mA
DAC Code 0010	RED, GREEN, BLUE = 1V			0.32		mA
DAC Code 0011	RED, GREEN, BLUE = 1V			0.46		mA
DAC Code 0100	RED, GREEN, BLUE = 1V			0.63		mA
DAC Code 0101	RED, GREEN, BLUE = 1V			0.89		mA
DAC Code 0110	RED, GREEN, BLUE = 1V			1.22		mA
DAC Code 0111	RED, GREEN, BLUE = 1V			1.74		mA
DAC Code 1000	RED, GREEN, BLUE = 1V			2.42		mA
DAC Code 1001	RED, GREEN, BLUE = 1V			3.47		mA
DAC Code 1010	RED, GREEN, BLUE = 1V			4.73		mA
DAC Code 1011	RED, GREEN, BLUE = 1V			6.7		mA
DAC Code 1100	RED, GREEN, BLUE = 1V			9.47		mA
DAC Code 1101	RED, GREEN, BLUE = 1V			13.56		mA
DAC Code 1110	RED, GREEN, BLUE = 1V			19.05		mA
DAC Code 1111	RED, GREEN, BLUE = 1V			27.06		mA
Charge Pump (CPO)						
1x Mode Output Impedance				0.35		
1.5x Mode Output Impedance	V_{BAT} = 3V, V_{CPO} = 4.2V (Note 5)			2		
2x Mode Output Impedance	V_{BAT} = 3V, V_{CPO} = 4.8V (Note 5)			2.2		
CPO Voltage Regulation	1.5x Mode, I_{CPO} = 2mA 2x Mode, I_{CPO} = 2mA			4.53 5.02		V V
CLOCK Frequency		●	0.6	0.9	1.2	MHz
SDA, SCL, ENRGBS, CAMHL						
V_{IL}, (Low Level Input Voltage)		●			0.3 • DV_{CC}	V
V_{IH}, (High Level Input Voltage)		●	0.7 • DV_{CC}			V
V_{OL}, Digital Output Low (SDA)	I_{PULLUP} = 3mA	●		0.18	0.4	V
I_{IH}	SDA, SCL, ENRGBS, CAMHL = DV_{CC}	●	–1		1	µA
I_{IL}	SDA, SCL, ENRGBS, CAMHL = 0V	●	–1		1	µA
Serial Port Timing (Notes 6, 7)						
t_{SCL}	Clock Operating Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition		0.6			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BAT} = 3.6V, DV_{CC} = 3V, ENRGBS = Hi, R_{REF} = 24k, C2 = C3 = 2.2µF, C1 = C4 = 4.7µF, unless otherwise noted.

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU,STA}$	Repeated Start Condition Setup Time		0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		0.6			µs
$t_{HD,DAT(OUT)}$	Data Hold Time		0		900	ns
$t_{HD,DAT(IN)}$	Input Data Hold Time		0			ns
$t_{SU,DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
t_f	Clock Data Fall Time		20		300	ns
t_r	Clock Data Rise Time		20		300	ns
t_{SP}	Spike Suppression Time		50			ns

Note 1: Absolute Maximum Ratings are those values beyond which the MTBF of a device may be impaired.

Note 2: Based on long-term current density limitations. Assumes an operating duty cycle of ≤10% under absolute maximum conditions for durations less than 10 seconds. Max charge pump current for continuous operation is 500mA.

Note 3: Based on long-term current density limitations.

Note 4: The LTC3208E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C ambient operating temperature range are assured by design, characterization and correlation with statistical process controls.

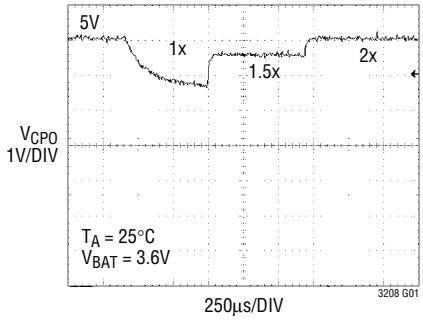
Note 5: 1.5x mode output impedance is defined as $(1.5V_{BAT} – V_{CPO})/I_{OUT}$. 2x mode output impedance is defined as $(2V_{BAT} – V_{CPO})/I_{OUT}$.

Note 6: All values are referenced to V_{IH} and V_{IL} levels.

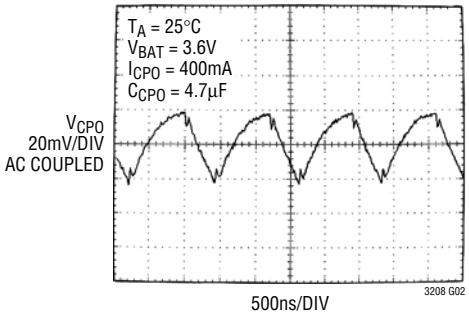
Note 7: Guaranteed by Design.

TYPICAL PERFORMANCE CHARACTERISTICS

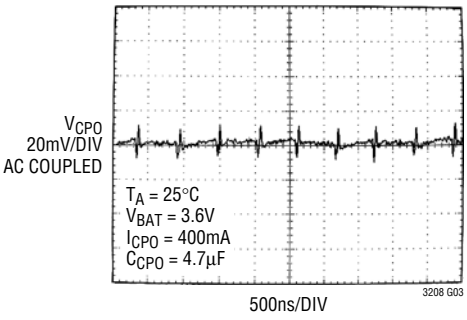
Mode Switch Dropout Times



1.5x Mode CPO Ripple

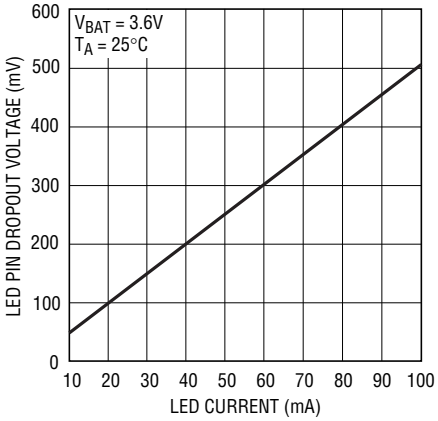


2x Mode CPO Ripple



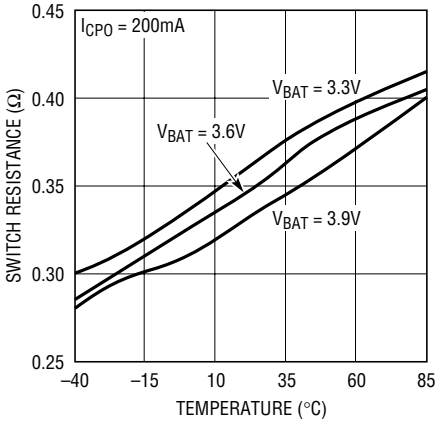
TYPICAL PERFORMANCE CHARACTERISTICS

LED Pin Dropout Voltage vs LED Pin Current



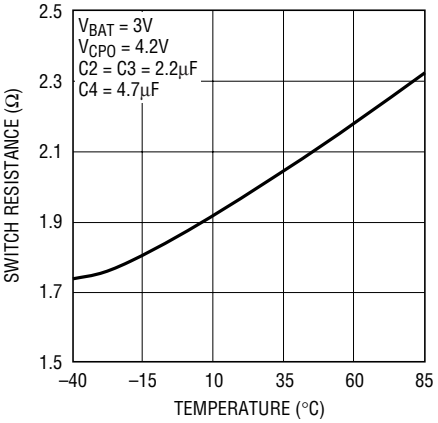
3208 G04

1x Mode Switch Resistance vs Temperature



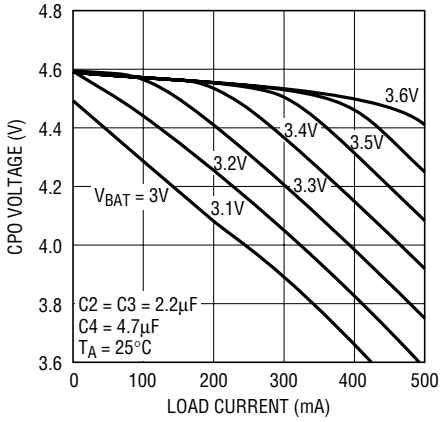
3208 G05

1.5x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(1.5V_{BAT} – V_{CPO})/I_{CPO}$



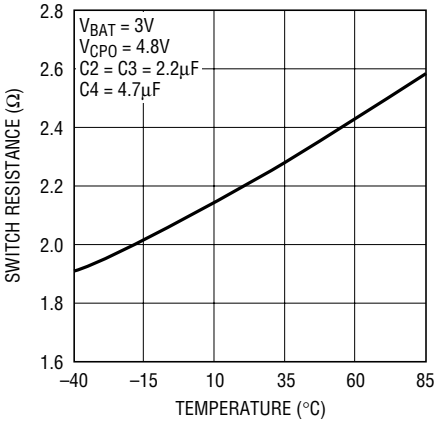
3208 G06

1.5x Mode CPO Voltage vs Load Current



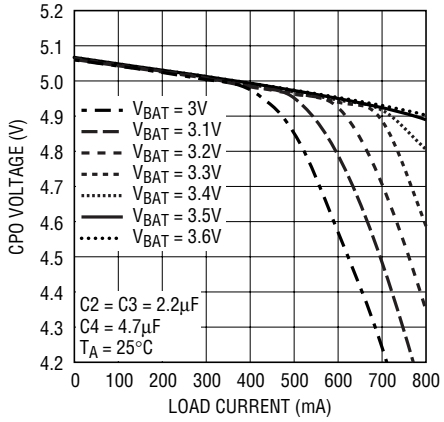
3208 G07

2x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(2V_{BAT} – V_{CPO})/I_{CPO}$



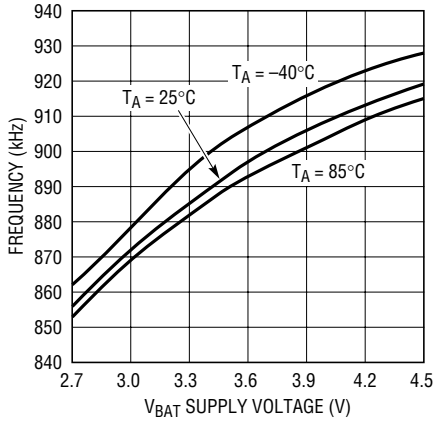
3208 G08

2x Mode CPO Voltage vs Load Current



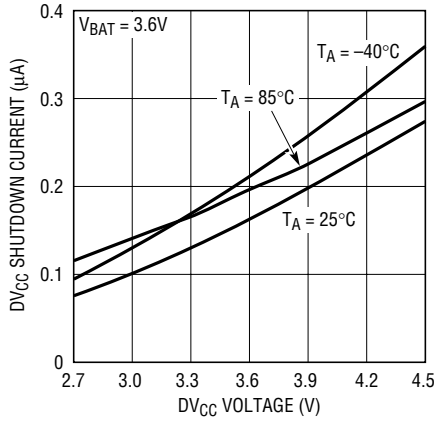
3208 G09

Oscillator Frequency vs Supply Voltage



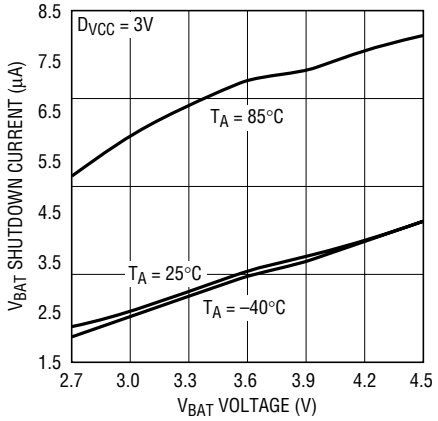
3208 G10

DV_{CC} Shutdown Current vs DV_{CC} Voltage



3208 G11

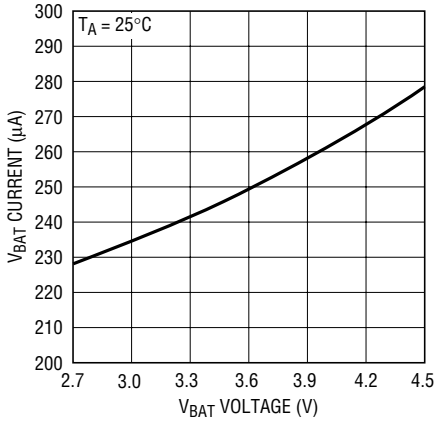
V_{BAT} Shutdown Current vs V_{BAT} Voltage



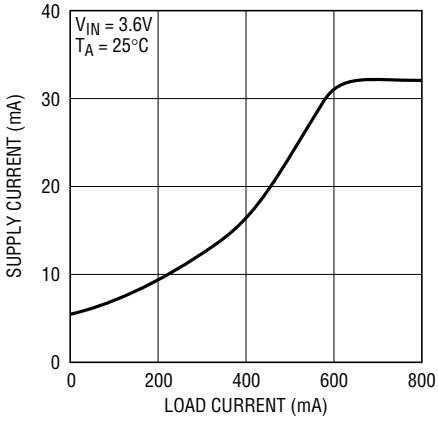
3208 G12

TYPICAL PERFORMANCE CHARACTERISTICS

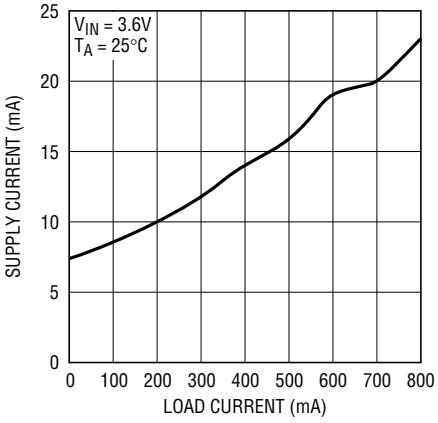
1x Mode No Load V_{BAT} Current vs V_{BAT} Voltage



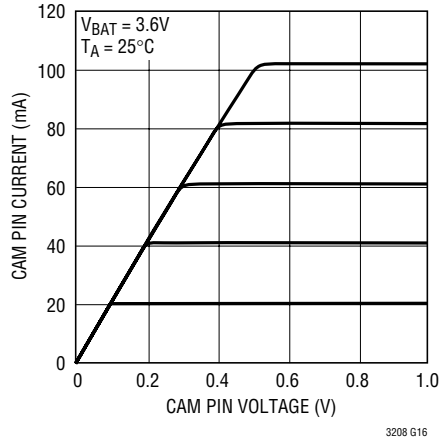
1.5x Mode Supply Current vs I_{CPO} ($IV_{BAT} - 1.5I_{CPO}$)



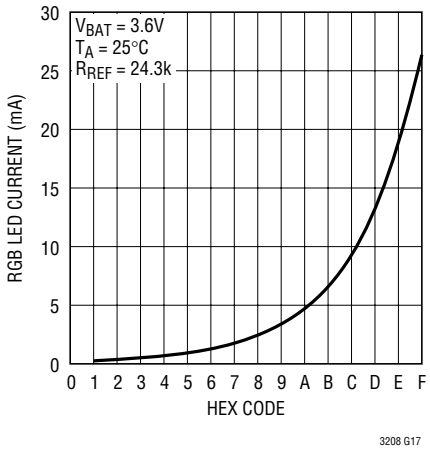
2x Mode Supply Current vs I_{CPO} ($IV_{BAT} - 2I_{CPO}$)



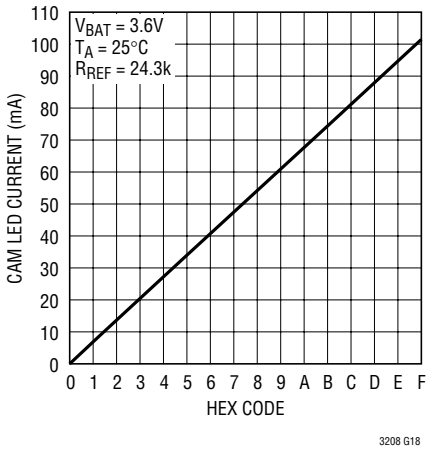
CAM Pin Current vs CAM Pin Voltage



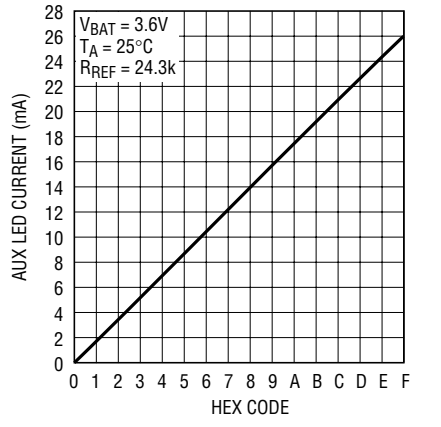
RGB LED Current vs Input Code



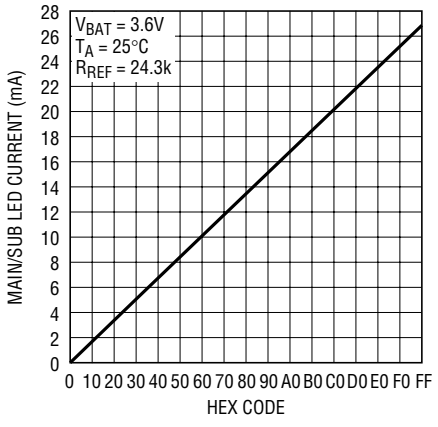
CAM LED Current vs Input Code



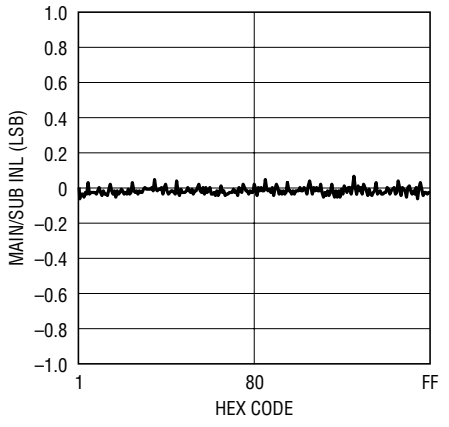
AUX LED Current vs Input Code



Main/Sub LED Current vs Input Code



Main/Sub INL



PIN FUNCTIONS

CAM1-4 (Pins 1, 2, 3, 4): Current Source Outputs for the CAM Display White LEDs. The LEDs on the CAM display can be set from 0mA to 102mA in 16 steps via software control and internal 4-bit linear DAC. Two 4-bit registers are available. One is used to program the high camera current and the second the low camera current. These registers can be selected via the serial port or the CAMHL pin. Each output can be disabled by connecting the output to CPO. Setting data in REGF to 0 disables all CAM outputs. (See Applications Information.)

AUX1-4 (Pins 5, 6, 7, 8): Current Source Outputs for the AUX Display White LEDs. When used as a separate display, the LED current sources of the AUX display can be set from 0mA to 26mA in 16 steps via software control and internal 4-bit linear DAC. In addition, these outputs can be connected individually as needed to the CAM, SUB or MAIN displays and driven from each display's associated DAC. AUX 1, 2 and 3 can be disabled by connecting the output to CPO. AUX 4 can be used as an open drain I^2C controlled logic output but cannot be disabled by connecting to CPO when configured as logic output. Setting data in REGE and REGB2 to 0 disables all AUX outputs. (See Applications Information.)

CAMHL (Pin 9): Logic Input. Selects CAM high register when asserted High and CAM Low Register when low. The high to low transition automatically resets the charge pump mode to 1x.

SCL (Pin 10): I^2C Clock Input. The logic level for SCL is referenced to DV_{CC}.

SDA (Pin 11): I^2C Data Input for the Serial Port. Serial data is shifted in one bit per clock to control the LTC3208. The logic level is referenced to DV_{CC}.

$V_{BAT3, 2, 1}$ (Pins 12, 24, 30): Supply Voltage for the Entire Device. Three separate pins are used to isolate the charge pump from the analog sections to reduce noise. All pins must be connected together externally and bypassed with a 4.7µF low ESR ceramic capacitor. The 4.7µF bypass capacitor should be connected close to V_{BAT2}. A 0.1µF capacitor should be connected close to V_{BAT3}.

R_{REF} (Pin 13): Controls the Maximum Amount of LED Current for all Displays. The R_{REF} voltage is 1.215V. An external resistor to ground sets the reference currents for all display DACs and support circuits. Since this resistor biases all circuits within the LTC3208, the value is limited to a range of 22k to 30k.

DV_{CC} (Pin 14): Supply Voltage for all Digital I/O Lines. This pin sets the logic reference level of the LTC3208. A UVLO circuit on the DV_{CC} pin forces all registers to all 0s whenever DV_{CC} is below the DV_{CC} UVLO threshold. Bypass to GND with a 0.1µF capacitor.

MAIN1-4 (Pins 15,16,17,18): Current Source Outputs for the MAIN Display White LEDs. The LEDs on the MAIN display can be set from 0µA to 27.5mA in 256 steps via software control and internal 8-bit linear DAC. Each output can be disabled externally by connecting the output to CPO. Setting data in REGC to 0 disables all MAIN outputs.

SUB2, SUB1 (Pins 19, 20): Current Source Outputs for the SUB Display White LEDs. The LEDs on the SUB display can be set from 0µA to 27.5mA in 256 steps via software control and an internal 8-bit linear DAC. Each output can be disabled externally by connecting the output to CPO. Setting the data in REGD to 0 disables all SUB outputs.

PIN FUNCTIONS

BLUE, GRN, RED (Pins 21, 22, 23): Current Source Outputs for the RGB Illuminator LEDs. The RGB currents can be independently set via the serial port. Currents up to 27mA can be programmed over 16 steps via the three internal 4-bit exponential DACs. These outputs can also be used as open drain I^2C controlled logic outputs. When configured this way, these outputs cannot be externally disabled by connecting to CPO. Setting data to 0 in REGA1 disables RED, REGA2 disables GREEN and REGB1 disables BLUE.

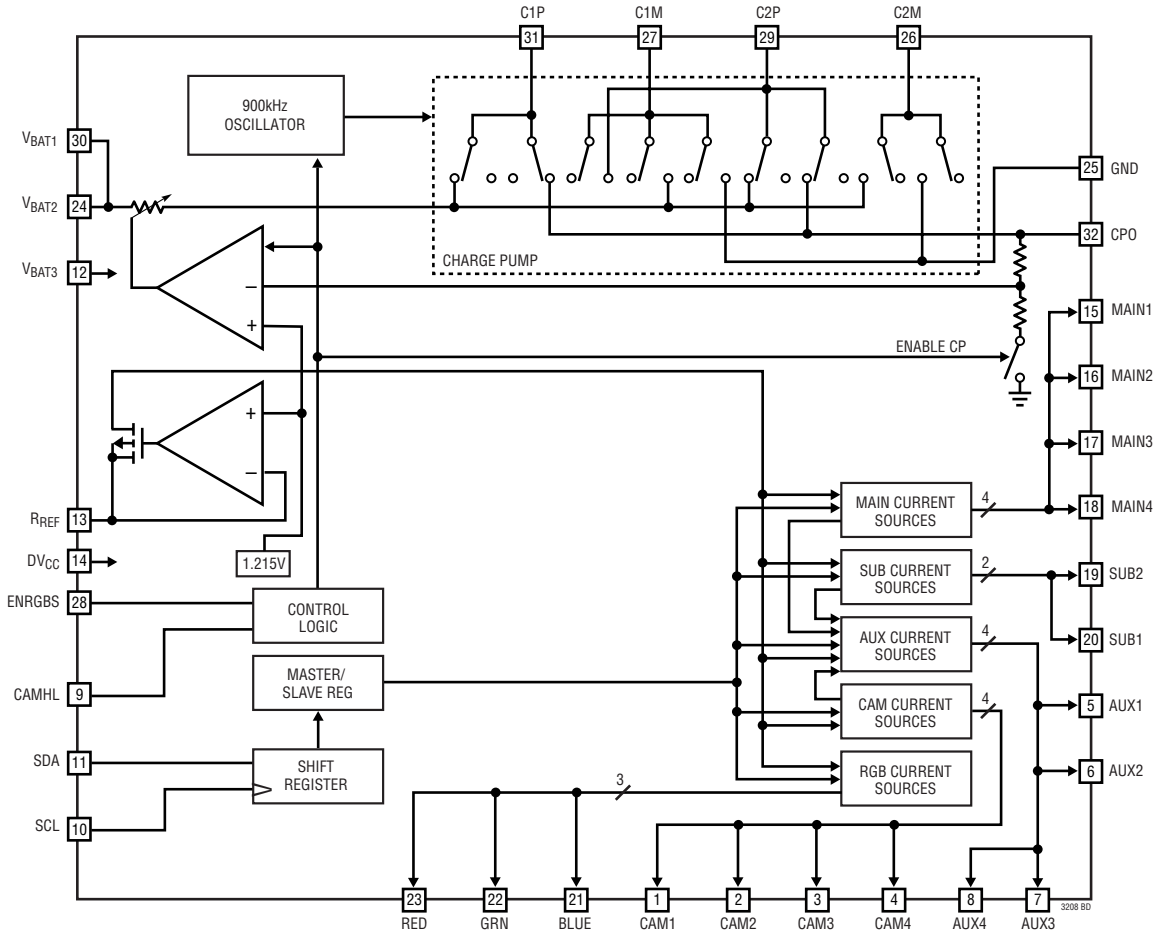
GND (Pins 25, 33): System Ground. Connect Pin 25 and exposed pad Pin 33 directly to a low impedance ground plane.

C2M, C1M, C2P, C1P (Pins 26, 27, 29, 31): Charge Pump Flying Capacitor Pins. 2.2µF X7R or X5R ceramic capacitors should be connected from C1P to C1M and C2P to C2M.

ENRGBS (Pin 28): Logic Input. This pin is normally high and is used to enable or disable the RED, GREEN and BLUE LEDs or the SUB LEDs. The selection between RGB or SUB is made via an internal programmable bit. When the pin is toggled from low (disable) to high (enable), the LTC3208 illuminates either the RGB display with a color combination that was previously programmed, or the SUB display at its previously programmed current. The logic level is referenced to DV_{CC}.

CPO (Pin 32): Output of the Charge Pump Used to Power All LEDs. A 4.7µF X5R or X7R ceramic capacitor should be connected to ground.

BLOCK DIAGRAM



OPERATION

Power Management

The LTC3208 uses a switched capacitor charge pump to boost CPO to as much as 2 times the input voltage up to 5V. The part starts up in 1x mode. In this mode, $V_{BAT1,2}$ are connected directly to CPO. This mode provides maximum efficiency and minimum noise. The LTC3208 will remain in this mode until an LED current source drops out. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. When dropout is detected, the LTC3208 will switch into 1.5x mode. The CPO voltage will then start to increase and will attempt to reach 1.5x V_{BAT} up to 4.5V. Any subsequent dropout will cause the part to enter the 2X mode. The CPO voltage will attempt to reach 2x V_{BAT} up to 5V. The part will be reset to 1x mode whenever a DAC data bit is updated via the I^2C port or on the falling edge of the CAMHL signal.

A two-phase nonoverlapping clock activates the charge pump switches. In the 2x mode the flying capacitors are charged on alternate clock phases from V_{BAT} to minimize input current ripple and CPO voltage ripple. In 1.5x mode the flying capacitors are charged in series during the first clock phase and stacked in parallel on V_{BAT} during the second phase. This sequence of charging and discharging the flying capacitors continues at a constant frequency of 900kHz.

The currents delivered by the LED current sources are controlled by an associated DAC. Each DAC is programmed via the I^2C port. The full scale DAC currents are set by R_{REF}. The value of R_{REF} is limited to the range of 22k to 30k.

OPERATION

Soft-Start

Initially, when the part is in shutdown, a weak switch connects V_{BAT} to CPO. This allows $V_{BAT1,2}$ to slowly charge the CPO output capacitor and prevent large charging currents to occur.

The LTC3208 also employs a soft-start feature on its charge pump to prevent excessive inrush current and supply voltage droop when switching into the step-up modes. The current available to the CPO pin is increased linearly over a typical period of 150µs. Soft start occurs at the start of both 1.5x and 2x mode changes.

Charge Pump Strength

When the LTC3208 operates in either 1.5x mode or 2x mode, the charge pump can be modeled as a Thevenin-equivalent circuit to determine the amount of current available from the effective input voltage and effective open-loop output resistance, R_{OL} (Figure 1).

R_{OL} is dependent on a number of factors including the switching term, $1/(2f_{OSC} \bullet C_{FLY})$, internal switch resistances and the nonoverlap period of the switching circuit. However, for a given R_{OL}, the amount of current available will be directly proportional to the advantage voltage of $1.5V_{BAT}$ - CPO for 1.5x mode and $2V_{BAT}$ - CPO for 2x mode. Consider the example of driving white LEDs from a 3.1V supply. If the LED forward voltage is 3.8V and the current sources require 100mV, the advantage voltage for 1.5x mode is $3.1V \bullet 1.5 - 3.8V - 0.1V$ or 750mV. Notice that if the input voltage is raised to 3.2V, the advantage voltage jumps to 900mV-a 20% improvement in available strength.

From Figure 1, for 1.5x mode the available current is given by:

$$I_{OUT} = \frac{1.5V_{BAT} - V_{CPO}}{R_{OL}} \quad (1)$$

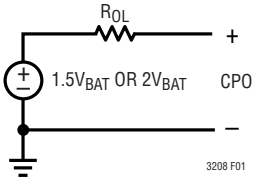


Figure 1. Charge Pump Thevenin–Equivalent Open-Loop Circuit

For 2X mode, the available current is given by:

$$I_{OUT} = \frac{2V_{BAT} - V_{CPO}}{R_{OL}} \quad (2)$$

Notice that the advantage voltage in the 2x case is $3.1V \bullet 2 - 3.8V - 0.1V = 2.3V$. R_{OL} is higher in 2x mode, but a significant overall increase in available current is achieved.

Typical values of R_{OL} as a function of temperature are shown in Figure 2 and Figure 3.

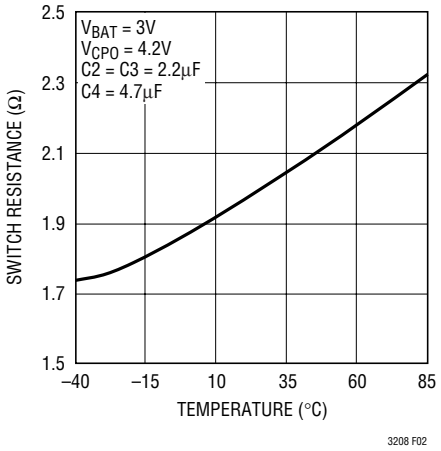


Figure 2. Typical 1.5x R_{OL} vs Temperature

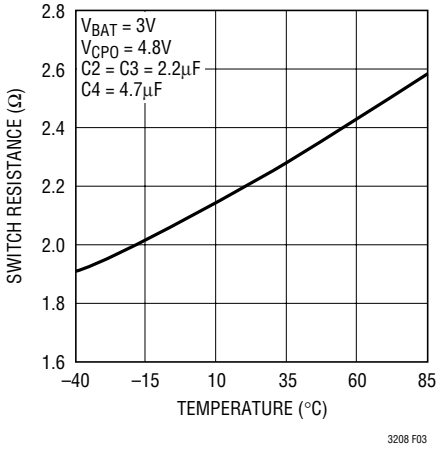


Figure 3. Typical 2x R_{OL} vs Temperature

OPERATION

Shutdown Current

Shutdown occurs when all the current source data bits have been written to zero or when DV_{CC} is below the DV_{CC} UVLO threshold.

Although the LTC3208 is designed to have very low shutdown current, it will draw about 3µA from V_{BAT} when in shutdown. Internal logic ensures that the LTC3208 is in shutdown when DV_{CC} is grounded. Note, however, that all of the logic signals that are referenced to DV_{CC} (SCL, SDA, ENRGBS, CAMHL) will need to be at DV_{CC} or below (i.e., ground) to avoid violation of the absolute maximum specifications on these pins.

Serial Port

The microcontroller compatible I^2C serial port provides all of the command and control inputs for the LTC3208. Data on the SDA input is loaded on the rising edge of SCL. D7 is loaded first and D0 last. There are seven data registers, one address register and one sub-address register. Once all address bits have been clocked into the address register acknowledgment occurs. The sub-address register is then written followed by writing the data register. Each data register has a sub-address. After the data register has been written a load pulse is created after the stop bit. The load pulse transfers all of the data held in the data registers to the DAC registers. The stop bit can be delayed until all of the data master registers have been written. At this point the LED current will be changed to the new settings. The serial port uses static logic registers so there is no minimum speed at which it can be operated.

MAIN and SUB Current Sources

There are four MAIN current sources and two SUB current sources. Each bank of current sources has an 8-bit linear DAC for current control. The output current range is 0 to 27.5mA in 256 steps.

The current sources are disabled when a block receives an all zero data word. The supply current for that block is reduced to zero. In addition each individual LED output can be connected to CPO to turn off that particular current source output and reduce operating current of the disabled output to typically 10µA.

Camera Current Sources

There are four CAM current sources. This bank of current sources has a 4-bit linear DAC for current control. The output current range is 0 to 102mA in 16 steps.

The current sources are disabled when the block receives an all zero data word. The supply current for the block is reduced to zero. In addition each individual LED output can be connected to CPO to turn off that particular current source output and reduce operating current of the disabled output to typically 10µA.

RGB Illuminators

The RED, GREEN and BLUE LEDs can be individually set from 0µA to 27mA in 16 steps via three 4-bit exponential DACs.

The current sources are individually disabled when an all-zero data word is received. The supply current for the current source is reduced to zero. These outputs can also be used as open drain logic control outputs. For this reason they will not be disabled when connected to CPO.

Auxiliary Current Sources

There are four AUX current sources. This bank of current sources has a 4-bit linear DAC for current control. The output current range is 0mA to 26mA in 16 steps.

In addition, each current source can be independently connected to the CAM, SUB or MAIN DAC outputs. The selection is made through the I^2C port. The output current will then match the corresponding selected current source bank. In this case a range of 0mA to 27.5mA for SUB and MAIN or 0mA to 102mA for CAM will be achieved.

The current sources are disabled when the block receives an all-zero data word in both REGE and REGB2. The supply current for the block is reduced to zero. AUX 1, 2 and 3 LED outputs can be connected to CPO to turn off that particular current source output and reduce operating current of the disabled output to typically 10µA. AUX 4 can be used as an open drain logic output and for this reason will not be disabled if connected to CPO.

OPERATION

Disabling Current Source Outputs

Unused CAM, SUB and MAIN outputs can be disabled by using two different methods depending on the application requirement. If the entire group is to be disabled (ie MAIN), then the data register for that group is written to zero. The unused outputs can be open circuit. If one or more of the group outputs is to be enabled then the unused outputs must be connected to CPO to prevent a false dropout signal from occurring.

AUX has a mixture of disable requirements. If AUX is not used then the data register is written to zero and all outputs can be left open circuit. If one or more output is to be enabled then AUX1, AUX2 and AUX3 can be disabled by connecting the unused output to CPO. AUX 4 cannot be disabled by connecting to CPO but can be left open circuit if $X_{RGBDROP}$ is set high. This setting removes the dropout detector from the AUX4 output but also removes the dropout detectors from the RED, GRN and BLUE LED outputs. To avoid disabling the RED, GRN and BLUE dropout detectors, AUX4 should be one of the enabled outputs whenever a mixture of enabled and disabled AUX outputs are used.

RED, GRN and BLUE outputs are disabled by writing the unused output register to zero. The unused output can be left open circuit.

CAMHL

The CAMHL pin quickly selects the camera high register for flash applications without reaccessing the I^2C port. When low, the CAM current range will be controlled by the camera low 4-bit register. When CAMHL is asserted high, the current range will be set by the camera high 4-bit register.

ENRGBS Pin

The ENRGBS pin can be used to enable or disable the LTC3208 without re-accessing the I^2C port. This might be useful to indicate an incoming phone call without waking the microcontroller. ENRGBS can be software programmed as an independent control for either the RGB display or the SUB display. Options REGG bit G1 determines which display ENRGBS controls. When bit G1 is 0, the ENRGBS pin controls the RGB display. If it is set to 1, then ENRGBS controls the SUB display.

To use the ENRGBS pin, the I^2C port must first be configured to the desired setting. For example, if the ENRGBS pin will be used to control the SUB display, then a nonzero code must reside in REGD and Command register REGG bit G1 must be set to 1. Now when ENRGBS is high (DV_{CC}), the SUB display will be on with the REGD setting. When ENRGBS is low the SUB display will be off. If no other displays are programmed to be on, the entire chip will be in shutdown.

Likewise if ENRGBS will be used to enable the RGB display, then a nonzero code must reside in one of the RED, GREEN or BLUE registers REGA1, REGA2 or REGB1, and options register REGG bit G1 is set to 0. Now when ENRGBS is high (DV_{CC}), the RGB display will light with the programmed color. When ENRGBS is low, the RGB display will be off. If no other displays are programmed to be on, the entire chip will be in shutdown.

If options register REGG bit G1 is set to 1 (SUB display control), then ENRGBS will have no effect on the RGB display. Likewise, if bit G1 is set to 0 (RGB display control), then ENRGBS will have no effect on the SUB display.

If the ENRGBS pin is not used, it must be connected to DV_{CC}. It should not be grounded or left floating.

Thermal Protection

The LTC3208 has built-in overtemperature protection. At internal die temperatures of around 150°C thermal shutdown will occur. This will disable all of the current sources and charge pump until the die has cooled by about 15°C. This thermal cycling will continue until the fault has been corrected.

OPERATION

R_{REF} Current Set Resistor

The current set resistor is connected between RREF and ground. The value of this resistor should typically be near 24k since all of the DAC reference currents and support circuit currents are related to this set current.

This input is protected against shorts to ground or low value resistors <10k. When a fault is detected the reference current amplifier is current limited. In addition, the current source outputs and charge pump are disabled.

Fullscale LED Current Equations

$$\text{AUX fullscale LED current (Amps)} = \frac{1.215V}{R_{REF}} \bullet 518$$

$$\text{SUB / MAIN fullscale LED current (Amps)} = \frac{1.215V}{R_{REF}} \bullet 543$$

$$\text{CAM fullscale LED current (Amps)} = \frac{1.215V}{R_{REF}} \bullet 2025$$

$$\text{RGB fullscale LED current (Amps)} = \frac{1.215V}{R_{REF}} \bullet 533$$

Mode Switching

The LTC3208 will automatically switch from 1x mode to 1.5x mode and subsequently to 2x mode whenever a dropout condition is detected at an LED pin. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. The dropout delay is typically 400µs.

The mode will automatically switch back to 1x whenever a data bit is updated via the I^2C port or when the CAMHL pin switches from high to low.

I^2C Interface

The LTC3208 communicates with a host (master) using the standard I^2C 2-wire interface. The Timing Diagram (Figure 5) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines.

The LTC3208 is a receive-only (slave) device.

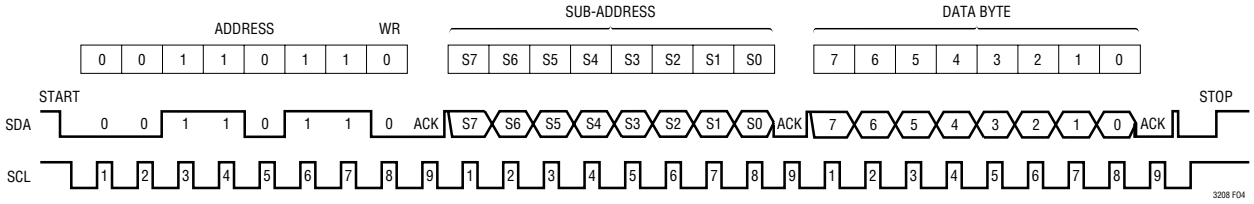


Figure 4. Bit Assignments

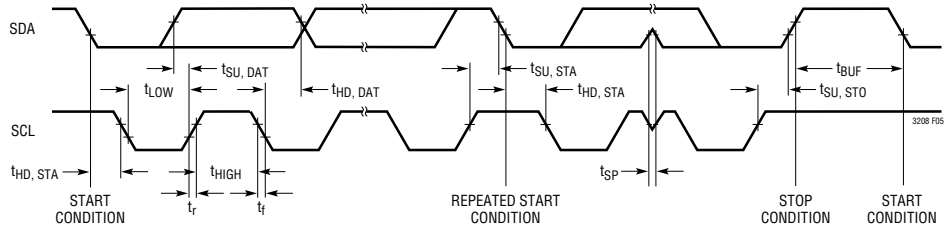


Figure 5. Timing Parameters

OPERATION

Write Word Protocol Used By the LTC3208

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	WR	A	*SUB-ADDRESS	A	DATA BYTE	A	P**

S = Start Condition, Wr = Write Bit = 0, A = Acknowledge,
P = Stop Condition

*The sub-address uses only the first 3 bits, D0, D1 and D2.

**Stop can be delayed until all of the data registers have been written.

Sub-Address Byte

MSB							LSB	
S7	S6	S5	S4	S3	S2	S1	S0	REGISTER
X	X	X	X	X	0	0	0	NONE
X	X	X	X	X	0	0	1	REGA
X	X	X	X	X	0	1	0	REGB
X	X	X	X	X	0	1	1	REGC
X	X	X	X	X	1	0	0	REGD
X	X	X	X	X	1	0	1	REGE
X	X	X	X	X	1	1	0	REGF
X	X	X	X	X	1	1	1	REGG

REGA, RED LED and GREEN LED 4-Bit DAC Data, Register Sub-Address = 001

MSB	REGA2		LSB	MSB	REGA1		LSB
A7	A6	A5	A4	A3	A2	A1	A0
GRN D3	GRN D2	GRN D1	GRN D0	RED D3	RED D2	RED D1	RED D0

REGB, BLUE LED and AUXILIARY 4-Bit DAC Data, Register Sub-Address = 010

MSB	REGB2		LSB	MSB	REGB1		LSB
B7	B6	B5	B4	B3	B2	B1	B0
AUX D3	AUX D2	AUX D1	AUX D0	BLUE D3	BLUE D2	BLUE D1	BLUE D0

REGC, MAIN LED 8-Bit DAC Data, Register Sub-Address = 011

MSB							LSB
C7	C6	C5	C4	C3	C2	C1	C0
MAIN D7	MAIN D6	MAIN D5	MAIN D4	MAIN D3	MAIN D2	MAIN D1	MAIN D0

REGD, SUB LED 8-Bit DAC Data, Register Sub-Address = 100

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
SUB D7	SUB D6	SUB D5	SUB D4	SUB D3	SUB D2	SUB D1	SUB D0

OPERATION

REGE, AUXILIARY LED 8-Bit MUX Data, Selects DAC for Each AUX Output, Register Sub-Address = 101

AUX4			AUX3			AUX2			AUX1		
E7	E6	SELECT	E5	E4	SELECT	E3	E2	SELECT	E1	E0	SELECT
0	0	AUX	0	0	AUX	0	0	AUX	0	0	AUX
0	1	MAIN	0	1	MAIN	0	1	MAIN	0	1	MAIN
1	0	SUB	1	0	SUB	1	0	SUB	1	0	SUB
1	1	CAM	1	1	CAM	1	1	CAM	1	1	CAM

REGF, CAMERA LED 4-Bit High and 4-Bit Low DAC Data, Register Sub-Address = 110

MSB	HIGH BITS		LSB	MSB	LOW BITS		LSB
F7	F6	F5	F4	F3	F2	F1	F0
CAM D3	CAM D2	CAM D1	CAM D0	CAM D3	CAM D2	CAM D1	CAM D0

REGG, Options Byte, Sub-Address = 111

MSB							LSB
G7	G6	G5	G4	G3	G2	G1	G0
Force2x	Force1p5	D_{TH2}	D_{TH1}	$X_{RGBDROP}$	$S_{CAMHILO}$	S_{ELRGBS}	Not Used

S_{ELRGBS} (G1)	1 0	Selects SUB displays for control by the ENRGBS pin Selects RGB displays for control by the ENRGBS pin
$S_{CAMHILO}$ (G2)	1 0	Selects CAM high register, disables CAMHL pin Selects CAM low register, enables CAMHL pin
$X_{RGBDROP}$ (G3)	1 0	Disables RGB and AUX4 dropout signals when outputs used as logic signals Enables RGB and AUX4 dropout signals
D_{TH1} (G4)	0	Test hook, must always be 0
D_{TH2} (G5)	0	Test hook, must always be 0
Force1p5 (G6)	1 0	Forces charge pump into 1.5x mode Enables mode logic to control mode changes based on dropout signal
Force2x (G7)	1 0	Forces charge pump into 2x mode, overrides Force1p5 signal Enables mode logic to control mode changes based on dropout signal

OPERATION

Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

START and STOP Conditions

A bus-master signals the beginning of a communication to a slave device by transmitting a START condition.

A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I²C device.

Byte Format

Each byte sent to the LTC3208 must be 8 bits long followed by an extra clock cycle for the Acknowledge bit to be returned by the LTC3208. The data should be sent to the LTC3208 most significant bit (MSB) first.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave (LTC3208) lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock cycle. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse.

Slave Address

The LTC3208 responds to only one 7-bit address which has been factory programmed to 0011011. The eighth bit of the address byte (R/W) must be 0 for the LTC3208 to recognize the address since it is a write only device. This effectively forces the address to be 8 bits long where the least significant bit of the address is 0. If the correct seven bit address is given but the R/W bit is 1, the LTC3208 will not respond.

Bus Write Operation

The master initiates communication with the LTC3208 with a START condition and a 7-bit address followed by the Write Bit R/W = 0. If the address matches that of the LTC3208, the LTC3208 returns an Acknowledge. The master should then deliver the most significant sub-address byte for the data register to be written. Again the LTC3208 acknowledges and then the data is delivered starting with the most significant bit. This cycle is repeated until all of the required data registers have been written. Any number of data latches can be written. Each data byte is transferred to an internal holding latch upon the return of an Acknowledge. After all data bytes have been transferred to the LTC3208, the master may terminate the communication with a STOP condition. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3208 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP condition can be sent and the LTC3208 will update all registers with the data that it had received.

In certain circumstances the data on the I²C bus may become corrupted. In these cases the LTC3208 responds appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3208 has been successfully addressed and is receiving data when a STOP condition mistakenly occurs. The LTC3208 will ignore this stop condition and will not respond until a new START condition, correct address, sub-address and new set of data and STOP condition are transmitted.

Likewise, if the LTC3208 was previously addressed and sent valid data but not updated with a STOP, it will respond to any STOP that appears on the bus with only one exception, independent of the number of REPEAT-START's that have occurred. If a REPEAT-START is given and the LTC3208 successfully acknowledges its address, it will not respond to a STOP until all bytes of the new data have been received and acknowledged.

Shared data registers will have all 8 bits rewritten since a common acknowledge signal writes these registers. The shared registers include REGA, REGB and REGF.

APPLICATIONS INFORMATION

V_{BAT}, CPO Capacitor Selection

The value and type of capacitors used with the LTC3208 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) ceramic capacitors are used for both CV_{BAT} and C_{CPO}. Tantalum and aluminum capacitors are not recommended due to high ESR.

The value of C_{CPO} directly controls the amount of output ripple for a given load current. Increasing the size of C_{CPO} will reduce output ripple at the expense of higher start-up current. The peak-to-peak output ripple of the 1.5X mode is approximately given by the expression

$$V_{RIPPLE\ P-P} = \frac{I_{OUT}}{3f_{OSC} \bullet C_{CPO}} \quad (3)$$

Where f_{OSC} is the LTC3208 oscillator frequency or typically 900kHz and C_{CPO} is the output storage capacitor.

The output ripple in 2x mode is very small due to the fact that load current is supplied on both cycles of the clock.

Both value and type of output capacitor can significantly affect the stability of the LTC3208. As shown in the block diagram, the LTC3208 uses a control loop to adjust the strength of the charge pump to match the required output current. The error signal of the loop is stored directly on the output capacitor. The output capacitor also serves as the dominant pole for the control loop. To prevent ringing or instability, it is important for the output capacitor to maintain at least 2.2µF of capacitance over all conditions.

In addition, excessive output capacitor ESR will tend to degrade the loop stability. The closed loop output resistance is about 80m . For a 100mA load current change, the error signal will change by about 8mV. If the output capacitor has 80m or more of ESR, the closed loop frequency response will cease to roll off in a simple one-pole fashion and poor load transient response or instability may occur. Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout will result in very good stability. As the value of C_{CPO} controls the amount of output ripple, the value of CV_{BAT} controls the amount of ripple present at the input pin (V_{BAT}). The LTC3208 input current will be relatively constant while the charge pump is either in the input charging phase or the output charging phase but will drop to zero during the clock nonoverlap times. Since the nonoverlap time is small (~25ns), these missing "notches" will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the higher ESR. Therefore, ceramic capacitors are recommended for low ESR. Input noise can be further reduced by powering the LTC3208 through a very small series inductor as shown in Figure 6. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

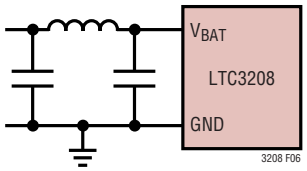


Figure 6. 10nH Inductor Used for Input Noise Reduction (Approximately 1cm of Board Trace)

Flying Capacitor Selection

Warning: Polarized capacitors such as tantalum or aluminum should never be used for the flying capacitors since their voltage can reverse upon start-up of the LTC3208. Ceramic capacitors should always be used for the flying capacitors.

The flying capacitors control the strength of the charge pump. In order to achieve the rated output current it is necessary to have 2.2µF of capacitance for each of the flying capacitors. Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X7R material will retain most of its capacitance from – 40°C to 85°C, whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a very poor voltage coefficient causing them to lose 60% or more of their capacitance when

APPLICATIONS INFORMATION

the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, overrated voltage and temperature conditions, a 1µF, 10V, Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF, 10V, X7R available in the same case. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitances at all temperatures and voltages.

Table 1 shows a list of ceramic capacitor manufacturers and how to contact them:

Table 1. Recommended Capacitor Vendors

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com

Layout Considerations and Noise

Due to its high switching frequency and the transient currents produced by the LTC3208, careful board layout is necessary. A true ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions.

The flying capacitor pins C1P, C2P, C1M and C2M will have very high edge rate waveforms. The large dv/dt on these pins can couple energy capacitively to adjacent PCB runs. Magnetic fields can also be generated if the flying capacitors are not close to the LTC3208 (i.e., the loop area is large). To decouple capacitive energy transfer, a Faraday shield may be used. This is a grounded PCB trace between the sensitive node and the LTC3208 pins. For a high quality AC ground, it should be returned to a solid ground plane that extends all the way to the LTC3208.

The following guidelines should be followed when designing a PCB layout for the LTC3208.

- The exposed pad should be soldered to a large copper plane that is connected to a solid, low impedance ground plane using plated, through-hole vias for proper heat sinking and noise protection.
- Input and output capacitors (C1 and C4) must be placed close to the part.
- The flying capacitors (C2 and C3) must be placed close to the part. The traces running from the pins to the capacitor pads should be as wide as possible.
- V_{BAT}, CPO traces must be made wide to minimize inductance and handle the high currents.
- LED pads must be large and connected to other layers of metal to ensure proper heat sinking.

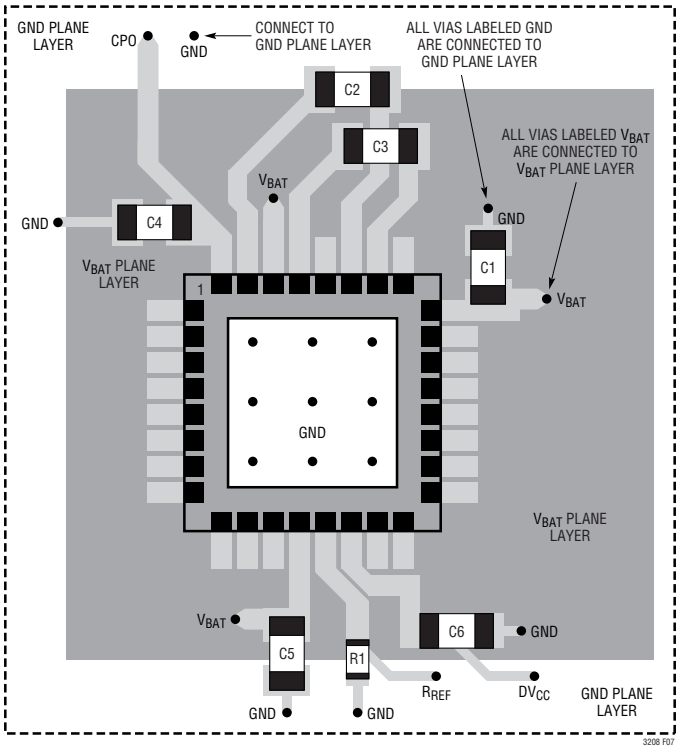


Figure 7. PC Board Layout Example

APPLICATIONS INFORMATION

Power Efficiency

To calculate the power efficiency (η) of a white LED driver chip, the LED power should be compared to the input power. The difference between these two numbers represents lost power whether it is in the charge pump or the current sources. Stated mathematically, the power efficiency is given by:

$$\eta = \frac{P_{LED}}{P_{IN}} \quad (4)$$

The efficiency of the LTC3208 depends upon the mode in which it is operating. Recall that the LTC3208 operates as a pass switch, connecting V_{BAT} to CPO, until dropout is detected at the I_{LED} pin. This feature provides the optimum efficiency available for a given input voltage and LED forward voltage. When it is operating as a switch, the efficiency is approximated by:

$$\eta = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet I_{BAT}} = \frac{V_{LED}}{V_{BAT}} \quad (5)$$

since the input current will be very close to the sum of the LED currents.

At moderate to high output power, the quiescent current of the LTC3208 is negligible and the expression above is valid.

Once dropout is detected at any LED pin, the LTC3208 switches the charge pump to 1.5x mode.

In 1.5x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 1.5 times the actual input voltage. This is because the input current for a 1.5x charge pump is approximately 1.5 times the load current. In an ideal 1.5x charge pump, the power efficiency would be given by:

$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet 1.5 \bullet I_{LED}} = \frac{V_{LED}}{1.5 \bullet V_{BAT}}$$

Similarly, in 2x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 2 times the actual input voltage. In an ideal 2x charge pump, the power efficiency would be given by:

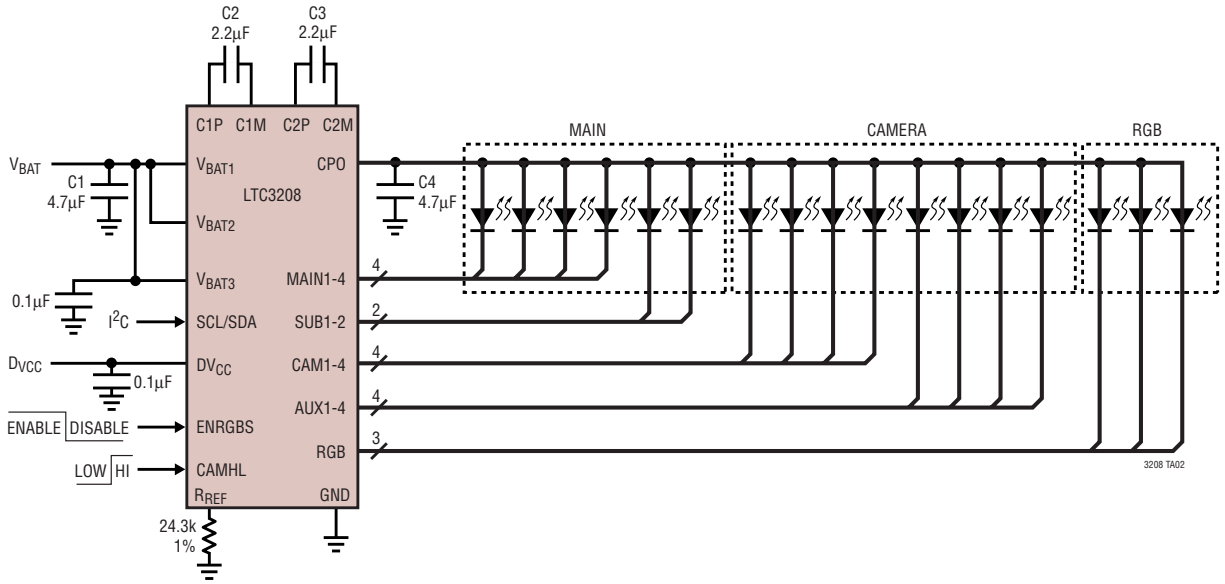
$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet 2 \bullet I_{LED}} = \frac{V_{LED}}{2 \bullet V_{BAT}}$$

Thermal Management

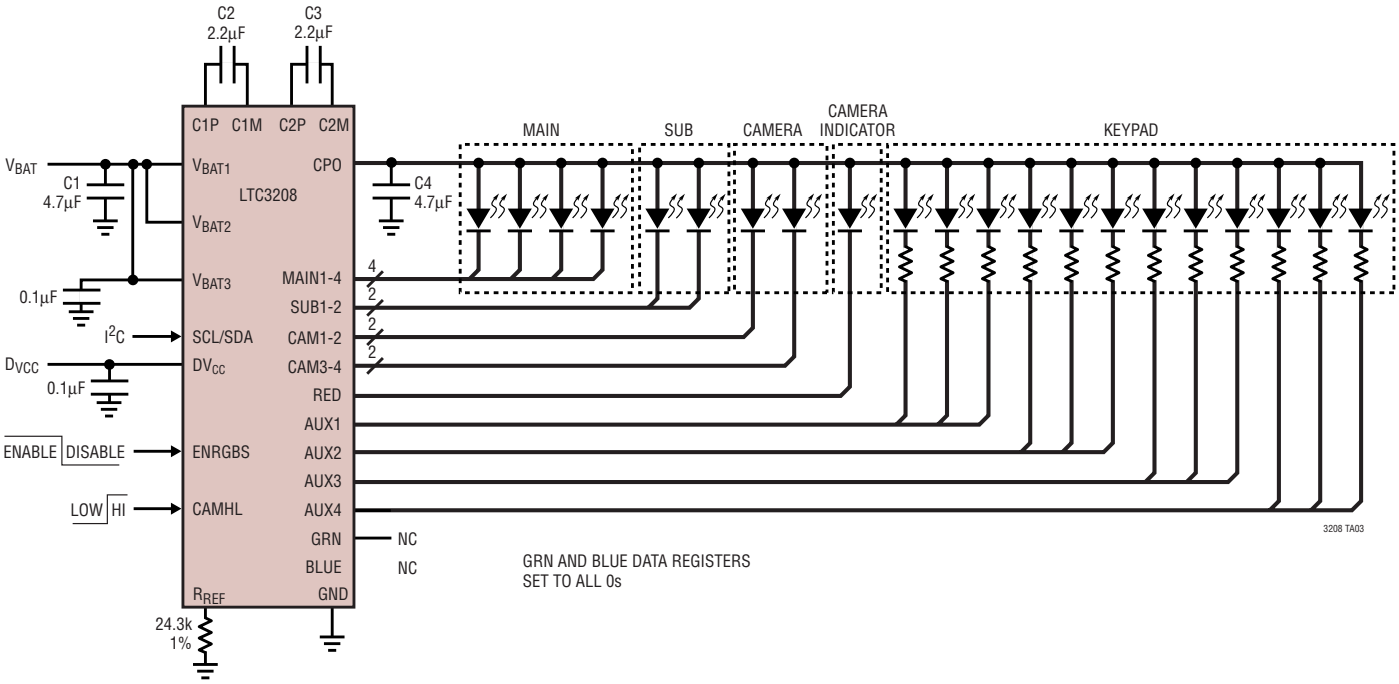
For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3208. If the junction temperature increases above approximately 150°C, the thermal shutdown circuitry will automatically deactivate the output current sources and charge pump. To reduce maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the Exposed Pad to a ground plane and maintaining a solid ground plane under the device will reduce the thermal resistance of the package and PC board considerably.

TYPICAL APPLICATIONS

6-LED MAIN, RGB Plus Low/High Current 8-LED Camera Light

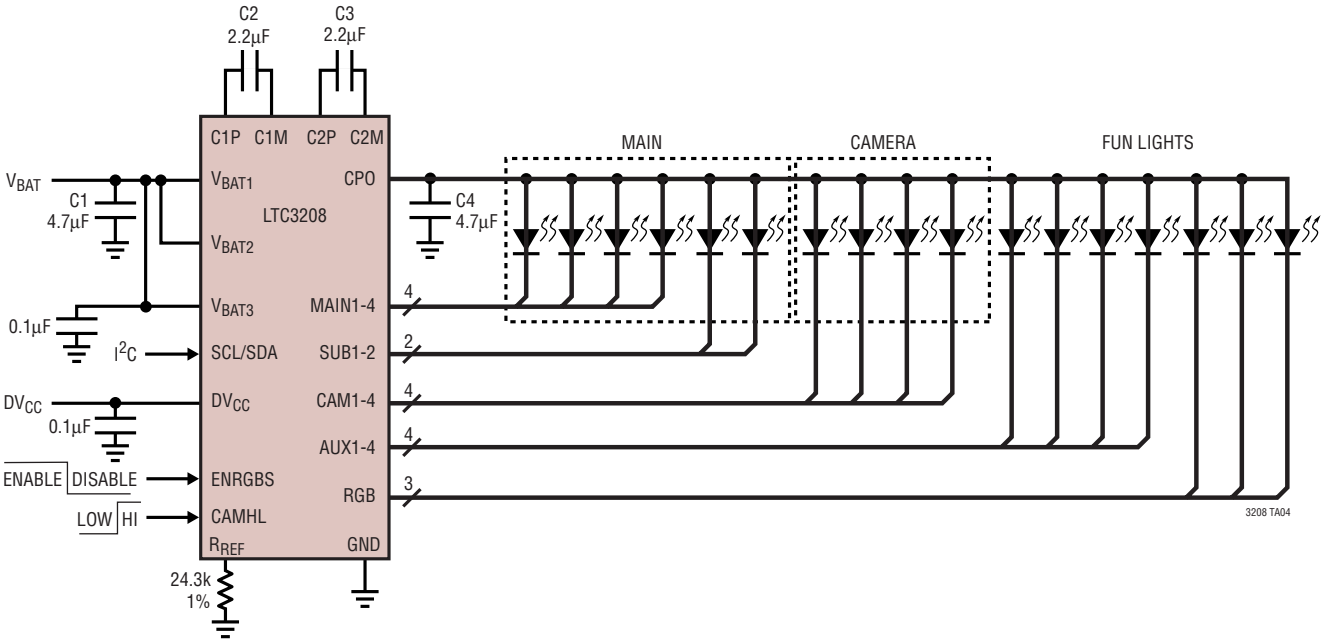


MAIN and SUB Backlight, Keypad Backlight, Camera Light and Camera Indicator

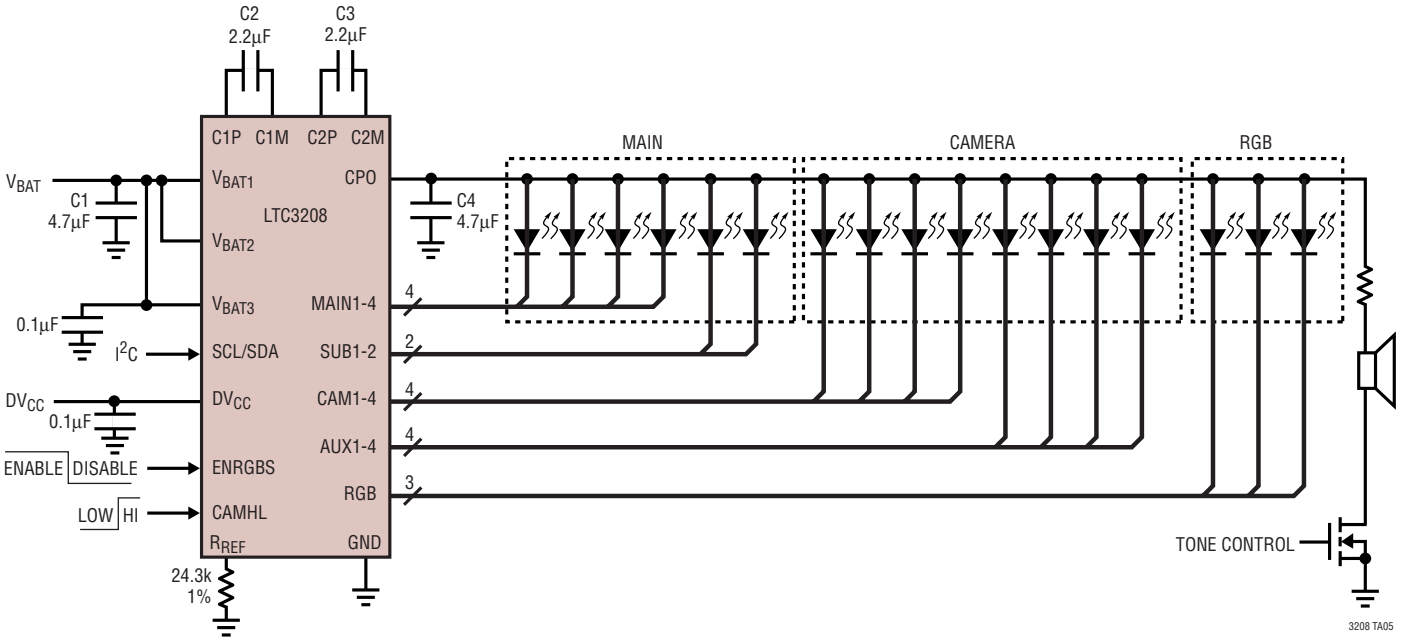


TYPICAL APPLICATIONS

6-LED MAIN, 4-LED Camera Light, 7-LED Fun Lights

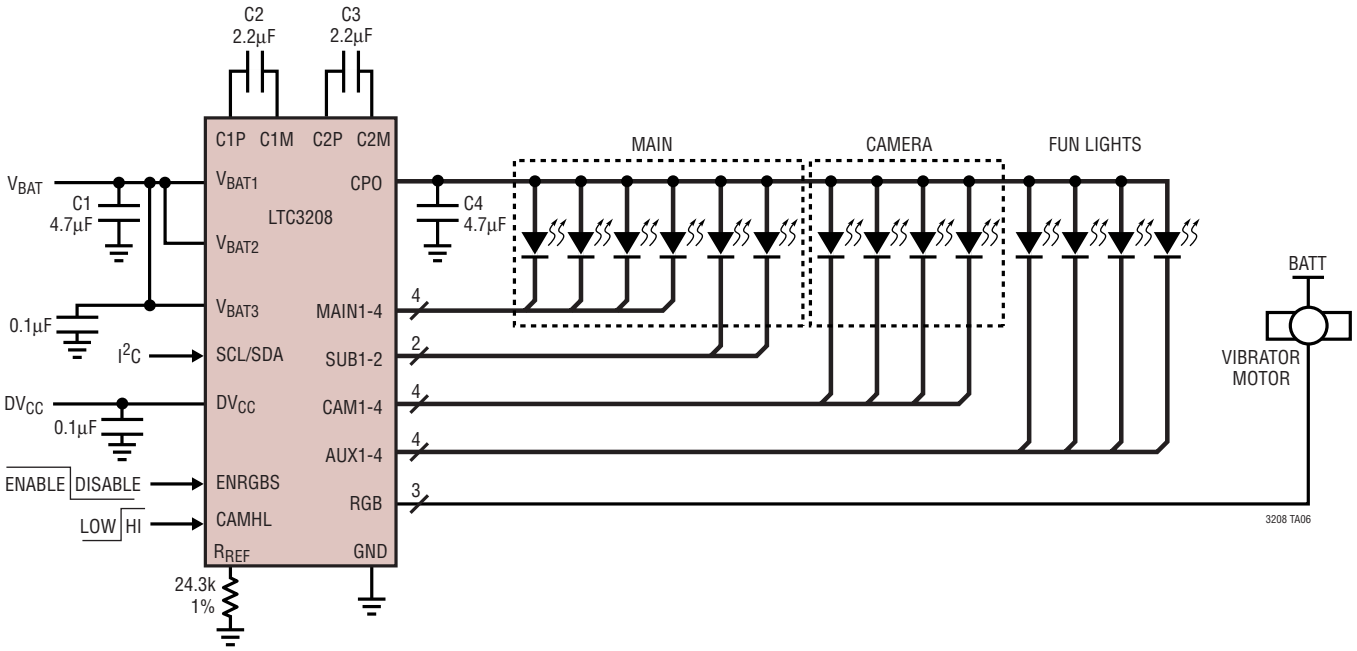


6-LED MAIN, RGB Plus Low/High Current 8-LED Camera Light with Tone Generator

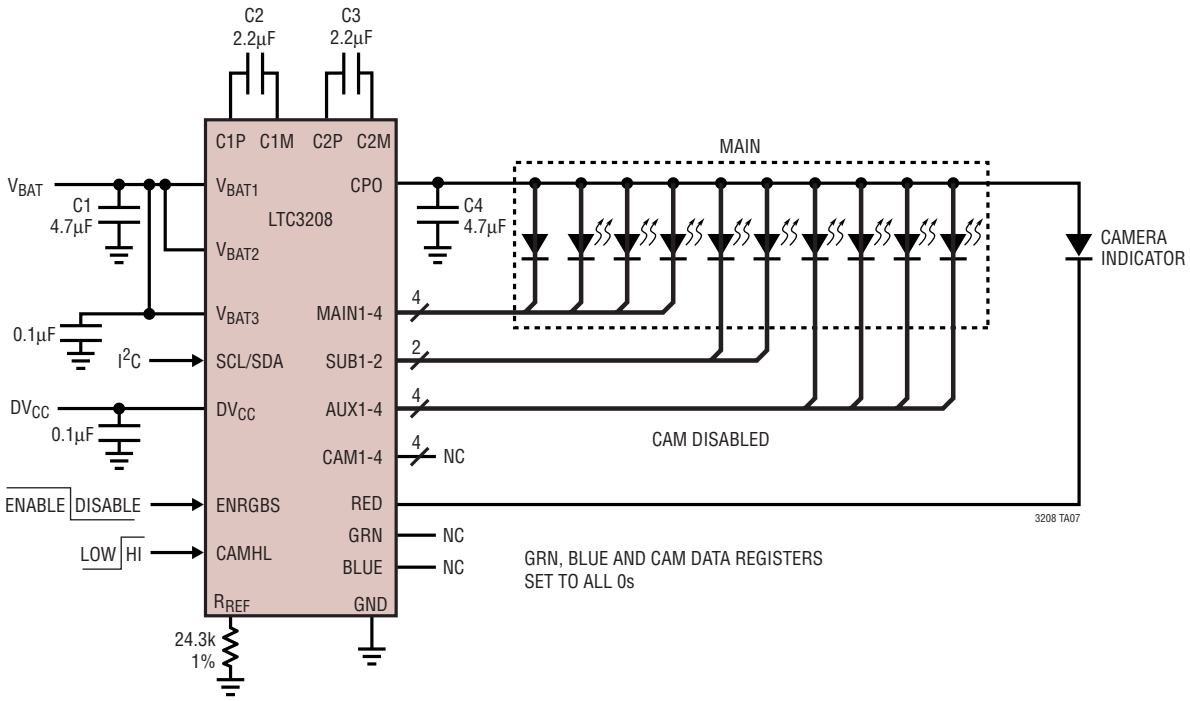


TYPICAL APPLICATIONS

6-LED MAIN, 4-LED Camera Light, 4-LED Fun Lights with Vibrator Motor

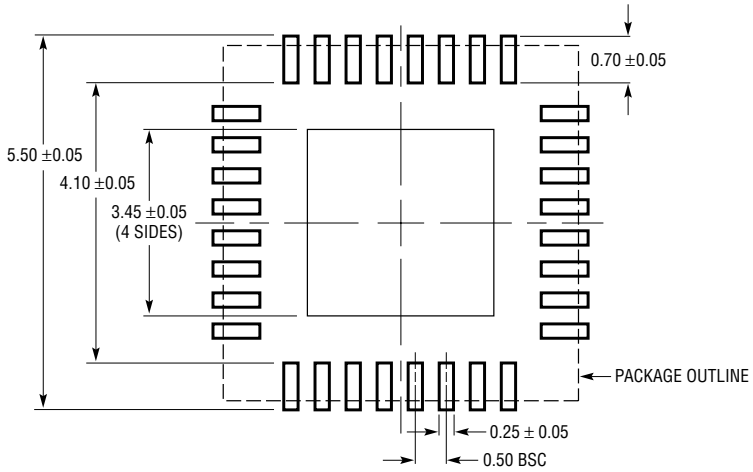


10-LED MAIN with RED Camera Indicator, CAM Displays Disabled

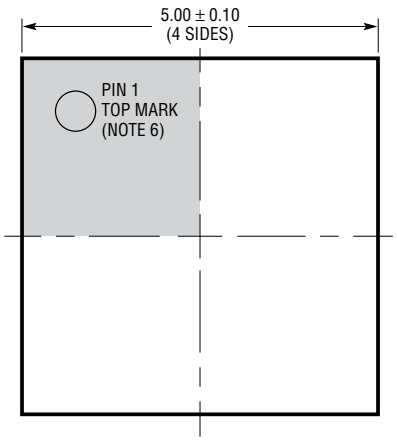


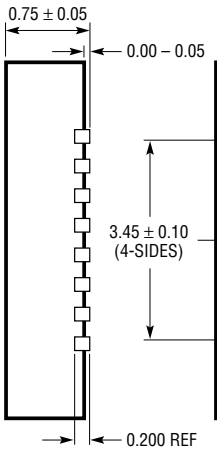
PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)

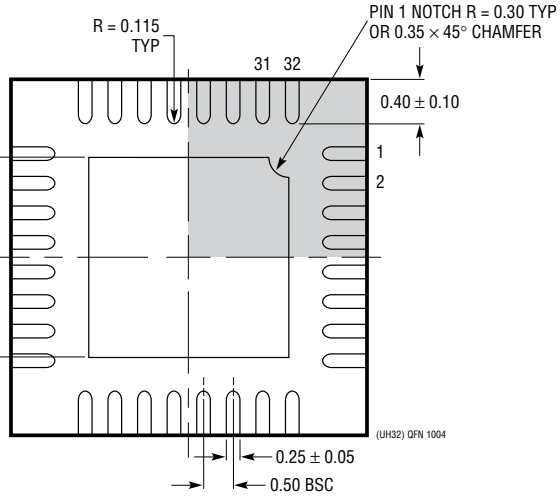


RECOMMENDED SOLDER PAD LAYOUT





BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE