360mA Universal 18-Channel LED Driver

FEATURES

- **Eighteen 20mA Universal Current Sources with 64-Step Linear Brightness Control**
- **Independent On/Off, Brightness Level, Blinking and Gradation Control for Each Current Source Using 2-Wire I²C Interface**
- **Low Noise Multi-Mode Charge Pump (1x, 1.5x, 2x) Provides Up to 91% Efficiency**
- **Slew Limited Switching Reduces Conducted and Radiated Noise (EMI)**
- **Up to 360mA Total Output Current**
- **Internal Current Reference**
- Single Reset Pin for Asynchronous Shutdown and Reset of All Data Registers
- Two I²C Addresses Are Available (LTC3220: 0011100, LTC3220-1: 0011101)
- Automatic or Forced Mode Switching
- Internal Soft-Start Limits Inrush Current
- Short-Circuit/Thermal Protection
- 4mm × 4mm Ultrathin (0.55mm) 28-Lead QFN Package

APPLICATIONS

- Video Phones with QVGA+ Displays
- Keypad Lighting
- General/Miscellaneous Lighting

DESCRIPTION

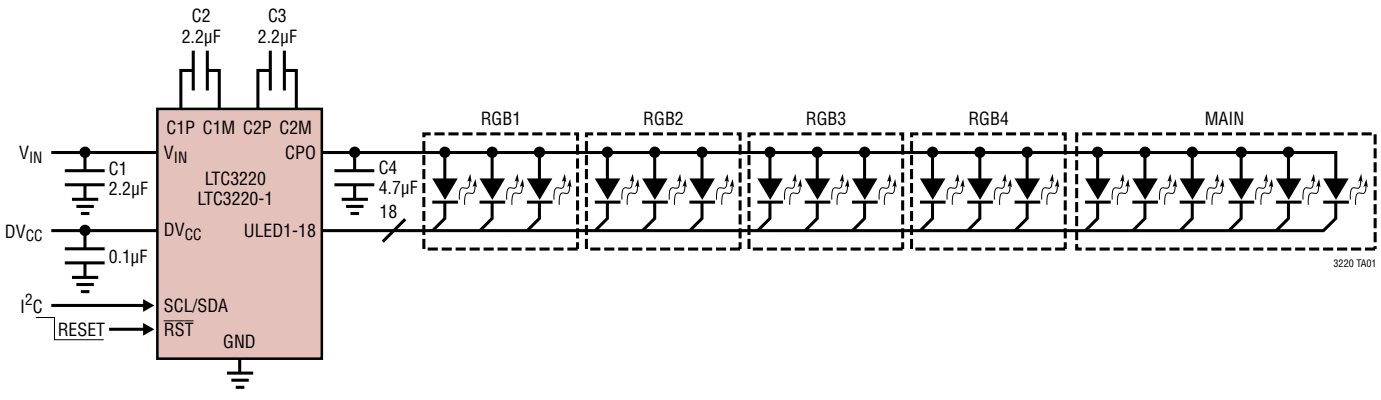
The LTC®3220/LTC3220-1 are highly integrated multi-display LED drivers. These parts contain a high efficiency, low noise charge pump to provide power to up to eighteen universal LED current sources. The LTC3220/LTC3220-1 require only five small ceramic capacitors to form a complete LED power supply and current controller.

The LED currents are set by an internal precision current reference. Independent dimming, on/off, blinking and gradation control for all universal current sources are achieved via the I²C serial interface. 6-bit linear DACs are available to adjust brightness levels independently for each universal LED current source.

The LTC3220/LTC3220-1 charge pump optimizes efficiency based on the voltage across the LED current sources. The part powers up in 1x mode and will automatically switch to boost mode whenever any enabled LED current source begins to enter dropout. The first dropout switches the parts into 1.5x mode and a subsequent dropout switches the LTC3220/LTC3220-1 into 2x mode. The parts reset to 1x mode whenever a data bit is updated via the I²C port.

TYPICAL APPLICATION

6-LED Main, 4 RGB LEDs

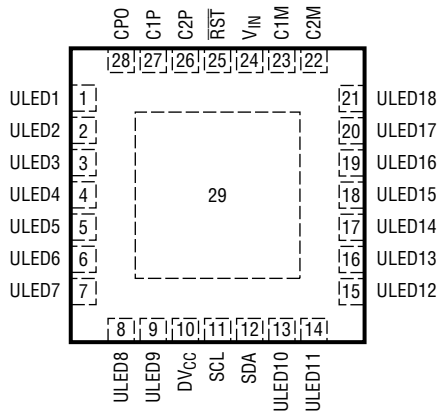


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 4)

V_{IN}, DV_{CC}, CPO to GND ..... –0.3V to 6V
ULED1-ULED18 to GND ..... –0.3V to 6V
SDA, SCL, $\overline{RST}$ ..... –0.3V to (DV_{CC} + 0.3V)
I_{CPO} (Continuous) (Note 2) 360mA
$I_{ULED1-18}$ (Note 2) 25mA
CPO Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 3)
LTC3220E/LTC3220E-1 ..... –40°C to 85°C
LTC3220I/LTC3220I-1 ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



PF PACKAGE
28-LEAD UTQFN (4mm × 4mm)

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3220EPF#PBF	LTC3220EPF#TRPBF	3220T	28-Lead UTQFN (4mm × 4mm)	–40°C to 85°C
LTC3220EPF-1#PBF	LTC3220EPF-1#TRPBF	2201T	28-Lead UTQFN (4mm × 4mm)	–40°C to 85°C
LTC3220IPF#PBF	LTC3220IPF#TRPBF	3220T	28-Lead UTQFN (4mm × 4mm)	–40°C to 125°C
LTC3220IPF-1#PBF	LTC3220IPF-1#TRPBF	2201T	28-Lead UTQFN (4mm × 4mm)	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, DV_{CC} = 3V, $\overline{RST}$ = high, C1 = C2 = C3 = 2.2µF, C4 = 4.7µF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Operating Voltage		●	2.9		5.5	V
	I_{VIN} Operating Current	I_{CPO} = 0, 1x Mode I_{CPO} = 0, 1.5x Mode I_{CPO} = 0, 2x Mode			580 2.4 3.2		µA mA mA
	DV_{CC} UVLO Threshold				1		V
	DV_{CC} Operating Voltage		●	1.5		5.5	V
	V_{IN} UVLO Threshold				1.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, DV_{CC} = 3V, $\overline{RST}$ = high, C1 = C2 = C3 = 2.2µF, C4 = 4.7µF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	V_{IN} Shutdown Current		●		3.2	7	µA
	DV_{CC} Shutdown Current		●			1	µA
Universal LED Current, 6-Bit Linear DACs, ULED = 1V							
	Full-Scale LED Current		●	18	20	22	mA
	Minimum (I_{LSB}) LED Current Step				0.314		mA
	Minimum Programmable Current	ULED Data Register Programmed to 0b00000001			0.395		mA
	LED Current Matching	Any Two Outputs, 50% of FS			1.5		%
	LED Dropout Voltage	I_{LED} = FS			120		mV
	Blink Rate Period	REG19, D4 = 0 REG19, D4 = 1			1.25 2.5		Sec Sec
	ULED Up/Down Gradation Ramp Times	REG19, D1 = 1, D2 = 0 REG19, D1 = 0, D2 = 1 REG19, D1 = 1, D2 = 1			0.24 0.48 0.96		Sec Sec Sec
	Gradation Period	REG19, D1 = 1, D2 = 0 REG19, D1 = 0, D2 = 1 REG19, D1 = 1, D2 = 1			0.313 0.625 1.25	0.410 0.820 1.640	Sec Sec Sec
	V_{OL} General Purpose Output Mode (GPO)	I_{OUT} = 1mA, Single Output Enabled			5		mV
	LED Turn-On Delay	From Stop Bit, Part Enabled			4		µs
Charge Pump (CPO)							
	1x Mode Output Impedance				0.6		Ω
	1.5x Mode Output Impedance	V_{IN} = 3V, V_{CPO} = 4.2V (Note 5)			3.6		Ω
	2x Mode Output Impedance	V_{IN} = 3V, V_{CPO} = 4.8V (Note 5)			4.1		Ω
	CPO Regulation Voltage	1.5x Mode, I_{CPO} = 20mA 2x Mode, I_{CPO} = 20mA			4.5 5.03		V V
	Clock Frequency		●	0.65	0.85	1.05	MHz
CPO Short-Circuit Detection							
	Threshold Voltage		●	0.4		1.3	V
	Test Current	CPO = 0V	●	10		30	mA
SDA, SCL, $\overline{RST}$							
V_{IL}			●			0.3 • DV_{CC}	V
V_{IH}			●	0.7 • DV_{CC}			V
I_{IH}		SDA, SCL, $\overline{RST}$ = DV_{CC}	●	–1		1	µA
I_{IL}		SDA, SCL, $\overline{RST}$ = 0V	●	–1		1	µA
V_{OL}	Digital Output Low (SDA)	I_{PULLUP} = 3mA	●		0.12	0.4	V
$\overline{RST}$ Timing	Reset Pulse Duration			20			ns
Serial Port Timing (Notes 6, 7)							
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time			0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time			0.6			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, DV_{CC} = 3V, $\overline{RST}$ = high, C1 = C2 = C3 = 2.2µF, C4 = 4.7µF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{HD,DAT(OUT)}$	Data Hold Time			0		900	ns
$t_{HD,DAT(IN)}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Setup Time			100			ns
t_{LOW}	Clock Low Period			1.3			µs
t_{HIGH}	Clock High Period			0.6			µs
t_f	Clock Data Fall Time			20		300	ns
t_r	Clock Data Rise Time			20		300	ns
t_{SP}	Spike Suppression Time					50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Based on long term current density limitations.

Note 3: The LTC3220E/LTC3220E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3220I/LTC3220I-1 are guaranteed to meet performance specifications over the full –40°C to 125°C operating temperature range.

Note 4: These devices include overtemperature protection that is intended to protect the devices during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 5: 1.5x mode output impedance is defined as $(1.5V_{IN} – V_{CPO})/I_{OUT}$. 2x mode output impedance is defined as $(2V_{IN} – V_{CPO})/I_{OUT}$.

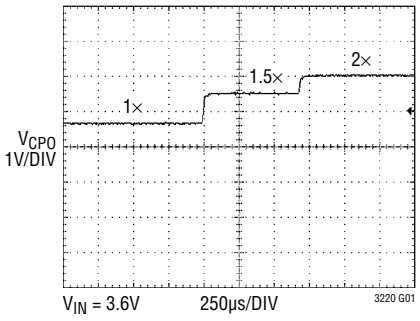
Note 6: All values are referenced to V_{IH} and V_{IL} levels.

Note 7: Guaranteed by design.

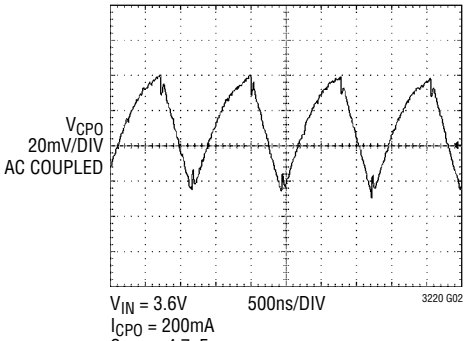
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

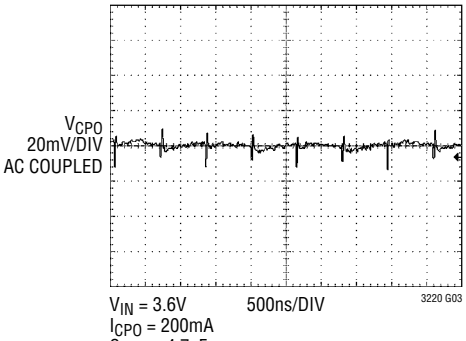
Mode Switch Dropout Times



1.5x Mode CPO Ripple

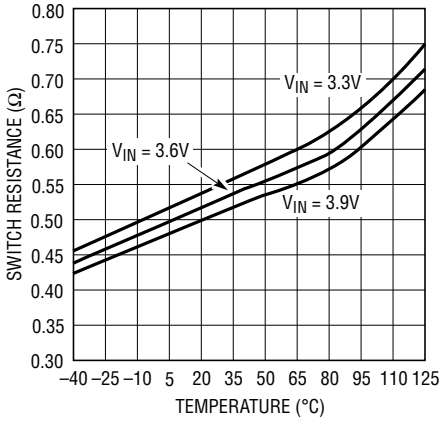


2x Mode CPO Ripple

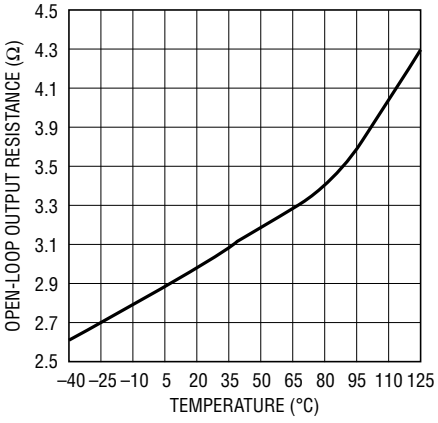


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

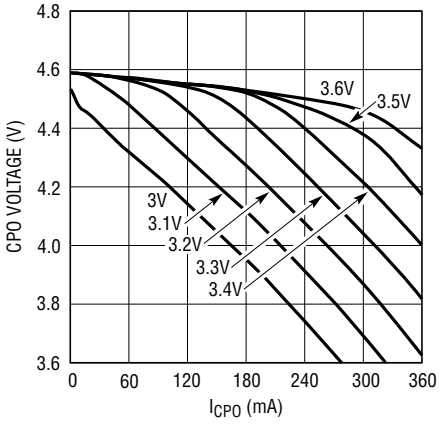
1x Mode Switch Resistance vs Temperature



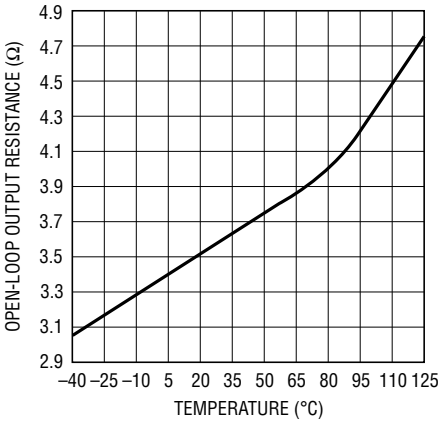
1.5x Mode Charge Pump Open-Loop Output Resistance vs Temperature



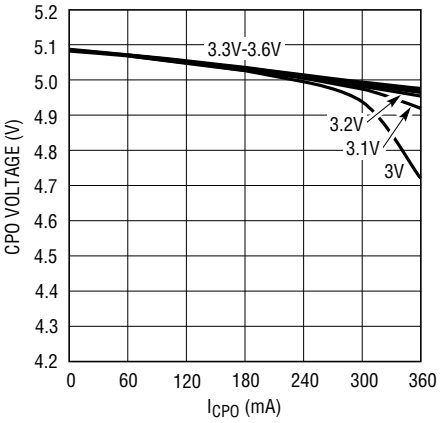
1.5x Mode CPO Voltage vs I_{CPO}



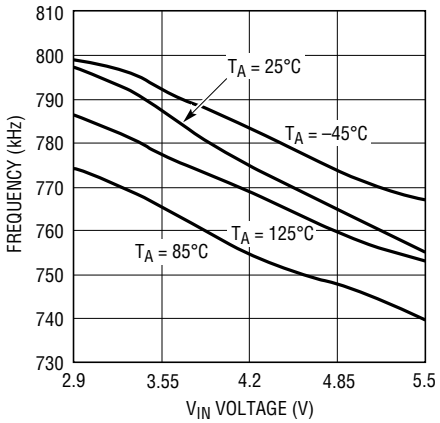
2x Mode Charge Pump Open-Loop Output Resistance vs Temperature



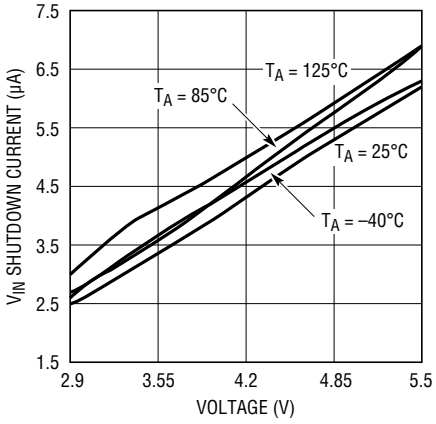
2x Mode CPO Voltage vs I_{CPO}



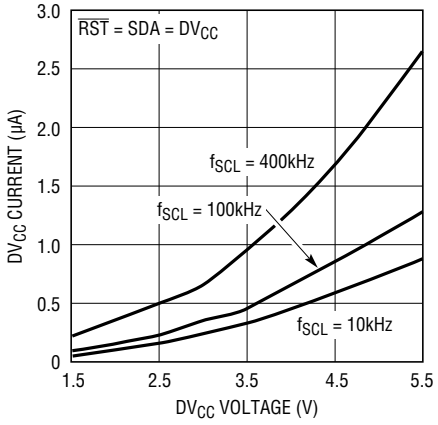
Oscillator Frequency vs V_{IN} Voltage



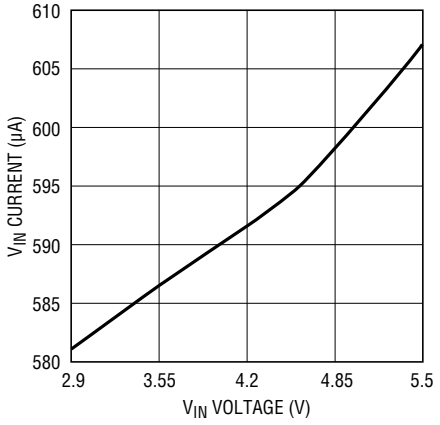
V_{IN} Shutdown Current vs V_{IN} Voltage



DV_{CC} Current vs DV_{CC} Voltage

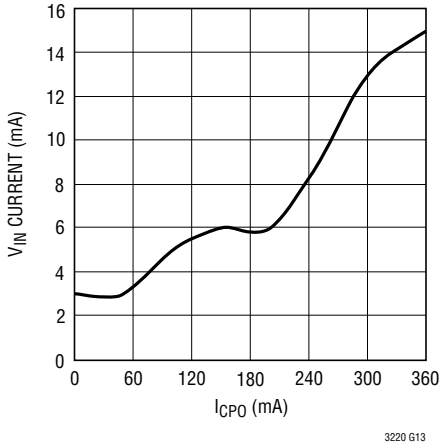


1x Mode No Load V_{IN} Current vs V_{IN} Voltage

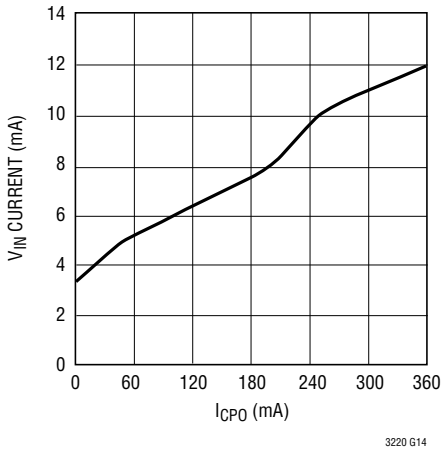


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

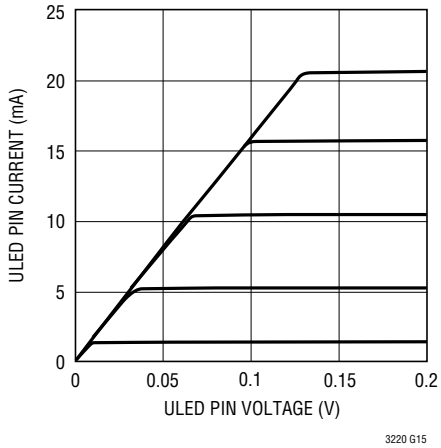
1.5x Mode V_{IN} Current vs I_{CPO} ($I_{VIN} - 1.5I_{CPO}$)



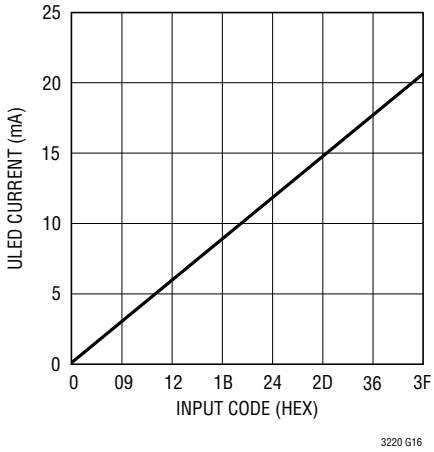
2x Mode V_{IN} Current vs I_{CPO} ($I_{VIN} - 2I_{CPO}$)



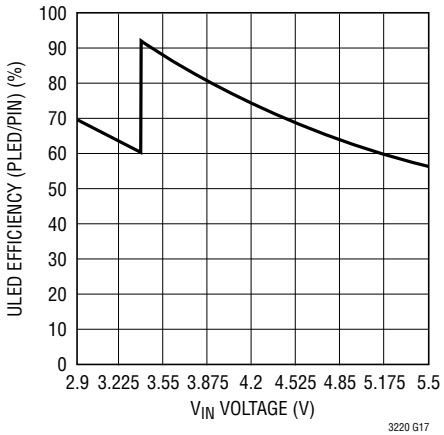
ULED Pin Current vs ULED Pin Voltage



ULED Current vs Input Code



18-LED ULED Display Efficiency vs V_{IN} Voltage



PIN FUNCTIONS

ULED1-ULED18 (Pins 1-9,13-21): Current Source Outputs for Driving LEDs. The LED current can be set from 0mA to 20mA in 64 steps via software control and internal 6-bit linear DAC. Each output can be disabled by setting the associated data register REG1 to REG18 low. ULED1 to ULED18 can also be used as I^2C controlled open-drain general purpose outputs. Connect unused outputs to ground.

DV_{CC} (Pin 10): Supply Voltage for All digital I/O lines. This pin sets the logic reference level of the LTC3220/LTC3220-1. DV_{CC} will reset the data registers when set below the undervoltage lockout threshold. A 0.1µF X5R or X7R ceramic capacitor should be connected to ground.

SCL (Pin 11): I^2C Clock Input. The logic level for SCL is referenced to DV_{CC}.

PIN FUNCTIONS

SDA (Pin 12): Input Data for the Serial Port. Serial data is shifted in one bit per clock cycle to control the LTC3220/LTC3220-1. The logic level is referenced to DV_{CC}.

C1P, C2P, C1M, C2M (Pins 27, 26, 23, 22): Charge Pump Flying Capacitor Pins. A 2.2µF X7R or X5R ceramic capacitor should be connected from C1P to C1M and C2P to C2M.

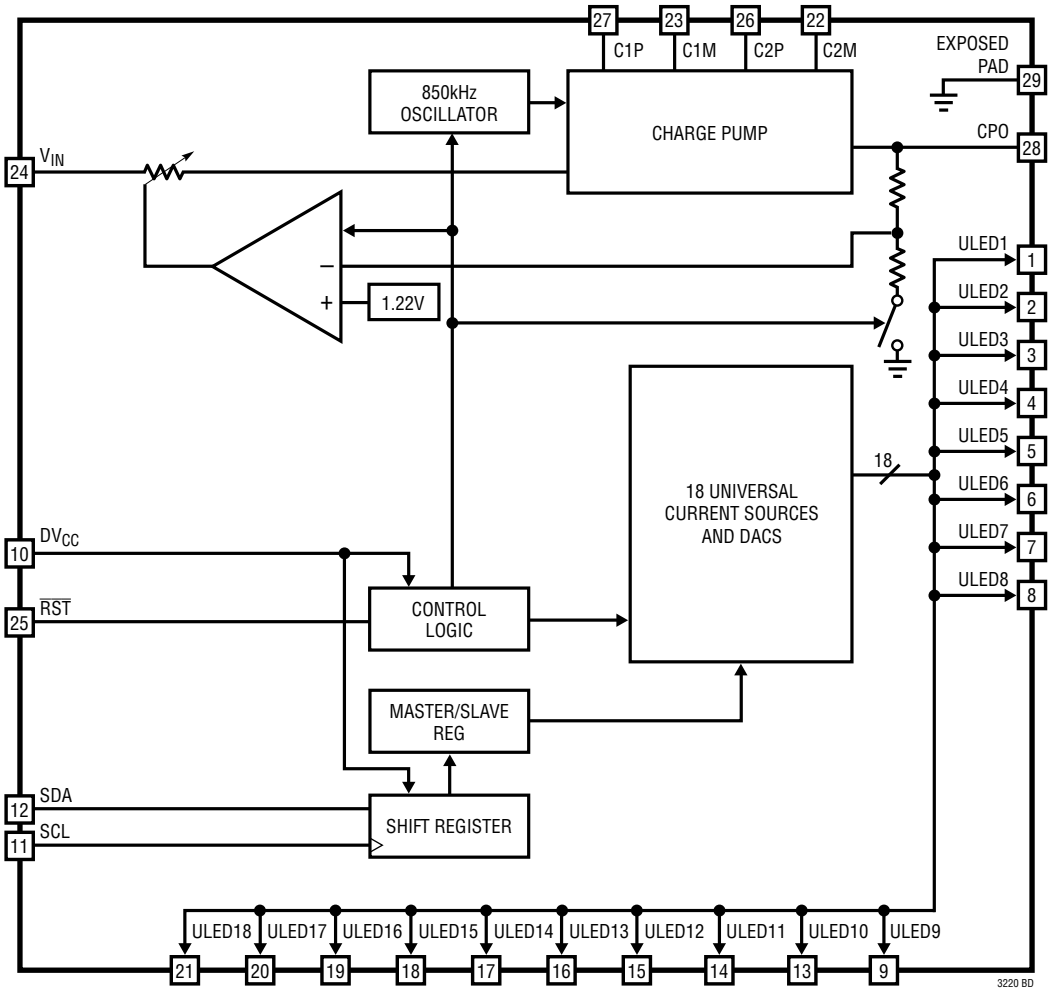
V_{IN} (Pin 24): Supply Voltage for the Entire Device. This pin must be bypassed with a single 2.2µF low ESR ceramic capacitor.

$\overline{RST}$ (Pin 25): Active Low Reset Input. $\overline{RST}$ Resets all internal registers and forces LTC3220/LTC3220-1 into shutdown mode.

CPO (Pin 28): Output of the Charge Pump. Used to power all LEDs. A 4.7µF X5R or X7R ceramic capacitor should be connected to ground.

Exposed Pad (Pin 29): Ground. The Exposed Pad must be soldered to PCB ground.

BLOCK DIAGRAM



OPERATION

Power Management

The LTC3220/LTC3220-1 use a switched capacitor charge pump to boost CPO as much as 2 times the input voltage up to 5.1V. The part starts up in 1x mode. In this mode, V_{IN} is connected directly to CPO. This mode provides maximum efficiency and minimum noise. The LTC3220/LTC3220-1 will remain in 1x mode until an LED current source drops out. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. When dropout is detected, the LTC3220/LTC3220-1 will switch into 1.5x mode. The CPO voltage will then start to increase and will attempt to reach 1.5× V_{IN} up to 4.6V. Any subsequent dropout will cause the part to enter the 2x mode. The CPO voltage will attempt to reach 2× V_{IN} up to 5.1V.

A 2-phase non-overlapping clock activates the charge pump switches. In the 2x mode the flying capacitors are charged on alternate clock phases from V_{IN} to minimize CPO voltage ripple. In 1.5x mode the flying capacitors are charged in series during the first clock phase and stacked in parallel on V_{IN} during the second phase. This sequence of charging and discharging the flying capacitors continues at a constant frequency of 850kHz.

The current delivered by each LED current source is controlled by an associated DAC. Each DAC is programmed via the I^2C port.

Soft-Start

Initially, when the part is in shutdown, a weak switch connects V_{IN} to CPO. This allows V_{IN} to slowly charge the CPO output capacitor and prevent large charging currents from occurring.

The LTC3220/LTC3220-1 also employ a soft-start feature on the charge pump to prevent excessive inrush current and supply droop when switching into the step-up modes. The current available to the CPO pin is increased linearly over a typical period of 125µs. Soft-start occurs at the start of both 1.5x and 2x mode changes.

Charge Pump Strength

When the LTC3220/LTC3220-1 operate in either 1.5x mode or 2x mode, the charge pump can be modeled as a Thevenin-equivalent circuit to determine the amount of current available from the effective input voltage and effective open-loop output resistance, R_{OL} (Figure 1).

R_{OL} is dependent on a number of factors including the switching term, $1/(2f_{OSC} \bullet C_{FLY})$, internal switch resistances and the non-overlap period of the switching circuit. However, for a given R_{OL}, the amount of current available will be directly proportional to the advantage voltage of $1.5V_{IN}$ – CPO for 1.5x mode and $2V_{IN}$ – CPO for 2x mode. Consider the example of driving LEDs from a 3.1V supply.

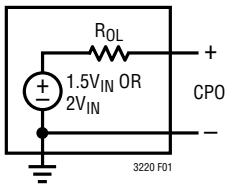


Figure 1. Charge Pump Open-Loop Thevenin Equivalent Circuit

OPERATION

If the LED forward voltage is 3.8V and the current sources require 100mV, the advantage voltage for 1.5x mode is 3.1V • 1.5 – 3.8V – 0.1V or 750mV. Notice that if the input voltage is raised to 3.2V, the advantage voltage jumps to 900mV, a 20% improvement in available strength.

From Figure 1, for 1.5x mode the available current is given by:

$$I_{OUT} = \frac{1.5V_{IN} - V_{CPO}}{R_{OL}} \quad (1)$$

For 2x mode, the available current is given by:

$$I_{OUT} = \frac{2V_{IN} - V_{CPO}}{R_{OL}} \quad (2)$$

Notice that the advantage voltage in this case is 3.1V • 2 – 3.8V – 0.1V = 2.3V. R_{OL} is higher in 2x mode but a significant overall increase in available current is achieved.

Mode Switching

The LTC3220/LTC3220-1 will automatically switch from 1x mode to 1.5x mode and subsequently to 2x mode whenever a dropout condition is detected at an LED pin. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. The mode change will not occur unless dropout exists for approximately 400µs.

The mode will automatically switch back to 1x whenever a register is updated via the I^2C port, when gradation completes ramping down and after each blink period.

The parts can be forced to operate in 1x, 1.5x or 2x mode by writing the appropriate bits into REG0. This feature may be used for operating loads powered by CPO.

Non-programmed current sources do not affect dropout.

Universal Current Sources (ULED1 to ULED18)

There are eighteen universal 20mA current sources. Each current source has a 6-bit linear DAC for current control. The output current range is 0mA to 20mA in 64 steps.

Each current source is disabled when an all zero data word is written. The supply current for that source is reduced to zero. Unused outputs should be connected to GND.

GPO Mode

ULED1 to ULED18 can be used as general purpose outputs (GPO). Current sources in the GPO mode can be used as I^2C controlled open-drain drivers. A ULED output can be selected to operate in GPO mode by programming both Bit 6 and Bit 7 of its data register (REG1 to REG18) to a logic high. In the GPO mode, dropout detection is disabled and output swings to ground will not cause mode switching.

The GPOs can be programmed to either act as a switch (strong pull-down mode) in which the part will only consume approximately 3µA of quiescent current, or they can be programmed to have a regulated current of up to 20mA (current limit mode), which would require several hundred microamps of additional quiescent current.

When a ULED output is used in GPO mode during shutdown, CPO should not be used as a power source since the current available from the CPO pin would be limited by the weak pull-up current source. This weak pull-up is only meant to keep the output capacitor charged to V_{IN} during shutdown and is unable to supply large amounts of current. CPO can, however, be used as a power source when the part is enabled.

Conversely, when a ULED output is used in GPO strong pull-down mode, a current limiting resistor should be used in series with the ULED output so that the current does not exceed the Absolute Maximum rated current.

OPERATION

Blinking

Each universal output (ULED1 to ULED18) can be set to blink with an on time of 0.156 seconds, or 0.625 seconds and a period of 1.25 seconds, or 2.5 seconds via the I^2C port. The blinking rate is selected via REG19 and ULED outputs are selected via REG1 to REG18. Blinking and gradation rates are independent. Please refer to Application Note 115 for detailed information and examples on programming blinking.

Gradation

Universal LED outputs ULED1 to ULED18 can be set to have the current ramp up and down at 0.24 seconds, 0.48 seconds and 0.96 seconds rates via the I^2C port. Each of these outputs can have either blinking or gradation enabled. The gradation time is set via REG19 and ULED outputs are selected via REG1 to REG18. The ramp direction is also controlled via REG19. Setting the up bit high causes gradation to ramp up, setting this bit to a low causes gradation to ramp down. Please refer to Application Note 115 for detailed information and examples on programming gradation.

When gradation is disabled the LED output current remains at the programmed value.

The charge pump mode is reset to 1x mode after gradation completes ramping down.

Chip Reset ($\overline{RST}$)

The $\overline{RST}$ pin is used to turn off the chip, including the charge pump and all ULED outputs, and clear all registers in the LTC3220/LTC3220-1. When $\overline{RST}$ is low, the part is in shutdown and cannot be programmed through the I^2C port.

Shutdown Current

Shutdown occurs when all the current source data bits have been written to zero, when the shutdown bit in REG0 is written with a logic 1, when $\overline{RST}$ is pulled low, or when DV_{CC} is set below the undervoltage lockout voltage.

Although the LTC3220/LTC3220-1 are designed to have very low shutdown current, they will draw about 3µA from V_{IN} when in shutdown. Internal logic ensures that the LTC3220/LTC3220-1 are in shutdown when DV_{CC} is low. Note, however that all of the logic signals that are referenced to DV_{CC} (SCL, SDA and $\overline{RST}$) will need to be at DV_{CC} or below (i.e., ground) to avoid violation of the absolute maximum specifications on these pins.

EMI Reduction

The flying capacitor pins C1M, C1P, C2M and C2P have controlled slew rates to reduce conducted and radiated noise.

Serial Port

The microcontroller compatible I^2C serial port provides all of the command and control inputs for the LTC3220/LTC3220-1. Data on the SDA input is loaded on the rising edge of SCL. D7 is loaded first and D0 last. There are 20 data registers, one address register and one sub-address register. Once all address bits have been clocked into the address register, an acknowledge occurs. The sub-address

OPERATION

register is then written to, followed by the data register. Each data register has a sub-address. After the data register has been written a load pulse is created after the stop bit. The load pulse transfers all of the data held in the data registers to the DAC registers. The stop bit can be delayed until all of the data master registers have been written. At this point the LED current will be changed to the new settings. The serial port uses static logic registers so there is no minimum speed at which it can be operated.

I²C Interface

The LTC3220/LTC3220-1 communicate with a host (master) using the standard I²C 2-wire interface. The Timing Diagram (Figure 3) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines.

The LTC3220/LTC3220-1 are receive-only (slave) devices.

There are two I²C addresses available. The LTC3220 I²C address is 0011100 and the LTC3220-1 I²C address is 0011101. The I²C address is the only difference between the LTC3220 and LTC3220-1.

Write Word Protocol Used By the LTC3220/LTC3220-1

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	*Sub-Address	A	Data Byte	A	P**

S = Start Condition, Wr = Write Bit = 0, A = Acknowledge,
P = Stop Condition
*The sub-address uses only the first 5 bits, D0, D1, D2, D3 and D4.
**Stop can be delayed until all of the data registers have been written.

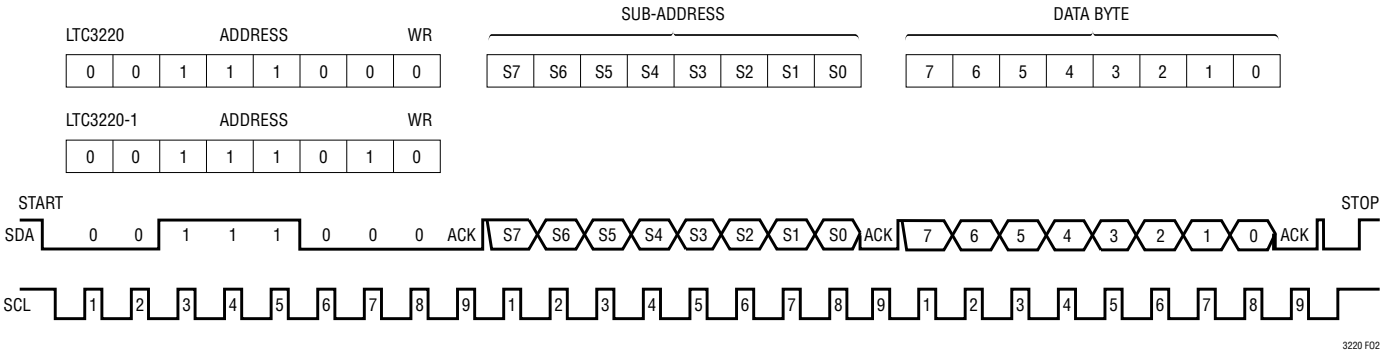


Figure 2. Bit Assignments

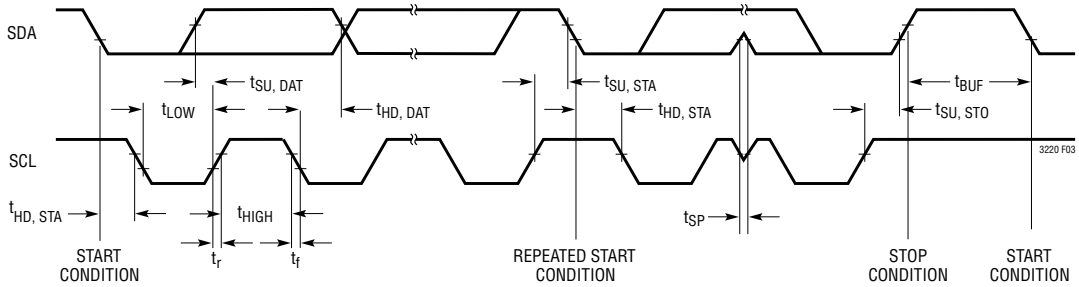


Figure 3. Timing Parameters

OPERATION

Sub-Address Byte

MSB							LSB		
7	6	5	4	3	2	1	0	Register	Function
0	0	0	0	0	0	0	0	REG0	COMMAND
0	0	0	0	0	0	0	1	REG1	ULED1
0	0	0	0	0	0	1	0	REG2	ULED2
0	0	0	0	0	0	1	1	REG3	ULED3
0	0	0	0	0	1	0	0	REG4	ULED4
0	0	0	0	0	1	0	1	REG5	ULED5
0	0	0	0	0	1	1	0	REG6	ULED6
0	0	0	0	0	1	1	1	REG7	ULED7
0	0	0	0	1	0	0	0	REG8	ULED8
0	0	0	0	1	0	0	1	REG9	ULED9
0	0	0	0	1	0	1	0	REG10	ULED10
0	0	0	0	1	0	1	1	REG11	ULED11
0	0	0	0	1	1	0	0	REG12	ULED12
0	0	0	0	1	1	0	1	REG13	ULED13
0	0	0	0	1	1	1	0	REG14	ULED14
0	0	0	0	1	1	1	1	REG15	ULED15
0	0	0	1	0	0	0	0	REG16	ULED16
0	0	0	1	0	0	0	1	REG17	ULED17
0	0	0	1	0	0	1	0	REG18	ULED18
0	0	0	1	0	0	1	1	REG19	GRAD/ BLINK

REG0, Command Byte.

Register Sub-Address = 0000

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
Unused	Unused	Unused	Unused	Shutdown	Force2x	Force1p5x	Quick write

Quick write	0 1	Serial write to each register Parallel write, REG1 data is written to all eighteen universal registers
Force1p5	1 0	Forces charge pump into 1.5x mode Enables mode logic to control mode changes based on dropout signal
Force2x	1 0	Forces charge pump into 2x mode Enables mode logic to control mode changes based on dropout signal
Force1x		D1 (Force1p5x) = 1 D2 (Force2x) = 1 } Forces Charge Pump into 1x Mode
Shutdown	1 0	Shuts down part while preserving data in registers Normal operation

OPERATION

Data Bytes

REG1 to REG18, Universal LED 6-bit linear DAC data with blink/gradation.

Sub-Address 00001 to 10010 per Sub-Address Table

Blink/Gradation/Dropout Enable MSB			LED Current Data					LSB
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Normal	0	0	D5	D4	D3	D2	D1	D0
Blink Enabled	0	1	D5	D4	D3	D2	D1	D0
Gradation Enabled	1	0	D5	D4	D3	D2	D1	D0
GPO Mode*								
Strong Pull-Down Mode	1	1	0	0	0	0	0	0
Current Limited Mode	1	1	D5	D4	D3	D2	D1	D0
High Impedance/Off	0	0	0	0	0	0	0	0
*(Gradation/Blink/Dropout Off)								

REG19, Gradation and Blinking

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
Unused	Unused	Unused	GB4	GB3	GB2	GB1	Up

Up	0	Gradation counts down
	1	Gradation counts up

Blink Times and Period				Gradation Ramp Times and Period			
D4 (GB4)	D3 (GB3)	On Time	Period	D2 (GB2)	D1 (GB1)	Ramp Time	Period
0	0	0.625s	1.25s	0	0	Disabled	Disabled
0	1	0.156s	1.25s	0	1	0.24s	0.313s
1	0	0.625s	2.5s	1	0	0.48s	0.625s
1	1	0.156s	2.5s	1	1	0.96s	1.25s

Bus Speed

The I^2C port is designed to be operated at speeds up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I^2C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

Start and Stop Conditions

A bus-master signals the beginning of a communication to a slave device by transmitting a START condition.

A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

OPERATION

Byte Format

Each byte sent to the LTC3220/LTC3220-1 must be 8 bits long followed by an extra clock cycle for the acknowledge bit to be returned by the LTC3220/LTC3220-1. The data should be sent to the LTC3220/LTC3220-1 most significant bit (MSB) first.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. An acknowledge (active low) generated by the slave (LTC3220/LTC3220-1) lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (high) during the acknowledge clock cycle. The slave-receiver must pull down the SDA line during the acknowledge clock pulse so that it remains a stable low during the high period of this clock pulse.

Slave Address

Each version of LTC3220/LTC3220-1 responds to a unique address which has been factory programmed (Table 1). The eighth bit of the address byte (R/W) must be 0 for the LTC3220/LTC3220-1 to recognize the address since it is a write only device. This effectively forces the address to be 8 bits long where the least significant bit of the address is 0. If the correct seven bit address is given but the R/W bit is 1, the LTC3220/LTC3220-1 will not respond.

Table 1. LTC3220/LTC3220-1 Factory Programmed Slave Address

PART NUMBER	SLAVE ADDRESS
LTC3220	0011100
LTC3220-1	0011101

Bus Write Operation

The master initiates communication with the LTC3220/LTC3220-1 with a START condition and a 7-bit address followed by the write bit R/W = 0. If the address matches that of the LTC3220/LTC3220-1, the LTC3220/LTC3220-1 return an acknowledge. The master should then deliver the most significant sub-address byte for the data register to be written. Again the LTC3220/LTC3220-1 acknowledge and then the data is delivered starting with the most significant bit. This cycle is repeated until all of the required data registers have been written. Any number of data latches can be written. Each data byte is transferred to an internal holding latch upon the return of an acknowledge. After all data bytes have been transferred to the LTC3220/LTC3220-1, the master may terminate the communication with a STOP condition. Alternatively, a Repeat-START condition can be initiated by the master and another chip on the I^2C bus can be addressed. This cycle can continue indefinitely and the LTC3220/LTC3220-1 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP condition can be sent and the LTC3220/LTC3220-1 will update all registers with the data that it had received.

In certain circumstances the data on the I^2C bus may become corrupted. In these cases the LTC3220/LTC3220-1 respond appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3220/LTC3220-1 has been successfully addressed and is receiving data when a STOP condition mistakenly occurs. The LTC3220/LTC3220-1 will ignore this STOP condition and will not respond until a new START condition, correct address, sub-address and new set of data and STOP condition are transmitted.

Likewise, if the LTC3220/LTC3220-1 were previously addressed and sent valid data but not updated with a STOP, they will respond to any STOP that appears on the bus with only one exception, independent of the number of Repeat-START's that have occurred. If a Repeat-START is given and the LTC3220/LTC3220-1 successfully acknowledge their addresses and first byte, they will not respond to a STOP until all bytes of the new data have been received and acknowledged.

Quick Write

Registers REG1 to REG18 can be written in parallel by setting Bit 0 of REG 0 high. When this bit is set high the next write sequence to REG1 will write the data to REG1 through REG18, which are all of the universal LED registers.

APPLICATIONS INFORMATION

V_{IN}, CPO Capacitor Selection

The style and value of the capacitors used with the LTC3220/LTC3220-1 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) ceramic capacitors are used for both C_{VIN} and C_{CPO}. Tantalum and aluminum capacitors are not recommended due to high ESR.

The value of C_{CPO} directly controls the amount of output ripple for a given load current. Increasing the size of C_{CPO} will reduce output ripple at the expense of higher start-up current. The peak-to-peak output ripple of the 1.5x mode is approximately given by the expression:

$$V_{RIPPLEP-P} = \frac{I_{OUT}}{3f_{OSC} \bullet C_{CPO}} \quad (3)$$

where f_{OSC} is the LTC3220/LTC3220-1 oscillator frequency or typically 850kHz and C_{CPO} is the output storage capacitor.

The output ripple in 2x mode is very small due to the fact that load current is supplied on both cycles of the clock.

Both type and value of the output capacitor can significantly affect the stability of the LTC3220/LTC3220-1. As shown in the Block Diagram, the LTC3220/LTC3220-1 use a control loop to adjust the strength of the charge pump to match the required output current. The error signal of the loop is stored directly on the output capacitor. The output capacitor also serves as the dominant pole for the control loop. To prevent ringing or instability, it is important for the output capacitor to maintain at least 3.2µF of capacitance over all conditions and the ESR should be less than 80mΩ.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout will result in very good stability. As the value of C_{CPO} controls the amount of output ripple, the value of C_{VIN} controls the amount of ripple present at the input pin (V_{IN}). The LTC3220/LTC3220-1 input current will be relatively constant while the charge pump is either in the input charging phase or the output charging phase but will drop to zero during the clock nonoverlap times. Since the nonoverlap time is small (~25ns), these missing "notches" will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the higher ESR. Therefore, ceramic capacitors are recommended for low ESR. Input noise can be further reduced by powering the LTC3220/LTC3220-1 through a very small series inductor as shown in Figure 4. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

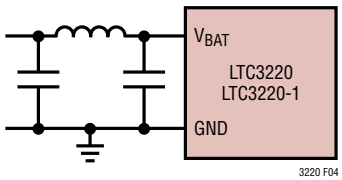


Figure 4. 10nH Inductor Used for Input Noise Reduction (Approximately 1cm of Board Space)

APPLICATIONS INFORMATION

Flying Capacitor Selection

Warning: Polarized capacitors such as tantalum or aluminum should never be used for the flying capacitors since their voltage can reverse upon start-up of the LTC3220/LTC3220-1. Ceramic capacitors should always be used for the flying capacitors.

The flying capacitors control the strength of the charge pump. In order to achieve the rated output current it is necessary to have at least 1.6µF of capacitance for each of the flying capacitors. Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X7R material will retain most of its capacitance from –40°C to 85°C, whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a very poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1µF, 10V, Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF, 10V, X7R available in the same case. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitances at all temperatures and voltages.

Table 2 shows a list of ceramic capacitor manufacturers and how to contact them:

Table 2. Recommended Capacitor Vendors

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com

Layout Considerations and Noise

The LTC3220/LTC3220-1 have been designed to minimize EMI. However due to their high switching frequency and the transient currents produced by the LTC3220/LTC3220-1, careful board layout is necessary. A true ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions.

The flying capacitor pins C1P, C2P, C1M and C2M have controlled edge rate waveforms. The large dV/dt on these pins can couple energy capacitively to adjacent PCB runs. Magnetic fields can also be generated if the flying capacitors are not close to the LTC3220/LTC3220-1 (i.e., the loop area is large). To decouple capacitive energy transfer, a Faraday shield may be used. This is a grounded PCB trace between the sensitive node and the LTC3220/LTC3220-1 pins. For a high quality AC ground, it should be returned to a solid ground plane that extends all the way to the LTC3220/LTC3220-1.

APPLICATIONS INFORMATION

Power Efficiency

To calculate the power efficiency (η) of an LED driver chip, the LED power should be compared to the input power. The difference between these two numbers represents lost power whether it is in the charge pump or the current sources. Stated mathematically, the power efficiency is given by:

$$\eta = \frac{P_{LED}}{P_{IN}} \quad (4)$$

The efficiency of the LTC3220/LTC3220-1 depends upon the mode in which it is operating. Recall that the LTC3220/LTC3220-1 operate as pass switches, connecting V_{IN} to CPO, until dropout is detected at the I_{LED} pin. This feature provides the optimum efficiency available for a given input voltage and LED forward voltage. When it is operating as a switch, the efficiency is approximated by:

$$\eta = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{IN} \bullet I_{IN}} = \frac{V_{LED}}{V_{IN}} \quad (5)$$

since the input current will be very close to the sum of the LED currents.

At moderate to high output power, the quiescent current of the LTC3220/LTC3220-1 is negligible and the expression above is valid.

Once dropout is detected at any LED pin, the LTC3220/LTC3220-1 enable the charge pump in 1.5x mode.

In 1.5x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 1.5 times the actual input voltage. This is because the input current for a 1.5x charge pump is approximately 1.5 times the load current. In an ideal 1.5x charge pump, the power efficiency would be given by:

$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{IN} \bullet 1.5 \bullet I_{LED}} = \frac{V_{LED}}{1.5 \bullet V_{IN}}$$

Similarly, in 2x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 2 times the actual input voltage. In an ideal 2x charge pump, the power efficiency would be given by:

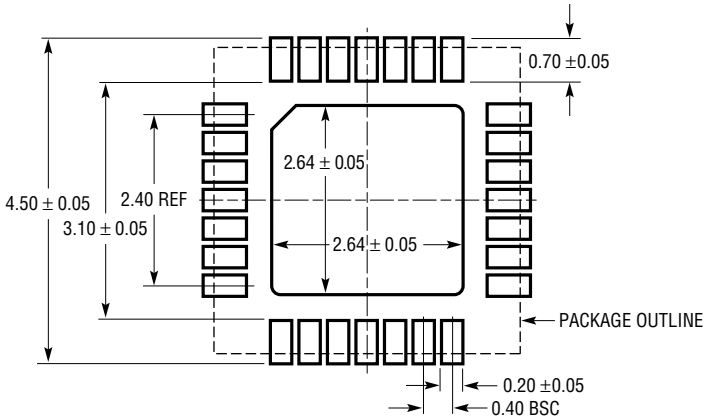
$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{IN} \bullet 2 \bullet I_{LED}} = \frac{V_{LED}}{2 \bullet V_{IN}}$$

Thermal Management

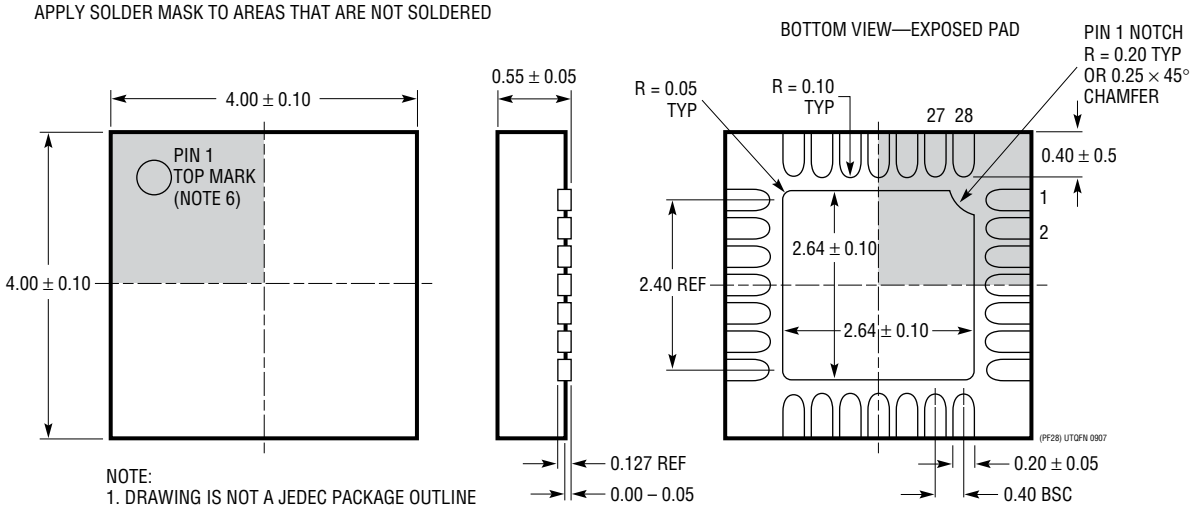
For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3220/LTC3220-1. If the junction temperature increases above approximately 150°C, the thermal shutdown circuitry will automatically deactivate the output current sources and charge pump. To reduce maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the Exposed Pad to a ground plane and maintaining a solid ground plane under the device will reduce the thermal resistance of the package and PC board considerably.

PACKAGE DESCRIPTION

PF Package
28-Lead UTQFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1759 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	06/15	Modified REG0, Command Byte table	12