Wide V_{IN} Range Dual Output 350mA Step-Down Charge Pump with Watchdog Timer

FEATURES

- **Input Voltage Range: 5.5V to 38V**
- **Independently Enabled 5V and 3.3V Fixed Outputs**
- **5V Output: 100mA Max**
- **3.3V LDO Output: 250mA Max**
- **Multimode Step-Down Charge Pump (2:1, 1:1) with Automatic Mode Switching**
- **Low Quiescent Current**
  - **20µA with Both Outputs Regulating (No Load)**
  - **0.5µA in Shutdown**
- **Engineered for Diagnostic Coverage in ISO26262 Systems**
- 1.1V Reference Output for System Diagnostics
- Power-On Reset and Watchdog Controller with Adjustable Timing
- Overcurrent Fault Protection on Each Output
- Overtemperature Protection
- 150°C Max Operating Junction Temperature
- Thermally Enhanced 16-Lead MSOP Package

APPLICATIONS

- Automotive ECU/CAN Transceiver Supplies
- Industrial/Telecom Housekeeping Supplies
- Low Power 12V to 5V and 3.3V Conversion

DESCRIPTION

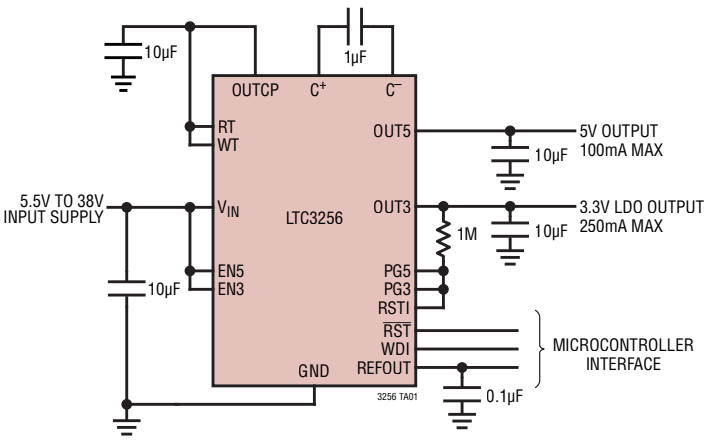
The LTC®3256 is a wide input range switched capacitor step-down DC/DC converter that produces two regulated outputs: a 5V output via direct connection to the charge pump output, and a 3.3V output via a low dropout (LDO) linear post-regulator. The device provides up to 350mA of total output current. At 12V V_{IN} and maximum load on both outputs, power dissipation is reduced by over 2W compared to a dual LDO regulator solution.

The LTC3256 maximizes efficiency by running the charge pump in 2:1 mode over as wide an operating range as possible, and automatically switches to 1:1 mode as needed due to V_{IN} and load conditions. Controlled input current and switching slew rates minimize conducted and radiated EMI. An integrated watchdog timer, independent power good outputs and reset input ensure reliable system operation and fault monitoring. A buffered 1.1V reference output enables system self-testing for safety critical applications.

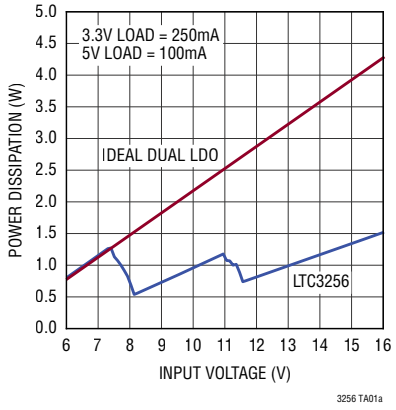
The LTC3256 has numerous safety features including overcurrent fault protection, overtemperature protection and tolerance of 38V input transients. The LTC3256 is available in a thermally enhanced 16-lead MSOP plastic package with exposed pad (MSE16).

TYPICAL APPLICATION

High Efficiency Dual Output Power Supply



Power Dissipation vs Input Voltage

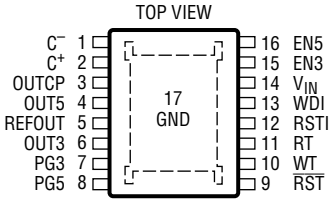


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, EN3, EN5, WDI ..... –0.3V to 38V
OUTCP, OUT3, OUT5 ..... –0.3V to 5.5V
OUT3, OUT5 Short Circuit Duration ..... Indefinite
PG3, PG5, REFOUT ..... –0.3V to V_{OUTCP}
$\overline{RST}$ ..... –0.3V to 5.5V
WT, RT ..... –0.3V to V_{OUTCP}
RSTI ..... –0.3V to 5.5V
Operating Junction Temperature Range (Notes 3, 4)
LTC3256E ..... –40°C to 125°C
LTC3256I ..... –40°C to 125°C
LTC3256H ..... –40°C to 150°C
LTC3256MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JC} = 10°C/W
θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3256#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3256EMSE#PBF	LTC3256EMSE#TRPBF	3256	16-Lead Plastic MSOP	–40°C to 125°C
LTC3256IMSE#PBF	LTC3256IMSE#TRPBF	3256	16-Lead Plastic MSOP	–40°C to 125°C
LTC3256HMSE#PBF	LTC3256HMSE#TRPBF	3256	16-Lead Plastic MSOP	–40°C to 150°C
LTC3256MPMSE#PBF	LTC3256MPMSE#TRPBF	3256	16-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 12V, C_{FLY} = 1µF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Input Voltage Range (Note 5)		●	5.5		38	V
	V_{IN} Undervoltage Lockout Threshold		●		1.8	2.7	V
	V_{IN} Quiescent Current EN5 = EN3 = 0V Only One Output Enabled Both OUT3 and OUT5 Enabled	 Shutdown Output In Regulation, No Load Output In Regulation, No Load			 0.5 15 20	 2 30 35	 µA µA µA
	EN3, EN5 Input High Voltage				1.2	2	V
	EN3, EN5 Input Low Voltage			0.4	0.9		V
	EN3, EN5 Input Low Current	V_{PIN} = 0V		–1	0	1	µA
	EN3, EN5 Input High Current	V_{PIN} = 38V			1	3	µA
Charge Pump Operation							
V_{OUTCP}	OUTCP Regulation Voltage	EN3 and/or EN5 High			5.05		V
	OUTCP Short Circuit Current	V_{OUTCP} = GND			600		mA
	Charge Pump Output Impedance	2:1 Step-Down Mode 1:1 Step-Down Mode, V_{IN} = 5.5V			2 2		Ω Ω
5V Output Operation							
V_{OUT5}	Fixed 5V Output Regulation (Note 5)	EN5 High, V_{IN} = 5.5V, $I_{OUT} \le$ 100mA EN5 High, V_{IN} = 12V, $I_{OUT} \le$ 100mA EN5 High, V_{IN} = 38V, I_{OUT} = 0mA	● ● ●	4.85 4.85 4.85	5.05 5.05 5.05	5.19 5.19 5.19	V V V
	OUTCP to OUT5 Power Switch On-Resistance	EN5 High			0.6		Ω
	OUT5 Overvoltage Threshold	V_{OUT5} Rising Makes PG5 Go Low V_{OUT5} Falling Makes PG5 Go Hi-Z	●		5.25 5.1	5.4	V V
	OUT5 Undervoltage Threshold	V_{OUT5} Rising Makes PG5 go Hi-Z V_{OUT5} Falling Makes PG5 go Low	 ●	 4.6	4.9 4.75		V V
	PG5 Output Low Voltage	I_{PG5} = 100µA	●		0.1	0.4	V
	PG5 Output Hi-Z Leakage	V_{PG5} = 5V	●	–1	0	1	µA
3.3V LDO Operation							
V_{OUT3}	Fixed 3.3V LDO Output Regulation (Note 5)	EN3 High, V_{IN} = 5.5V, $I_{OUT} \le$ 250mA EN3 High, V_{IN} = 12V, $I_{OUT} \le$ 250mA EN3 High, V_{IN} = 38V, I_{OUT} = 0mA	● ● ●	3.170 3.200 3.234	3.30 3.30 3.30	3.366 3.366 3.366	V V V
	OUT3 Overvoltage Threshold	V_{OUT3} Rising Makes PG3 Go Low V_{OUT3} Falling Makes PG3 Go Hi-Z	●		3.465 3.35	3.58	V V
	OUT3 Undervoltage Threshold	V_{OUT3} Rising Makes PG3 Go Hi-Z V_{OUT3} Falling Makes PG3 Go Low	 ●	 3.04	3.24 3.135		V V
	PG3 Output Low Voltage	I_{PG3} = 100µA	●		0.1	0.4	V
	PG3 Output Hi-Z Leakage	V_{PG3} = 5V	●	–1	0	1	µA
Buffered 1.1V Reference Output (REFOUT)							
	REFOUT Pin Output Voltage	EN3 and/or EN5 High, I_{REFOUT} = 0mA	●	1.068	1.1	1.132	V
	REFOUT Pin Output Resistance				2	4	kΩ
Reset Timer Control (RT)							
	External Timer RT Pull-Up Current	V_{RT} = 0.3V	●	–1.1	–1.9	–2.6	µA
	External Timer RT Pull-Down Current	V_{RT} = 1.3V	●	1.1	1.9	2.6	µA
	Internal Timer RT Pull Down Current	V_{RT} = V_{OUTCP}	●		0.25	1	µA
	RT Internal Timer Select Threshold		●	1.8	2.3	2.7	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). V_{IN} = 12V, C_{FLY} = 1µF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reset Timer Input (RSTI)							
	RSTI Input High Voltage		●		1.2	1.26	V
	RSTI Input Low Voltage		●	1.1	1.16		V
	RSTI Input Low Current	V_{RST_IN} = 0V	●	–1	0	1	µA
	RSTI Input High Current	V_{RST_IN} = 5V	●	–1	0	1	µA
Reset Output ($\overline{RST}$)							
$t_{RST(INT)}$	Internal Reset Timeout Period	V_{RT} = V_{OUTCP}	●	150	200	260	ms
$t_{RST(EXT)}$	External Reset Timeout Period	C_{RT} = 2.2nF	●	26	32	44	ms
t_{UV}	RSTI Low to $\overline{RST}$ Asserted	From RSTI falling to 1V or less	●	10	80	150	µs
	$\overline{RST}$ Output Voltage Low	V_{OUTCP} = 5V, I_{RST} = 100µA	●		0.1	0.4	V
	$\overline{RST}$ Output Voltage High Leakage	$\overline{RST}$ = 5V	●	–1	0	1	µA
Watchdog Timer Control (WT)							
	External Timer WT Pull-Up Current	V_{WT} = 0.3V	●	–1.1	–1.9	–2.6	µA
	External Timer WT Pull-Down Current	V_{WT} = 1.3V	●	1.1	1.9	2.6	µA
	Internal Timer WT Detect Pull Down Current	V_{WT} = V_{OUTCP}	●		0.25	1	µA
	WT Internal Timer Select Threshold		●	1.8	2.3	2.7	V
Watchdog Input (WDI)							
$t_{WDU(INT)}$	Internal Watchdog Upper Boundary	V_{WT} = V_{OUTCP}	●	1.3	1.6	2	s
$t_{WDL(INT)}$	Internal Watchdog Lower Boundary	V_{WT} = V_{OUTCP}	●	37.5	50	62.5	ms
$t_{WDR(EXT)}$	External Watchdog Reset Time	C_{WT} = 2.2nF	●	200	260	340	ms
$t_{WDU(EXT)}$	External Watchdog Upper Boundary			$t_{WDR(EXT)}$ • (128/129)			ms
$t_{WDL(EXT)}$	External Watchdog Lower Boundary			$t_{WDR(EXT)}$ • (5/129)			ms
	WDI Input High Voltage				1.2	2	V
	WDI Input Low Voltage			0.4	0.9		V
	WDI Input Low Current	V_{WD_IN} = 0V		–1	0	1	µA
	WDI Input High Current	V_{WD_IN} = 5V		–1	0	1	µA
	Input Pulsewidth		●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are referenced to GND unless otherwise specified.

Note 3: The LTC3256E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3256I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3256H is guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3256MP is guaranteed and tested over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

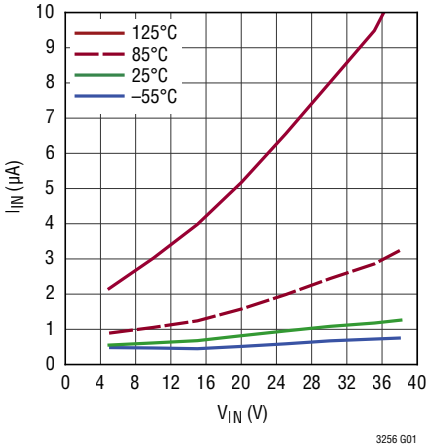
where θ_{JA} (in °C/W) is the package thermal impedance.

Note 4: This IC has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

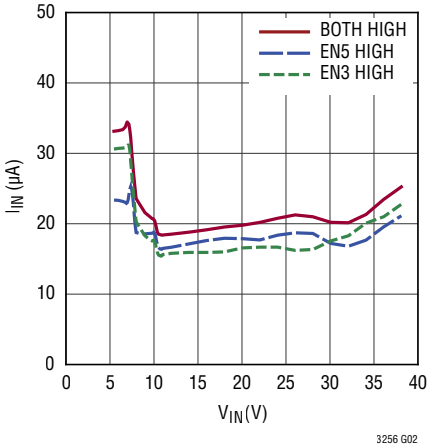
Note 5: The maximum operating junction temperature of 150°C must be followed. Certain combinations of input voltage and output current will cause the junction temperature to exceed 150°C and must be avoided. See Thermal Management section for information on calculating maximum operating conditions. Due to thermal limitations of production equipment, only no load regulation is checked at 38V.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

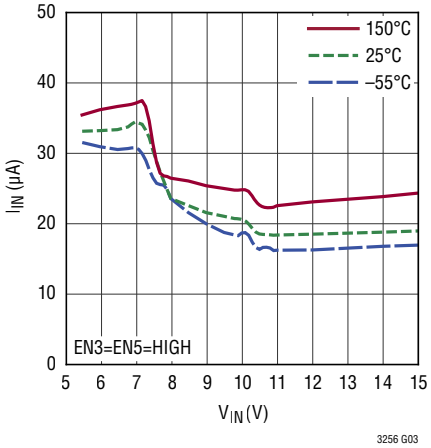
Input Shutdown Current vs Input Voltage



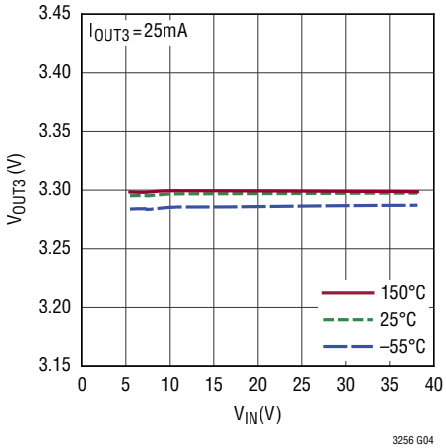
No Load Input Current vs Input Voltage



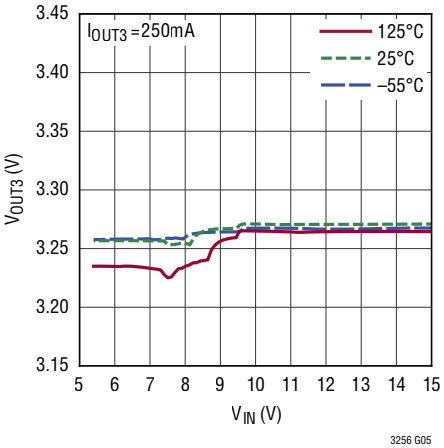
Input Operating Current vs Input Voltage



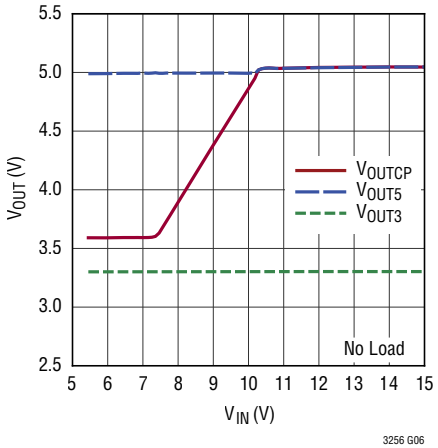
3.3V Output Voltage vs Input Voltage at 25mA



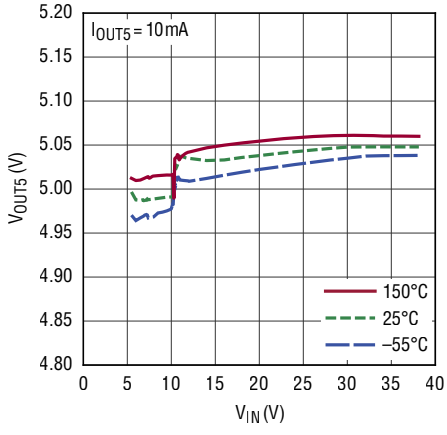
3.3V Output Voltage vs Input Voltage at 250mA



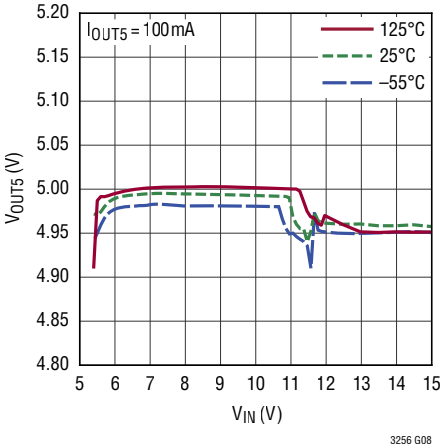
Output Voltages vs Input Voltage



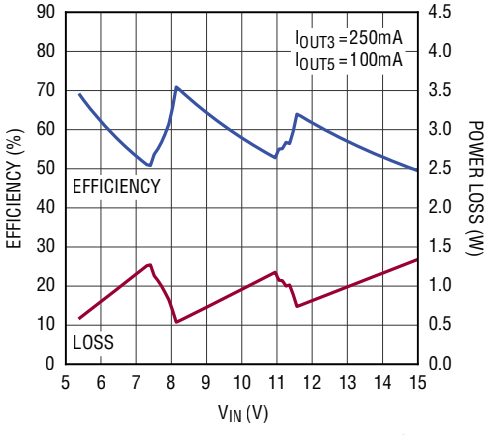
5V Output Voltage vs Input Voltage at 10mA



5V Output Voltage vs Input Voltage at 100mA

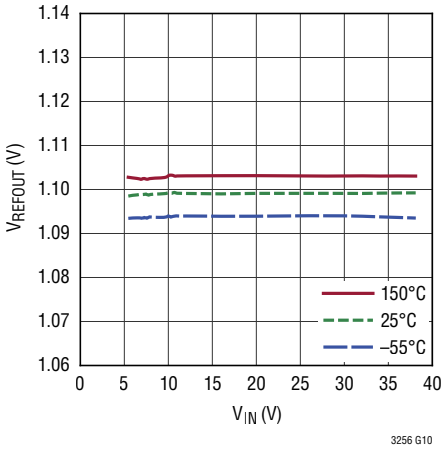


Efficiency and Power Loss vs Input Voltage

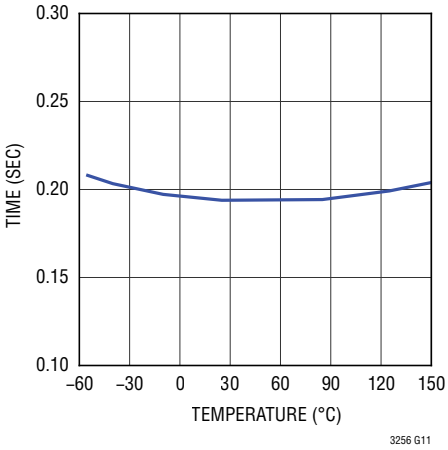


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

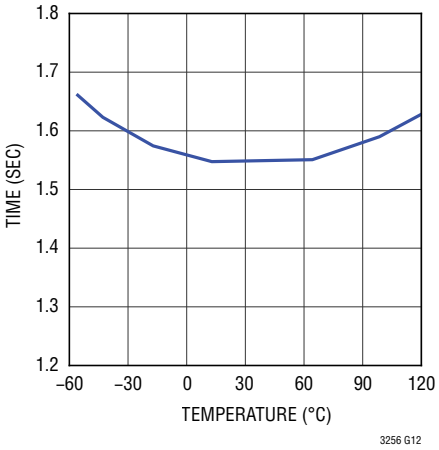
REFOUT Voltage vs Input Voltage



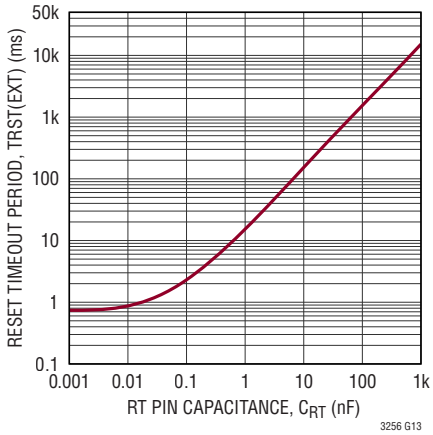
Internal Reset Timeout Period vs Temperature



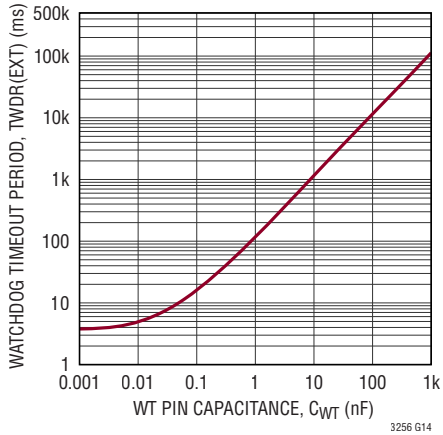
Internal Watchdog Timeout Period vs Temperature



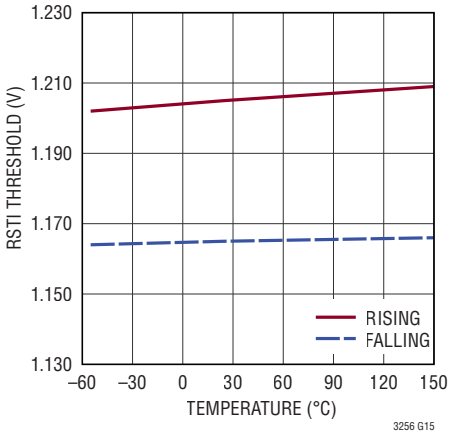
Reset Timeout Period vs RT Capacitance



Watchdog Timeout Period vs WT Capacitance

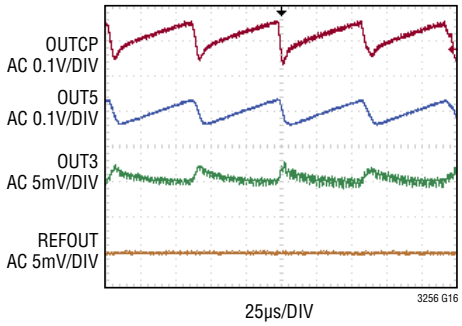


RSTI Threshold vs Temperature



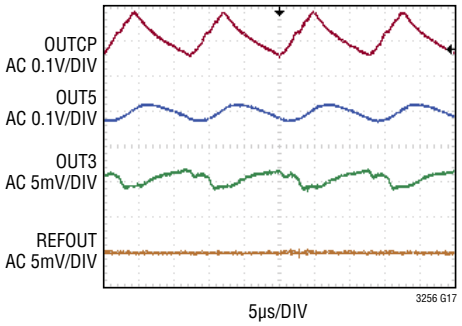
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Output Ripple



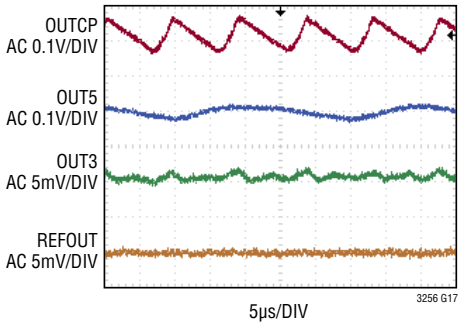
V_{IN} = 12V
I_{OUT5} = 100mA
I_{OUT3} = 250mA

Output Ripple



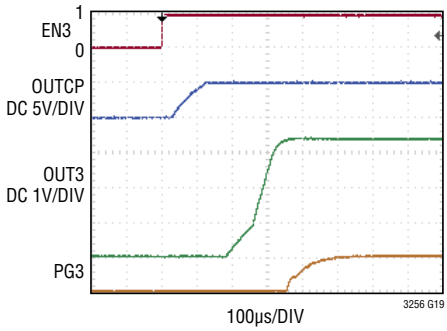
V_{IN} = 12V
I_{OUT5} = 20mA
I_{OUT3} = 100mA

Output Ripple



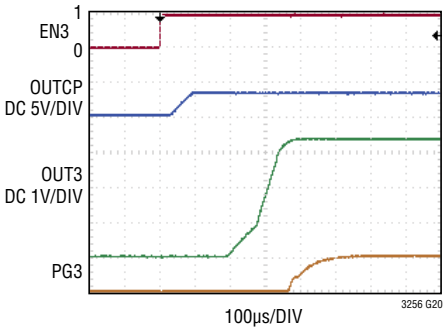
V_{IN} = 5.5V
OUT5 = 20mA
I_{OUT3} = 100mA

OUT3 Power-Up



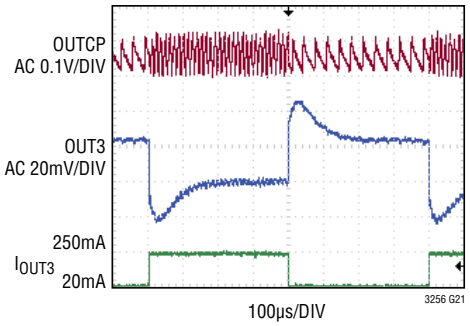
V_{IN} = 12V
R_{OUT3} = 33Ω

OUT3 Power-Up



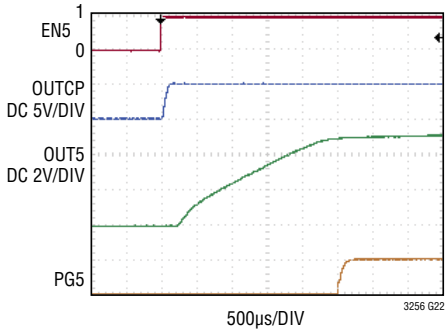
V_{IN} = 5.5V
R_{OUT3} = 33Ω

OUT3 Transient Response



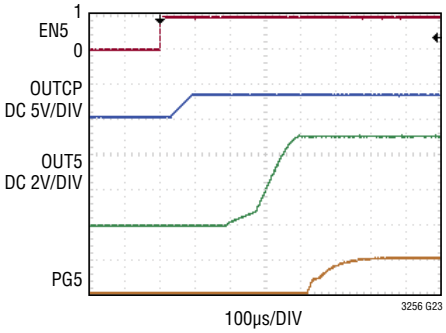
V_{IN} = 12V

OUT5 Power-Up



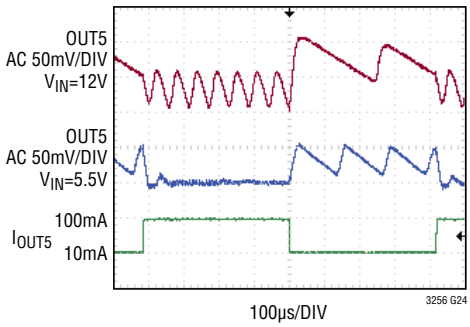
V_{IN} = 12V
R_{OUT5} = 100Ω

OUT5 Power-Up



V_{IN} = 5.5V
R_{OUT5} = 100Ω

OUT5 Transient Response



PIN FUNCTIONS

C^- (Pin 1): Charge Pump Flying Capacitor Negative Connection.

C^+ (Pin 2): Charge Pump Flying Capacitor Positive Connection.

OUTCP (Pin 3): Charge Pump Output. The charge pump output should be bypassed with a 10µF or greater X7R ceramic capacitor. The charge pump output is enabled if either ENx pin is logic high. OUTCP is the input supply for the 3.3V LDO.

OUT5 (Pin 4): 5V Output Pin. Connects to the charge pump output, OUTCP, through an internal power switch controlled by the EN5 input when V_{IN} > 10V (typical), and regulates to 5V with V_{IN} as a power source when V_{IN} < 10V (typical).

REFOUT (Pin 5): 1.1V Reference Output. Provides a buffered version of the LTC3256's internal bandgap reference voltage with 2k output impedance (typical). To maximize supply rejection, REFOUT should be bypassed with a 0.1µF ceramic capacitor.

OUT3 (Pin 6): 3.3V Low-Dropout Linear Regulator (LDO) Output Pin. The charge pump output, OUTCP, serves as the 3.3V LDO's input supply.

PG3 (Pin 7): Power Good Open Drain Logic Output. Goes high impedance when OUT3 is near its final operating voltage. PG3 is intended to be pulled up to a low voltage supply (such as OUT3, OUT5 or OUTCP) with an external resistor.

PG5 (Pin 8): Power Good Open Drain Logic Output. Goes high impedance when OUT5 is near its final operating voltage. PG5 is intended to be pulled up to a low voltage supply (such as OUT3, OUT5 or OUTCP) with an external resistor.

$\overline{RST}$ (Pin 9): Reset Open Drain Logic Output. The $\overline{RST}$ pin is low impedance to GND during the reset period, and goes high impedance during the watchdog period. $\overline{RST}$ is intended to be pulled up to low voltage supply (such as OUT3, OUT5, or OUTCP) with an external resistor.

WT (Pin 10): Watchdog Timer Control Pin. Attach an external capacitor (C_{WT}) to GND to set the watchdog upper boundary timeout. Tie WT to OUTCP to generate a timeout of about 1.6s. Tie WT and WDI to GND to disable the watchdog timer.

RT (Pin 11): Reset Timeout Control Pin. Attach an external capacitor (C_{RT}) to GND to set the reset timeout period, RT can be left open to minimize the reset timeout. Tie RT to OUTCP to generate a reset timeout of about 200ms.

RSTI (Pin 12): Reset Logic Comparator Input Pin. The RSTI input is compared to a 1.2V (typical) threshold voltage. If RSTI is below the threshold voltage the LTC3256 will enter the reset state and drive the $\overline{RST}$ pin low. Once RSTI rises above the threshold voltage, the reset timer is started and the $\overline{RST}$ pin is held low until the reset period times out.

WDI (Pin 13): Watchdog Logic Input Pin. Application circuitry must toggle the logic state of this pin such that falling edges occur at a rate faster than the watchdog upper boundary time but slower than the watchdog lower boundary time. If these conditions are not met, $\overline{RST}$ will be asserted low. Tie WT and WDI to GND to disable the watchdog timer. Do not float this pin.

V_{IN} (Pin 14): Power Input Pin. Input voltage for both charge pump and IC control circuitry.

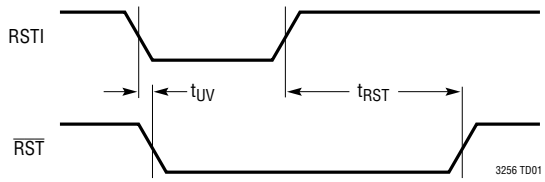
EN3 (Pin 15): Logic input pin which enables the 3.3V LDO when high and disables it when low. Bringing EN3 high causes the charge pump to enable if it isn't already on. The LDO powers up once the charge pump output, OUTCP, rises above 97.5% of its regulation value (typical). The EN3 pin has a 1µA (typical) pull down current to ground and can tolerate 38V inputs.

EN5 (Pin 16): Logic Input Pin. Enables or disables the 5V output, OUT5. Bringing EN5 high causes the charge pump to enable if it isn't already on. When the charge pump output rises above 97.5% of its regulation value (typical), a fault protected internal power switch connects OUTCP to OUT5, delivering power to any OUT5 load. A soft-start circuit limits any inrush current through the switch to help avoid glitching the charge pump output. If the input voltage falls below 10V (typical) and the charge pump regulates to a voltage lower than 5V, OUT5 receives its power directly from a V_{IN}-powered 1:1 mode regulator. The EN5 pin has a 1µA (typical) pull down current to ground and can tolerate 38V inputs.

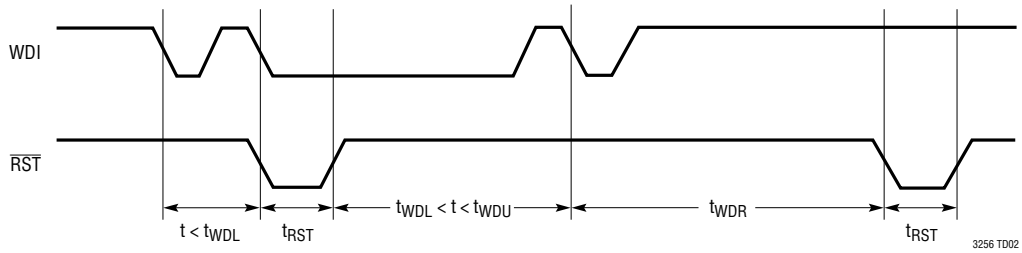
GND (Exposed Pad): Ground. The exposed package pad is ground and must be soldered to the PC board ground plane for proper functionality and for rated thermal performance.

TIMING DIAGRAM

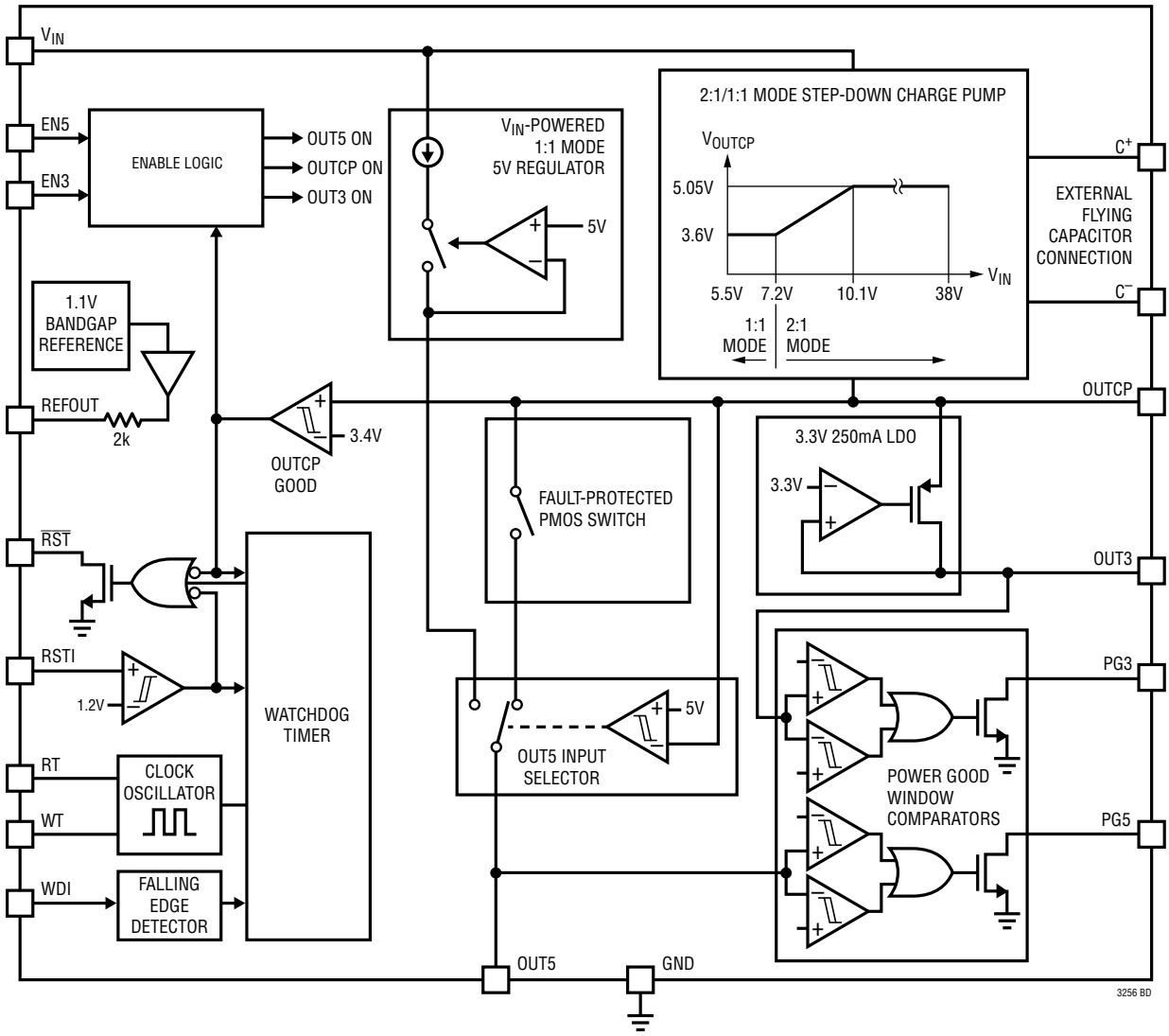
Reset Timing



Watchdog Timing



SIMPLIFIED BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LTC3256 is an inductorless wide input range step-down DC/DC converter that produces 5V and 3.3V regulated outputs with a total output current of 350mA. It uses a step-down charge pump with automatic 2:1/1:1 mode switching as a pre-regulator for the 5V and 3.3V outputs. This optimizes system efficiency and minimizes thermal problems due to excess power dissipation. In typical 12V automotive systems, the LTC3256 reduces power dissipation by a full 2W at maximum load relative to a dual LDO solution.

Each regulated output may be independently enabled to provide maximum flexibility. Enabling either of the regulator outputs will first turn on the step-down charge pump. Once the charge pump nears its regulation point, the enabled outputs will turn on in a controlled, soft-started manner. The 3.3V output is provided by an LDO that is always powered from the charge pump output. The 5V output is typically powered from the regulated charge pump via an overcurrent protected switch directly connected to the charge pump output.

The charge pump typically produces a regulated 5.05V output but allows this output to drop as needed in order to stay in 2:1 mode and maximize overall efficiency whenever V_{IN} falls below ~10.1V. If V_{IN} falls near the low end of its operating range, the charge pump automatically enters 1:1 mode as required to keep the 3.3V LDO in regulation. Whenever the charge pump output drops below 5V, the regulated 5V output will automatically be supplied using a simple gated switch regulator powered from V_{IN}.

2:1 Step-Down Charge Pump Operation (V_{IN} > ~10.1V)

The increased efficiency and reduced power dissipation advantages of the LTC3256 arise from the use of a 2:1 step-down charge pump to perform the bulk of the voltage step-down from V_{IN} to 5V and 3.3V. An ideal 2:1 charge-pump has the property that its input current is exactly half its output current (See Figure 1). In real-world charge pumps like the LTC3256, input current slightly exceeds half the output current due to additional current needed for biasing and for driving power switches.

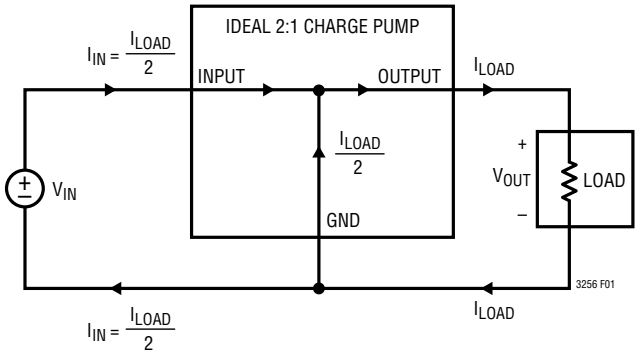


Figure 1. Steady-State Time-Averaged Current Flows in an Ideal 2:1 Charge Pump

Figure 2 shows the power switch topology of the 2:1 step-down charge pump in the LTC3256. When operating in 2:1 mode, the part employs a two phase clock to turn on only switches A and C in one phase followed by switches B and D only in the other phase. Current source I_A controls the maximum output current that the part can deliver. When the charge pump clock is active, V_{OUTCP} will increase towards $V_{IN}/2$. Once V_{OUTCP} reaches the appropriate regulation point, the charge pump shuts off all four switches and enters a SLEEP state to minimize quiescent current until the output voltage falls below its regulation point.

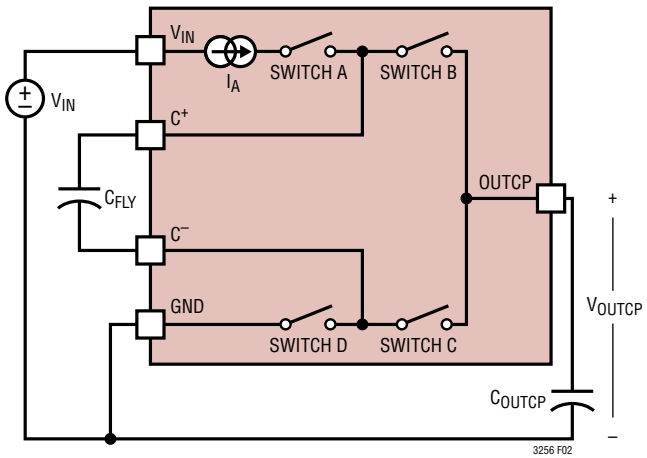


Figure 2. LTC3256 2:1 Step-Down Charge Pump Power Switch Topology

APPLICATIONS INFORMATION

Under typical conditions (V_{IN} > 10.1V), the LTC3256 operates in 2:1 mode and both the 5V output and 3.3V LDO are powered directly from the charge pump output (see Figure 3).

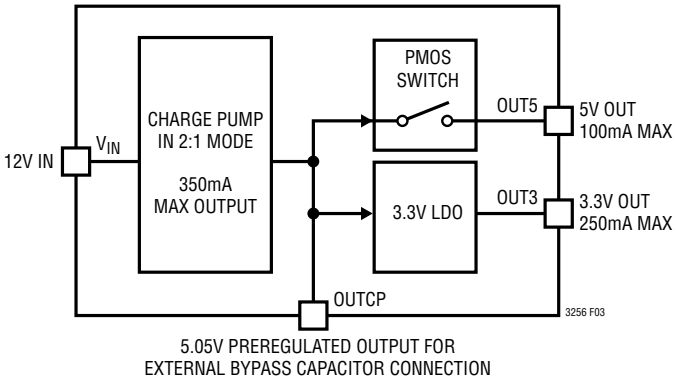


Figure 3. Power Connections for Typical 12V V_{IN} Operation

The overall efficiency and power dissipation under typical 2:1 step-down conditions can be approximated with the equations below.

Total LTC3256 efficiency when V_{IN} > ~10.1V:

$$\eta \cong \frac{5V \bullet I_{OUT5} + 3.3V \bullet I_{OUT3}}{V_{IN} \bullet \left(\frac{I_{OUT5}}{2} + \frac{I_{OUT3}}{2} \right)}$$

Total LTC3256 power dissipation when V_{IN} > ~10.1V:

$$P_D \cong \left(\frac{V_{IN}}{2} - 5V \right) \bullet I_{OUT5} + \left(\frac{V_{IN}}{2} - 3.3V \right) \bullet I_{OUT3}$$

2:1 Step-Down Charge Pump Operation (~7.2V < V_{IN} < ~10.1V)

In this operating region, the charge pump regulates slightly below $V_{IN}/2$ in order to remain in 2:1 mode and maximize overall V_{IN} to 3.3V conversion efficiency. Figure 4 shows typical charge pump step-down mode and output voltage as a function of V_{IN}.

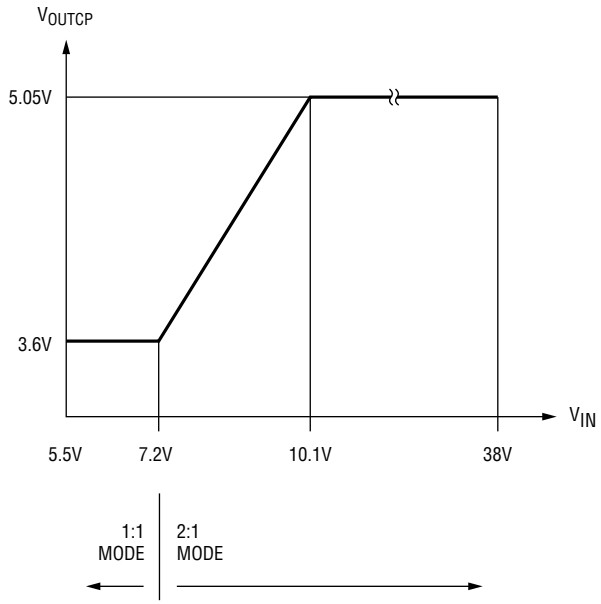


Figure 4. Typical Charge Pump Output Voltage and Mode vs V_{IN}

If OUT5 is enabled and the charge pump output falls below 5V, OUT5 is disconnected from the charge pump output and a separate internal V_{IN}-powered 1:1 step-down mode regulator is used to regulate 5V at the OUT5 pin. Refer to the Simplified Block Diagram. The 3.3V LDO remains powered by the 2:1 charge pump output.

Overall efficiency and power dissipation in this operating region can be approximated by the equations below.

Total LTC3256 efficiency when ~7.2V < V_{IN} < ~10.1V:

$$\eta \cong \frac{5V \bullet I_{OUT5} + 3.3V \bullet I_{OUT3}}{V_{IN} \bullet \left(I_{OUT5} + \frac{I_{OUT3}}{2} \right)}$$

Total LTC3256 power dissipation when ~7.2V < V_{IN} < ~10.1V:

$$P_D \cong (V_{IN} - 5V) \bullet I_{OUT5} + \left(\frac{V_{IN}}{2} - 3.3V \right) \bullet I_{OUT3}$$

APPLICATIONS INFORMATION

1:1 Step-Down Charge Pump Operation (V_{IN} < ~7.2V)

At the low end of the V_{IN} operating range, the minimum charge pump regulation point is typically V_{OUTCP} = 3.6V, with the charge pump automatically switching to 1:1 mode as needed to maintain regulation. Under 1:1 mode conditions, both the 5V and 3.3V outputs are powered directly from V_{IN} with no improvement in efficiency over a dual LDO solution. The overall efficiency and power dissipation in 1:1 step-down mode can be approximated by the equations below.

Total LTC3256 efficiency when V_{IN} < ~7.2V:

$$\eta \cong \frac{5V \bullet I_{OUT5} + 3.3V \bullet I_{OUT3}}{V_{IN} \bullet (I_{OUT5} + I_{OUT3})}$$

Total LTC3256 power dissipation when V_{IN} < ~7.2V:

$$P_D \cong (V_{IN} - 5V) \bullet I_{OUT5} + (V_{IN} - 3.3V) \bullet I_{OUT3}$$

Referring to Figure 2, in 1:1 mode, charge pump switches C and D remain off, and switches A and B are pulsed on and off together to transfer charge directly from V_{IN} to OUTCP.

V_{IN} Bypass Capacitor Selection

The total amount and type of capacitance necessary for input bypassing is very dependent on the impedance of the input power source as well as existing bypassing already on the V_{IN} node. For optimal input noise and ripple reduction, it is recommended that a low ESR ceramic capacitor be used for V_{IN} bypassing. Low ESR will reduce the voltage steps caused by changing input current, while the absolute capacitor value will determine the level of ripple. An electrolytic or tantalum capacitor may be used in parallel with the ceramic capacitor on V_{IN} to increase the total capacitance, but due to the higher ESR, it is not recommended that an electrolytic or tantalum capacitor be used alone for input bypassing. The LTC3256 will operate with capacitors less than 10µF, but depending on the source impedance, input noise can feed through to the output causing degraded performance. For best performance, 10µF or greater total capacitance is suggested for V_{IN} bypassing.

Flying Capacitor Selection

The flying capacitor should always be a ceramic type. Polarized capacitors such as tantalum or aluminum electrolytics are not recommended. The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary for the flying capacitor to have at least 0.4µF of capacitance over operating temperature at 5.05V (see Ceramic Capacitor Selection Guidelines). The voltage rating of the ceramic capacitor should be 6V or greater.

Ceramic Capacitor Selection Guidelines

Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C, whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range (60% to 80% loss typical). Z5U and Y5V capacitors may also have a very strong voltage coefficient, causing them to lose an additional 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 4.7µF, 10V, Y5V ceramic capacitor in an 0805 case may not provide any more capacitance than a 1µF, 10V, X5R or X7R available in the same 0805 case. In fact, over bias and temperature range, the 1µF, 10V, X5R or X7R will provide more capacitance than the 4.7µF, 10V, Y5V. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitance values are met over operating temperature and bias voltage. Table 1 is a list of ceramic capacitor manufacturers in alphabetical order:

APPLICATIONS INFORMATION

Table 1

CERAMIC CAPACITOR MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
TDK	www.tdk.com
Wurth Elektronik	www.we-online.com

3.3V LDO Operation (OUT3)

The 3.3V LDO post-regulates the charge pump output to produce a lower noise output than is typically available from switching regulators, and supports a load of up to 250mA. To ensure stability, the LDO output should be bypassed to ground with at least a 10µF X7R ceramic capacitor.

Drive the EN3 pin high or low to turn the LDO on or off, respectively. When turning on the LDO, the LTC3256 checks whether the charge pump output (OUTCP) is on, enabling the charge pump automatically if needed.

3.3V LDO Fault Protection

The 3.3V LDO output is current limited to 350mA (typical) to protect against overloads and short circuits. In addition, to reduce power dissipation during an output fault condition, foldback circuitry reduces the LDO current limit to 116mA (typical) for V_{OUT3} < 0.9V (typical).

To avoid startup issues due to the foldback feature, it is recommended that heavy loads on OUT3 be held off during LDO startup until the PG3 pin goes Hi-Z to indicate that the LDO has completed power up.

5V Output Operation (OUT5)

Bringing EN5 high enables the 5V output at the OUT5 pin. When the 5V output is enabled, the LTC3256 checks whether the charge pump output (OUTCP) is on, enabling the charge pump automatically if needed.

As shown in the Block Diagram, two on-board regulators can drive the 5V output: the 2:1 charge pump and the V_{IN}-powered gated-switch regulator. Regulator selection is automatic. The LTC3256 prefers the 2:1 charge pump whenever possible due to its increased efficiency, but transitions automatically to the V_{IN}-powered gated-switch regulator as needed to maintain regulation depending on line and load conditions.

To reduce 5V output noise and ripple, it is suggested that a low ESR (equivalent series resistance < 0.1Ω) ceramic capacitor (10µF or greater) be used for OUT5 bypass. Tantalum or aluminum electrolytic capacitors can be used in parallel with a ceramic capacitor to increase the total capacitance but should not be used alone because of their high ESR.

5V Output from 2:1 Charge Pump via Fault-Protected PMOS Switch

If at least 5V (typical) is present at OUTCP when EN5 is brought high, the LTC3256 connects OUT5 to OUTCP via an internal PMOS power switch. Soft-start circuitry controls the PMOS turn-on rate to limit in-rush current draw from OUTCP. See Figure 5.

Upon a hard short circuit to ground, OUT5's foldback cir-

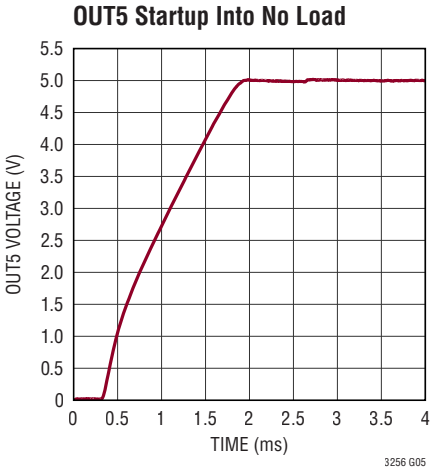


Figure 5. OUT5 Startup

APPLICATIONS INFORMATION

cuitry limits current to 85mA (typical). This limit remains in effect for $V_{OUT5} < 0.8V$ (typical). To avoid startup issues due to this foldback feature, heavy loads on OUT5 should be held off during OUT5 startup until PG5 goes Hi-Z.

The LTC3256 has current limit circuitry to protect against overcurrent faults beyond hard shorts to ground.

Reset Generation (RSTI input, $\overline{RST}$ output)

The LTC3256 pulls the $\overline{RST}$ open-drain output low whenever RSTI is below threshold (typically 1.2V) or OUTCP is not in regulation. $\overline{RST}$ remains asserted low for a reset timeout period (t_{RST}) once RSTI goes above the threshold and OUTCP is in regulation. Requiring that OUTCP is in regulation ensures that at least one of the outputs (OUT5 or OUT3) is enabled before the reset timeout period starts. $\overline{RST}$ deasserts by going high impedance at the end of the reset timeout period.

The reset timeout can be configured to use an internal timer without external components, or an adjustable timer programmed by connecting an external capacitor from the RT pin to GND. Glitch filtering ensures reliable reset operation without false triggering.

During initial power up, the RST output asserts low while V_{IN} is below the V_{IN} undervoltage lockout threshold. The state of OUTCP and RSTI have no effect on RST while V_{IN} is below the undervoltage lockout threshold. The reset timeout period cannot start until V_{IN} exceeds the undervoltage lockout threshold.

Selecting the Reset Timing Capacitor

The reset timeout period can be set to a fixed internal timer or programmed with a capacitor in order to accommodate a variety of applications. Connecting a capacitor, C_{RT}, between the RT pin and GND sets the reset timeout period, t_{RST}. The following formula approximates the value of capacitor needed for a particular timeout:

$$C_{RT} = (t_{RST} - 0.75ms) \bullet \frac{67pF}{ms}$$

For example, using a standard capacitor value of 2.2nF would give a 32ms reset timeout period.

Figure 6 shows the desired reset timeout period as a function of the value of the timer capacitor. Leaving RT open with no external capacitor generates a reset timeout of approximately 0.75ms. Shorting RT to OUTCP generates a reset timeout of approximately 0.2s.

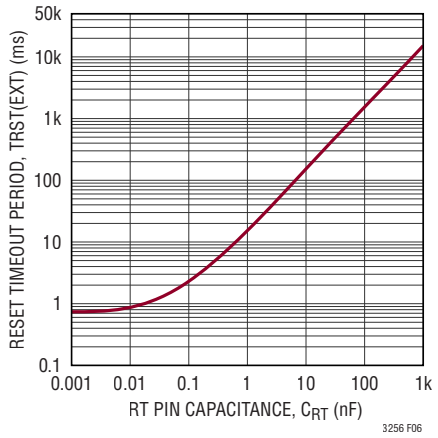


Figure 6. Reset Timeout Period vs RT Pin Capacitance

$\overline{RST}$ Output Characteristics

$\overline{RST}$ is an open-drain pin and thus requires an external pull-up resistor to the logic supply. $\overline{RST}$ is typically pulled up to OUT5, OUT3, or OUTCP, but can be pulled up to any other supply voltage providing the voltage limits of the pin are observed.

Watchdog Timer (WDI input, $\overline{RST}$ output)

The LTC3256 includes a windowed watchdog function that can continuously monitor the application's logic or microprocessor and issue automatic resets to aid recovery from unintended lockups or crashes. With the RSTI input held above threshold, the application must periodically toggle the logic state of the watchdog input (WDI pin) in order to clear the watchdog timer. Specifically, successive

APPLICATIONS INFORMATION

falling edges on the WDI pin must be spaced by more than the watchdog lower boundary but less than the watchdog upper boundary. As long as this condition holds, $\overline{RST}$ remains high impedance.

If a falling edge arrives before the watchdog lower boundary, or if the watchdog timer reaches the upper boundary without seeing a falling edge on WDI, the watchdog timer enters its reset state and asserts $\overline{RST}$ low for the reset timeout period. Once the reset timeout completes, $\overline{RST}$ is released to go high and the watchdog timer starts again.

During power-up, the watchdog timer remains cleared while $\overline{RST}$ is asserted low. As soon as the reset timer times out, $\overline{RST}$ goes high and the watchdog timer is started.

Setting the Watchdog Reset Time

The watchdog upper boundary (t_{WDU}) and lower boundary (t_{WDL}) are not observable outside the part, only the watchdog reset time (t_{WDR}) of the part is observable via the $\overline{RST}$ pin. The watchdog upper boundary (t_{WDU}) occurs one watchdog clock cycle before the watchdog reset time (t_{WDR}). The internal watchdog reset time consists of 8193 clock cycles, so the internal watchdog upper boundary time is essentially the same as the internal watchdog reset time. Conversely the external watchdog reset time consists of only 129 clock cycles, so the external watchdog upper boundary should be more accurately calculated as:

$$t_{WDU(EXT)} = t_{WDR(EXT)} \bullet \left(\frac{128}{129}\right)$$

The external watchdog lower boundary ($t_{WDL(EXT)}$) occurs five clock cycles into the watchdog reset time ($t_{WDR(EXT)}$). Thus the external watchdog lower boundary can be calculated from the external watchdog reset time as:

$$t_{WDU(EXT)} = t_{WDR(EXT)} \bullet \left(\frac{5}{129}\right)$$

The internal watchdog lower boundary can be calculated from the internal watchdog reset time by the following:

$$t_{WDL(INT)} = \frac{t_{WDR(INT)}}{32}$$

The watchdog reset time is adjustable and can be optimized for software execution. The watchdog reset time is adjusted by connecting a capacitor, C_{WT}, between the WT and GND pins. Given a desired watchdog reset time t_{WDR}, the capacitor value is approximately:

$$C_{WT} = \left(t_{WDR} - 3.8ms\right) \bullet \frac{8.8nF}{s}$$

For example, using a standard capacitor value of 0.047µF would give a 5.3s watchdog reset time. Shorting WT to BIAS generates a timeout of approximately 1.6s. Connecting WT to GND disables the watchdog function.

Power Good Output Operation (PG3, PG5 Outputs)

A built-in dual supply monitor indicates which of the OUT3 and OUT5 voltages are in regulation. The monitor detects both overvoltage and undervoltage faults, reporting Power Good status via the PG3 and PG5 open-drain outputs. These will be referred to as the PGx pins in the description below.

If the LTC3256 is shut down (EN3 and EN5 both low) or in undervoltage lockout, both PGx pins are pulled low. Otherwise, behavior is as follows:

If the OUTx pin voltage is greater than the overvoltage threshold or less than the undervoltage threshold, the corresponding PGx pin will pull low. PGx becomes high impedance when the OUTx pin voltage is between the overvoltage and undervoltage thresholds. Hysteresis is built into the overvoltage and undervoltage comparators to ensure PGx holds it's state when in regulation.

APPLICATIONS INFORMATION

A pull-up resistor can be inserted between PGx and a valid logic supply (i.e. OUTCP, OUT5 or OUT3) to signal a power good condition. The use of a large value pull-up resistor on PGx and a capacitor placed between PGx and GND can be used to delay the Power Good signal if desired.

1.1V Reference Output (REFOUT Output)

An internal bandgap voltage reference determines the regulation voltages at OUT3 and OUT5. A buffered version of this voltage reference appears at the REFOUT pin when the LTC3256 is enabled. The output has a typical impedance of 2k and can source but not sink current. To maximize supply rejection, REFOUT should be bypassed with a 0.1µF ceramic capacitor.

Thermal Management/Thermal Shutdown

The on chip power dissipation in the LTC3256 will cause the junction to ambient temperature to rise at rate of 40°C/W or more. To reduce the maximum junction temperature, a good thermal connection to the PC board is recommended.

Connecting the die paddle (Pin 17) with multiple vias to a large ground plane under the device can reduce the thermal resistance of the package and PC board considerably. Poor board layout and failure to connect the die paddle (Pin 17) to a large ground plane can result in thermal junction to ambient impedance well in excess of 40°C/W. See Linear Technology's Application Notes for thermally Enhanced Leaded packages.

Because of the wide input operating range it is possible to exceed the specified operating junction temperature and even reach thermal shutdown (175°C typ).

The LTC3256 can operate up to 95°C at full load (I_{OUT3} = 250mA, I_{OUT5} = 100mA) with V_{IN} < 15V. Above 95°C, or with input voltages greater than 15V, it is the responsibility of the user to calculate worst-case power dissipation to make sure the LTC3256's specified operating junction temperature is not exceeded for extended periods of time.

Refer to the power dissipation equations provided earlier for calculating power dissipation (P_D) in the different modes of operation.

For example, if it is determined that the maximum power dissipation (P_D) is 1.2W under normal operation, then the junction to ambient temperature rise will be:

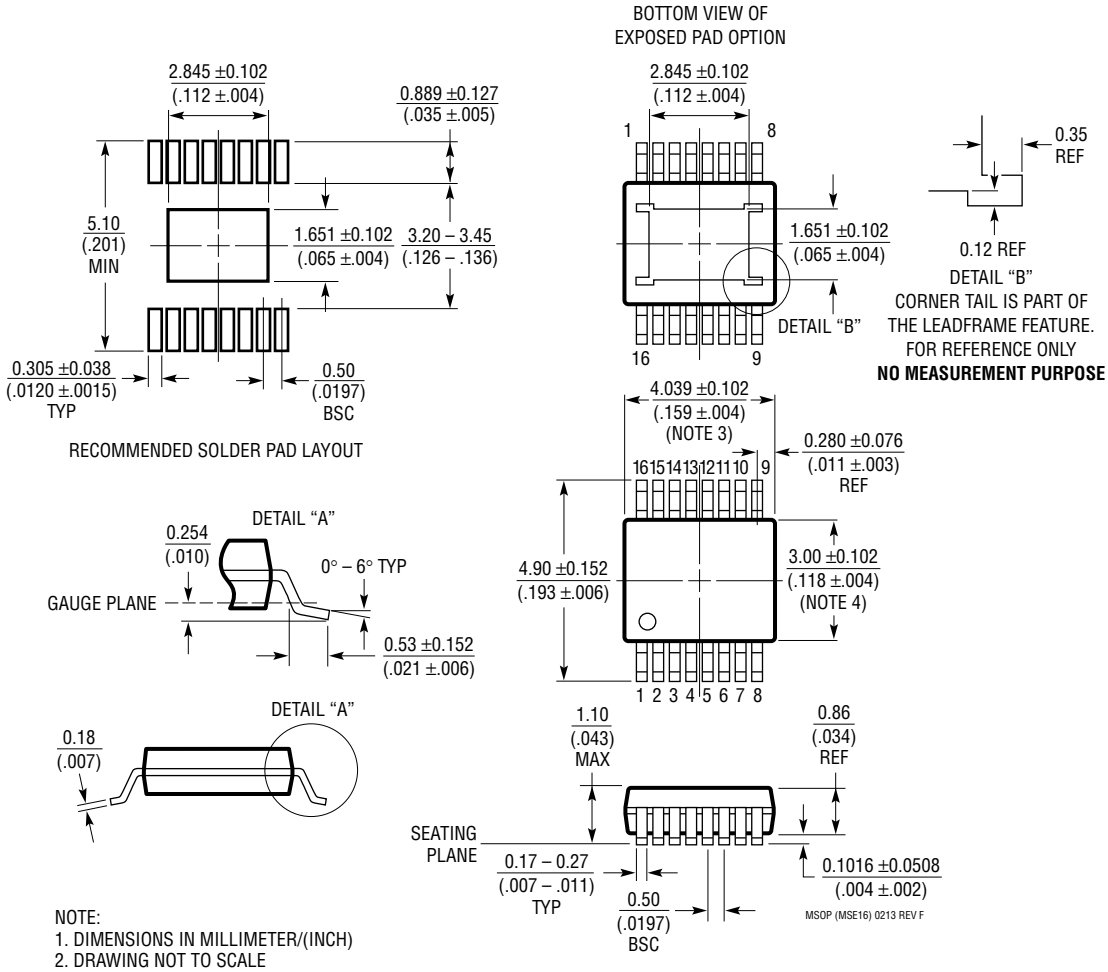
Junction to Ambient = 1.2W • 40°C/W = 48°C

Thus, the ambient temperature under this condition cannot exceed 102°C if the junction temperature is to remain below 150°C and if the ambient temperature exceeds about 127°C the device will cycle in and out of the thermal shutdown.

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3256#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	08/16	Updated feature list	1
B	12/16	Changed Reset Timer Control (RT) conditions	3
		Changed Watchdog Timer Control (WDT) conditions	4
		Changed title of graph G12	6
		Modified 5V Output from 2:1 Charge Pump section	14