Low Noise Dual Supply with Boost and Inverting Charge Pumps

FEATURES

- **Boost Charge Pump Generates 2 • V_{IN_P} (V_{IN_P} Range: 4.5V to 16V)**
- **Inverting Charge Pump Generates –V_{IN_N} (V_{IN_N} Range: 4.5V to 32V)**
- **Low Noise Positive LDO Post Regulator Up to 50mA**
- **Low Noise Negative LDO Post Regulator Up to 50mA**
- **135µA Quiescent Current in Burst Mode® Operation with Both LDO Regulators On**
- **50kHz to 500kHz Programmable Oscillator Frequency**
- Stable with Ceramic Capacitors
- Short-Circuit/Thermal Protection
- Low Profile 3mm × 5mm 18-Lead DFN and Thermally Enhanced 20-Lead TSSOP Packages

APPLICATIONS

- Low Noise Bipolar/Inverting Supplies
- Industrial/Instrumentation Low Noise Bias Generators

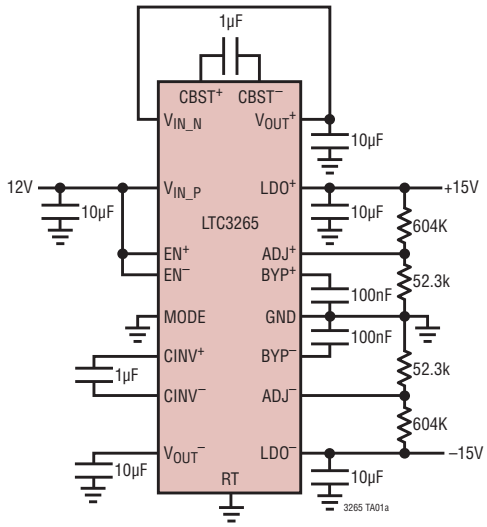
DESCRIPTION

The LTC®3265 is a low noise dual polarity output power supply including a boost charge pump, an inverting charge pump and two low noise positive and negative LDO post regulators. The boost charge pump powers the positive LDO post regulator while the inverting charge pump powers the negative LDO regulator. Each LDO can provide up to 50mA of output current. The LDO output voltages can be adjusted using external resistor dividers.

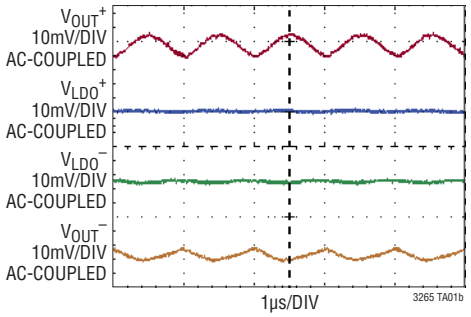
The charge pumps employ low quiescent current Burst Mode operation or low noise constant frequency mode. During Burst Mode operation, the boost charge pump regulates its output (V_{OUT}^+) to 0.94 • 2 • V_{IN_P} while the inverting charge pump regulates its output (V_{OUT}^-) to –0.94 • V_{IN_N}. In Burst Mode operation the LTC3265 draws only 135µA of quiescent current with both LDOs on. In constant frequency mode, the boost and inverting charge pumps produce outputs equal to 2 • V_{IN_P} and –V_{IN_N} respectively and operate at a fixed 500kHz or to a programmed value between 50kHz to 500kHz using an external resistor. The LTC3265 is available in low profile 3mm × 5mm × 0.75mm 18-lead DFN and thermally enhanced 20-lead TSSOP packages.

TYPICAL APPLICATION

Low Noise ±15V Outputs from a Single 12V Input



LDO Rejection of $V_{OUT}^±$ Ripple

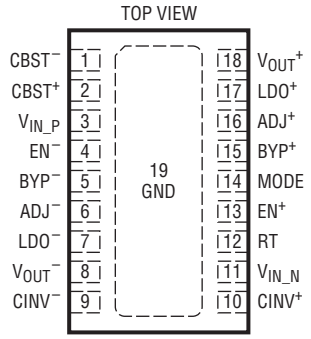


V_{IN_P} = 12V, V_{IN_N} = V_{OUT}^+
V_{LDO}^+ = 15V
V_{LDO}^- = –15V
f_{OSC} = 500kHz
I_{LDO}^+ = 20mA
I_{LDO}^- = –20mA

ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

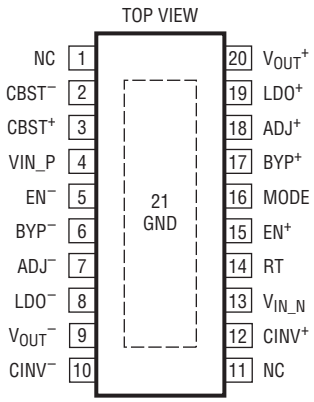
V_{IN_P}, EN^+, EN^-, MODE ..... –0.3V to 18V
V_{OUT}^+, V_{IN_N} ..... –0.3V to 36V
LDO^+ ..... –16V to 36V
V_{OUT}^-, LDO^- ..... –36V to 0.3V
RT, ADJ^+ ..... –0.3V to 6V
BYP^+ ..... –0.3V to 2.5V
ADJ^- ..... –6V to 0.3V
BYP^- ..... –2.5V to 0.3V
$LDO^\pm$ Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range
(Note 2) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Only ..... 300°C

PIN CONFIGURATION



DHC PACKAGE
18-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 42°C/W
EXPOSED PAD (PIN 19) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC3265#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3265EDHC#PBF	LTC3265EDHC#TRPBF	3265	18-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3265IDHC#PBF	LTC3265IDHC#TRPBF	3265	18-Lead (5mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3265HDHC#PBF	LTC3265HDHC#TRPBF	3265	18-Lead (5mm × 3mm) Plastic DFN	–40°C to 150°C
LTC3265MPDHC#PBF	LTC3265MPDHC#TRPBF	3265	18-Lead (5mm × 3mm) Plastic DFN	–55°C to 150°C
LTC3265EFE#PBF	LTC3265EFE#TRPBF	LTC3265	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3265IFE#PBF	LTC3265IFE#TRPBF	LTC3265	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3265HFE#PBF	LTC3265HFE#TRPBF	LTC3265	20-Lead Plastic TSSOP	–40°C to 150°C
LTC3265MPFE#PBF	LTC3265MPFE#TRPBF	LTC3265	20-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN_P} = V_{IN_N} = EN^+ = EN^- = 10V, MODE = 0V, R_T = 200kΩ

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Boost Charge Pump							
V_{IN_P}	V_{IN_P} Input Voltage Range		●	4.5		16	V
V_{UVLO}	V_{IN_P} Undervoltage Lockout Threshold	V_{IN_P} Rising V_{IN_P} Falling	● ●	 3.4	3.8 3.6	4	V V
I_{VIN_P}	V_{IN_P} Quiescent Current	Shutdown, EN^+ = EN^- = 0V MODE = V_{IN_P}, EN^- = 0V, I_{VOUT}^+ = I_{LDO}^+ = 0mA MODE = V_{IN_P}, I_{VOUT} = I_{LDO}^+ = I_{LDO-} = 0mA MODE = 0V, I_{VOUT}^+ = 0mA			3 85 110 3	6 170 220 6	µA µA µA mA
V_{RT}	RT Regulation Voltage				1.200		V
V_{OUT}^+	V_{OUT}^+ Regulation Voltage	MODE = 10V MODE = 0V			2 • 0.94 • V_{IN_P} 2 • V_{IN_P}		V V
f_{OSC}	Oscillator Frequency	RT = GND		450	500	550	kHz
R_{OUTBST}	Boost Charge Pump Output Impedance	MODE = 0V, RT = GND			32		Ω
$I_{VOUT+(SC)}$	Max I_{VOUT}^+ Short-Circuit Current	V_{OUT}^+ = GND	●	100	220	300	mA
$V_{MODE(H)}$	MODE Threshold Rising		●		1.1	2	V
$V_{MODE(L)}$	MODE Threshold Falling		●	0.4	1.0		V
I_{MODE}	MODE Pin Internal Pull-Down Current	V_{IN_P} = MODE = 16V			0.7		µA
Inverting Charge Pump							
V_{IN_N}	V_{IN_N} Input Voltage Range		●	4.5		32	V
I_{VIN_N}	V_{IN_N} Quiescent Current	Shutdown, EN^- = 0V MODE = V_{IN_P}, I_{VOUT}^- = I_{LDO}^- = 0mA MODE = 0V, I_{VOUT}^- = 0mA			1 25 3	3 50 5	µA µA mA
V_{OUT}^-	V_{OUT}^- Regulation Voltage	MODE = 10V MODE = 0V			–0.94 • V_{IN_N} –V_{IN_N}		V V
R_{OUTINV}	Inverting Charge Pump Output Impedance	MODE = 0V, RT = GND			32		Ω
$I_{VOUT-(SC)}$	Max I_{VOUT}^- Short-Circuit Current	V_{OUT}^- = GND, $\|I_{VOUT-}\|$	●	100	160	250	mA
Positive Regulator							
	LDO^+ Output Voltage Range		●	1.2		32	V
V_{ADJ}^+	ADJ^+ Reference Voltage	I_{LDO}^+ = 1mA	●	1.176	1.200	1.224	V
I_{ADJ}^+	ADJ^+ Input Current	V_{ADJ}^+ = 1.2V		–50		50	nA
$I_{LDO}^+(SC)$	LDO^+ Short-Circuit Current		●	50	100		mA
	Line Regulation				0.04		mV/V
	Load Regulation				0.03		mV/mA
$V_{DROPOUT}^+$	LDO+ Dropout Voltage	I_{LDO}^+ = 50mA			400	800	mV
	Output Voltage Noise	C_{BYP}^+ = 100nF			100		μV_{RMS}
$V_{EN}^+(H)$	EN^+ Threshold Rising		●		1.1	2	V
$V_{EN}^+(L)$	EN^+ Threshold Falling		●	0.4	1.0		V
I_{EN}^+	EN^+ Pin Internal Pull-Down Current	V_{IN_P} = EN^+ = 16V			0.7		µA
Negative Regulator							
	LDO^- Output Voltage Range		●	–32		–1.2	V
V_{ADJ}^-	ADJ^- Reference Voltage	I_{LDO-} = –1mA	●	–1.224	–1.200	–1.176	V
I_{ADJ}^-	ADJ^- Input Current	V_{ADJ}^- = –1.2V		–50		50	nA
$I_{LDO}^-(SC)$	LDO^- Short-Circuit Current	$\|I_{LDO-}\|$	●	50	100		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN_P} = V_{IN_N} = EN^+ = EN^- = 10V, MODE = 0V, R_T = 200kΩ

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Line Regulation				0.002		mV/V
	Load Regulation				0.02		mV/mA
$V_{DROPOUT^-}$	LDO^- Dropout Voltage	I_{LDO^-} = –50mA			200	500	mV
	Output Voltage Noise	C_{BYP^-} = 100nF			100		μV_{RMS}
$V_{EN^-(H)}$	EN^- Threshold Rising		●		1.1	2	V
$V_{EN^-(L)}$	EN^- Threshold Falling		●	0.4	1.0		V
I_{EN^-}	EN^- Pin Internal Pull-Down Current	V_{IN_P} = V_{IN_N} = EN^- = 16V			0.7		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3265 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3265E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3265I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3265H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3265MP is guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

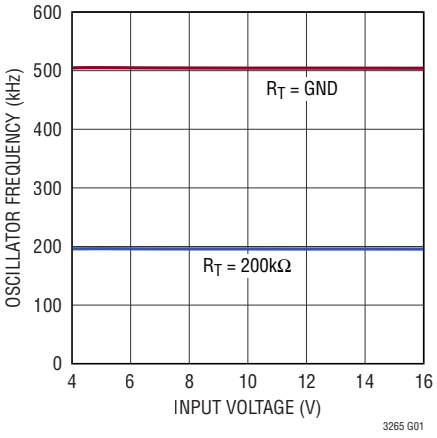
where θ_{JA} is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

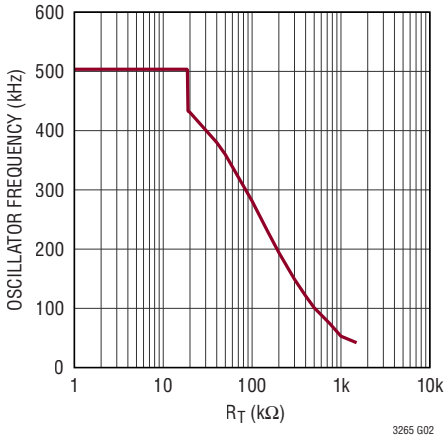
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, C_{BST} = C_{INV} = 1µF, C_{IN_P} = C_{IN_N} = C_{OUT^+} = C_{OUT^-} = C_{LDO^+} = C_{LDO^-} = 10µF, unless otherwise noted.

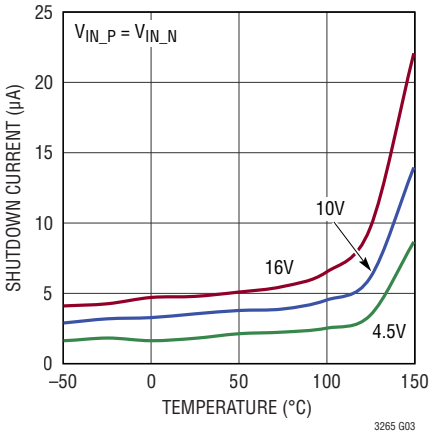
Oscillator Frequency vs Supply Voltage



Oscillator Frequency vs R_T



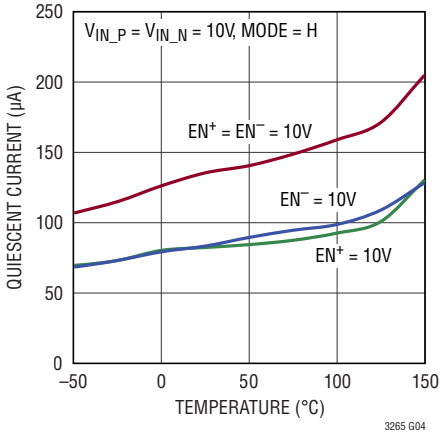
Shutdown Current vs Temperature



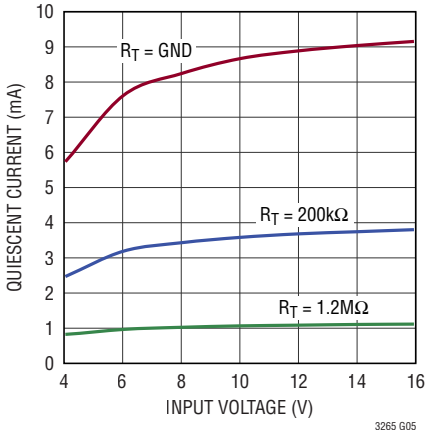
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, C_{BST} = C_{INV} = 1µF, C_{IN_P} = C_{IN_N} = C_{OUT}^+ = C_{OUT}^- = C_{LDO}^+ = C_{LDO}^- = 10µF, unless otherwise noted.

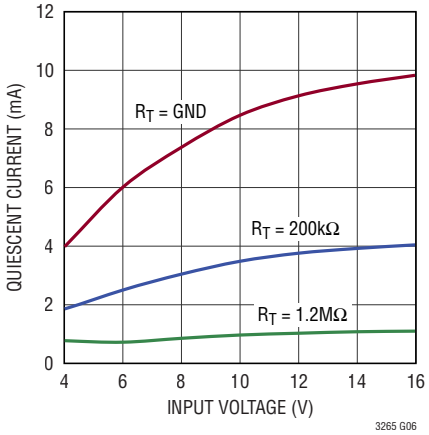
Quiescent Current vs Temperature (Burst Mode Operation)



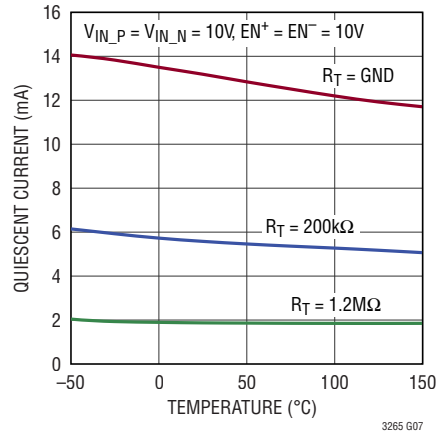
Boost Charge Pump Quiescent Current vs Supply Voltage (Constant Frequency Mode)



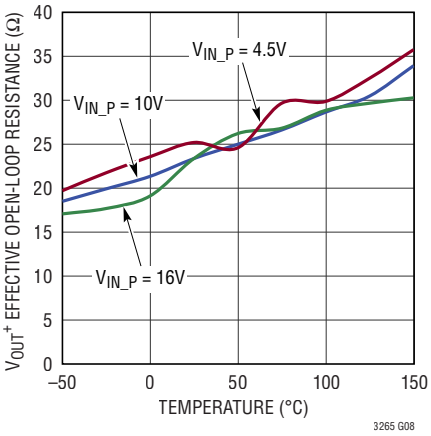
Inverting Charge Pump Quiescent Current vs Supply Voltage (Constant Frequency Mode)



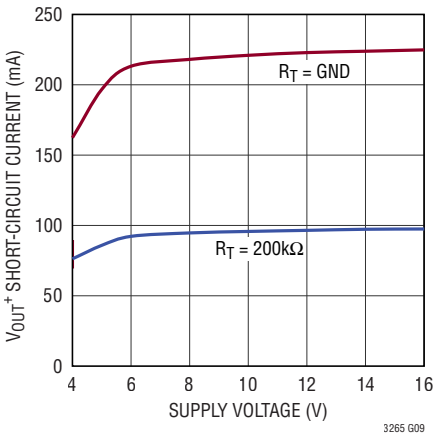
Quiescent Current vs Temperature (Constant Frequency Mode)



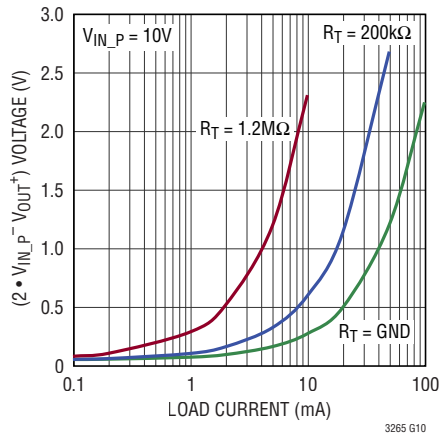
V_{OUT}^+ Effective Open-Loop Resistance vs Temperature



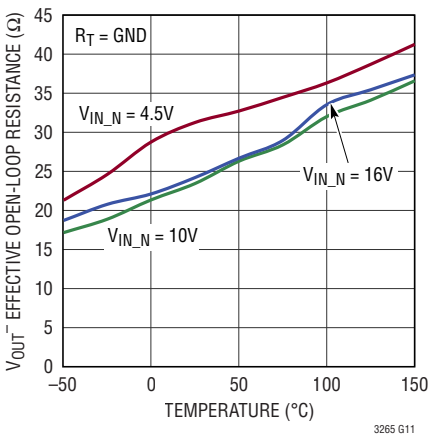
V_{OUT}^+ Short-Circuit Current vs Supply Voltage



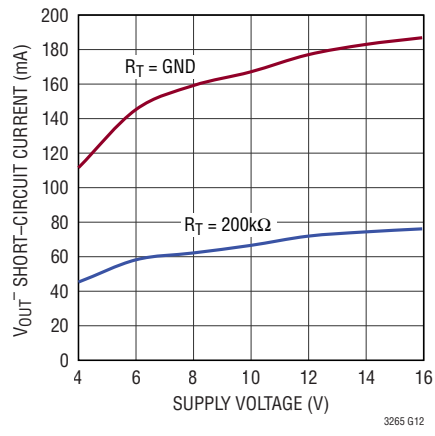
V_{OUT}^+ Voltage Loss vs Output Current (Constant Frequency Mode)



V_{OUT}^- Effective Open-Loop Resistance vs Temperature



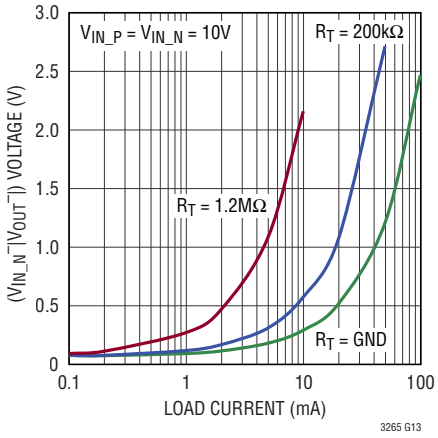
V_{OUT}^- Short-Circuit Current vs Supply Voltage



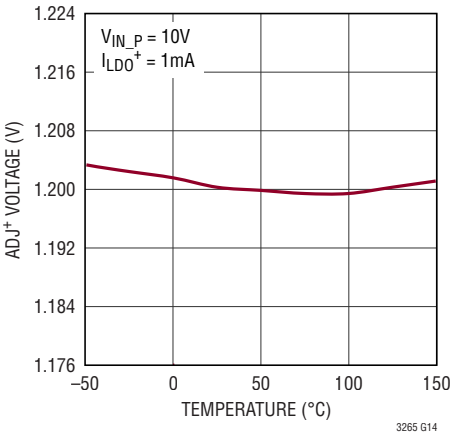
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, C_{BST} = C_{INV} = 1µF, C_{IN_P} = C_{IN_N} = C_{OUT}^+ = C_{OUT}^- = C_{LDO}^+ = C_{LDO}^- = 10µF, unless otherwise noted.

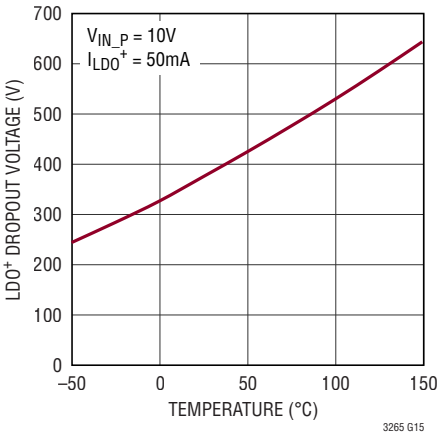
V_{OUT}^- Voltage Loss vs Output Current (Constant Frequency Mode)



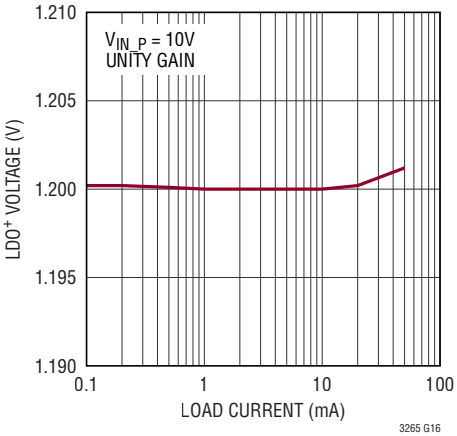
ADJ⁺ Pin Voltage vs Temperature



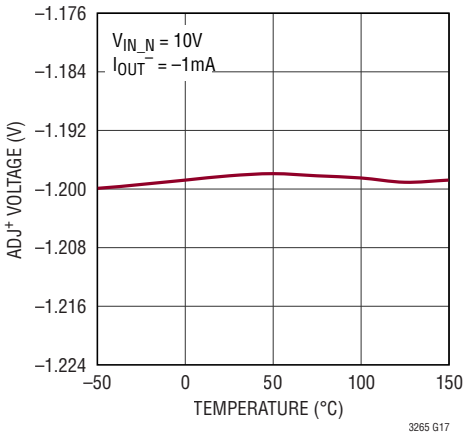
LDO^+ Dropout Voltage vs Temperature



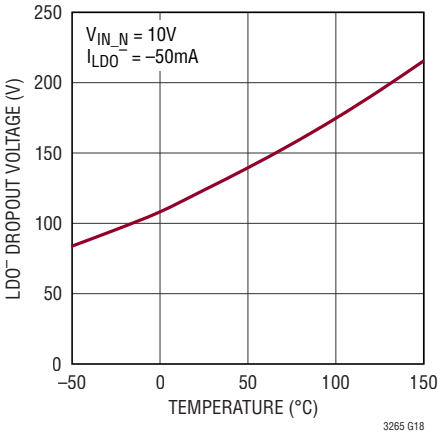
LDO^+ Load Regulation



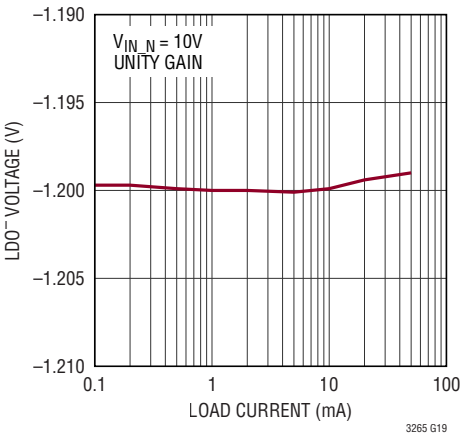
ADJ^- Pin Voltage vs Temperature



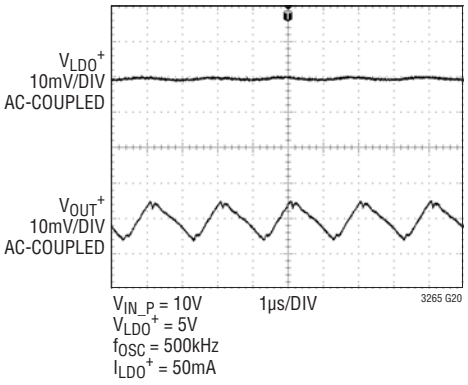
LDO^- Dropout Voltage vs Temperature



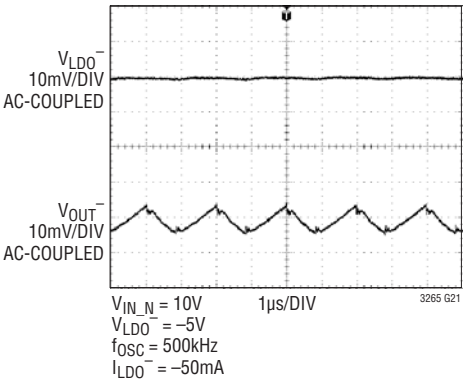
LDO^- Load Regulation



LDO^+ Rejection of V_{OUT}^+ Ripple



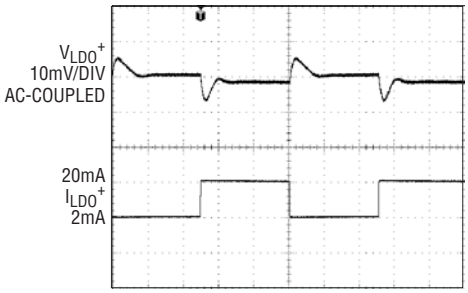
LDO^- Rejection of V_{OUT}^- Ripple



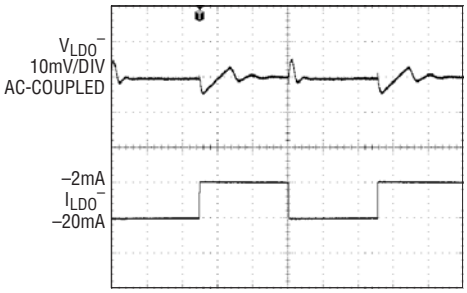
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, C_{BST} = C_{INV} = 1µF, C_{IN_P} = C_{IN_N} = C_{OUT}^+ = C_{OUT}^- = C_{LDO}^+ = C_{LDO}^- = 10µF, unless otherwise noted.

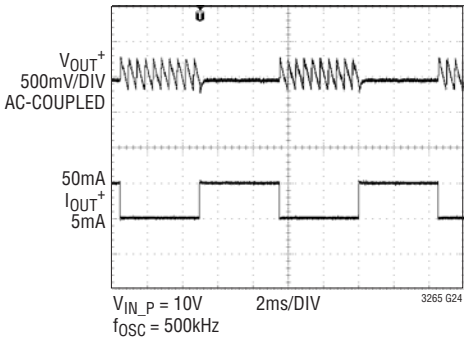
LDO+ Load Transient



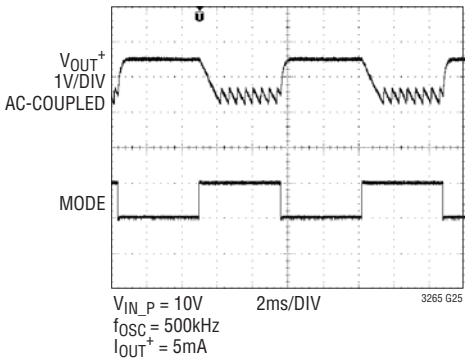
LDO– Load Transient



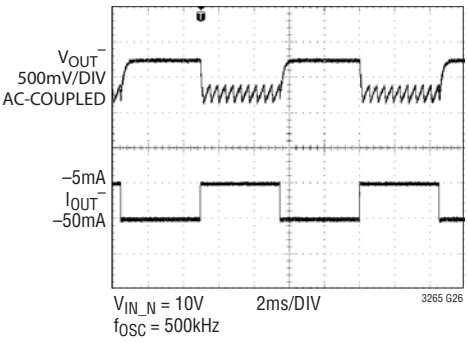
VOUT+ Transient (Burst Mode Operation, MODE = H)



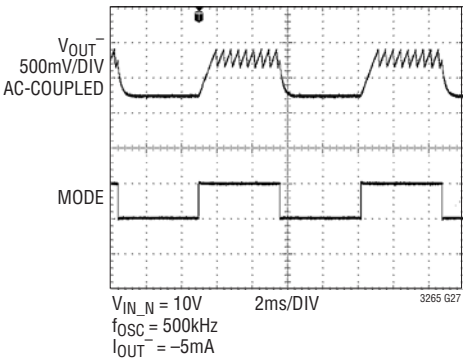
VOUT+ Transient (MODE = Low to High)



VOUT– Transient (Burst Mode Operation, MODE = H)



VOUT– Transient (MODE = Low to High)



PIN FUNCTIONS (DFN/TSSOP)

$CBST^-$ (Pin 1/Pin 2): Boost Charge Pump Flying Capacitor Negative Connection.

NC (Pins 1, 11 TSSOP Only): No Connect. These pins are not connected to LTC3265 die. These pins should be left floating or connected to ground.

$CBST^+$ (Pin 2/Pin 3): Boost Charge Pump Flying Capacitor Positive Connection.

V_{IN_P} (Pin 3/Pin 4): Input Voltage for Boost Charge Pump. V_{IN_P} should be bypassed with a low impedance ceramic capacitor.

EN^- (Pin 4/Pin 5): Logic Input. A logic "high" on the EN^- pin enables the inverting charge pump as well as the negative LDO regulator. Do not float this pin.

BYP^- (Pin 5/Pin 6): LDO^- Reference Bypass Pin. Connect a capacitor from BYP^- to GND to reduce LDO^- output noise. Leave floating if unused.

ADJ^- (Pin 6/Pin 7): Feedback Input for the Negative Low Dropout Regulator. This pin servos to a fixed voltage of –1.2V when the control loop is complete.

LDO^- (Pin 7/Pin 8): Negative Low Dropout (LDO^-) Linear Regulator Output. This pin requires a low ESR (equivalent series resistance) capacitor with at least 2µF capacitance to ground for stability.

V_{OUT}^- (Pin 8/Pin 9): Inverting Charge Pump Output Voltage. In constant frequency mode (MODE = low) this pin is driven to $–V_{IN\_N}$. In Burst Mode operation, (MODE = high) this pin voltage is regulated to $– 0.9 • V_{IN\_N}$ using an internal burst comparator with hysteretic control.

$CINV^-$ (Pin 9/Pin 10): Inverting Charge Pump Flying Capacitor Positive Connection.

$CINV^+$ (Pin 10/Pin 12): Inverting Charge Pump Flying Capacitor Negative Connection.

V_{IN_N} (Pin 11/Pin 13): Input Voltage for Inverting Charge Pump. This pin should be tied to V_{IN_P} or V_{OUT}^+ pins depending on the desired output voltage at the V_{OUT}^- pin. If V_{IN_N} is tied to V_{OUT}^+, the output at V_{OUT}^- will be $–V_{OUT}^+$ or $–2 • V_{IN\_P}$. This configuration is suitable for symmetric outputs at LDO^+ and LDO^- pins. If V_{IN_N} is tied to V_{IN_P}, the output at V_{OUT}^- will be $–V_{IN\_P}$. This configuration is suitable for asymmetric outputs at LDO^+ and LDO^- pins. See Applications Information for additional details. V_{IN_N} should be bypassed with a low impedance ceramic capacitor.

RT (Pin 12/Pin 14): Input Connection for Programming the Switching Frequency. The RT pin servos to a fixed 1.2V when the EN^+ or EN^- pin is driven to a logic "high". A resistor from RT to GND sets the charge pump switching frequency. If the RT pin is tied to GND, the switching frequency defaults to a fixed 500kHz.

EN^+ (Pin 13/Pin 15): Logic Input. A logic "high" on the EN^+ pin enables the boost charge pump as well as the positive LDO regulator. Do not float this pin.

MODE (Pin 14/Pin 16): Logic Input. The MODE pin determines the charge pump operating mode. A logic "high" on the MODE pin forces the charge pumps to operate in Burst Mode operation. The boost charge pump regulates the V_{OUT}^+ pin to $0.94 • 2 • V_{IN\_P}$ with hysteretic control. The inverting charge pump regulates the V_{OUT}^- pin to $(–0.94 • V_{IN\_N})$. A logic "low" on the MODE pin forces the charge pumps to operate in open-loop mode with a constant switching frequency. The boost charge pump doubles the input to $2 • V_{IN\_P}$ in this mode while the inverting charge pump inverts its input to $(–V_{IN\_N})$. The switching frequency in both modes is determined by an external resistor from the RT pin to GND. In Burst Mode operation, this represents the frequency of the burst cycles before the part enters the low quiescent current sleep state. Do not float this pin.

PIN FUNCTIONS (DFN/TSSOP)

BYP+ (Pin 15/Pin 17): LDO+ Reference Bypass Pin. Connect a capacitor from BYP+ to GND to reduce LDO+ output noise. Leave floating if unused.

ADJ+ (Pin 16/Pin 18): Feedback Input for the Positive Low Dropout (LDO+) Regulator. This pin servos to a fixed voltage of 1.2V when the control loop is complete.

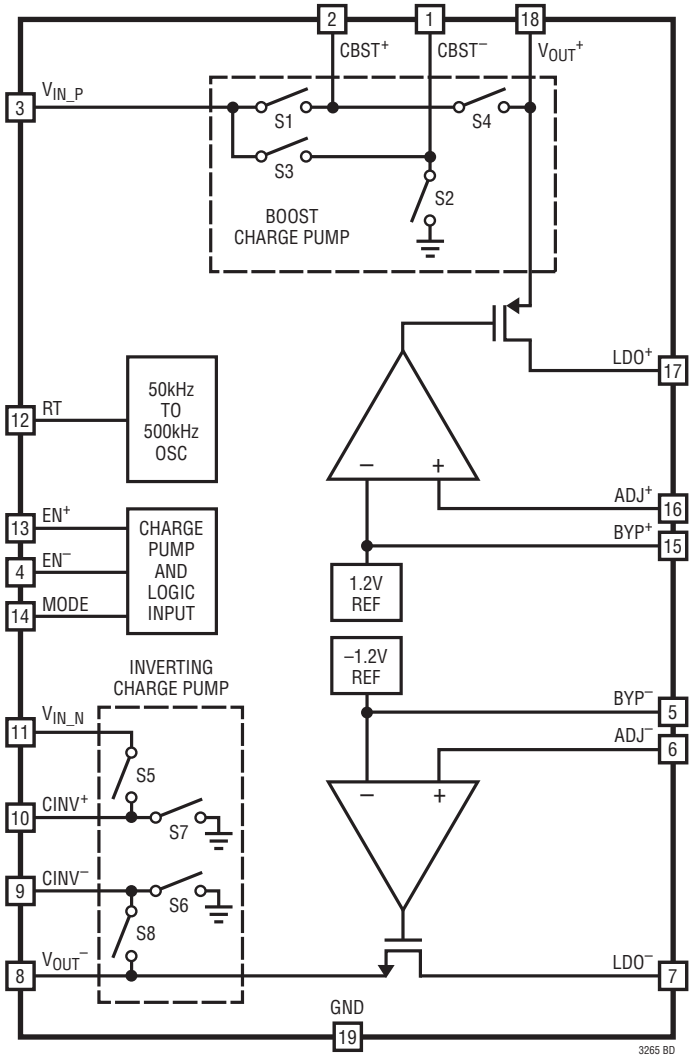
LDO+ (Pin 17/Pin 19): Positive Low Dropout (LDO+) Output. This pin requires a low ESR capacitor with at least 2µF capacitance to ground for stability.

V_{OUT}+ (Pin 18/Pin 20): Boost Charge Pump Output Voltage. In constant frequency mode (MODE = low) this pin is driven to $2 \bullet V_{IN\_P}$. In Burst Mode operation, (MODE = high) this pin voltage is regulated to $0.94 \bullet 2 \bullet V_{IN\_P}$ using an internal burst comparator with hysteretic control.

GND (Exposed Pad Pin 19/Exposed Pad Pin 21): Ground. The exposed package pad is ground and must be soldered to the PC board ground plane for proper functionality and for rated thermal performance.

BLOCK DIAGRAM

Note: Pin numbers are as per DFN package. Refer to the Pin Functions section for corresponding TSSOP pin numbers.



OPERATION (Refer to the Block Diagram)

The LTC3265 is a high voltage low noise dual output regulator. It includes a boost charge pump, an inverting charge pump and two LDO regulators to generate bipolar low noise supply rails from a single positive input. It supports a wide input power supply range from 4.5V to 16V for the boost charge pump and a 4.5V to 32V range for the inverting charge pump.

Shutdown Mode

In shutdown mode, all circuitry except the internal bias is turned off. The LTC3265 is in shutdown when a logic low is applied to both the enable inputs (EN^+ and EN^-). The LTC3265 only draws 3µA (typ) from the V_{IN_P} supply in shutdown. If the V_{IN_N} pin is tied to V_{IN_P} it draws an additional 1µA (typ) in shutdown. If the V_{IN_N} pin is tied to V_{OUT}^+ then it does not carry any additional current in shutdown.

Boost Charge Pump Constant Frequency Operation

The LTC3265 boost charge pump provides low noise constant frequency operation when a logic low is applied to the MODE pin. The boost charge pump and oscillator circuit are enabled using the EN^+ pin. At the beginning of a clock cycle, switches S1 and S2 are closed. The external flying capacitor across $CBST^+$ and $CBST^-$ pins is charged to the V_{IN_P} supply. In the second phase of the clock cycle, switches S1 and S2 are opened, while switches S3 and S4 are closed. In this configuration the $CBST^-$ side of the flying capacitor is connected to V_{IN_P} and charge is delivered through the $CBST^+$ pin to V_{OUT}^+. In steady state the V_{OUT}^+ pin regulates at $2 \bullet V_{IN\_P}$ less any voltage drop due to the load current on V_{OUT}^+.

Boost Charge Pump Burst Mode Operation

The LTC3265 boost charge pump provides low power Burst Mode operation when a logic high is applied to the MODE pin. In Burst Mode operation, the boost charge pump charges the V_{OUT}^+ pin to $0.94 \bullet 2 \bullet V_{IN\_P}$ (typ). The part then shuts down the internal oscillator to reduce switching losses and goes into a low current state. This state is referred to as the sleep state in which the part consumes only about 85µA from the V_{IN_P} pin. When the output voltage droops enough to overcome the burst comparator hysteresis, the part wakes up and commences boost charge pump cycles until V_{OUT}^+ output voltage exceeds $-0.94 \bullet 2 \bullet V_{IN\_P}$ (typ). This mode provides lower operating current at the cost of higher output ripple and is ideal for light load operation.

Inverting Charge Pump Constant Frequency Operation

The LTC3265 inverting charge pump provides low noise constant frequency operation when a logic low is applied to the MODE pin. The inverting charge pump and oscillator circuit are enabled using the EN^- pin. At the beginning of a clock cycle, switches S5 and S6 are closed. The external flying capacitor across $CINV^+$ and $CINV^-$ pins is charged to the V_{IN_N} pin voltage. The V_{IN_N} pin must be tied to V_{IN_P} or V_{OUT}^+ pins depending on the desired output voltage at the V_{OUT}^- pin. In the second phase of the clock cycle, switches S5 and S6 are opened, while switches S7 and S8 are closed. In this configuration the $CINV^+$ side of the flying capacitor is grounded and charge is delivered through the $CINV^-$ pin to V_{OUT}^-. In steady state the V_{OUT}^- pin regulates at $-V_{IN\_N}$ less any voltage drop due to the load current on V_{OUT}^-.

Inverting Charge Pump Burst Mode Operation

The LTC3265 inverting charge pump provides low power Burst Mode operation when a logic high is applied to the MODE pin. In Burst Mode, the charge pump charges the V_{OUT}^- pin to $-0.94 \bullet V_{IN\_N}$ (typ). The part then shuts down the internal oscillator to reduce switching losses

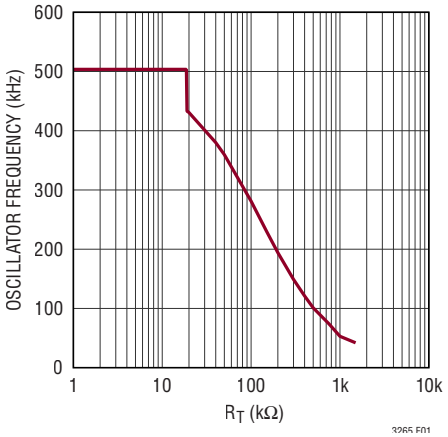


Figure 1. Oscillator Frequency vs R_T

OPERATION (Refer to the Block Diagram)

and goes into a low current state. This state is referred to as the sleep state in which the IC consumes only about 25µA from the V_{IN_N} pin. When the V_{OUT}^- output voltage droops enough to overcome the burst comparator hysteresis, the part wakes up and commences charge pump cycles until the output voltage exceeds –0.94 • V_{IN} (typ). This mode provides lower operating current at the cost of higher output ripple and is ideal for light load operation.

Charge Pump Frequency Programming

The charge transfer frequency can be adjusted between 50kHz and 500kHz using an external resistor on the RT pin. At slower frequencies the effective open-loop output resistance (R_{OL}) of the charge pumps are larger and they provide smaller average output current. Figure 1 can be used to determine a suitable value of R_T to achieve a required oscillator frequency. If the RT pin is grounded, the part operates at a constant frequency of 500kHz.

The charge pumps have lower R_{OL} at higher frequencies. For Burst Mode operation it is recommended that the RT pin be tied to GND. This minimizes the charge pump R_{OL}, quickly charges the output up to the burst threshold and optimizes the duration of the low current sleep state.

Charge Pump Soft-Start

The LTC3265 has built in soft-start circuitry to prevent excessive current flow during start-up. The soft-start is achieved by internal circuitry that slowly ramps the amount of current available at the output storage capacitors on the V_{OUT}^+ and V_{OUT}^- pins. The soft-start circuitry is reset in the event of a commanded shutdown or thermal shutdown.

Charge Pump Short-Circuit/Thermal Protection

The LTC3265 charge pumps have built-in short-circuit current limit as well as overtemperature protection. During a short-circuit condition, the part automatically limits its output currents from the V_{OUT}^+ and V_{OUT}^- pins to 220mA and 160mA respectively. If the junction temperature exceeds approximately 175°C the thermal shutdown circuitry disables current delivery to the outputs. Once the junction temperature drops back to approximately 165°C current delivery to the outputs is resumed. When thermal protection is active the junction temperature is beyond the specified operating range. Thermal protection is intended for momentary overload conditions outside normal operation. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Positive Low Dropout Linear Regulator (LDO+)

The positive low dropout regulator (LDO+) supports a load of up to 50mA. The LDO+ takes power from the V_{OUT}^+ pin (output of the boost charge pump) and drives the LDO+ output pin to a voltage programmed by the resistor divider connected between LDO+, ADJ+ and GND pins. For stability, the LDO+ output must be bypassed to ground with a low ESR ceramic capacitor that maintains a capacitance of at least 2µF across operating temperature and voltage.

The boost charge pump and LDO+ are enabled or disabled via the EN+ logic input pin. Internal circuitry delays enabling the LDO+ output until reasonable voltage has developed on the charge storage capacitor on the V_{OUT}^+ pin. When the LDO+ is enabled, a soft-start circuit ramps its regulation point from zero to the final value over a period of 75µs, reducing the inrush current on V_{OUT}^+ pin.

Figure 2 shows the LDO+ regulator application circuit. The LDO+ output voltage V_{LDO}^+ can be programmed by choosing suitable values of R1 and R2 such that:

$$V_{LDO}^+ = 1.2V \bullet \left(\frac{R1}{R2} + 1\right)$$

An optional capacitor of 100nF can be connected from the BYP+ pin to ground. This capacitor bypasses the internal 1.2V reference of the LTC3265 and improves the noise performance of the LDO+. If this function is not used the BYP+ pin should be left floating.

An optional feedback capacitor (C_{OPT}) can be added for improved transient response. A value of 10pF is recommended for most applications but experimentation with capacitor sizes between 2pF and 22pF may yield further improvement in the transient response.

OPERATION

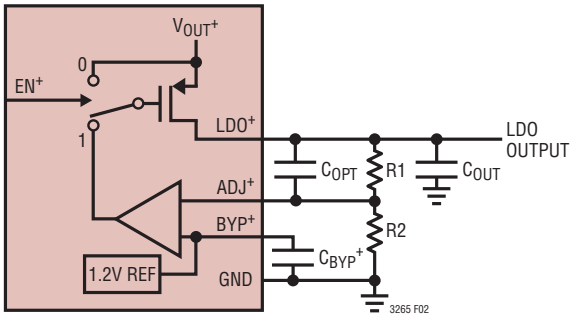


Figure 2. Positive LDO Application Circuit

Negative Low Dropout Linear Regulator (LDO⁻)

The negative low dropout regulator (LDO⁻) supports a load of up to 50mA. The LDO⁻ takes power from the V_{OUT}^- pin (output of the inverting charge pump) and drives the LDO⁻ output pin to a voltage programmed by the resistor divider connected between LDO⁻, ADJ⁻ and GND pins. For stability, the LDO⁻ output must be bypassed to ground with a low ESR ceramic capacitor that maintains a capacitance of at least 2µF across operating temperature and voltage.

The LDO⁻ is enabled or disabled via the EN⁻ logic input pin. Initially, when the EN⁻ logic input is low, the charge pump circuitry is disabled and the V_{OUT}^- pin is at GND. When EN⁻ is switched high, the V_{OUT}^- pin will be driven negative by the charge pump circuitry. Soft-start circuitry in the charge pump also provides soft-start functionality for the LDO⁻ and prevents excessive inrush currents.

Figure 3 shows the LDO⁻ regulator application circuit. The LDO⁻ output voltage V_{LDO}^- can be programmed by choosing suitable values of R1 and R2 such that:

$$V_{LDO}^- = -1.2V \bullet \left(\frac{R1}{R2} + 1\right)$$

An optional capacitor of 100nF can be connected from the BYP⁻ pin to ground. This capacitor bypasses the internal –1.2V reference of the LTC3265 and improves the noise performance of the LDO⁻. If this function is not used the BYP⁻ pin should be left floating.

An optional feedback capacitor (C_{OPT}) can be added for improved transient response. A value of 10pF is recommended for most applications but experimentation with capacitor sizes between 2pF and 22pF may yield further improvement in the transient response.

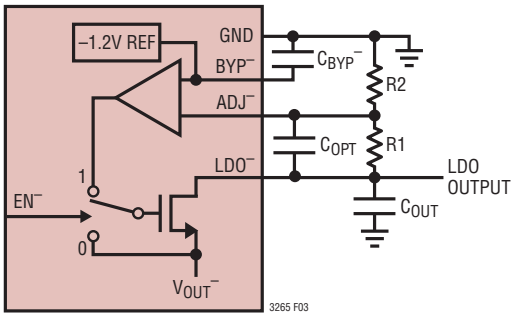


Figure 3: Negative LDO Application Circuit

APPLICATIONS INFORMATION

Effective Open-Loop Output Resistance

The effective open-loop output resistance (R_{OL}) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator frequency (f_{OSC}), value of the flying capacitor (C_{FLY}), the nonoverlap time, the internal switch resistances (R_S) and the ESR of the external capacitors.

Typical R_{OL} values of the boost charge pump as a function of temperature are shown in Figure 4.

Typical R_{OL} values of the inverting charge pump as a function of temperature are shown in Figure 5.

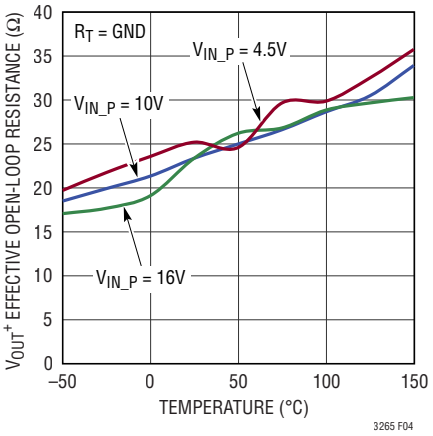


Figure 4. Typical R_{OL} vs Temperature (Boost Charge Pump)

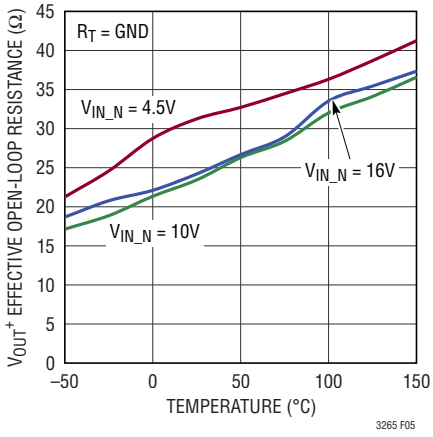


Figure 5. Typical R_{OL} vs Temperature (Inverting Charge Pump)

Input/Output Capacitor Selection

The style and value of capacitors used with the LTC3265 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum turn-on time. To reduce noise and ripple, it is recommended that low ESR ceramic capacitors be used for the charge pumps and LDO outputs. All capacitors should retain at least 2µF of capacitance over operating temperature and bias voltage. Tantalum and aluminum capacitors can be used in parallel with a ceramic capacitor to increase the total capacitance but should not be used alone because of their high ESR. In constant frequency mode, the values of C_{OUT}^+ and C_{OUT}^- directly control the amount of output ripple for a given load current. Increasing the sizes of C_{OUT}^+ and C_{OUT}^- will reduce the output ripple at the expense of higher minimum turn-on time. The peak-to-peak output ripple at the V_{OUT}^+ pin is approximately given by the expression:

$$V_{RIPPLE(P-P)} \approx \frac{I_{OUT}^+}{C_{OUT}^+}\left[\frac{1}{f_{OSC}} - t_{ON}\right]$$

where f_{OSC} is the oscillator frequency, C_{OUT}^+ is the value of the output capacitor and t_{ON} is the on-time of the oscillator (1µs typical). The output ripple at the V_{OUT}^- pin can be calculated using the corresponding I_{OUT}^- and C_{OUT}^- values.

Just as the value of C_{OUT} controls the amount of output ripple, the value of C_{IN} controls the amount of ripple present at the input pins (V_{IN_P} and V_{IN_N}). The amount of bypass capacitance required at the input depends on the source impedance driving V_{IN_P} and V_{IN_N}. For best results it is recommended that V_{IN_P} and V_{IN_N} be bypassed with at least 2µF of low ESR capacitance. A high ESR capacitor such as tantalum or aluminum will have higher input noise than a low ESR ceramic capacitor. Therefore, a ceramic capacitor is recommended as the main bypass capacitance with a tantalum or aluminum capacitor used in parallel if desired.

Flying Capacitor Selection

The flying capacitors (C_{BST} and C_{INV}) controls the strength of the charge pumps. A 1µF or greater ceramic capacitor is suggested for the flying capacitor for applications requiring the full rated output current of the charge pump.

For very light load applications, the flying capacitor may be reduced to save space or cost. For example, a 0.2µF capacitor might be sufficient for load currents up to 20mA.

APPLICATIONS INFORMATION

A smaller flying capacitor leads to a larger effective open-loop resistance (R_{OL}) and thus limits the maximum load current that can be delivered by the charge pump.

Ceramic Capacitors

Ceramic capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. The capacitor manufacturer's data sheet should be consulted to ensure the desired capacitance at all temperatures and voltages. Table 1 is a list of ceramic capacitor manufacturers and their websites.

Table 1

AVX	www.avx.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com
TDK	www.component.tdk.com
Würth Elektronik	www.we-online.com

Layout Considerations

Due to high switching frequency and high transient currents produced by LTC3265, careful board layout is necessary for optimum performance. A true ground plane and short connections to all the external capacitors will improve performance and ensure proper regulation under all conditions. Figure 6 shows an example layout for the LTC3265.

The flying capacitor nodes C_{BST}^+, C_{BST}^-, C_{INV}^+ and C_{INV}^- switch large currents at a high frequency. These nodes should not be routed close to sensitive pins such as the LDO feedback pins (ADJ^+ and ADJ^-) and internal reference bypass pins (BYP^+ and BYP^-).

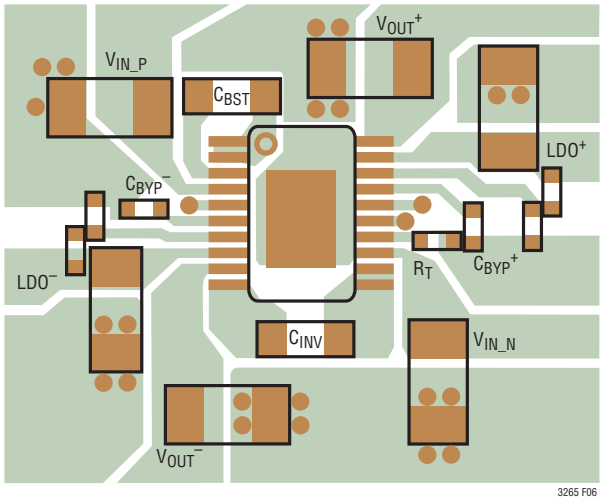


Figure 6. Recommended Layout

Thermal Management

At high input voltages and maximum output current, there can be substantial power dissipation in the LTC3265. If the junction temperature increases above approximately 175°C, the thermal shutdown circuitry will automatically deactivate the output. To reduce the maximum junction temperature, a good thermal connection to the PC board ground plane is recommended. Connecting the exposed pad of the package to a ground plane under the device on two layers of the PC board can reduce the thermal resistance of the package and PC board considerably.

Derating Power at High Temperatures

To prevent an overtemperature condition in high power applications, Figure 7 should be used to determine the maximum combination of ambient temperature and power dissipation.

The power dissipated in the LTC3265 should always fall under the line shown for a given ambient temperature. The power dissipated in the LTC3265 has four components.

Power dissipated in boost charge pump:

$$P_{BOOST} = (2 \bullet V_{IN\_P} – V_{OUT}^+) \bullet (I_{OUT}^+ + I_{LDO}^+)$$

Power dissipated in the positive LDO:

$$P_{LDO}^+ = (V_{OUT}^+ – V_{LDO}^+) \bullet I_{LDO}^+$$

APPLICATIONS INFORMATION

Power dissipated in the negative LDO:

$$P_{LDO^-} = (|V_{OUT^-}| - |V_{LDO^-}|) \bullet I_{LDO^-}$$

And, power dissipated in the inverting charge pump:

$$P_{INV} = (V_{IN\_N} - |V_{OUT^-}|) \bullet (I_{OUT^-} + I_{LDO^-})$$

where I_{OUT^+} denotes any additional current that might be pulled directly from the V_{OUT^+} pin and I_{OUT^-} denotes any additional current out of the V_{OUT^-} pin. The LDO^+ current is supplied by the boost charge pump through V_{OUT^+} and is therefore included in the boost charge pump power dissipation. The LDO^- current is supplied by the inverting charge pump through V_{OUT^-} and is therefore included in the inverting charge pump power dissipation.

The total power dissipation of the LTC3265 is given by:

$$P_D = P_{BOOST} + P_{LDO^+} + P_{LDO^-} + P_{INV}$$

The derating curve in Figure 7 assumes a maximum thermal resistance, θ_{JA}, of 38°C/W for the 20-lead TSSOP package. This can be achieved with a 4-layer PCB that includes 2oz Cu traces and six vias from the exposed pad of the LTC3265 to the ground plane.

It is recommended that the LTC3265 be operated in the region corresponding to $T_J \leq 150°C$ for continuous operation as shown in Figure 7. Operation beyond 150°C should be avoided as it may degrade part performance and lifetime. At high temperatures, typically around 175°C, the part is placed in thermal shutdown and all outputs are disabled. When the part cools back down to a low enough temperature, typically around 165°C, the outputs are re-enabled and the part resumes normal operation.

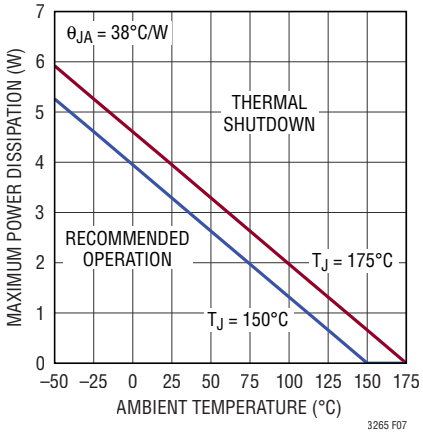
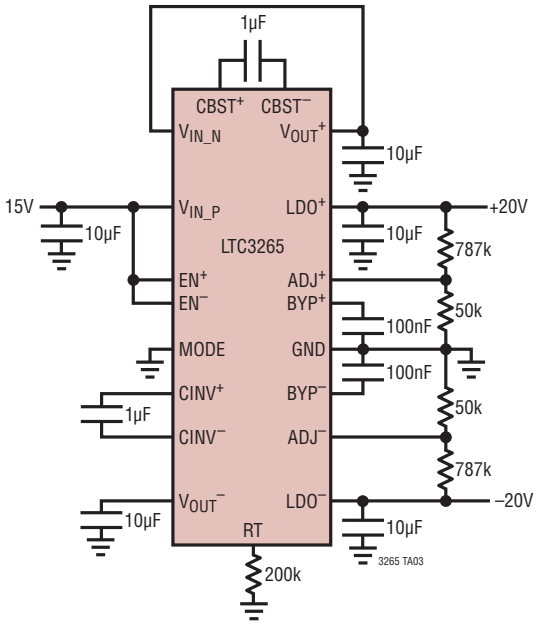


Figure 7. Maximum Power Dissipation vs Ambient Temperature

TYPICAL APPLICATIONS

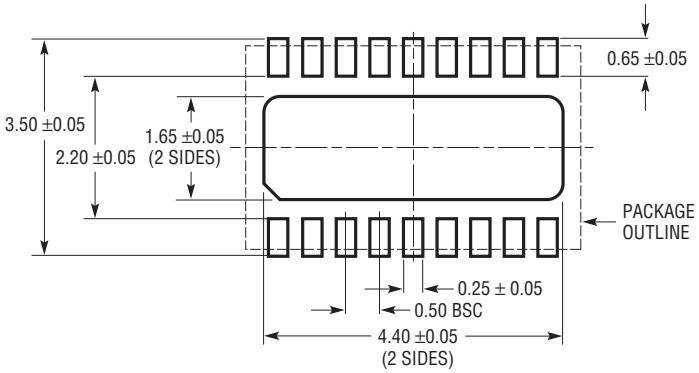
Low Power ±20V Power Supply from a Single-Ended 15V Input Supply



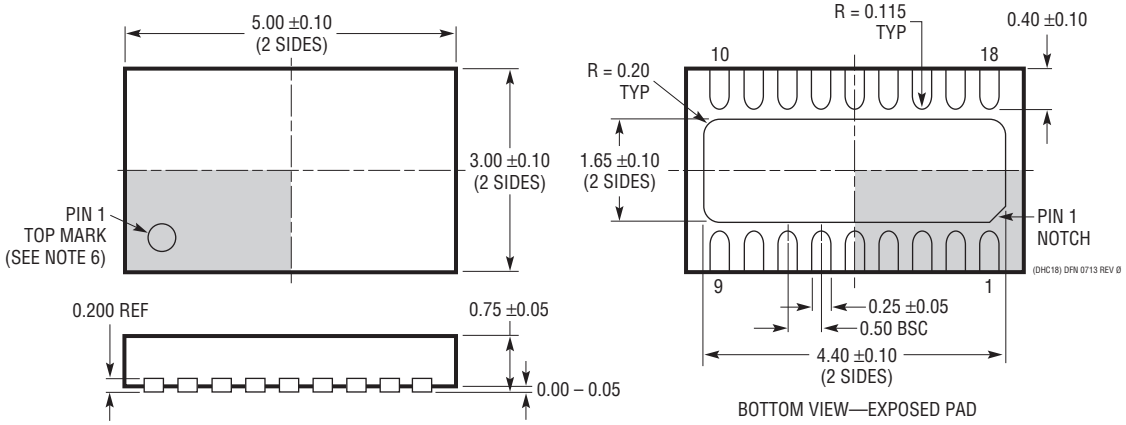
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3265#packaging for the most recent package drawings.

DHC Package
18-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1955 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



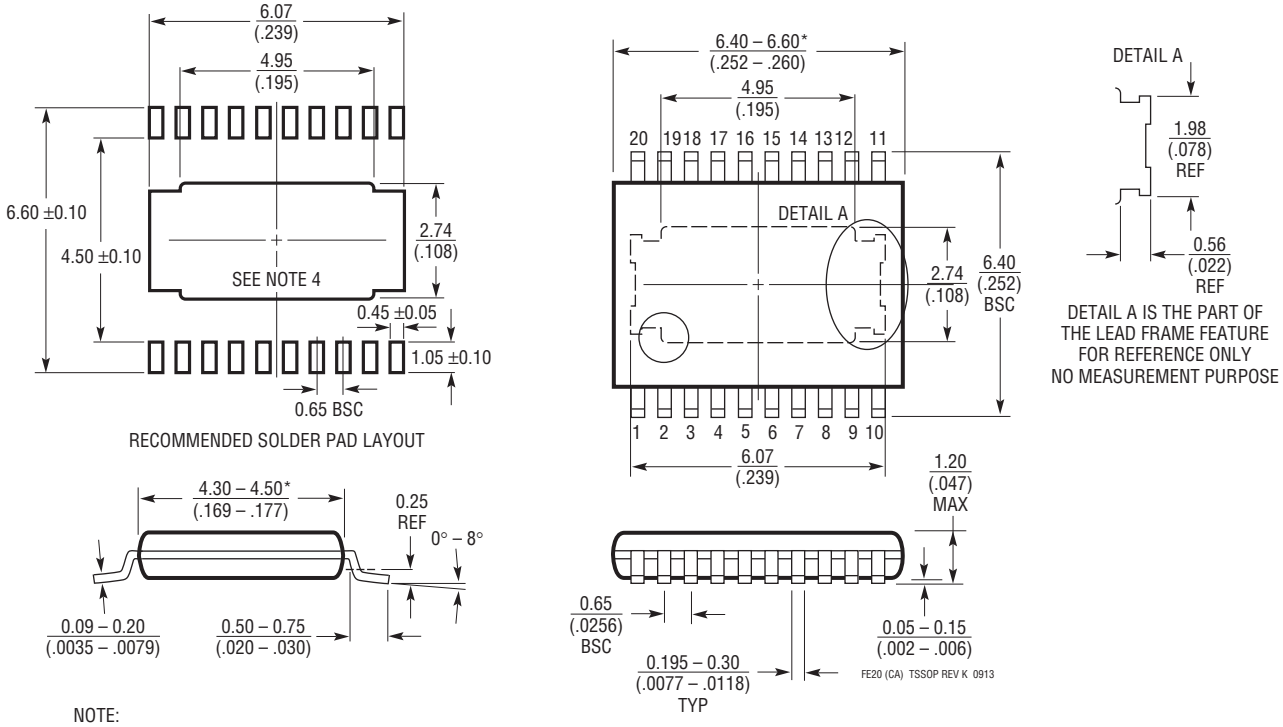
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3265#packaging for the most recent package drawings.

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev K)
Exposed Pad Variation CA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	03/16	Changed conditions of R_T in V_{OUT}^- Voltage Loss curve.	6