

# Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Charger

## FEATURES

- Dual Input, Single Output DC/DCs with Input Prioritizer
  - Energy Harvesting Input: 3.0V to 19V Buck DC/DC
  - Battery Input: Up to 4.2V Buck-Boost DC/DC
- 10mA Shunt Battery Charger with Programmable Float Voltages: 3.45V, 4.0V, 4.1V, 4.2V
- Low Battery Disconnect
- Ultra Low Quiescent Current: 950nA at no Load
- Integrated Supercapacitor Balancer
- Up to 50mA of Output Current
- Programmable DC/DC Output Voltage, Buck UVLO, and Buck-Boost Peak Input Current
- Integrated Low-Loss Full-Wave Bridge Rectifier
- Input Protective Shunt: Up to 25mA at  $V_{IN} \geq 20V$
- 5mm × 5mm QFN-32 Package

## APPLICATIONS

- Energy Harvesting
- Solar Powered Systems with Battery Backup
- Wireless HVAC Sensors and Security Devices
- Mobile Asset Tracking

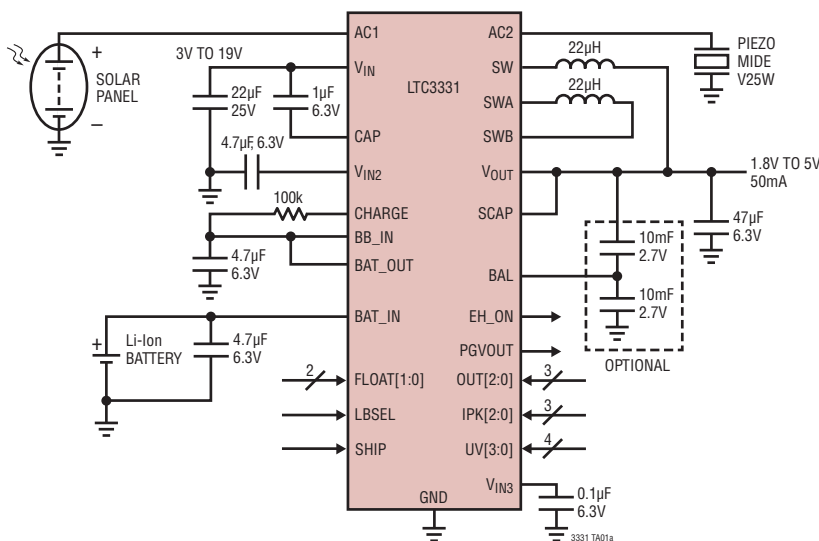
## DESCRIPTION

The **LTC<sup>®</sup>3331** integrates a high voltage energy harvesting power supply plus a buck-boost DC/DC powered from a rechargeable battery to create a single output supply for alternative energy applications. A 10mA shunt allows simple charging of the battery with harvested energy while a low battery disconnect function protects the battery from deep discharge. The energy harvesting power supply, consisting of an integrated full-wave bridge rectifier and a high voltage buck DC/DC, harvests energy from piezoelectric, solar, or magnetic sources. Either DC/DC converter can deliver energy to a single output. The buck operates when harvested energy is available, reducing the quiescent current draw on the battery to the 200nA required by the shunt charger, thereby extending the life of the battery. The buck-boost powers  $V_{OUT}$  only when harvested energy is unavailable.

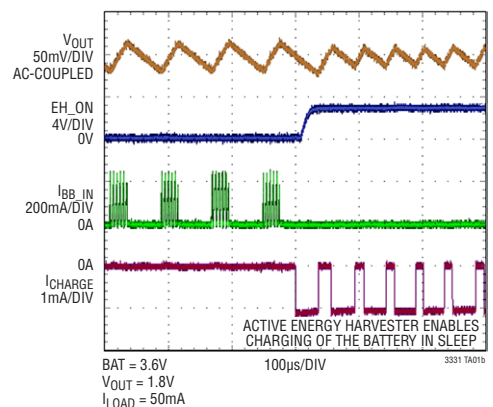
A supercapacitor balancer is also integrated, allowing for increased energy storage. Voltage and current settings for both inputs and outputs are programmable via pin-strapped logic inputs. The LTC3331 is available in a 5mm × 5mm QFN-32 package.

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## TYPICAL APPLICATION



### Charging a Battery with Harvested Energy



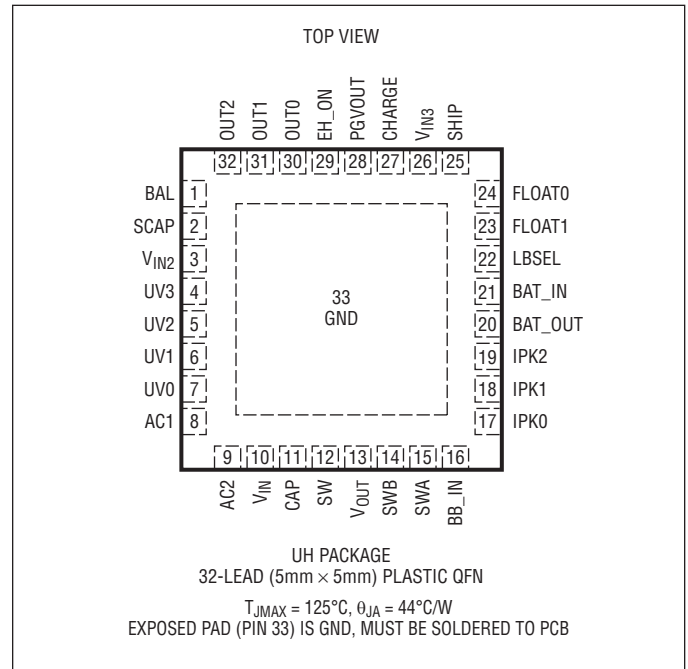
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$	Low Impedance Source .....	-0.3 to 19V*
	Current-Fed, $I_{SW} = 0A$ .....	25mA
AC1, AC2 .....		0 to $V_{IN}$
BB_IN, $V_{OUT}$ , $V_{IN3}$ , BAT_IN, SCAP, PGVOUT, CHARGE, SHIP .....		-0.3 to 6V
BAT_OUT ....	-0.3V to [Lesser of (BAT_IN + 0.3V) or 6V]	
$V_{IN2}$ .....	-0.3V to [Lesser of ( $V_{IN} + 0.3V$ )] or 6V	
CAP .....	[Higher of -0.3V or ( $V_{IN} - 6V$ )] to $V_{IN}$	
BAL .....	-0.3V to ( $SCAP + 0.3V$ )	
OUT[2:0] .....	-0.3V to [Lesser of ( $V_{IN3} + 0.3V$ ) or 6V]	
IPK[2:0] .....	-0.3V to [Lesser of ( $V_{IN3} + 0.3V$ ) or 6V]	
EH_ON .....	-0.3V to [Lesser of ( $V_{IN3} + 0.3V$ ) or 6V]	
FLOAT[1:0] ...	-0.3V to [Lesser of (BB_IN + 0.3V) or 6V]	
LBSEL .....	-0.3V to [Lesser of (BB_IN + 0.3V) or 6V]	
UV[3:0] .....	-0.3V to [Lesser of ( $V_{IN2} + 0.3V$ ) or 6V]	
$I_{AC1}$ , $I_{AC2}$ .....		$\pm 50mA$
$I_{SWA}$ , $I_{SWB}$ , $I_{VOUT}$ .....		350mA
$I_{SW}$ .....		500mA
Operating Junction Temperature Range (Notes 2, 3) .....		-40°C to 125°C
Storage Temperature Range .....		-65°C to 150°C

\* $V_{IN}$  has an internal 20V clamp

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3331EUH#PBF	LTC3331EUH#TRPBF	3331	32-Lead (5mm × 5mm) Plastic QFN	-40°C to 85°C
LTC3331IUH#PBF	LTC3331IUH#TRPBF	3331	32-Lead (5mm × 5mm) Plastic QFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 2).  $V_{IN} = 5\text{V}$ ,  $BAT\_IN = BAT\_OUT = BB\_IN = 3.6\text{V}$ ,  $SHIP = 0\text{V}$ ,  $SCAP = 0\text{V}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{IN}$	Buck Input Voltage Range	●			19	V	
$V_{BB\_IN}$	Buck-Boost Input Voltage Range	(Note 7) ●	1.8		5.5	V	
$I_{VIN}$	$V_{IN}$ Quiescent Current $V_{IN}$ Input in UVLO $V_{IN}$ Input in UVLO Buck Enabled, Sleeping Buck Enabled, Sleeping Buck Enabled, Not Sleeping	$V_{IN} = 2.5\text{V}$ , $V_{BB\_IN} = 0\text{V}$ $V_{IN} = 16\text{V}$ , $V_{BB\_IN} = 0\text{V}$ $V_{IN} = 4\text{V}$ , $V_{BB\_IN} = 0\text{V}$ $V_{IN} = 18\text{V}$ , $V_{BB\_IN} = 0\text{V}$ $V_{IN} = 5\text{V}$ , $V_{BB\_IN} = 0\text{V}$ , $I_{SW} = 0\text{A}$ (Note 4)		450 800 1300 1800 150	700 1400 2000 2700 225	nA nA nA nA $\mu\text{A}$	
$I_{BB\_IN}$	$BB\_IN$ Quiescent Current (Note 6) $BB\_IN$ Input with $V_{IN}$ Active Buck-Boost Enabled, Sleeping Buck-Boost Enabled, Not Sleeping	$V_{BB\_IN} = 3.6\text{V}$ , $V_{IN} = 5\text{V}$ $V_{BB\_IN} = 3.6\text{V}$ , $V_{IN} = 0\text{V}$ $V_{BB\_IN} = 3.6\text{V}$ , $V_{IN} = 0\text{V}$ , $I_{SWA} = I_{SWB} = 0\text{A}$ (Note 4)		200 950 200	300 1500 300	nA nA $\mu\text{A}$	
$I_{VOUT}$	$V_{OUT}$ Leakage Current	5V Output Selected, Sleeping		100	150	nA	
	$V_{IN}$ Undervoltage Lockout Thresholds (Rising or Falling)	3V Level Selected	●	2.91	3.00	3.09	V
		4V Level Selected	●	3.88	4.00	4.12	V
		5V Level Selected	●	4.85	5.00	5.15	V
		6V Level Selected	●	5.82	6.00	6.18	V
		7V Level Selected	●	6.79	7.00	7.21	V
		8V Level Selected	●	7.76	8.00	8.24	V
		9V Level Selected	●	8.73	9.00	9.27	V
		10V Level Selected	●	9.70	10.0	10.30	V
		11V Level Selected	●	10.67	11.0	11.33	V
		12V Level Selected	●	11.64	12.0	12.36	V
		13V Level Selected	●	12.61	13.0	13.39	V
		14V Level Selected	●	13.58	14.0	14.42	V
		15V Level Selected	●	14.55	15.0	15.45	V
		16V Level Selected	●	15.52	16.0	16.48	V
	17V Level Selected	●	16.49	17.0	17.51	V	
	18V Level Selected	●	17.46	18.0	18.54	V	
$V_{SHUNT}$	$V_{IN}$ Shunt Regulator Voltage	$I_{VIN} = 1\text{mA}$ ●	19.0	20.0	21.0	V	
$I_{SHUNT}$	Maximum Protective Shunt Current		25			$\text{mA}$	
	Internal Bridge Rectifier Loss ( $ V_{AC1} - V_{AC2}  - V_{IN}$ )	$I_{BRIDGE} = 10\mu\text{A}$ $I_{BRIDGE} = 50\text{mA}$	700 1350	800 1550	900 1750	mV mV	
	Internal Bridge Rectifier Reverse Leakage Current	$V_{REVERSE} = 18\text{V}$			20	nA	
	Internal Bridge Rectifier Reverse Breakdown Voltage	$I_{REVERSE} = 1\mu\text{A}$	$V_{SHUNT}$	30		V	

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{OUT}$	Regulated Buck/Buck-Boost Output Voltage	1.8V Output Selected Sleep Threshold Wake-Up Threshold	● ●	1.806 1.794	1.872	V V	
		2.5V Output Selected Sleep Threshold Wake-Up Threshold	● ●	2.508 2.492	2.575	V V	
		2.8V Output Selected Sleep Threshold Wake-Up Threshold	● ●	2.809 2.791	2.884	V V	
		3.0V Output Selected Sleep Threshold Wake-Up Threshold	● ●	3.010 2.990	3.090	V V	
		3.3V Output Selected Sleep Threshold Wake-Up Threshold	● ●	3.311 3.289	3.400	V V	
		3.6V Output Selected Sleep Threshold Wake-Up Threshold	● ●	3.612 3.588	3.708	V V	
		4.5V Output Selected Sleep Threshold Wake-Up Threshold	● ●	4.515 4.485	4.635	V V	
		5.0V Output Selected Sleep Threshold Wake-Up Threshold	● ●	5.017 4.983	5.150	V V	
	PGVOUT Falling Threshold	As a Percentage of $V_{OUT}$ Target (Note 5)	●	88	92	96	%
$I_{PEAK\_BB}$	Buck-Boost Peak Switch Current	250mA Target Selected		200	250	350	mA
		150mA Target Selected		120	150	210	mA
		100mA Target Selected		80	100	140	mA
		50mA Target Selected		40	50	70	mA
		25mA Target Selected		20	25	35	mA
		15mA Target Selected		12	15	21	mA
		10mA Target Selected		8	10	14	mA
		5mA Target Selected		4	5	7	mA
	Available Buck-Boost Current	$I_{PEAK\_BB} = 250\text{mA}$ , $V_{OUT} = 3.3\text{V}$		50		mA	
	Buck-Boost PMOS Input and Output Switch On-Resistance	IPK[2:0] = 111		0.8		$\Omega$	
IPK[2:0] = 110			1.0		$\Omega$		
IPK[2:0] = 101			1.4		$\Omega$		
IPK[2:0] = 100			2.4		$\Omega$		
IPK[2:0] = 011			4.5		$\Omega$		
IPK[2:0] = 010			7.3		$\Omega$		
IPK[2:0] = 001			10.7		$\Omega$		
IPK[2:0] = 000			20.5		$\Omega$		
	Buck-Boost NMOS Input and Output Switch On-Resistance	IPK2 = 1		0.6		$\Omega$	
IPK2 = 0			3.9		$\Omega$		

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	PMOS Switch Leakage	Buck/Buck-Boost Regulators	-20		20	nA
	NMOS Switch Leakage	Buck/Buck-Boost Regulators	-20		20	nA
	Maximum Buck Duty Cycle	Buck/Buck-Boost Regulators	● 100			%
$I_{PEAK\_BUCK}$	Buck Peak Switch Current		200	250	500	mA
	Available Buck Output Current		100			mA
	Buck PMOS Switch On-Resistance			1.4		$\Omega$
	Buck NMOS Switch On-Resistance			1.2		$\Omega$
	Maximum Battery Shunt Current		10			mA
$I_{BAT\_IN}$	Battery Disconnect Leakage Current	Battery Disconnected SHIP Mode Engaged	-10 -10	0 0	10 10	nA nA
$V_{FLOAT}$	Shunt Charger Float Voltage (BAT_OUT Voltage)	FLOAT[1:0] = 00, $I_{BB\_IN} = 1\text{mA}$ FLOAT[1:0] = 01, $I_{BB\_IN} = 1\text{mA}$ FLOAT[1:0] = 10, $I_{BB\_IN} = 1\text{mA}$ FLOAT[1:0] = 11, $I_{BB\_IN} = 1\text{mA}$	3.415 3.960 4.059 4.158	3.45 4.0 4.1 4.2	3.485 4.040 4.141 4.242	V V V V
		FLOAT[1:0] = 00, $I_{BB\_IN} = 1\text{mA}$ FLOAT[1:0] = 01, $I_{BB\_IN} = 1\text{mA}$ FLOAT[1:0] = 10, $I_{BB\_IN} = 1\text{mA}$ FLOAT[1:0] = 11, $I_{BB\_IN} = 1\text{mA}$	● 3.381 ● 3.920 ● 4.018 ● 4.116	3.45 4.0 4.1 4.2	3.519 4.080 4.182 4.284	V V V V
$V_{LBD}$	Low Battery Disconnect Threshold, BAT_IN Voltage (Falling)	LBSEL = 0, FLOAT[1:0] = 00, $I_{BAT\_IN} = -1\text{mA}$ LBSEL = 1, FLOAT[1:0] = 00, $I_{BAT\_IN} = -1\text{mA}$ LBSEL = 0, FLOAT[1:0] = 01, 10, 11, $I_{BAT\_IN} = -1\text{mA}$ LBSEL = 1, FLOAT[1:0] = 01, 10, 11, $I_{BAT\_IN} = -1\text{mA}$	● 1.98 ● 2.43 ● 2.62 ● 3.10	2.04 2.51 2.70 3.20	2.10 2.59 2.78 3.30	V V V V
$V_{LBC\_BAT\_IN}$	Low Battery Connect Threshold, BAT_IN Voltage (Rising)	LBSEL = 0, FLOAT[1:0] = 00, $I_{BAT\_IN} = -1\text{mA}$ LBSEL = 1, FLOAT[1:0] = 00, $I_{BAT\_IN} = -1\text{mA}$ LBSEL = 0, FLOAT[1:0] = 01, 10, 11, $I_{BAT\_IN} = -1\text{mA}$ LBSEL = 1, FLOAT[1:0] = 01, 10, 11, $I_{BAT\_IN} = -1\text{mA}$	2.26 2.74 2.91 3.39	2.35 2.85 3.03 3.53	2.44 2.96 3.15 3.67	V V V V
$V_{LBC\_BAT\_OUT}$	Low Battery Connect Threshold, BAT_OUT Voltage (Rising)	LBSEL = 0, FLOAT[1:0] = 00 LBSEL = 1, FLOAT[1:0] = 00 LBSEL = 0, FLOAT[1:0] = 01, 10, 11 LBSEL = 1, FLOAT[1:0] = 01, 10, 11		3.02 3.52 3.70 4.20		V V V V
	Battery Disconnect PMOS On-Resistance	$BAT\_IN = 3.3\text{V}$ , $I_{BAT\_IN} = 10\text{mA}$		5		$\Omega$
	Charge Pin Current	Current Out of CHARGE Pin	●		1 2	mA mA
	CHARGE Pin Voltage PMOS On-Resistance	2mA Out of CHARGE Pin		60		$\Omega$
$V_{SCAP}$	Supercapacitor Balancer Input Range		● 2.5		5.5	V
$I_{SCAP}$	Supercapacitor Balancer Quiescent Current	SCAP = 5.0V		150	225	nA
	Supercapacitor Balancer Source Current	SCAP = 5.0V, BAL = 2.4V	10			mA
	Supercapacitor Balancer Sink Current	SCAP = 5.0V, BAL = 2.6V	10			mA

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{BAL}$	Supercapacitor Balance Point	Percentage of SCAP Voltage	● 49	50	51	%
$V_{IH}$	Digital Input High Voltage	Pins: OUT[2:0], SHIP, FLOAT[1:0], LBSEL, IPK[2:0], UV[3:0]	● 1.2			V
$V_{IL}$	Digital Input Low Voltage	Pins: OUT[2:0], SHIP, FLOAT[1:0], LBSEL, IPK[2:0], UV[3:0]	●		0.4	V
$I_{IH}$	Digital Input High Current	Pins: OUT[2:0], SHIP, FLOAT[1:0], LBSEL, IPK[2:0], UV[3:0]		0	10	nA
$I_{IL}$	Digital Input Low Current	Pins: OUT[2:0], SHIP, FLOAT[1:0], LBSEL, IPK[2:0], UV[3:0]		0	10	nA
$V_{OH}$	PGVOUT, Output High Voltage EH_ON Output High Voltage	BB_IN = 5V, 1 $\mu\text{A}$ Out of Pin $V_{IN} = 6\text{V}$ , 1 $\mu\text{A}$ Out of Pin	● 4.0 ● 3.8			V V
$V_{OL}$	PGVOUT, EH_ON Output Low Voltage	BB_IN = 5V, 1 $\mu\text{A}$ into Pin	●		0.4	V

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3331 is tested under pulsed load conditions such that  $T_J \approx T_A$ . The LTC3331E is guaranteed to meet specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC3331I is guaranteed over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

**Note 3:**  $T_J$  is calculated from the ambient  $T_A$  and power dissipation PD according to the following formula:  $T_J = T_A + (P_D \cdot \theta_{JA})$ .

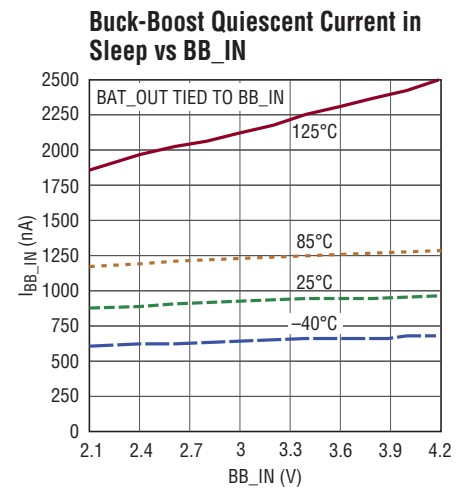
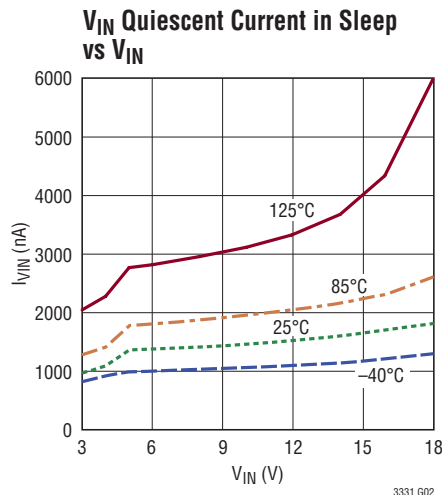
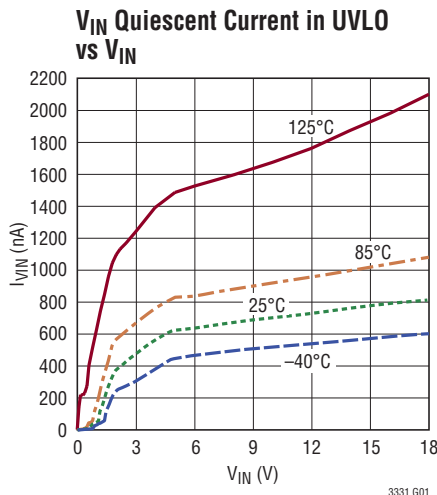
**Note 4:** Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

**Note 5:** The PGVOUT Rising threshold is equal to the sleep threshold. See  $V_{OUT}$  specification.

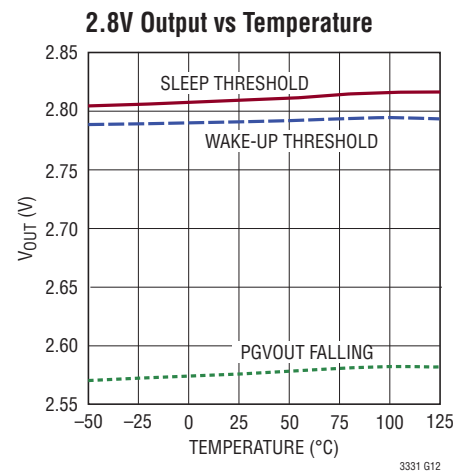
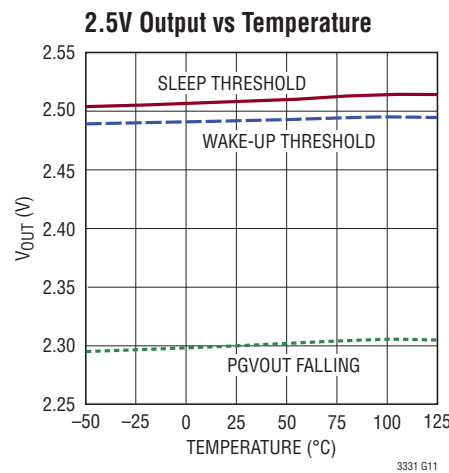
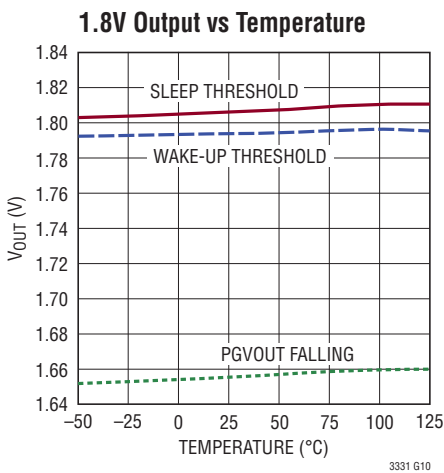
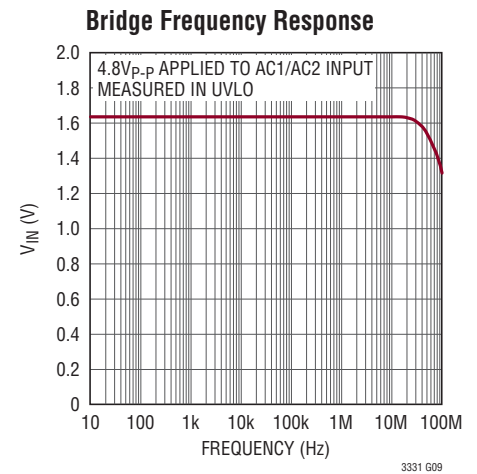
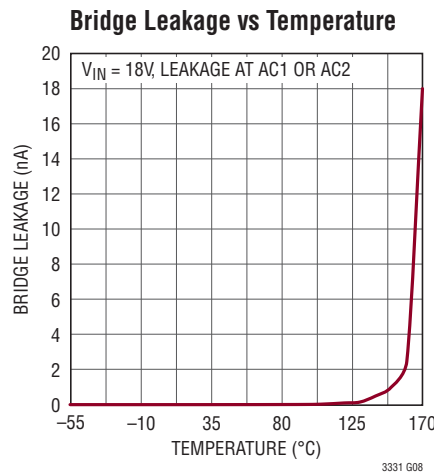
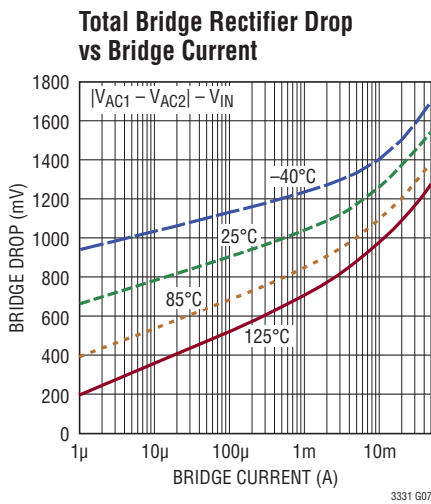
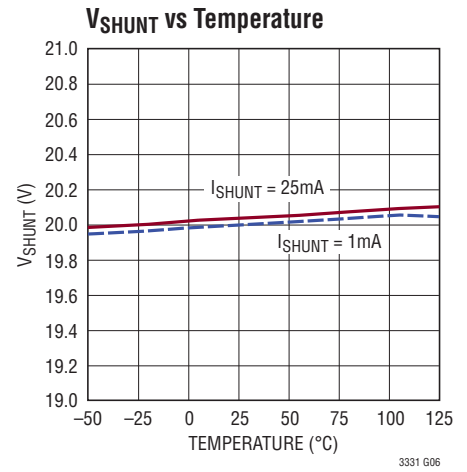
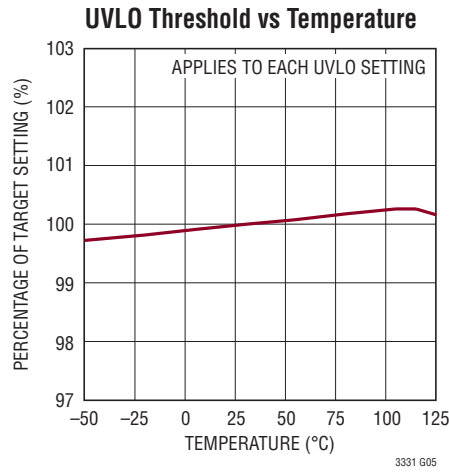
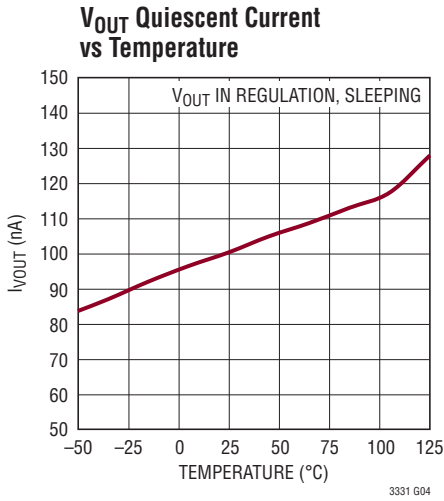
**Note 6:** These quiescent currents include the contribution from the internal resistor divider at the BAT\_OUT pin as BAT\_OUT must be tied to BB\_IN for all applications.

**Note 7:** The buck-boost operating voltage is further constrained to a narrower range by the programmed float voltage and the selected low battery disconnect and connect thresholds.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

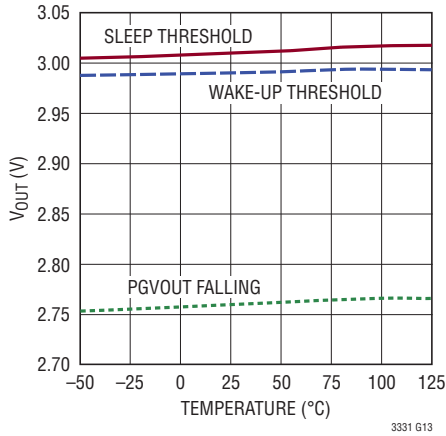


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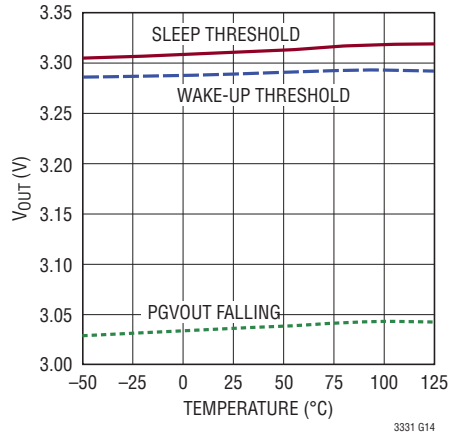


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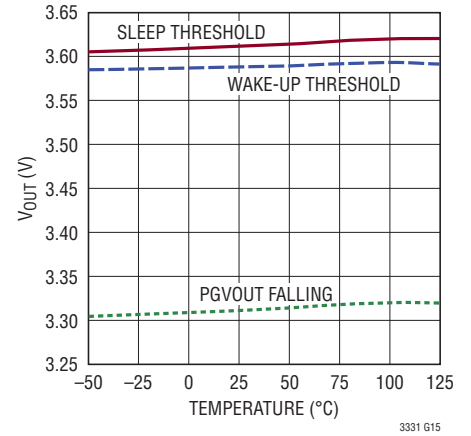
### 3V Output vs Temperature



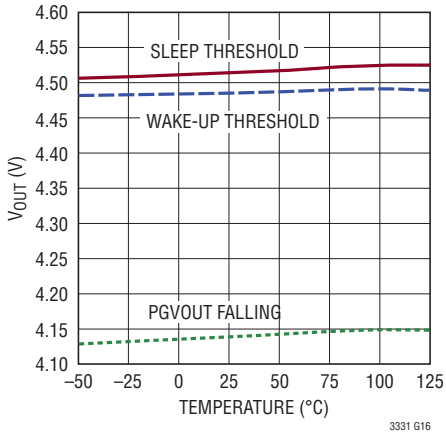
### 3.3V Output vs Temperature



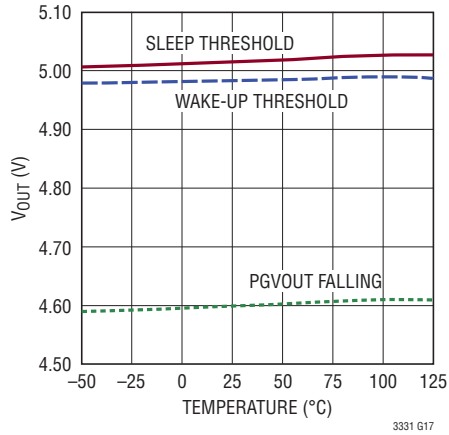
### 3.6V Output vs Temperature



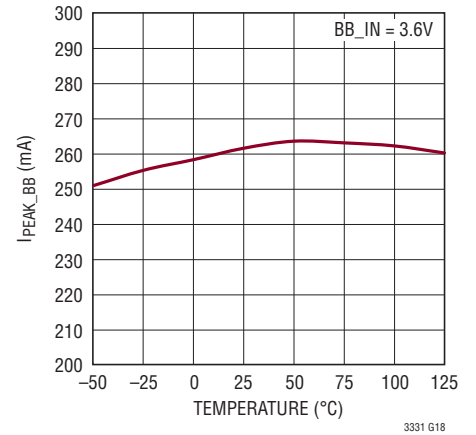
### 4.5V Output vs Temperature



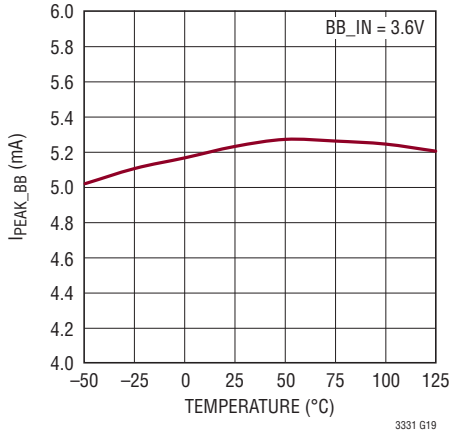
### 5V Output vs Temperature



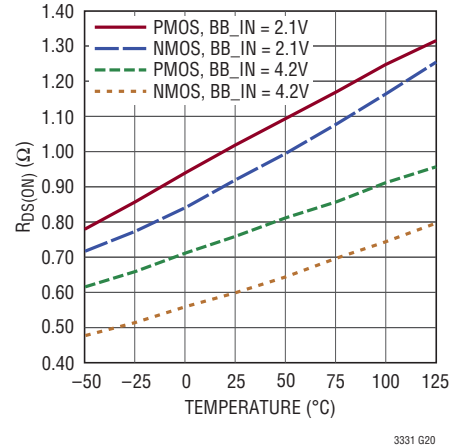
### Buck-Boost Peak Current vs Temperature, 250mA $I_{PEAK}$ Setting



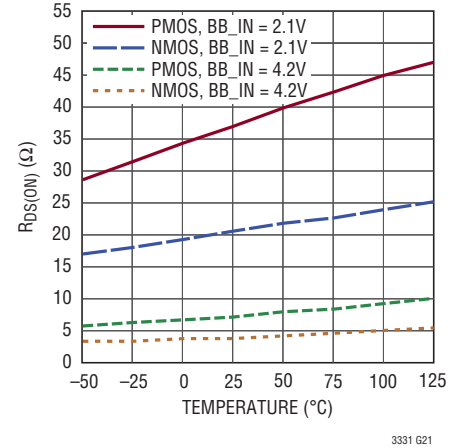
### Buck-Boost Peak Current vs Temperature, 5mA $I_{PEAK}$ Setting



### $R_{DS(ON)}$ of Buck-Boost PMOS/NMOS vs Temperature, 250mA $I_{PEAK}$ Setting



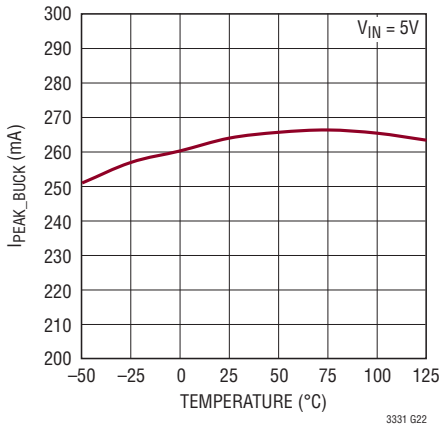
### $R_{DS(ON)}$ of Buck-Boost PMOS/NMOS vs Temperature, 5mA $I_{PEAK}$ Setting



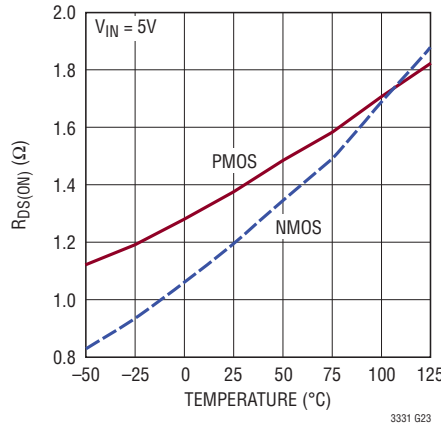


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

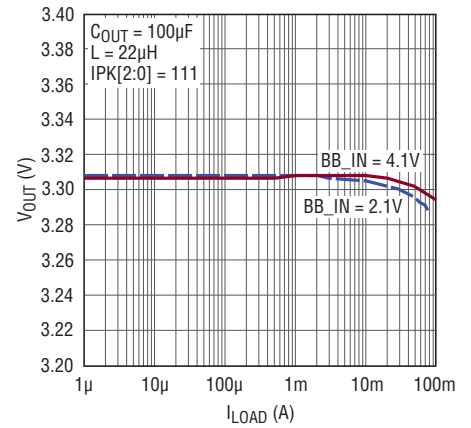
**Buck Peak Current vs Temperature**



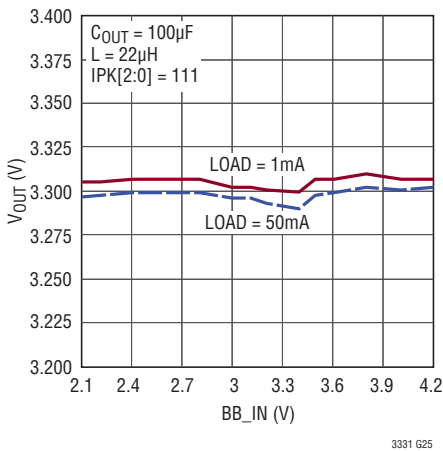
**$R_{DS(ON)}$  of Buck PMOS/NMOS vs Temperature**



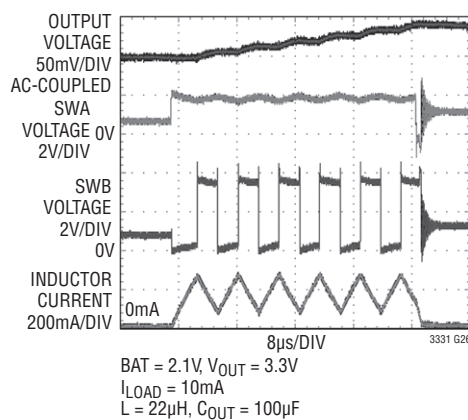
**Buck-Boost Load Regulation,  $V_{OUT} = 3.3\text{V}$**



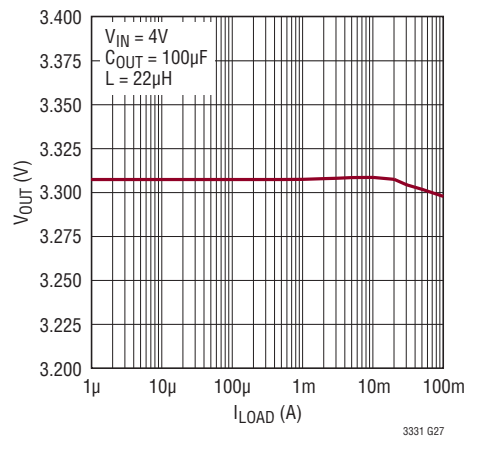
**Buck-Boost Line Regulation,  $V_{OUT} = 3.3\text{V}$**



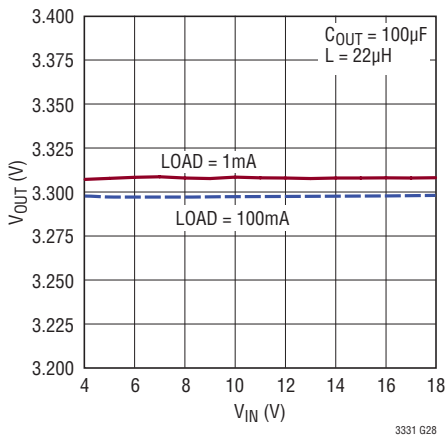
**Buck-Boost Switching Waveforms**



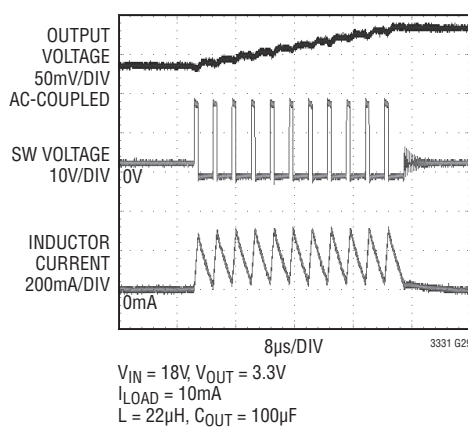
**Buck Load Regulation, 3.3V**



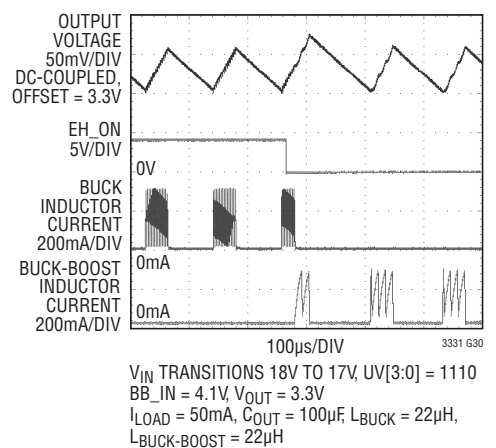
**Buck Line Regulation, 3.3V**



**Buck Switching Waveforms**

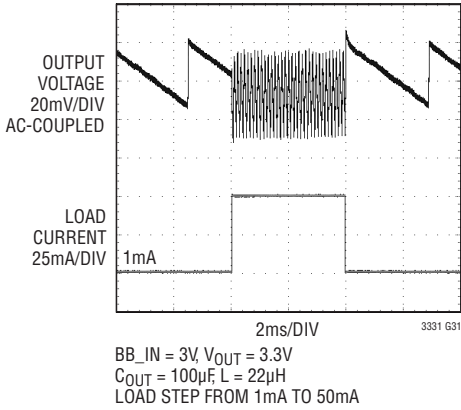


**Prioritizer Buck to Buck-Boost Transition**

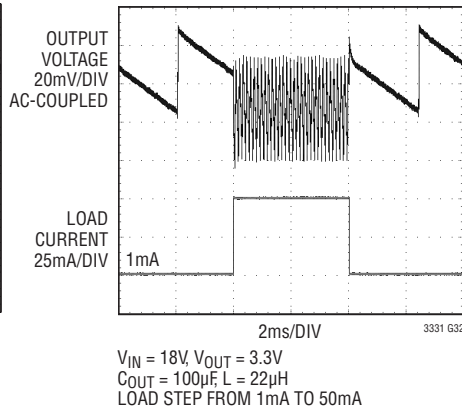


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

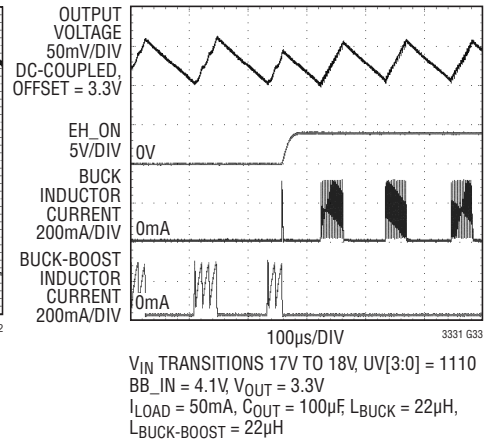
**Buck-Boost Load Step Response**



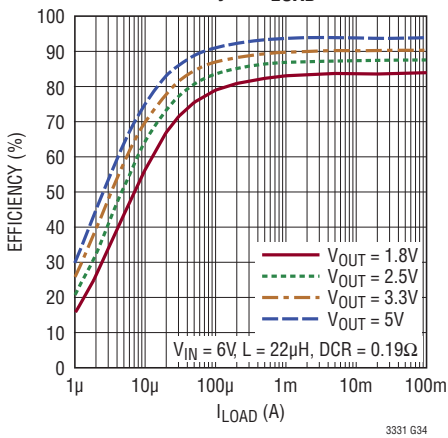
**Buck Load Step Response**



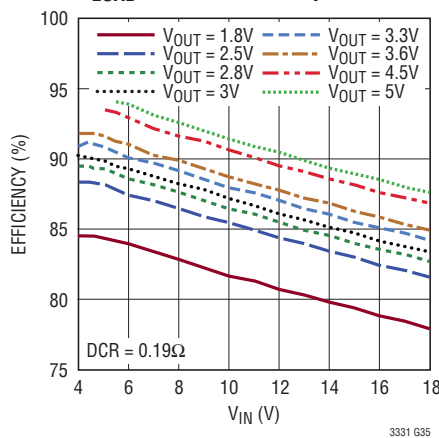
**Prioritizer Buck-Boost to Buck Transition**



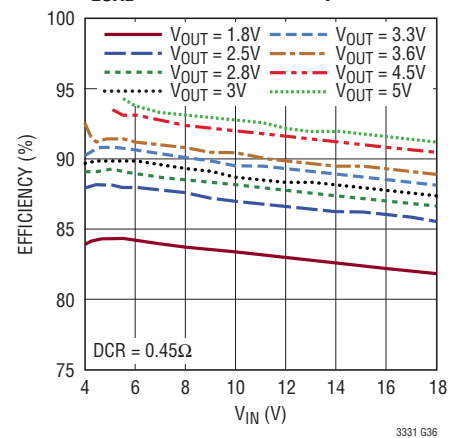
**Buck Efficiency vs I\_LOAD**



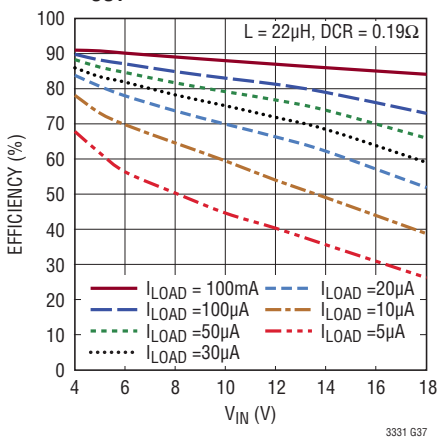
**Buck Efficiency vs V\_IN for I\_LOAD = 100mA, L = 22µH**



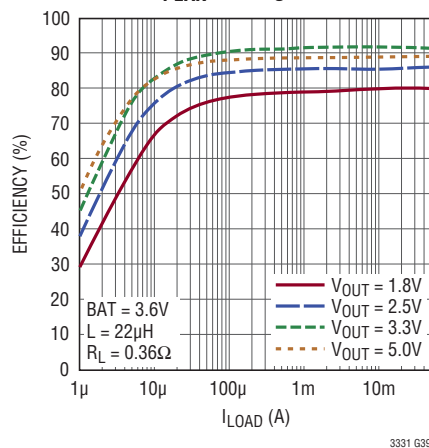
**Buck Efficiency vs V\_IN for I\_LOAD = 100mA, L = 100µH**



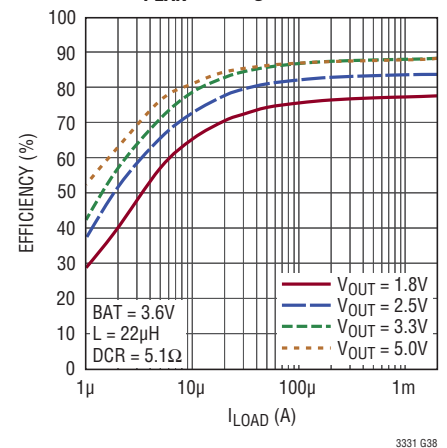
**Buck Efficiency vs V\_IN, for V\_OUT = 3.3V**



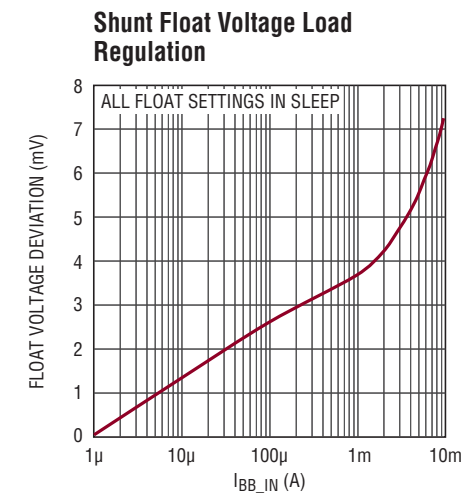
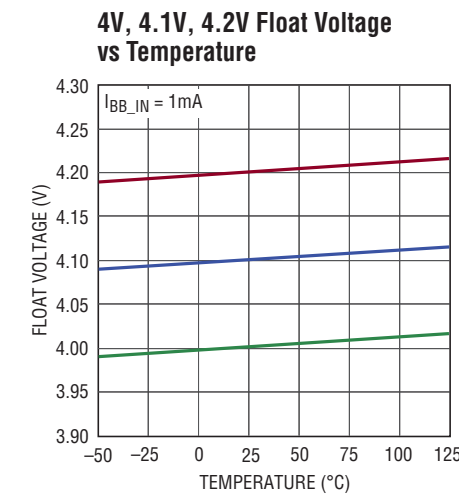
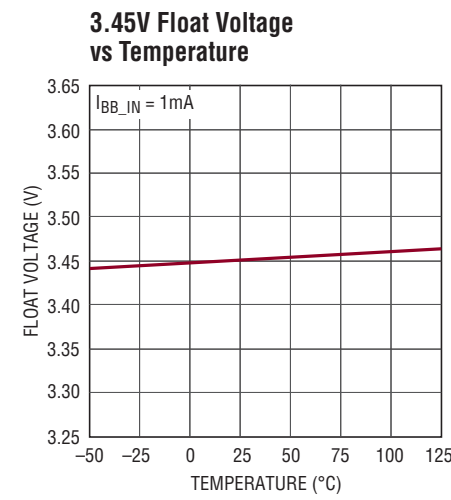
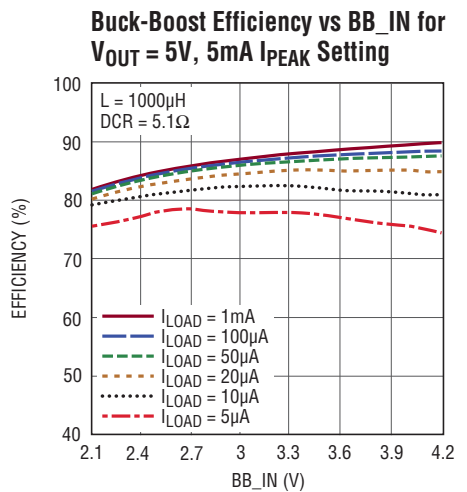
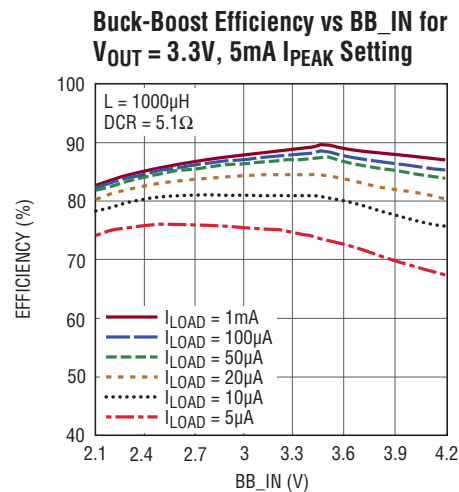
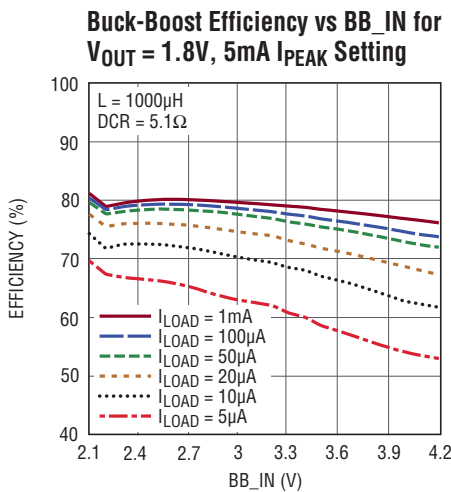
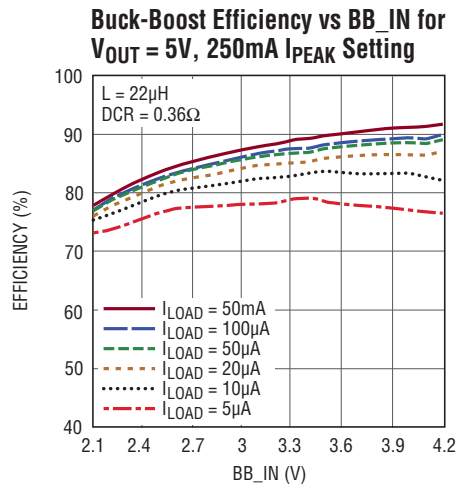
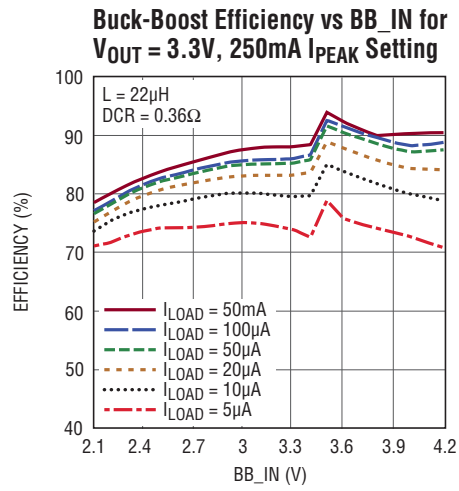
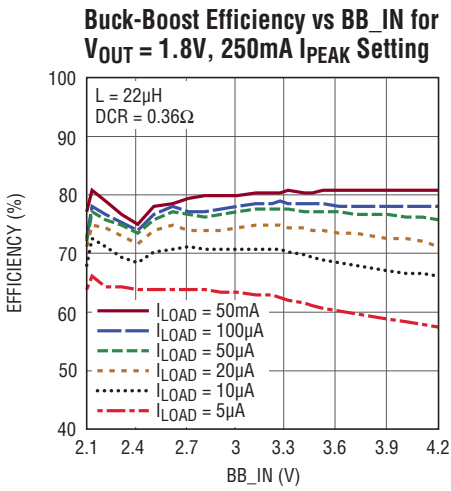
**Buck-Boost Efficiency vs I\_LOAD, 250mA I\_PEAK Setting**



**Buck-Boost Efficiency vs I\_LOAD, 5mA I\_PEAK Setting**

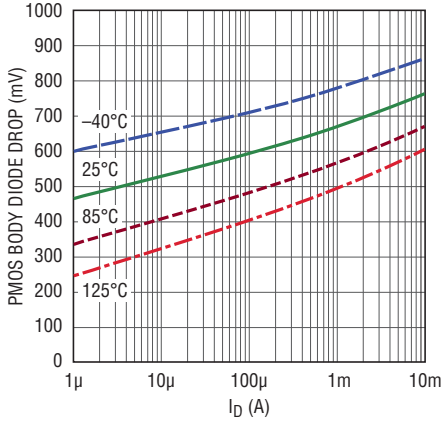


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.



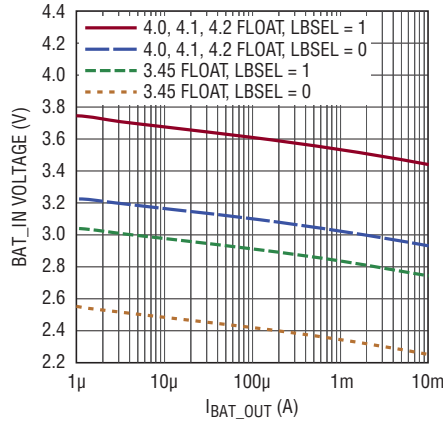
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Disconnect PMOS Body Diode Drop vs Current**



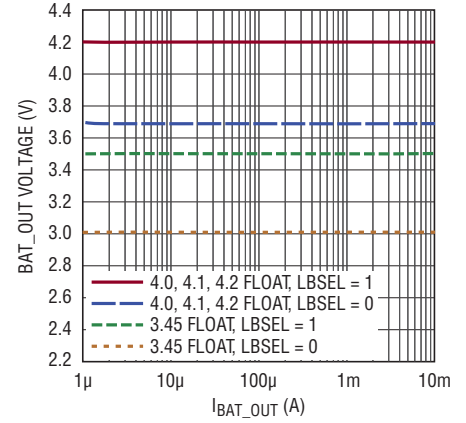
3331 G49

**Battery Connect Voltage at BAT\_IN vs  $I_{BAT\_OUT}$**



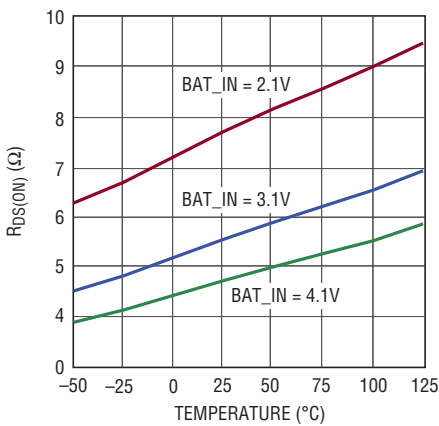
3331 G51

**Battery Connect Voltage at BAT\_OUT vs  $I_{BAT\_OUT}$**



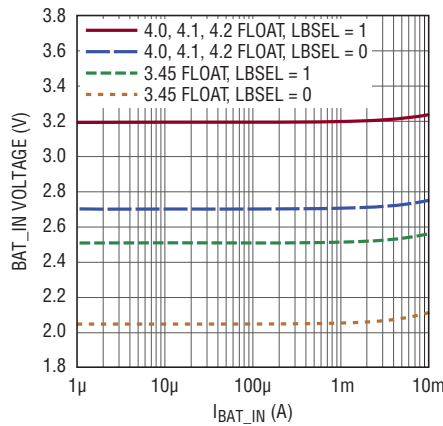
3331 G52

**$R_{DS(ON)}$  of Disconnect PMOS vs Temperature**



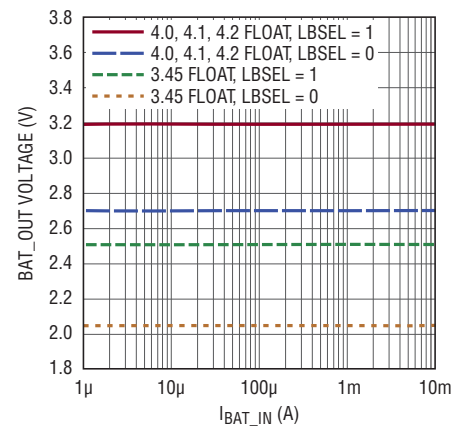
3331 G50

**Battery Disconnect Voltage at BAT\_IN vs  $I_{BAT\_IN}$**



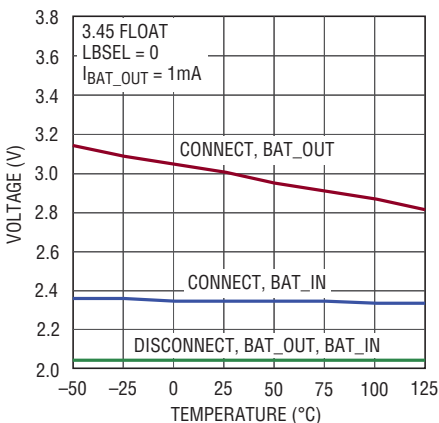
3331 G53

**Battery Disconnect Voltage at BAT\_OUT vs  $I_{BAT\_IN}$**



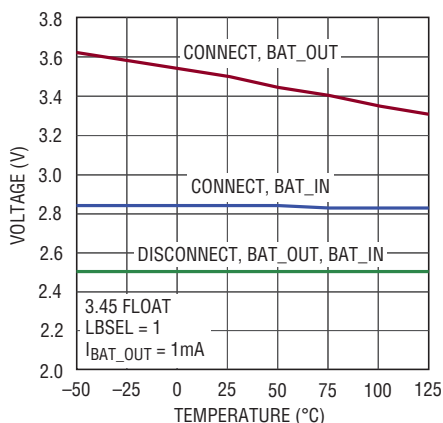
3331 G54

**Battery Connect/Disconnect vs Temperature**



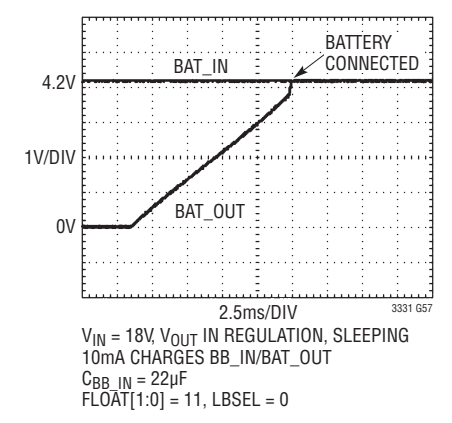
3331 G55

**Battery Connect/Disconnect vs Temperature**



3331 G56

**Battery Connect Transient**

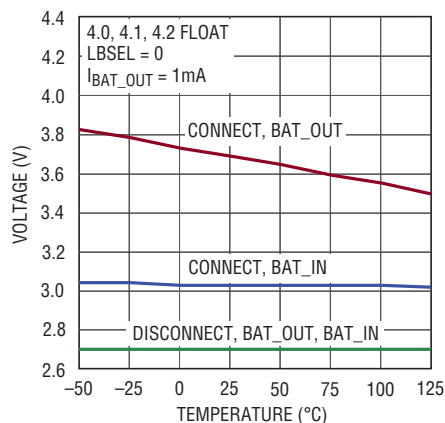


3331 G57

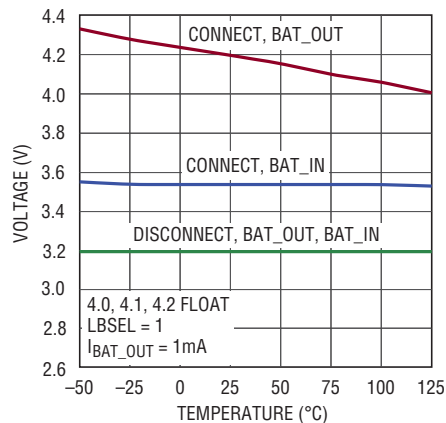
$V_{IN} = 18\text{V}$ ,  $V_{OUT}$  IN REGULATION, SLEEPING  
 $10\text{mA}$  CHARGES  $BB\_IN/BAT\_OUT$   
 $C_{BB\_IN} = 22\mu\text{F}$   
 $\text{FLOAT}[1:0] = 11$ ,  $\text{LBSEL} = 0$

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

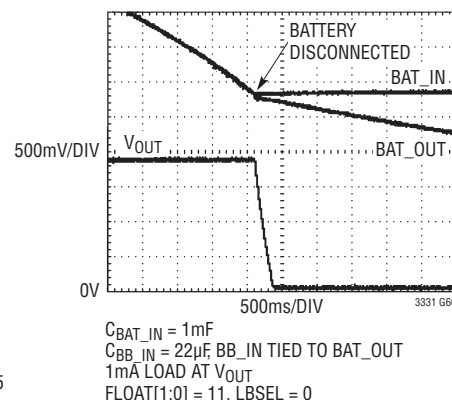
### Battery Connect/Disconnect vs Temperature



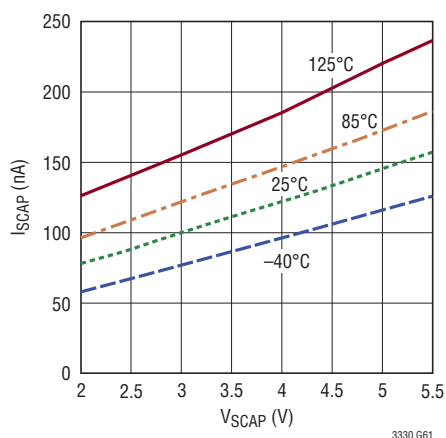
### Battery Connect/Disconnect vs Temperature



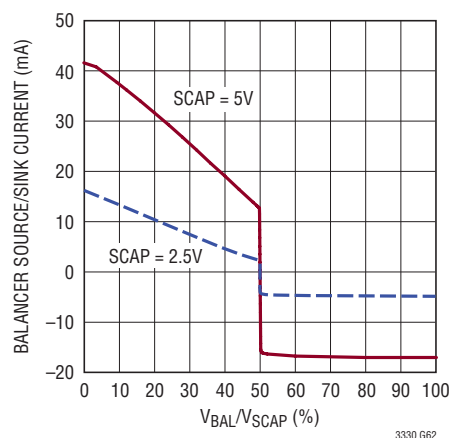
### Battery Connect Transient



### Supercapacitor Balancer Quiescent Current vs $V_{\text{SCAP}}$



### Supercapacitor Balancer Source/Sink Current



## PIN FUNCTIONS

**BAL (Pin 1):** Supercapacitor Balance Point. The common node of a stack of two supercapacitors is connected to BAL. A source/sink balancing current of up to 10mA is available. Tie BAL along with SCAP to GND to disable the balancer and its associated quiescent current.

**SCAP (Pin 2):** Supply and Input for Supercapacitor Balancer. Tie the top of a 2-capacitor stack to SCAP and the middle of the stack to BAL to activate balancing. Tie SCAP along with BAL to GND to disable the balancer and its associated quiescent current.

**$V_{\text{IN2}}$  (Pin 3):** Internal Low Voltage Rail to Serve as Gate Drive for Buck NMOS Switch. Connect a  $4.7\mu\text{F}$  (or larger) capacitor from  $V_{\text{IN2}}$  to GND. This pin is not intended for use as an external system rail.

**UV3, UV2, UV1, UV0 (Pins 4, 5, 6, 7):** UVLO Select Bits for the Buck Switching Regulator. Tie high to  $V_{\text{IN2}}$  or low to GND to select the desired UVLO rising and falling thresholds (see Table 4). The UVLO falling threshold must be greater than the selected  $V_{\text{OUT}}$  regulation level. Do not float.

## PIN FUNCTIONS

**AC1 (Pin 8):** Input Connection for piezoelectric element, other AC source, or current limited DC source (used in conjunction with AC2 for differential AC inputs).

**AC2 (Pin 9):** Input Connection for piezoelectric element, other AC source, or current limited DC source (used in conjunction with AC1 for differential AC inputs).

**V<sub>IN</sub> (Pin 10):** Rectified Input Voltage. A capacitor on this pin serves as an energy reservoir and input supply for the buck regulator. The V<sub>IN</sub> voltage is internally clamped to a maximum of 20V (typical).

**CAP (Pin 11):** Internal Rail Referenced to V<sub>IN</sub> to Serve as Gate Drive for Buck PMOS Switch. Connect a 1μF (or larger) capacitor between CAP and V<sub>IN</sub>. This pin is not intended for use as an external system rail.

**SW (Pin 12):** Switch Node for the Buck Switching Regulator. Connect a 22μH or greater external inductor between this node and V<sub>OUT</sub>.

**V<sub>OUT</sub> (Pin 13):** Regulated Output Voltage Derived from the Buck or Buck-Boost Switching Regulator.

**SWB (Pin 14):** Switch Node for the Buck-Boost Switching Regulator. Connect an external inductor (value in Table 3) between this node and SWA.

**SWA (Pin 15):** Switch Node for the Buck-Boost Switching Regulator. Connect an external inductor (value in Table 3) between this node and SWB.

**BB\_IN (Pin 16):** Input for the Buck-Boost Switching Regulator. BB\_IN must be tied to BAT\_OUT for proper operation.

**IPK0, IPK1, IPK2 (Pins 17, 18, 19):** I<sub>PEAK\_BB</sub> Select Bits for the Buck-Boost Switching Regulator. Tie high to V<sub>IN3</sub> or low to GND to select the desired I<sub>PEAK\_BB</sub> (see Table 3). Do not float.

**BAT\_OUT (Pin 20):** This is the output side of the battery disconnect switch. BAT\_OUT must be connected to BB\_IN to power the buck-boost regulator.

**BAT\_IN (Pin 21):** Input for backup battery and the input side to the battery disconnect switch. When the battery is disconnected there will be less than 10nA of quiescent current draw at BAT\_IN.

**LBSEL (Pin 22):** Low Battery Disconnect Select Pin. Connect LBSEL high to BB\_IN or low to GND to select the low battery disconnect level. See Table 2. Do not float.

**FLOAT1, FLOAT0 (Pins 23, 24):** Float Voltage Select Pins. Connect high to BB\_IN or low to GND to select battery float voltages of 3.45V, 4.0V, 4.1V, and 4.2V (see Table 2). Do not float.

**SHIP (Pin 25):** Input to select SHIP mode. Tie SHIP to at least 1.2V to select SHIP mode in which the battery disconnect switch will be forced off, ensuring there is no drain on the battery. Do not float.

**V<sub>IN3</sub> (Pin 26):** Internal Low Voltage Rail Used by the Prioritizer. Logic high reference for IPK[2:0] and OUT[2:0]. Connect a 0.1μF capacitor from V<sub>IN3</sub> to GND. This pin is not intended for use as an external system rail.

**CHARGE (Pin 27):** Connect a resistor from CHARGE to the common BAT\_OUT = BB\_IN node to enable charging of the battery. The CHARGE pin is controlled to provide excess energy from the energy harvesting input when the output is in regulation and the BUCK converter is in SLEEP mode.

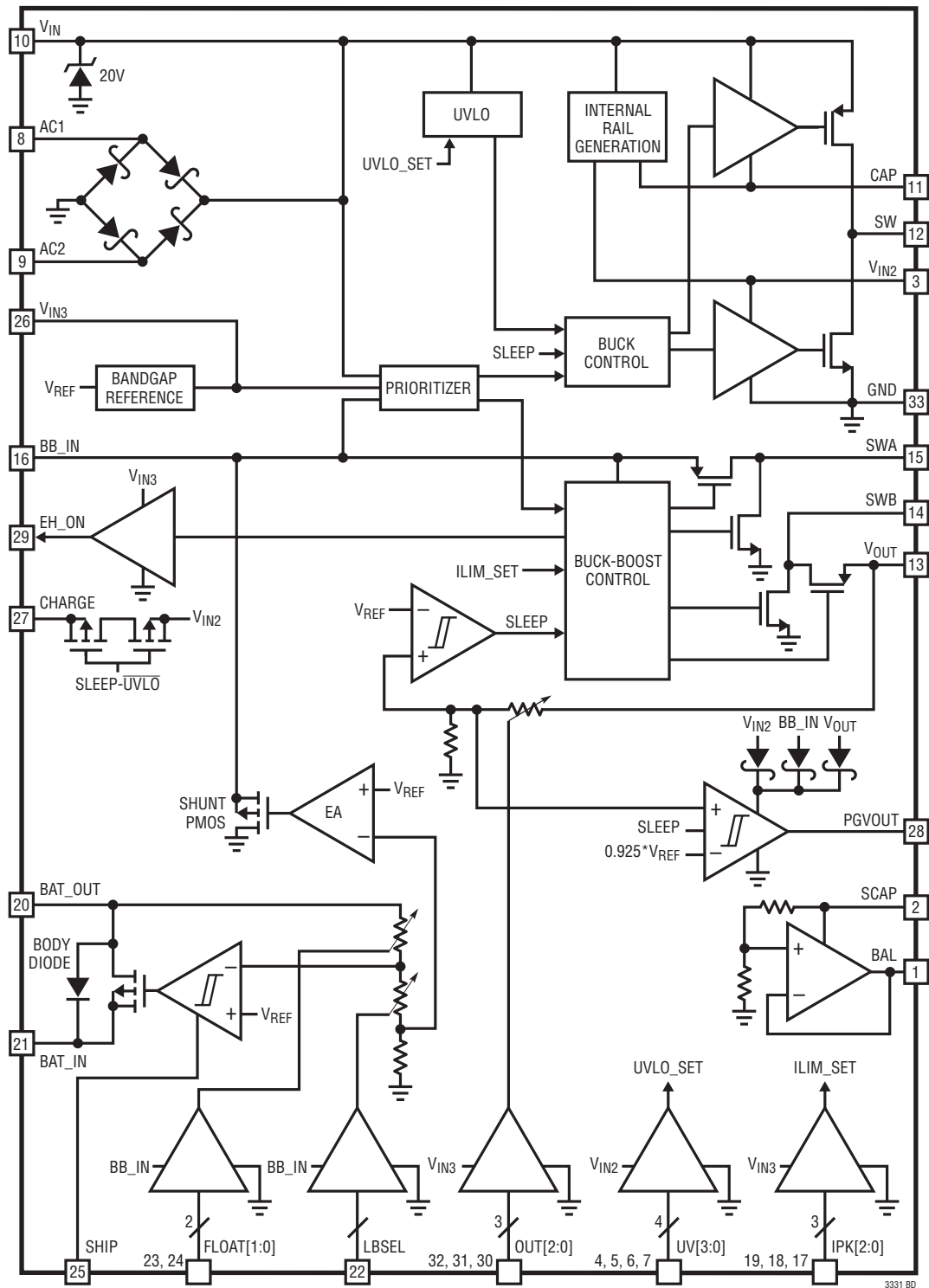
**PGVOUT (Pin 28):** Power Good Output for V<sub>OUT</sub>. Logic level output referenced to an internal maximum rail (see Operation). PGVOUT transitioning high indicates regulation has been reached on V<sub>OUT</sub> (V<sub>OUT</sub> = Sleep Rising). PGVOUT remains high until V<sub>OUT</sub> falls to 92% (typical) of the programmed regulation point.

**EH\_ON (Pin 29):** Switcher Status. Logic level output referenced to V<sub>IN3</sub>. EH\_ON is high when the buck switching regulator is in use (energy harvesting input). It is pulled low when the buck-boost switching regulator is in use (battery input).

**OUT0, OUT1, OUT2 (Pins 30, 31, 32):** V<sub>OUT</sub> Voltage Select Bits. Tie high to V<sub>IN3</sub> or low to GND to select the desired V<sub>OUT</sub> (see Table 1). Do not float.

**GND (Exposed Pad Pin 33):** Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3331.

# BLOCK DIAGRAM



3331 BD

## OPERATION

### Modes of Operation

The following four tables detail all programmable settings on the LTC3331.

**Table 1. Output Voltage Selection**

OUT2	OUT1	OUT0	V <sub>OUT</sub>
0	0	0	1.8V
0	0	1	2.5V
0	1	0	2.8V
0	1	1	3.0V
1	0	0	3.3V
1	0	1	3.6V
1	1	0	4.5V
1	1	1	5.0V

**Table 2. FLOAT Selection**

LBSEL	FLOAT1	FLOAT0	FLOAT	CONNECT	DISCONNECT
0	0	0	3.45V	2.35V	2.04V
0	0	1	4.0V	3.03V	2.70V
0	1	0	4.1V	3.03V	2.70V
0	1	1	4.2V	3.03V	2.70V
1	0	0	3.45V	2.85V	2.51V
1	0	1	4.0V	3.53V	3.20V
1	1	0	4.1V	3.53V	3.20V
1	1	1	4.2V	3.53V	3.20V

**Table 3. I<sub>PEAK\_BB</sub> Selection**

IPK2	IPK1	IPK0	I <sub>LIM</sub>	L <sub>MIN</sub>
0	0	0	5mA	1000μH
0	0	1	10mA	470μH
0	1	0	15mA	330μH
0	1	1	25mA	220μH
1	0	0	50mA	100μH
1	0	1	100mA	47μH
1	1	0	150mA	33μH
1	1	1	250mA	22μH

**Table 4. UVLO Selection**

UV3	UV2	UV1	UV0	UVLO RISING	UVLO FALLING
0	0	0	0	4V	3V
0	0	0	1	5V	4V
0	0	1	0	6V	5V
0	0	1	1	7V	6V
0	1	0	0	8V	7V
0	1	0	1	8V	5V
0	1	1	0	10V	9V
0	1	1	1	10V	5V
1	0	0	0	12V	11V
1	0	0	1	12V	5V
1	0	1	0	14V	13V
1	0	1	1	14V	5V
1	1	0	0	16V	15V
1	1	0	1	16V	5V
1	1	1	0	18V	17V
1	1	1	1	18V	5V



## OPERATION

### Overview

The LTC3331 combines a buck switching regulator and a buck-boost switching regulator to produce an energy harvesting solution with battery backup. The converters are controlled by a prioritizer that selects which converter to use based on the availability of a battery and/or harvestable energy. If harvested energy is available the buck regulator is active and the buck-boost is OFF. An onboard 10mA shunt battery charger with low battery disconnect enables charging of the backup battery to greatly extend the life of the battery. An optional supercapacitor balancer allows for significant energy storage at the output to handle a variety of load requirements.

### Energy Harvester

The energy harvester is an ultralow quiescent current power supply designed to interface directly to a piezoelectric or alternative A/C power source, rectify the input voltage, and store harvested energy on an external capacitor while maintaining a regulated output voltage. It can also bleed off any excess input power via an internal protective shunt regulator. It consists of an internal bridge rectifier, an undervoltage lockout circuit, and a synchronous buck DC/DC.

### Internal Bridge Rectifier

An internal full-wave bridge rectifier accessible via the differential AC1 and AC2 inputs rectifies AC sources such as those from a piezoelectric element. The rectified output is stored on a capacitor at the  $V_{IN}$  pin and can be used as an energy reservoir for the buck converter. The bridge rectifier has a total drop of about 800mV at typical piezo-generated currents ( $\sim 10\mu\text{A}$ ), but is capable of carrying up to 50mA. Either side of the bridge can be operated independently as a single-ended AC or DC input.

### Buck Undervoltage Lockout (UVLO)

When the voltage on  $V_{IN}$  rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled. These thresholds can be set according to Table 4 which

offers UVLO rising thresholds from 4V to 18V with large or small hysteresis windows. This allows for programming of the UVLO window near the peak power point of the input source. Extremely low quiescent current (450nA typical) in UVLO allows energy to accumulate on the input capacitor in situations where energy must be harvested from low power sources.

### Internal Rail Generation (CAP, $V_{IN2}$ , $V_{IN3}$ )

Two internal rails, CAP and  $V_{IN2}$ , are generated from  $V_{IN}$  and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the  $V_{IN2}$  rail serves as logic high for the UVLO threshold select bits UV[3:0]. The  $V_{IN2}$  rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below  $V_{IN}$ . These are not intended to be used as external rails. Bypass capacitors are connected to the CAP and  $V_{IN2}$  pins to serve as energy reservoirs for driving the buck switches. When  $V_{IN}$  is below 4.8V,  $V_{IN2}$  is equal to  $V_{IN}$  and CAP is held at GND. Figure 1 shows the ideal  $V_{IN}$ ,  $V_{IN2}$  and CAP relationship.

$V_{IN3}$  is an internal rail used by the buck and the buck-boost. When the LTC3331 runs the buck  $V_{IN3}$  will be a Schottky diode drop below  $V_{IN2}$ . When it runs the buck-boost  $V_{IN3}$  is equal to  $BB\_IN$ .

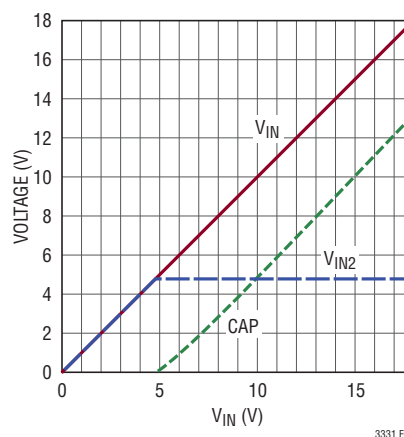


Figure 1. Ideal  $V_{IN}$ ,  $V_{IN2}$  and CAP Relationship

### Buck Operation

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the  $V_{OUT}$  sense pin. The buck converter charges an output

## OPERATION

capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to  $I_{PEAK\_BUCK}$  through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by  $V_{IN}$ ,  $V_{OUT}$ , and the inductor value. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During sleep load current is provided by the output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains the output at light loads. The buck delivers a minimum of 100mA of average load current when it is switching.  $V_{OUT}$  can be set from 1.8V to 5V via the output voltage select bits,  $OUT[2:0]$  (see Table 1).

When the sleep comparator senses that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still flowing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode. Instead, the NMOS switch is kept on to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero.

Though the quiescent current when the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when sufficient energy has been accumulated in the input capacitor and the length of time the converter needs to transfer energy to the output is much less than the time it takes to accumulate energy. Thus, the buck operating quiescent current is averaged over a long period of time so that the total average quiescent current is low. This feature accommodates sources that harvest small amounts of ambient energy.

### Buck-Boost Converter

The buck-boost uses the same hysteretic voltage algorithm as the buck to control the output,  $V_{OUT}$ , with the same sleep comparator. The buck-boost has three modes of operation: buck, buck-boost, and boost. An internal mode comparator determines the mode of operation based on  $BB\_IN$  and  $V_{OUT}$ . Figure 2 shows the four internal switches of the buck-boost converter. In each mode the inductor current is ramped up to  $I_{PEAK\_BB}$ , which is programmable via the  $IPK[2:0]$  bits and ranges from 5mA to 250mA (see Table 3).

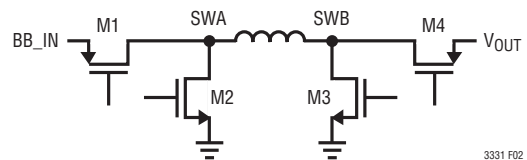


Figure 2: Buck-Boost Power Switches

In BUCK mode M4 is always on and M3 is always off. The inductor current is ramped up through M1 to  $I_{PEAK\_BB}$  and down to 0mA through M2. In boost mode M1 is always on and M2 is always off. The inductor current is ramped up to  $I_{PEAK\_BB}$  when M3 is on and is ramped down to 0mA when M4 is on as  $V_{OUT}$  is greater than  $BB\_IN$  in boost mode. Buck-boost mode is very similar to boost mode in that M1 is always on and M2 is always off. If  $BB\_IN$  is less than  $V_{OUT}$  the inductor current is ramped up to  $I_{PEAK\_BB}$  through M3. When M4 turns on the current in the inductor will start to ramp down. However, because  $BB\_IN$  is close to  $V_{OUT}$  and M1 and M4 have finite on-resistance the current ramp will exhibit a slow exponential decay, potentially lowering the average current delivered to  $V_{OUT}$ . For this reason the lower current threshold is set to  $I_{PEAK\_BB}/2$  in buck-boost mode to maintain high average current to the load. If  $BB\_IN$  is greater than  $V_{OUT}$  in buck-boost mode the inductor current still ramps up to  $I_{PEAK\_BB}$  and down to  $I_{PEAK\_BB}/2$ . It can still ramp down if  $BB\_IN$  is greater than  $V_{OUT}$  because the final value of the current in the inductor would be  $(V_{IN} - V_{OUT}) / (R_{ON1} + R_{ON4})$ . If  $BB\_IN$  is exactly  $I_{PEAK\_BB}/2 \cdot (R_{ON1} + R_{ON4})$  above  $V_{OUT}$  the inductor current will not reach the  $I_{PEAK\_BB}/2$  threshold and switches M1 and M4 will stay on all the time. For higher  $BB\_IN$  voltages the mode comparator will switch the converter to buck mode. M1 and M4 will remain on for  $BB\_IN$  voltages up to  $V_{OUT} + I_{PEAK\_BB} \cdot (R_{ON1} + R_{ON4})$ . At

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this point the current in the inductor is equal to  $I_{PEAK\_BB}$  and the  $I_{PEAK\_BB}$  comparator will trip turning off M1 and turning on M2 causing the inductor current to ramp down to  $I_{ZERO}$ , completing the transition from buck-boost mode to buck mode.

### V<sub>OUT</sub> Power Good

A power good comparator is provided for the V<sub>OUT</sub> output. It transitions high the first time the LTC3331 goes to sleep, indicating that V<sub>OUT</sub> has reached regulation. It transitions low when V<sub>OUT</sub> falls to 92% (typical) of its regulation value. The PGVOUT output is referenced to an internal rail that is generated to be the highest of V<sub>IN2</sub>, BB\_IN, and V<sub>OUT</sub> less a Schottky diode drop.

### Shunt Battery Charger

The LTC3331 provides a reliable low quiescent current shunt battery charger to facilitate charging a battery with harvested energy. A low battery disconnect feature provides protection to the battery from overdischarge by disconnecting the battery from the buck-boost input at a programmable level.

To use the charger connect the battery to the BAT\_IN pin. An internal low battery disconnect PMOS switch is connected between the BAT\_IN pin and the BAT\_OUT pin. The BAT\_OUT pin must be connected to BB\_IN for proper operation. A charging resistor connected from V<sub>IN</sub> to BAT\_OUT or from CHARGE to BAT\_OUT will charge the battery through the body diode of the disconnect PMOS until the battery voltage rises above the low-battery connect threshold. Depending on the capacity of the battery and the input decoupling capacitor, the common BAT\_OUT = BB\_IN node voltage generally rises or falls to V<sub>BAT\_IN</sub> when the PMOS turns on. Once the PMOS is on the charge current is determined by the charging resistor, the battery voltage, and the voltage of the charging source.

As the battery voltage approaches the float voltage, the LTC3331 shunts current away from the battery thereby reducing the charging current. The LTC3331 can shunt up to 10mA. Float voltages of 3.45V, 4.0V, 4.1V, and 4.2V are programmable via the FLOAT[1:0] pins (see Table 2).

Charging can occur through a resistor connected to V<sub>IN</sub> or the CHARGE pin. An internal set of back to back PMOS

switches are connected between CHARGE and V<sub>IN2</sub> and are turned on only when the energy harvesting buck converter is sleeping. In this way charging of the battery only happens when there is excess harvested energy available and the V<sub>OUT</sub> output is prioritized over charging of the battery. The charge current available from this pin is limited by the strength of the V<sub>IN2</sub> LDO and an appropriate charging resistor must be selected to limit this current. The on resistance of the internal charge switches combined is approximately 60Ω. To charge with higher currents connect a resistor directly to V<sub>IN</sub>. Note that when charging from V<sub>IN</sub> the battery is always being charged. Care must be taken to ensure that enough power is available to bring up the V<sub>OUT</sub> output.

### Low Battery Disconnect/Connect: LBD/LBC

The low battery disconnect (V<sub>LBD</sub>) and connect (V<sub>LBC</sub>) voltage levels are programmed by the LBSEL and FLOAT[1:0] pins (see Table 2). As shown in the Block Diagram the battery disconnects from the common BAT\_OUT = BB\_IN node by shutting off the PMOS switch when the BAT\_IN voltage falls below V<sub>LBD</sub>. This disconnect function protects Li-Ion batteries from permanent damage due to deep discharge. Disconnecting the battery from the common BAT\_OUT = BB\_IN node prevents the load as well as the LTC3331 quiescent current from further discharging the battery.

Once disconnected the common BAT\_OUT = BB\_IN node voltage collapses towards ground. When an input supply is reconnected the battery charges through the internal body diode of the disconnect PMOS. The input supply voltage should be larger than V<sub>LBC\_BAT\_OUT</sub> to ensure that the PMOS is turned on. When the voltage reaches V<sub>LBC\_BAT\_OUT</sub>, the PMOS turns on and connects the common BAT\_OUT = BB\_IN node to BAT\_IN. While disconnected, the BAT\_IN pin voltage is indirectly sensed through the PMOS body diode. Therefore V<sub>LBC\_BAT\_IN</sub> varies with charge current and junction temperature. See the Typical Performance Characteristics section for more information.

### Low Battery Select

The low battery disconnect voltage level is programmed by the LBSEL pin for each float setting. The LBSEL pin allows the user to trade-off battery run time and maximum shelf life. A lower battery disconnect threshold maximizes run

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time by allowing the battery to fully discharge before the disconnect event. Conversely, by increasing the low battery disconnect threshold more capacity remains following the disconnect event which extends the shelf life of the battery. For maximum run time, tie LBSEL to GND. For extended shelf life, tie LBSEL to the common BAT\_OUT = BB\_IN node. If a high peak current event is expected, users may temporarily select the lower disconnect threshold. This avoids disconnecting the battery too early when the load works against the battery series resistance and temporarily reduces the common BAT\_OUT = BB\_IN node.

### Ship Mode

A ship mode is provided which manually disconnects the battery. This may be useful to prevent discharge of the battery in situations when no harvestable energy is expected for a long period of time such as during shipping. Bring the SHIP pin high to engage ship mode. The low battery disconnect PMOS will turn off, disconnecting the battery at BAT\_IN from the common BAT\_OUT = BB\_IN node. If no harvestable energy is present to hold up the common BAT\_OUT = BB\_IN node that voltage will collapse. Typically an additional 1 $\mu$ A of quiescent current will appear on BB\_IN while SHIP mode is engaged.

To exit SHIP mode first bring the SHIP pin low. If the BB\_IN voltage had collapsed while in SHIP mode it must now be brought above the LBC threshold to reconnect the battery. This can be done manually or from an energy harvesting charging source. If harvestable energy had been propping up the common BAT\_OUT = BB\_IN node voltage above the LBC threshold then the battery will be connected immediately.

### Prioritizer

The input prioritizer on the LTC3331 decides whether to use the energy harvesting input or the battery input to power V<sub>OUT</sub>. If a battery is powering the buck-boost converter and harvested energy causes a UVLO rising transition on V<sub>IN</sub>, the prioritizer will shut off the buck-boost and turn on the buck, orchestrating a smooth transition that maintains regulation of V<sub>OUT</sub>.

When harvestable energy disappears, the prioritizer will first poll the BB\_IN voltage. If the BB\_IN voltage is above 1.8V the prioritizer will switch back to the buck-boost while maintaining regulation. If the BB\_IN voltage is below 1.8V the buck-boost is not enabled and V<sub>OUT</sub> cannot be supported until harvestable energy is again available. If the battery is connected then the BB\_IN voltage will be above 1.8V for every float and LBSEL combination. If the battery is disconnected the BB\_IN voltage will have collapsed below 1.8V and the prioritizer will not switch to the buck-boost when harvestable energy goes away. In the event that the battery is depleted and is disconnected while powering the buck-boost the prioritizer will not switch back to V<sub>IN</sub> until harvested energy is again available.

If either BB\_IN or V<sub>IN</sub> is grounded, the prioritizer allows the other input to run if its input is high enough for operation. The specified quiescent current in UVLO is valid upon start-up of the V<sub>IN</sub> input and when the battery has taken over regulation of the output. If the battery is less than 1.8V when UVLO is entered and the prioritizer does not enable the buck-boost several hundred nanoamperes of additional quiescent current will appear on V<sub>IN</sub>.

When the prioritizer selects the V<sub>IN</sub> input the current on the BB\_IN input drops to 200nA. However, if the voltage on BB\_IN is higher than V<sub>IN2</sub>, a fraction of the V<sub>IN</sub> quiescent current will appear on BB\_IN due to internal level shifting. This only affects a small range of battery voltages and UVLO settings.

A digital output, EH\_ON, is low when the prioritizer has selected the BB\_IN input and is high when the prioritizer has selected the V<sub>IN</sub> input. The EH\_ON output is referenced to V<sub>IN3</sub>.

### Supercapacitor Balancer

An integrated supercapacitor balancer with 150nA of quiescent current is available to balance a stack of two supercapacitors. Typically the input, SCAP, will tie to V<sub>OUT</sub> to allow for increased energy storage at V<sub>OUT</sub> with supercapacitors. The BAL pin is tied to the middle of the stack and can source and sink 10mA to regulate the BAL pin's voltage to half that of the SCAP pin's voltage. To disable the balancer and its associated quiescent current the SCAP and BAL pins can be tied to ground.

## APPLICATIONS INFORMATION

The LTC3331 allows for energy harvesting from a variety of alternative energy sources in order to power a wireless sensor system and charge a battery. The extremely low quiescent current of the LTC3331 facilitates harvesting from sources generating only microamps of current. The onboard bridge rectifier is suitable for AC piezoelectric or electromagnetic sources as well as providing reverse protection for DC sources such as solar and thermoelectric generators. The LTC3331 powers the  $V_{OUT}$  output continuously by seamlessly switching between the energy harvesting and battery inputs.

When harvestable energy is available, it is transferred through the bridge rectifier where it accumulates on the  $V_{IN}$  capacitor. A low quiescent current UVLO mode allows the voltage on the capacitor to increase towards a programmed UVLO rising threshold. When the voltage rises to this level, the buck converter turns on and transfers energy to  $V_{OUT}$ . As energy is transferred the voltage at  $V_{IN}$  may decrease to the UVLO falling threshold. If this happens, the buck converter turns off and the buck-boost then turns on to service the load from the battery input while more energy is harvested. When the buck is running the quiescent current on the BB\_IN pin drops to the 200nA required by the shunt battery charger.

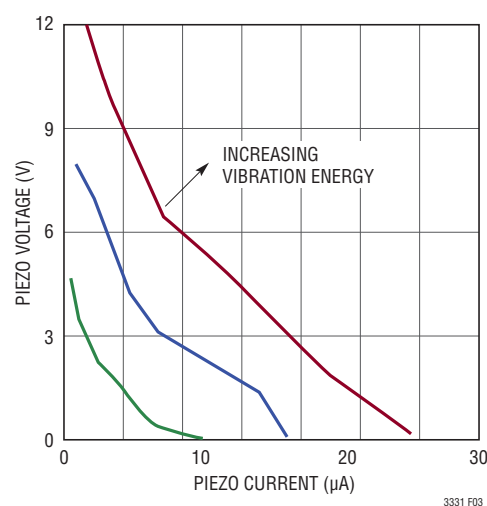
The LTC3331 is well suited to wireless systems which consume low average power but occasionally need a higher concentrated burst of power to accomplish a task. If these bursts occur with a low duty cycle such that the total energy needed for a burst can be accumulated between bursts then the output can be maintained entirely by the harvester. If the bursts need to happen more frequently or if harvestable energy goes away the battery will be used. If enough energy is available the energy harvester will bring the output up and enter the low quiescent current sleep state and excess energy can be used to charge the battery.

### Piezo Energy Harvesting

Ambient vibrational energy can be harvested with a piezoelectric transducer which produces a voltage and current in response to strain. Common piezoelectric elements are PZT (lead zirconate titanate) ceramics, PVDF

(polyvinylidene fluoride) polymers, or other composites. Ceramic piezoelectric elements exhibit a piezoelectric effect when the crystal structure of the ceramic is compressed and internal dipole movement produces a voltage. Polymer elements comprised of long-chain molecules produce a voltage when flexed as molecules repel each other. Ceramics are often used under direct pressure while a polymer is commonly used as a cantilevered beam.

A wide range of piezoelectric elements are available and produce a variety of open-circuit voltages and short-circuit currents. Typically the open-circuit voltage and short-circuit currents increase with available vibrational energy as shown in Figure 3. Piezoelectric elements can be placed in series or in parallel to achieve desired open-circuit voltages.



**Figure 3. Typical Piezoelectric Load Lines for Piezo Systems T220-A4-503X**

Piezos produce the most power when they operate at approximately half the open circuit voltage for a given vibration level. The UVLO window can be programmed to straddle this voltage so that the piezo operates near the peak power point. In addition to the normal configuration of connecting the piezo across the AC1 and AC2 inputs, a piezo can be connected from either AC1 or AC2 to ground. The resulting configuration is a voltage doubler as seen in Figure 4 where the intrinsic capacitance of the piezo is used as the doubling capacitor.

## APPLICATIONS INFORMATION

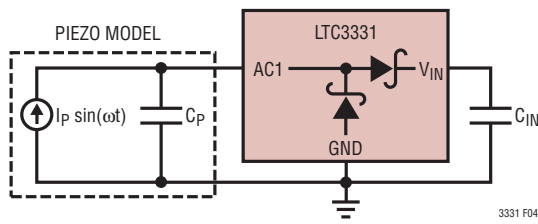


Figure 4. LTC3331 Voltage Doubler Configuration

A second piezo may be connected from AC2 to ground. This may be of use if the second piezo is mechanically tuned to a different resonant frequency present in the system than the first piezo. To achieve maximum power transfer from the piezo with the doubler the UVLO window should be set to the open circuit voltage of the piezo.

Piezoelectric elements are available from the manufacturers listed in Table 5.

Table 5. Piezoelectric Element Manufacturers

Advanced Cerametrics	<a href="http://www.advancedcerametrics.com">www.advancedcerametrics.com</a>
Piezo Systems	<a href="http://www.piezo.com">www.piezo.com</a>
Measurement Specialties	<a href="http://www.meas-spec.com">www.meas-spec.com</a>
PI (Physik Instrumente)	<a href="http://www.pi-usa.us">www.pi-usa.us</a>
MIDE Technology Corporation	<a href="http://www.mide.com">www.mide.com</a>
Morgan Technical Ceramics	<a href="http://www.morganelectroceramics.com">www.morganelectroceramics.com</a>

### Electromagnetic Energy Harvesting

Another alternative AC source is an electromagnetic vibration harvester in which a magnet vibrating inside a coil induces an AC voltage and current in the coil that can then be rectified and harvested by the LTC3331. The vibration could be ambient to the system or it could be caused by an impulse as in a spring loaded switch.

### Solar Energy Harvesting

The LTC3331 can harvest solar energy as the bridge rectifier can be used to provide reverse protection for a solar panel. A solar cell produces current in proportion to the amount of light falling on it. Figure 5 shows the relationship between current and voltage for a solar panel illuminated with several levels of light. The maximum power output occurs near the knee of each curve where the cell transitions from a constant current device to a constant voltage

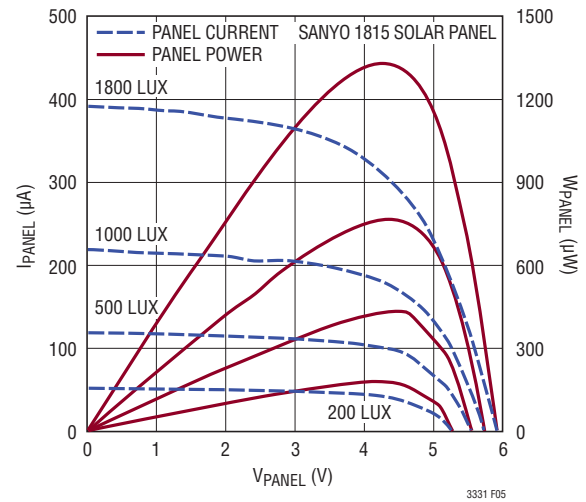


Figure 5. Typical Solar Panel Characteristics

device. Fortunately, the peak power point doesn't change much with illumination and an appropriate UVLO window can be selected so that the panel operates near the peak power point for a majority of light conditions.

Two solar panels can be connected to the LTC3331, one from AC1 to ground and another from AC2 to ground. Each panel could be aimed in a different direction to capture light from different angles or at different times of the day as the sun moves. The panels should be similar so that the selected UVLO window is optimal for both panels.

### BB\_IN/BAT\_OUT, BAT\_IN, V\_IN, and V\_OUT Capacitors

The input to the buck-boost, BB\_IN, must be connected to BAT\_OUT for proper operation. BAT\_OUT is the output side of the low battery disconnect switch. The series resistance of this switch must be considered when selecting a bypass capacitor for the common BAT\_OUT = BB\_IN node. At least 4.7μF to GND or greater should be used. For the higher I<sub>PEAK\_BB</sub> settings the capacitor may need to be larger to smooth the voltage at the common BAT\_OUT = BB\_IN node. The goal is to average the input current to the buck boost so that the voltage droop at the common BAT\_OUT = BB\_IN node is minimized.

A bypass capacitor of 1μF or greater can also be placed at the BAT\_IN pin. In cases where the series resistance of the battery is high, a larger capacitor may be desired to handle transients.

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The input capacitor to the buck on  $V_{IN}$  and the  $V_{OUT}$  capacitor can vary widely and should be selected to optimize the use of an energy harvesting source depending on whether storage of the harvested energy is needed at the input or the output. Storing energy at the input takes advantage of the high input voltage as the energy stored in a capacitor increases with the square of its voltage. Storage at the output may be necessary to handle load transients greater than the 100mA the buck can provide.

The input or output capacitor should be sized to store enough energy to provide output power for the length of time required. If enough energy is stored so that the buck does not reach the UVLO falling threshold during a load transient then the battery current will always be zero. Spacing load transients so that the average power required to service the application is less than or equal to the power available from the energy harvesting source will then greatly extend the life of the battery. The  $V_{IN}$  capacitor should be rated to withstand the highest voltage ever present at  $V_{IN}$ .

The following equation can be used to size the input capacitor to meet the power requirements of the output for the desired duration:

$$P_{LOAD} t_{LOAD} = \frac{1}{2} \eta C_{IN} (V_{IN}^2 - V_{UVLOFALLING}^2)$$

$$V_{UVLOFALLING} \leq V_{IN} \leq V_{SHUNT}$$

Here  $\eta$  is the average efficiency of the buck converter over the input voltage range and  $V_{IN}$  is the input voltage when the buck begins to switch. Typically  $V_{IN}$  will be the UVLO rising threshold. This equation may overestimate the input capacitor necessary as it may be acceptable to allow the load current to deplete the output capacitor all the way to the lower PGVOUT threshold. It also assumes that the input source charging has a negligible effect during this time.

The duration for which the buck or buck-boost regulator sleeps depends on the load current and the size of the  $V_{OUT}$  capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The DC sleep hysteresis window is  $\pm 6mV$  for the 1.8V output and scales linearly with the output voltage setting ( $\pm 12mV$

for the 3.6V setting, etc.). Ideally this means that the sleep time is determined by the following equation:

$$t_{SLEEP} = C_{OUT} \frac{12mV \cdot \frac{V_{OUT}}{1.8V}}{I_{LOAD}}$$

This is true for output capacitors on the order of 100 $\mu F$  or larger, but as the output capacitor decreases towards 10 $\mu F$ , delays in the internal sleep comparator along with the load current itself may result in the  $V_{OUT}$  voltage slewing past the DC thresholds. This will lengthen the sleep time and increase  $V_{OUT}$  ripple. A capacitor less than 10 $\mu F$  is not recommended as  $V_{OUT}$  ripple could increase to an undesirable level. If transient load currents above 100mA are required then a larger capacitor should be used at the output. This capacitor will be continuously discharged during a load condition and the capacitor can be sized for an acceptable drop in  $V_{OUT}$ :

$$C_{OUT} = (I_{LOAD} - I_{DC/DC}) \frac{t_{LOAD}}{V_{OUT+} - V_{OUT-}}$$

Here  $V_{OUT+}$  is the value of  $V_{OUT}$  when PGVOUT goes high and  $V_{OUT-}$  is the acceptable lower limit of  $V_{OUT}$ .  $I_{DC/DC}$  is the average current being delivered from either the buck converter or the buck-boost converter. The buck converter typically delivers 125mA on average to the output as the inductor current is ramped up to 250mA and down to zero. The current the buck-boost delivers depends on the mode of operation and the  $I_{PEAK\_BB}$  setting. In buck mode the deliverable current is  $I_{PEAK\_BB}/2$ . In buck-boost and boost modes the deliverable current also depends on the  $V_{IN}$  to  $V_{OUT}$  ratio:

$$\text{Buck-boost mode: } I_{DC/DC} = \frac{3}{4} I_{PEAK\_BB} \frac{V_{IN}}{V_{OUT}}$$

$$\text{Boost mode: } I_{DC/DC} = \frac{1}{2} I_{PEAK\_BB} \frac{V_{IN}}{V_{OUT}}$$

A standard surface mount ceramic capacitor can be used for  $C_{OUT}$ , though some applications may be better suited to a low leakage aluminum electrolytic capacitor or a supercapacitor. These capacitors can be obtained from manufacturers such as Vishay, Illinois Capacitor, AVX, or CAP-XX.

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### CAP, V<sub>IN2</sub>, and V<sub>IN3</sub> Capacitors

A 1μF or larger capacitor must be connected between V<sub>IN</sub> and CAP and a 4.7μF capacitor must be connected between V<sub>IN2</sub> and GND. These capacitors hold up the internal rails during buck switching and compensate the internal rail generation circuits. In applications where the voltage at V<sub>IN</sub> is limited to less than 6V, the CAP pin can be tied to GND and the V<sub>IN2</sub> pin can be tied to V<sub>IN</sub> as shown in Figure 6. An optional 5.6V Zener diode can be connected to V<sub>IN</sub> to clamp V<sub>IN</sub> in this scenario. The leakage of the Zener diode below its clamping voltage should be considered as it could be comparable to the quiescent current of the LTC3331. This circuit does not require the capacitors on V<sub>IN2</sub> and CAP, saving two components and allowing for a lower voltage rating for the single V<sub>IN</sub> capacitor.

A 0.1μF bypass capacitor must be connected from V<sub>IN3</sub> to ground. V<sub>IN3</sub> is an internal rail that is shared by both the buck and buck-boost. It is not intended for use as a system rail. It is used as a logic high reference level for the IPK[2:0] and OUT[2:0] digital inputs. In the event that these pins are dynamically driven in the application, external inverters may be needed and they must use V<sub>IN3</sub> as a rail. However, care must be taken not to overload V<sub>IN3</sub> and the quiescent current of such logic should be kept minimal. The output resistance of the V<sub>IN3</sub> pin is typically 15kΩ.

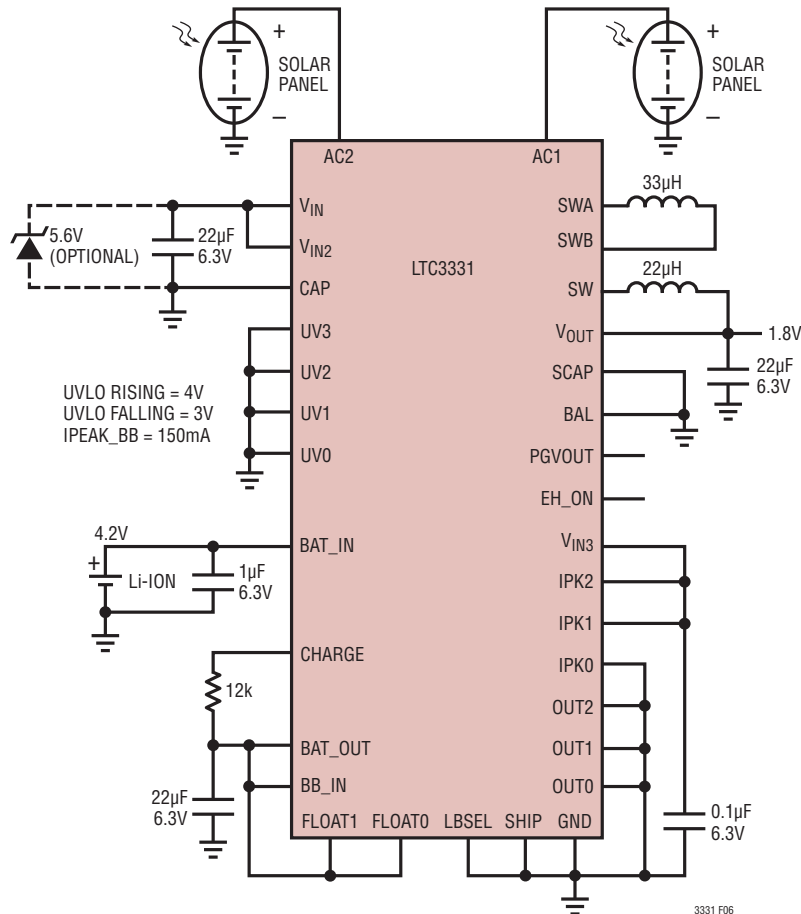


Figure 6. Low Voltage Solar Harvester with Reduced Component Count (V<sub>IN</sub> < 6V)



## APPLICATIONS INFORMATION

### Inductor Selection

The buck is optimized to work with a 22 $\mu$ H inductor in typical applications. A larger inductor will benefit high voltage applications by increasing the on-time of the PMOS switch and improving efficiency by reducing gate charge loss. Choose an inductor with a DC current rating greater than 500mA. The DCR of the inductor can have an impact on efficiency as it is a source of loss. Tradeoffs between price, size, and DCR should be evaluated.

The buck-boost is optimized to work with a minimum inductor of 22 $\mu$ H for the 250mA  $I_{PEAK\_BB}$  setting. For the other seven  $I_{PEAK\_BB}$  settings the inductor value should increase as the  $I_{PEAK\_BB}$  selection decreases to maintain the same  $I_{PEAK\_BB} \cdot L$  product. The minimum inductor values for the buck-boost for each  $I_{PEAK\_BB}$  setting are listed in Table 3. Larger inductors may increase efficiency. Choose an inductor with an  $I_{SAT}$  rating at least 50% greater than the selected  $I_{PEAK}$  value. Table 6 lists several inductors that work well with both the buck and the buck-boost.

**Table 6. Recommended Inductors for the LTC3331**

PART NUMBER	L( $\mu$ H)	MANUFACTURER	SIZE (mm) (L x W x H)	MAX IDC (mA)	MAX DCR ( $\Omega$ )
744043102	1000	Würth Elektronik	4.8 x 4.8 x 2.8	80	7
LPS5030-105ML		Coilcraft	5.51 x 5.51 x 2.9	110	5.1
LPS4018-105ML		Coilcraft	3.9 x 3.9 x 1.7	98	18
LPS3314-105ML		Coilcraft	3.3 x 3.3 x 1.3	99	31
B82442T1105K050		EPCOS	5.6 x 5 x 5	150	9.5
744043471	470	Würth Elektronik	4.8 x 4.8 x 2.8	125	2.6
LPS4018-474ML		Coilcraft	3.9 x 3.9 x 1.7	160	7.8
LPS3314-474ML		Coilcraft	3.3 x 3.3 x 1.3	110	12
B82442T147K050		EPCOS	5.6 x 5 x 5	240	4.73
744042331	330	Würth Elektronik	4.8 x 4.8 x 1.8	130	4.5
LPS4018-334ML		Coilcraft	3.9 x 3.9 x 1.7	190	5.9
LPS3314-334ML		Coilcraft	3.3 x 3.3 x 1.3	110	9.3
B82442T1334K050		EPCOS	5.6 x 5 x 5	280	3.29
744042221	220	Würth Elektronik	4.8 x 4.8 x 1.8	160	3.2
LPS4018-224ML		Coilcraft	3.9 x 3.9 x 1.7	260	3.7
LPS3314-224ML		Coilcraft	3.3 x 3.3 x 1.3	160	6
B82442T1224K050		EPCOS	5.6 x 5 x 5	330	2.2
744031101	100	Würth Elektronik	3.8 x 3.8 x 1.65	180	2.4
LPS4018-104ML		Coilcraft	3.9 x 3.9 x 1.7	360	1.4
LPS3314-104ML		Coilcraft	3.3 x 3.3 x 1.3	230	2.75
B82442T1104K050		EPCOS	5.6 x 5 x 5	510	0.99
744031470	47	Würth Elektronik	3.8 x 3.8 x 1.65	250	1
LPS4018-473ML		Coilcraft	3.9 x 3.9 x 1.7	550	0.65
LPS3314-473ML		Coilcraft	3.3 x 3.3 x 1.3	330	1.4
B82442T1473K050		EPCOS	5.6 x 5 x 5	700	0.519
744031330	33	Würth Elektronik	3.8 x 3.8 x 1.65	320	0.66
LPS4018-333ML		Coilcraft	3.9 x 3.9 x 1.7	640	0.42
LPS3314-333ML		Coilcraft	3.3 x 3.3 x 1.3	380	0.92
1070BS-330ML		Toko	3.2 x 3.2 x 2	230	0.61
B82442T1333K050		EPCOS	5.6 x 5 x 5	840	0.36
744031220	22	Würth Elektronik	3.8 x 3.8 x 1.65	360	0.45
LPS5030-223ML		Coilcraft	5.51 x 5.51 x 2.9	750	0.19
LPS4018-223ML		Coilcraft	3.9 x 3.9 x 1.7	800	0.36
LPS3314-223ML		Coilcraft	3.3 x 3.3 x 1.3	450	0.72
1070AS-220M		Toko	3.2 x 3.2 x 2	410	0.64
B82442T1223K050		EPCOS	5.6 x 5 x 5	1040	0.238
744029220	22	Würth Elektronik	2.8 x 2.8 x 1.35	300	0.97
1069BS-220M		Toko	3.2 x 3.2 x 1.8	290	0.495

## APPLICATIONS INFORMATION

### Supercapacitor Balancer

If supercapacitors are used at  $V_{OUT}$  the onboard supercapacitor balancer can be used to balance them with  $\pm 10\text{mA}$  of balance current. A list of supercapacitor suppliers is provided in Table 7.

**Table 7. Supercapacitor Manufacturers**

CAP-XX	www.cap-xx.com
NESS CAP	www.nesscap.com
Maxwell	www.maxwell.com
Bussman	www.cooperbussman.com
AVX	www.avx.com
Illinois Capacitor	www.illcap.com
Tecate Group	www.tecategroup.com

By seamlessly combining a battery source and an energy harvesting source, the LTC3331 enables the use of supercapacitors in energy harvesting applications. The battery provides the initial current required to overcome the effects of the diffusion current when voltage is first applied to the supercapacitors. The energy harvesting source can then support the lower steady state leakage current and average load current.

### Summary of Digital inputs and outputs

There are 14 digital pin-strapped logic inputs to the LTC3331 and two digital logic outputs. These and the rails they are referenced to are summarized in Table 8.

**Table 8. Digital Pin Summary**

INPUT PIN	LOGIC HIGH LEVEL
UV[3:0]	$V_{IN2}$
IPK[2:0]	$V_{IN3}$
OUT[2:0]	$V_{IN3}$
FLOAT[1:0], LBSEL	BAT_OUT = BB_IN
SHIP	$\geq 1.2\text{V}$

OUTPUT PIN	LOGIC HIGH LEVEL
PGVOUT	MAX (BB_IN, $V_{IN2}$ , $V_{OUT}$ )
EH_ON	$V_{IN3}$

### Battery Considerations

The shunt battery charger is designed to work with any single Li-Ion,  $\text{LiFePO}_4$ , or other chemistry with a termination voltage compatible with the available levels. Table 9 lists some batteries, their capacities and their equivalent series resistance (ESR). The ESR causes BAT\_OUT and BAT\_IN to droop by the product of the load current amplitude multiplied by the ESR. This droop may trigger the low battery disconnect while the battery itself may still have ample capacity. An appropriate bypass capacitor placed at BAT\_OUT will help prevent large, low duty cycle load transients from pulling down on BAT\_OUT. The bypass capacitor used at BB\_IN, which is tied to BAT\_OUT, to bypass the buck-boost may be sufficient.

**Table 9. Low Capacity Li-Ion and Thin-Film Batteries**

MANUFACTURER	P/N	CAPACITY	RESISTANCE	$V_{MIN}$
CYMBET	CBC012	12 $\mu\text{Ah}$	5k to 10k	3.0V
CYMBET	CBC050	50 $\mu\text{Ah}$	1500 $\Omega$ to 3k	3.0V
GM Battery	GMB031009	8mAh	10 $\Omega$ to 20 $\Omega$	2.75V
GS NanoTech	N/A	500 $\mu\text{Ah}$	40 $\Omega$	3.0V
Power Stream	LIR2032	40mAh	0.6 $\Omega$	3.0V

### Charging the Battery

Charging the battery with the CHARGE pin allows the battery to be charged only when the energy harvester is sleeping, which prioritizes the  $V_{OUT}$  output over the battery. The current that the CHARGE pin can supply is limited to 2mA and an appropriately chosen current limiting resistor should be used. Use the following equation to calculate the value of this resistor:

$$R_{\text{CHARGE}} = \frac{4.8\text{V} - V_{\text{LBD}}}{I_{\text{CHARGE}}} - 60\Omega$$

Here 4.8V is the output of the  $V_{IN2}$  LDO which is the supply to the CHARGE pin,  $V_{\text{LBD}}$  is the selected low battery disconnect threshold, 60 $\Omega$  is the resistance of the CHARGE pin PMOS, and  $I_{\text{CHARGE}}$  is the desired charge current. For high charging currents approaching 2mA, a larger  $V_{IN2}$  capacitor may improve transient behavior.



## APPLICATIONS INFORMATION

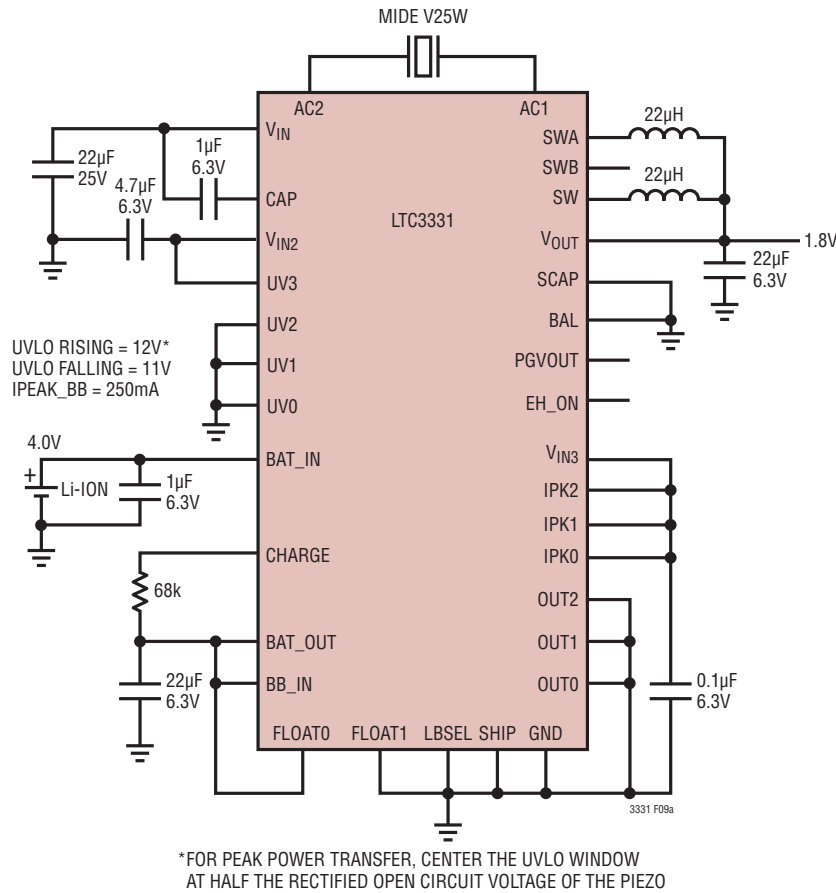


Figure 9a. Higher Efficiency Battery-Powered Buck Regulator

### Alternative Power Sources

The LTC3331 can accommodate a wide variety of input sources. Figure 10 shows the LTC3331 internal bridge rectifier connected to a 120V RMS AC line in series with four 3.9k current limiting resistors. This produces a peak current of 10mA with the LTC3331 shunt holding  $V_{IN}$  at 20V. This current may be increased by reducing the resistor values since the shunt can sink 25mA and the bridge is rated for 50mA. An optional external Zener diode (shown) may be required if the current exceeds 25mA. A transformer may also be used to step down the voltage and reduce the power loss in the current limiting resistors. The 3.3k charging resistor charges the battery from  $V_{IN}$  with approximately 5mA. This is a high voltage application and minimum spacing between the line, neutral, and any high voltage components should be maintained per the applicable UL specification. For general off-line applications refer to UL Regulation 1012.

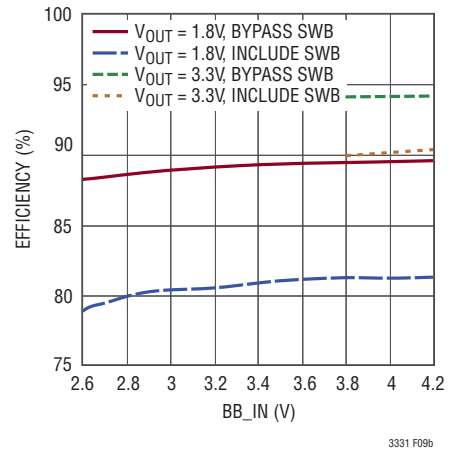


Figure 9b. Efficiency Comparison Between Normal Buck-Boost and Bypassed SWB Configuration

Figure 11 shows an application where copper panels are placed near a standard fluorescent room light to capacitively harvest energy from the electric field around the light. The frequency of the emission will be double the line frequency for magnetic ballasts but could be higher if the light uses electronic ballast. The peak AC voltage and the total available energy will scale with the size of the panels used and with the proximity of the panels to the electric field of the light.

The LTC3331 could also be used to wirelessly harvest energy and charge a battery by using a transmitter and receiver consisting of loosely coupled tuned resonant tanks as shown in Figure 12.

### Using EH\_ON to Program $V_{OUT}$

The EH\_ON output indicates whether the energy harvesting input or the battery is powering the output. The application

## APPLICATIONS INFORMATION

**DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS! BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS, USE CAUTION. ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.**

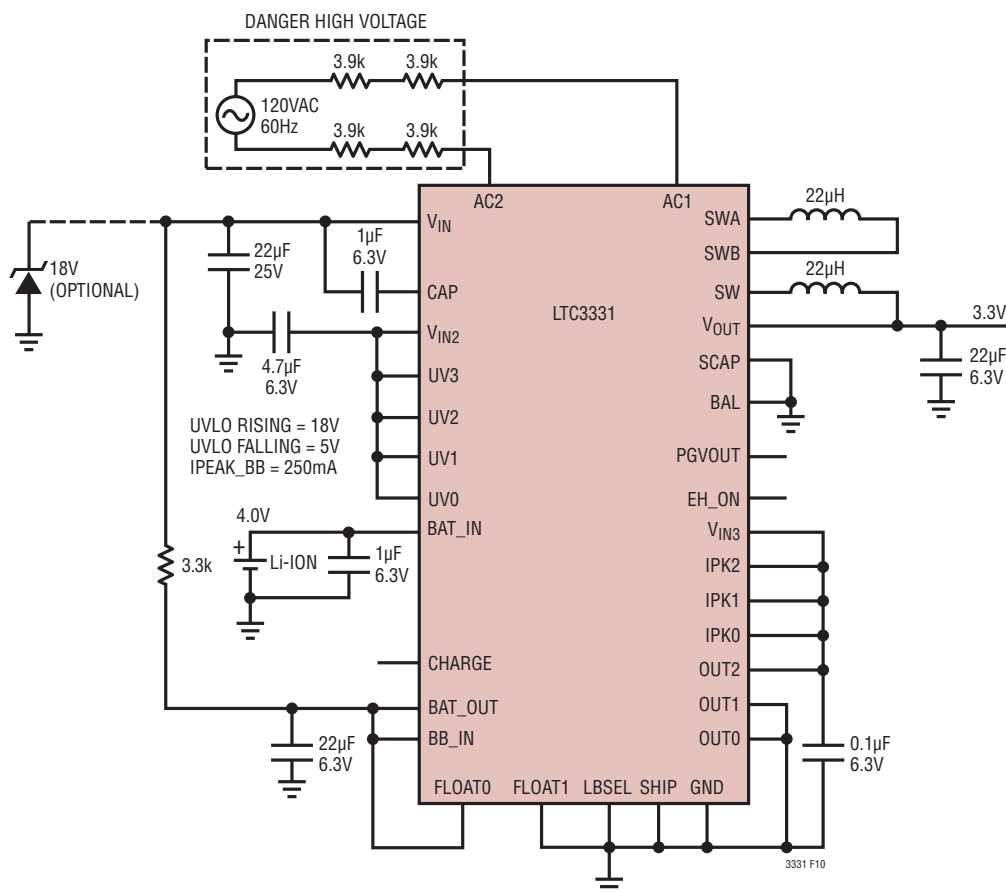


Figure 10. AC Line Powered 5V UPS

on the last page of this data sheet shows the EH\_ON output tied to the OUT2 input. When EH\_ON is low the output is programmed to 2.5V and the battery powers the output. When energy harvesting is available EH\_ON is high and the output is programmed to 3.6V allowing for increased storage of harvested energy. If energy harvesting goes

away, the output is again programmed to 2.5V and the buck-boost converter will be in sleep until the output is discharged to the wake-up threshold. If the energy stored at 3.6V is enough to ride through a temporary loss of energy harvesting then the only drain on the battery will be the quiescent current in sleep.

APPLICATIONS INFORMATION

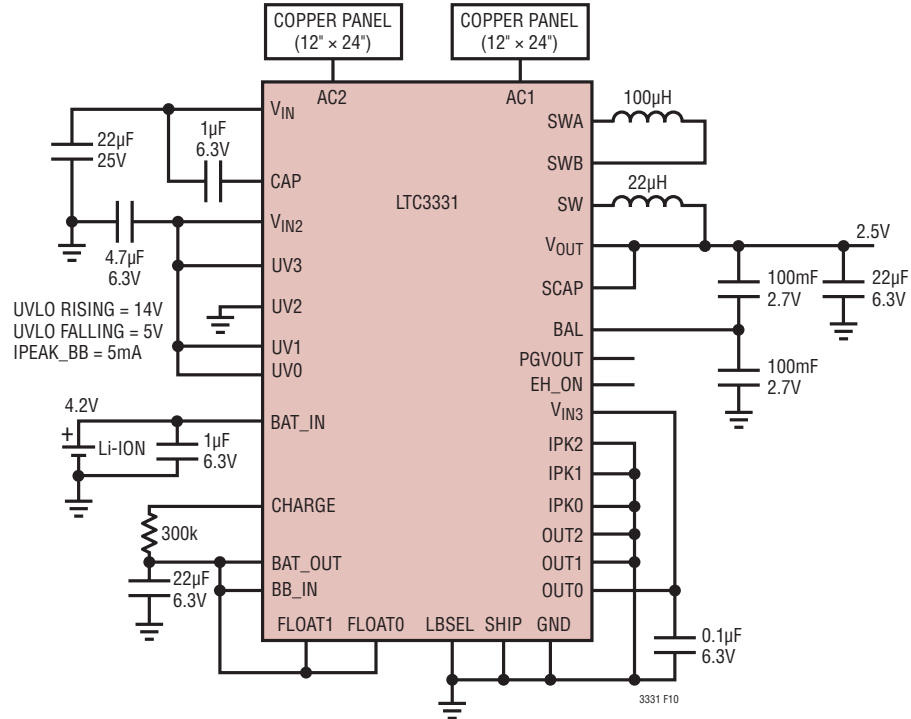


Figure 11. Electric Field Energy Harvester

# APPLICATIONS INFORMATION

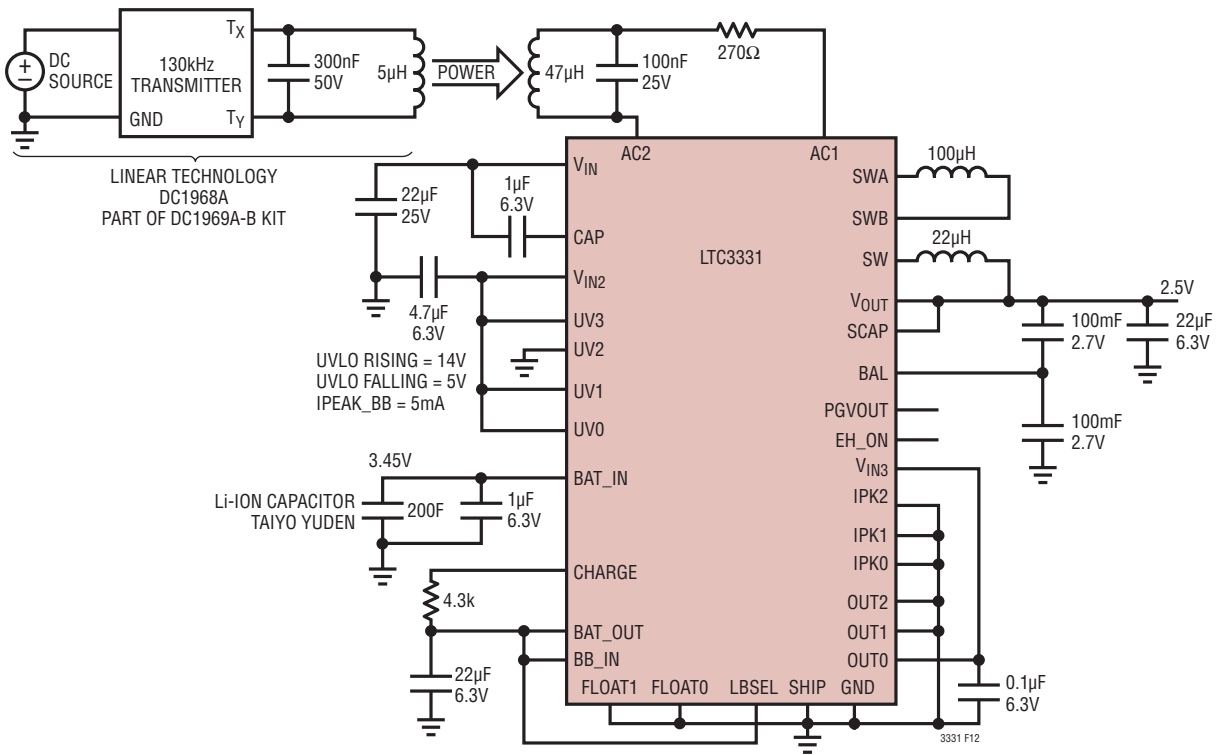
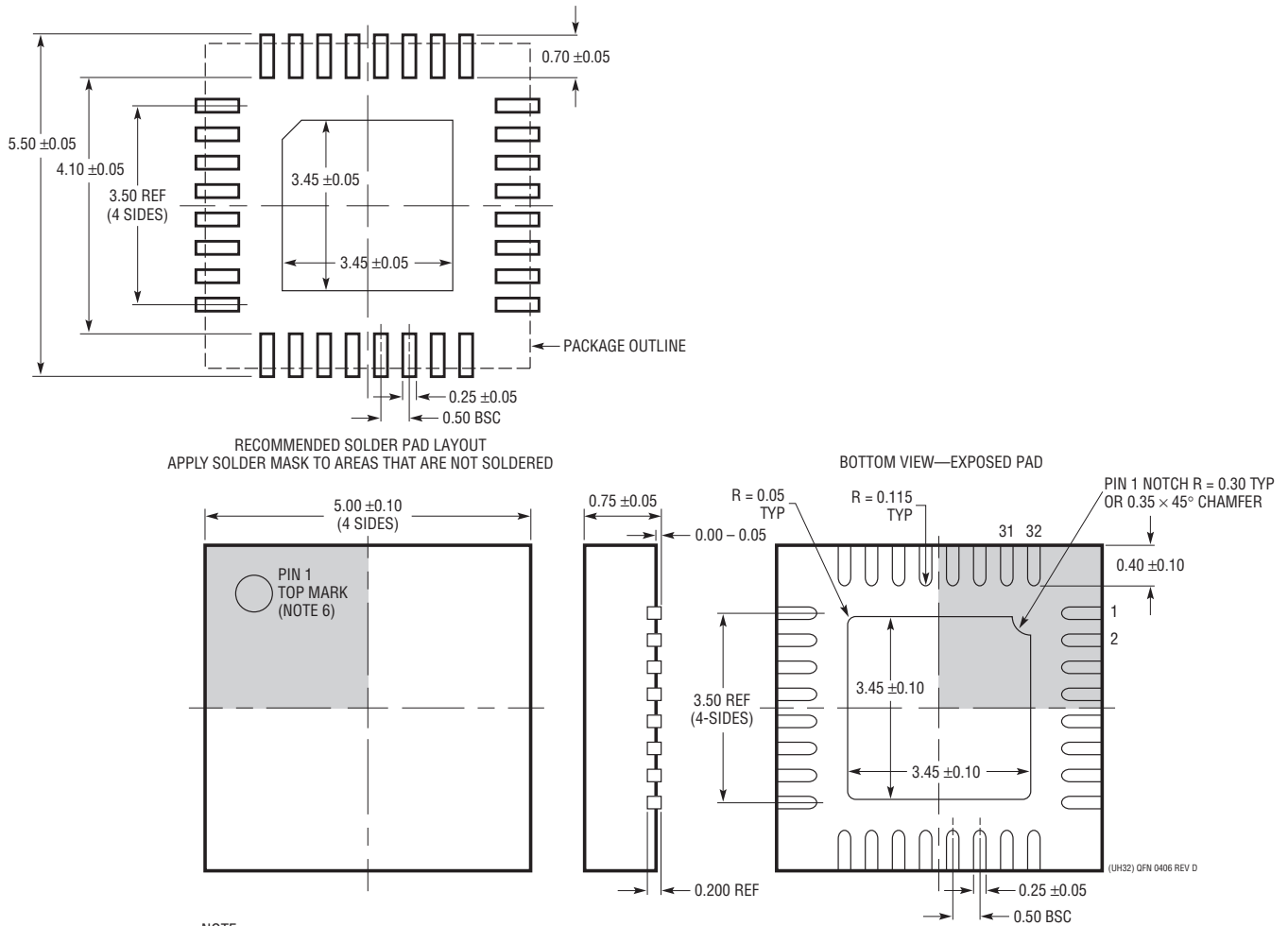


Figure 12. Wireless Battery Charger

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**UH Package**  
**32-Lead Plastic QFN (5mm × 5mm)**  
 (Reference LTC DWG # 05-08-1693 Rev D)



- NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE MO-220 VARIATION WHHD-(X) (TO BE APPROVED)
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/14	Clarified $I_Q$ on the LTC3330 in the Related Parts list	34
B	11/14	Clarified Description Clarified Available Buck-Boost Current Conditions Replaced PGOOD with PGVOUT in Graphs Clarified Table 2 Replaced PGOOD with PGVOUT in Text Clarified $t_{SLEEP}$ Formula Clarified Figure 6 Schematic Clarified Inductor Selection Paragraph Clarified Typical Application Schematic Clarified LTC3330 Comments in Related Parts	1 4 7, 8 16 23 23 24 25 34 34
C	08/15	Changed $C_{OUT}$ Equation	23