# 20V High Efficiency Nanopower Step-Down Regulator

## FEATURES

- **720nA Input $I_Q$ in Regulation (No Load), $V_{IN}$ = 4V**
- **820nA Input $I_Q$ in Regulation (No Load), $V_{IN}$ = 20V**
- **400nA Input $I_Q$ in UVLO**
- **2.7V to 20V Input Operating Range**
- **Up to 50mA of Output Current**
- **Pin Selectable Output Voltages:**
  - **1.2V, 1.5V, 1.8V, 2.5V (LTC3388-1)**
  - **2.8V, 3.0V, 3.3V, 5.0V (LTC3388-3)**
- High Efficiency Hysteretic Synchronous DC/DC Conversion
- Standby Mode Disables Buck Switching
- Available in 10-Lead MSE and 3mm × 3mm DFN Packages

## APPLICATIONS

- Keep Alive Power for Portable Products
- Industrial Control Supplies
- Distributed Power Systems
- Battery-Operated Devices

## DESCRIPTION

The LTC®3388-1/LTC3388-3 are high efficiency step-down DC/DC converters with internal high side and synchronous power switches that draw only 720nA typical DC supply current at no load while maintaining output voltage regulation.

Capable of supplying 50mA of load current, the LTC3388-1/LTC3388-3 also incorporate an accurate undervoltage lockout (UVLO) feature to disable the converter and maintain a low quiescent current state when the input voltage falls below 2.3V. In regulation, the LTC3388-1/LTC3388-3 enter a sleep state in which both input and output quiescent currents are minimal. The buck converter turns on and off as needed to maintain regulation. An additional standby mode disables buck switching while the output is in regulation for short duration loads requiring low ripple.

Output voltages of 1.2V, 1.5V, 1.8V, 2.5V (LTC3388-1) and 2.8V, 3.0V, 3.3V, 5.0V (LTC3388-3) are pin selectable. The LTC3388-1/LTC3388-3 can operate with $V_{IN}$ up to 20V while the no load quiescent current remains below 1µA.

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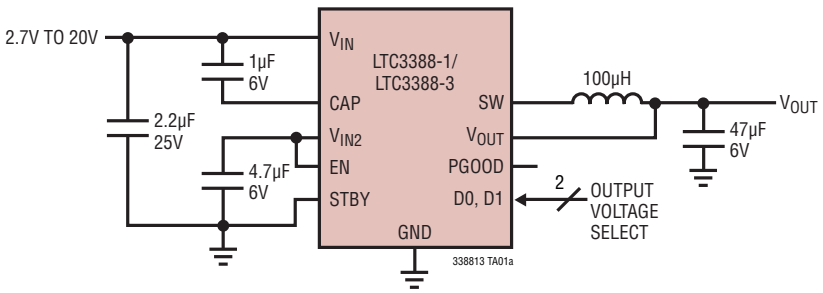
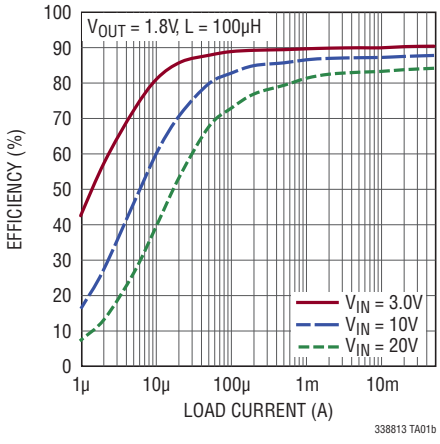
## TYPICAL APPLICATION

**50mA Step-Down Converter**



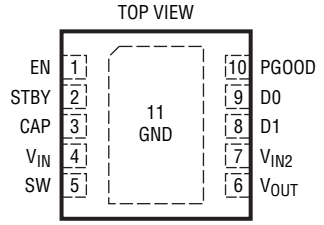

**Efficiency vs Load Current**



## ABSOLUTE MAXIMUM RATINGS (Note 1)

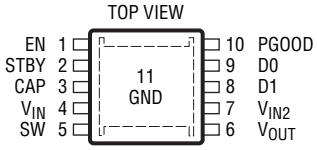
$V_{IN}$ ..... –0.3V to 22V
D0, D1 ..... –0.3V to [Lesser of ($V_{IN2}$ + 0.3V) or 6V]
CAP ..... [Higher of –0.3V or ($V_{IN}$ – 6V)] to $V_{IN}$
$V_{IN2}$, $V_{OUT}$ ..... –0.3V to [Lesser of ($V_{IN}$ + 0.3V) or 6V]
EN, STBY ..... –0.3V to 6V
PGOOD ..... –0.3V to 6V
$I_{SW}$ ..... 210mA
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSE Only ..... 300°C

## PIN CONFIGURATION




DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W, $\theta_{JC}$ = 7.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB




MSE PACKAGE
10-LEAD PLASTIC MSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 45°C/W, $\theta_{JC}$ = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3388EDD-1#PBF | LTC3388EDD-1#TRPBF | LFWN | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3388IDD-1#PBF | LTC3388IDD-1#TRPBF | LFWN | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3388EMSE-1#PBF | LTC3388EMSE-1#TRPBF | LTFWM | 10-Lead Plastic MSOP | –40°C to 125°C |
| LTC3388IMSE-1#PBF | LTC3388IMSE-1#TRPBF | LTFWM | 10-Lead Plastic MSOP | –40°C to 125°C |
| LTC3388EDD-3#PBF | LTC3388EDD-3#TRPBF | LFWQ | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3388IDD-3#PBF | LTC3388IDD-3#TRPBF | LFWQ | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3388EMSE-3#PBF | LTC3388EMSE-3#TRPBF | LTFWP | 10-Lead Plastic MSOP | –40°C to 125°C |
| LTC3388IMSE-3#PBF | LTC3388IMSE-3#TRPBF | LTFWP | 10-Lead Plastic MSOP | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for $T_A$ = 25°C (Note 2). Unless otherwise noted, $V_{IN}$ = 5.5V.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input Voltage Range | | ● | 2.7 | | 20 | V |
| $I_Q$ | $V_{IN}$ Quiescent Current When Enabled | | | | | | |
| | UVLO | $V_{IN}$ = 2V | | | 400 | 600 | nA |
| | Sleep | $V_{IN}$ = 4V | | | 720 | 1100 | nA |
| | Sleep | $V_{IN}$ = 20V | | | 820 | 1200 | nA |
| | Active | $I_{SW}$ = 0A (Note 4) | | | 150 | 250 | µA |
| $I_{Q,STBY}$ | $V_{IN}$ Quiescent Current Enabled, in Standby | | | | | | |
| | Sleeping | $V_{IN}$ = 4V | | | 720 | 1100 | nA |
| | Not Sleeping | $V_{IN}$ = 4V | | | 2000 | 3000 | nA |
| $I_{Q,SD}$ | $V_{IN}$ Quiescent Current When Disabled | $V_{IN}$ = 4V | | | 520 | 800 | nA |
| | | $V_{IN}$ = 20V | | | 620 | 900 | nA |
| $V_{UVLO}$ | $V_{IN}$ Undervoltage Lockout Threshold | $V_{IN}$ Rising | ● | | 2.5 | 2.65 | V |
| | | $V_{IN}$ Falling | ● | 2.15 | 2.3 | | V |
| $V_{OUT}$ | Regulated Output Voltage (LTC3388-1) | 1.2V Output Selected; D1 = 0, D0 = 0 | | | | | |
| | | Sleep Threshold | ● | | 1.208 | 1.260 | V |
| | | Wake-Up Threshold | ● | 1.140 | 1.192 | | V |
| | | 1.5V Output Selected; D1 = 0, D0 = 1 | | | | | |
| | | Sleep Threshold | ● | | 1.508 | 1.560 | V |
| | | Wake-Up Threshold | ● | 1.440 | 1.492 | | V |
| | | 1.8V Output Selected; D1 = 1, D0 = 0 | | | | | |
| | | Sleep Threshold | ● | | 1.808 | 1.863 | V |
| | | Wake-Up Threshold | ● | 1.737 | 1.792 | | V |
| | | 2.5V Output Selected; D1 = 1, D0 = 1 | | | | | |
| | | Sleep Threshold | ● | | 2.508 | 2.600 | V |
| | | Wake-Up Threshold | ● | 2.400 | 2.492 | | V |
| $V_{OUT}$ | Regulated Output Voltage (LTC3388-3) | 2.8V Output Selected; D1 = 0, D0 = 0 | | | | | |
| | | Sleep Threshold | ● | | 2.816 | 2.912 | V |
| | | Wake-Up Threshold | ● | 2.688 | 2.784 | | V |
| | | 3.0V Output Selected; D1 = 0, D0 = 1 | | | | | |
| | | Sleep Threshold | ● | | 3.016 | 3.105 | V |
| | | Wake-Up Threshold | ● | 2.895 | 2.984 | | V |
| | | 3.3V Output Selected; D1 = 1, D0 = 0 | | | | | |
| | | Sleep Threshold | ● | | 3.316 | 3.399 | V |
| | | Wake-Up Threshold | ● | 3.201 | 3.284 | | V |
| | | 5.0V Output Selected; D1 = 1, D0 = 1 | | | | | |
| | | Sleep Threshold | ● | | 5.016 | 5.180 | V |
| | | Wake-Up Threshold | ● | 4.820 | 4.984 | | V |
| | PGOOD Threshold | As a Percentage of the Selected $V_{OUT}$ | | 83 | 92 | | % |
| $V_{OL, PGOOD}$ | PGOOD Output Low Voltage | 100µA Into Pin | ● | | | 0.2 | V |
| $I_{VOUT}$ | Output Quiescent Current | LTC3388-1: $V_{OUT}$ = 2.5V | | | 60 | | nA |
| | | LTC3388-3: $V_{OUT}$ = 5.0V | | | 120 | | nA |
| $I_{PEAK}$ | PMOS Switch Peak Current | | ● | 100 | 150 | 210 | mA |
| $I_{OUT}$ | Available Output Current | | ● | 50 | | | mA |
| $R_{P, BUCK}$ | PMOS Switch On-Resistance | | | | 1.1 | | Ω |
| $R_{N, BUCK}$ | NMOS Switch On-Resistance | | | | 1.3 | | Ω |
| | Maximum Duty Cycle | | ● | 100 | | | % |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for $T_A$ = 25°C (Note 2). Unless otherwise noted, $V_{IN}$ = 5.5V.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | D0/D1/EN/STBY Input High Voltage | | ● | 1.2 | | | V |
| $V_{IL(D0, D1)}$ | D0/D1 Input Low Voltage | | ● | | | 0.4 | V |
| $V_{IL(EN,STBY)}$ | EN/STBY Input Low Voltage | | ● | | | 150 | mV |
| $I_{IH}$ | D0/D1/EN/STBY Input High Current | | | | | 10 | nA |
| $I_{IL}$ | D0/D1/EN/STBY Input Low Current | | | | | 10 | nA |
| | Additional $I_Q$ at $V_{IN}$ with EN at $V_{IH(MIN)}$ | $V_{EN}$ = 1.2V, $V_{IN}$ = 4V | | | 40 | | nA |
| | Additional $I_Q$ at $V_{IN}$ with STBY at $V_{IH(MIN)}$ | $V_{STBY}$ = 1.2V, $V_{IN}$ = 4V | | | 40 | | nA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

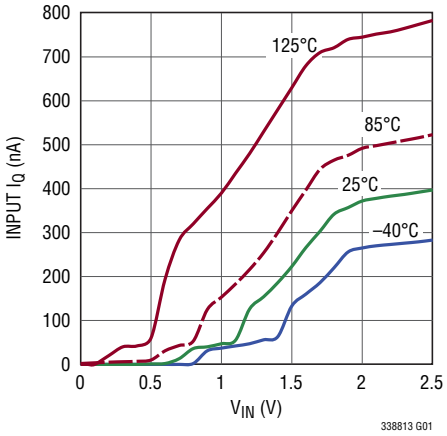
**Note 2:** The LTC3388-1/LTC3388-3 are tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3388E-1/LTC3388E-3 are guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3388I-1/LTC3388I-3 are guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

**Note 3:** The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation (PD, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

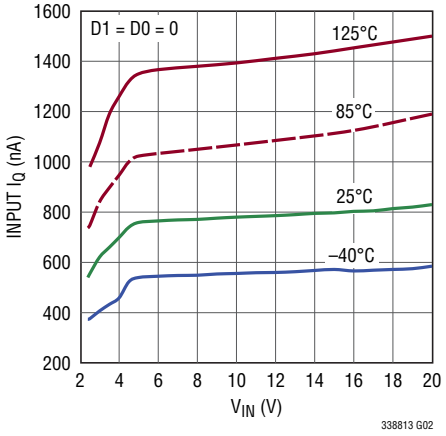
**Note 4:** Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

## TYPICAL PERFORMANCE CHARACTERISTICS

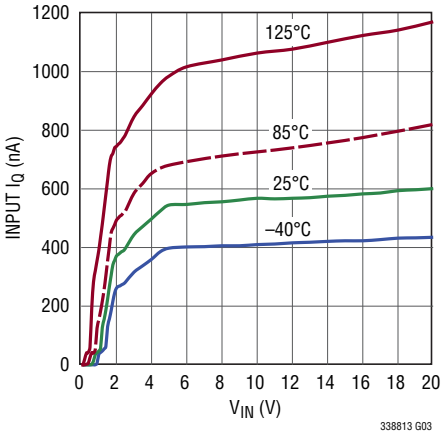
**Input $I_Q$ vs $V_{IN}$, UVLO**




**Input $I_Q$ vs $V_{IN}$, No Load**

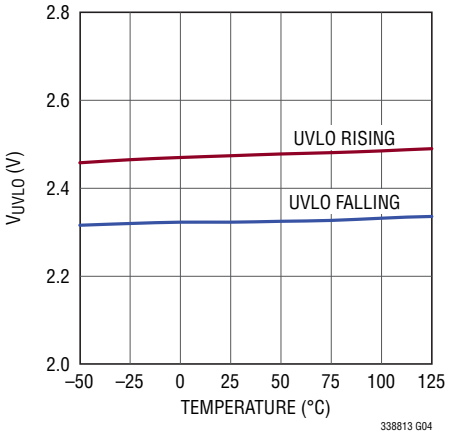



**Input $I_Q$ vs $V_{IN}$, EN Low**

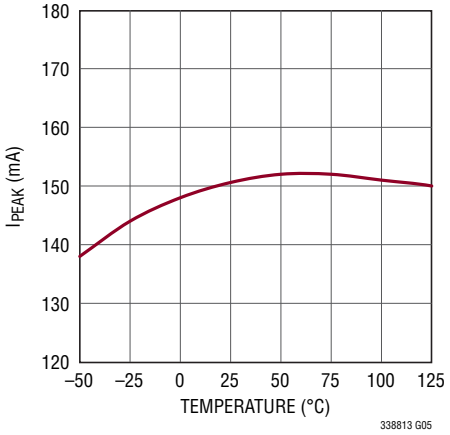


# TYPICAL PERFORMANCE CHARACTERISTICS

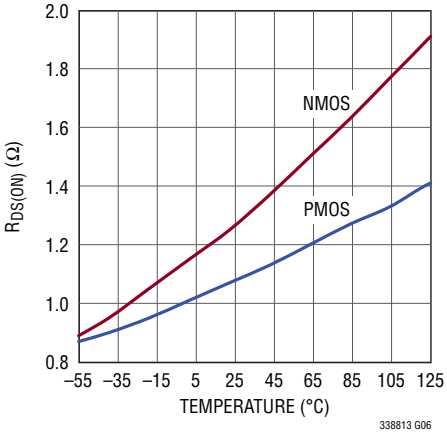
### UVLO vs Temperature



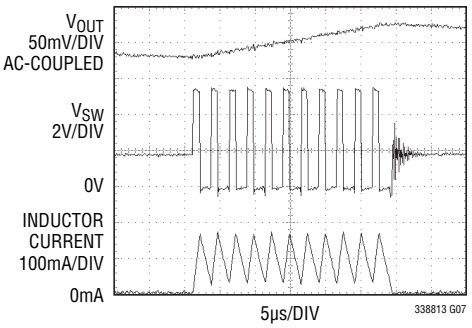

### IPEAK vs Temperature




### RP,BUCK/RN,BUCK vs Temperature

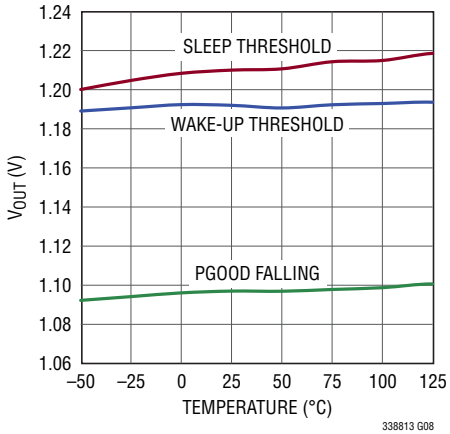



### Operating Waveforms

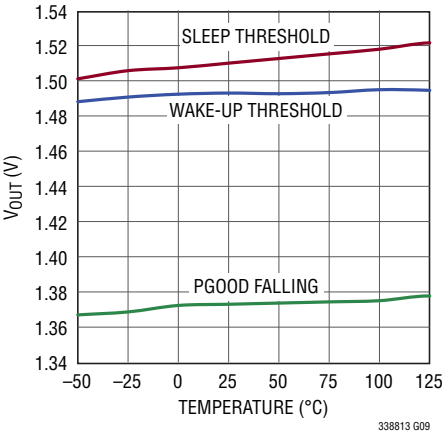



$V_{IN}$ = 5.5V, $V_{OUT}$ = 1.8V
$I_{LOAD}$ = 20mA
L = 22µH, $C_{OUT}$ = 47µF

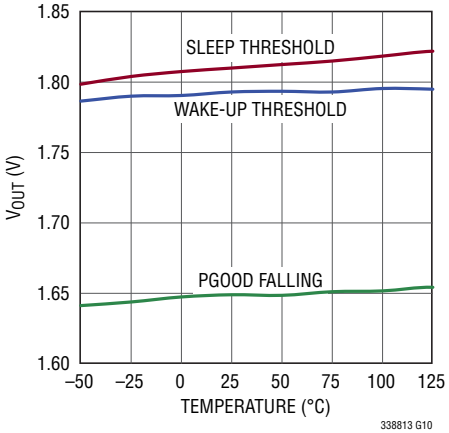
### 1.2V Output vs Temperature (LTC3388-1)



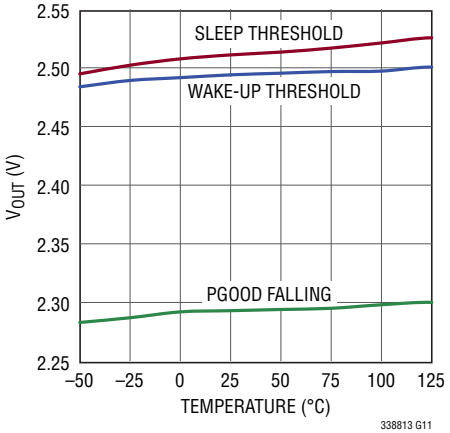

### 1.5V Output vs Temperature (LTC3388-1)



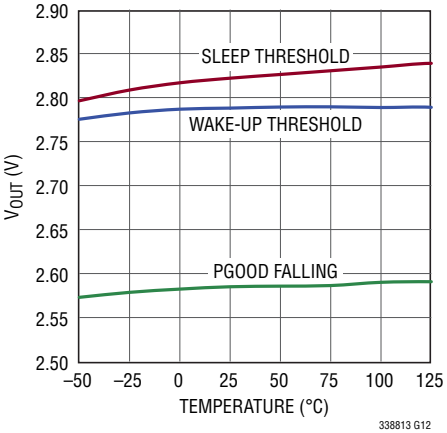

### 1.8V Output vs Temperature (LTC3388-1)




### 2.5V Output vs Temperature (LTC3388-1)

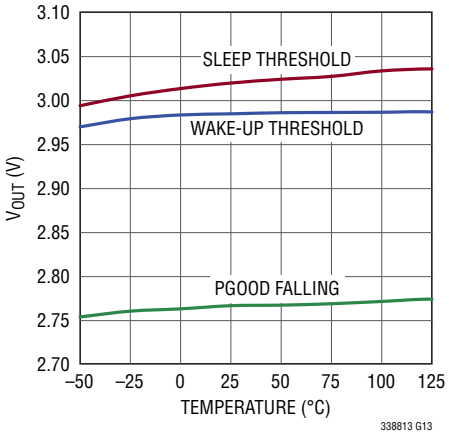



### 2.8V Output vs Temperature (LTC3388-3)

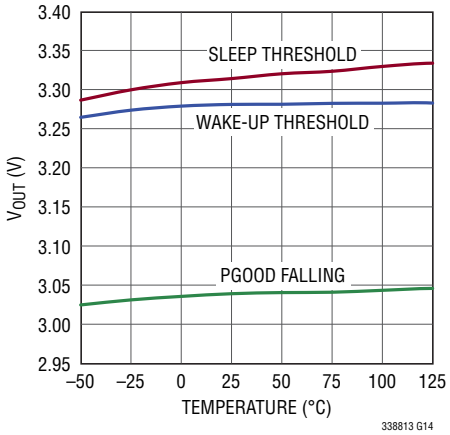


## TYPICAL PERFORMANCE CHARACTERISTICS

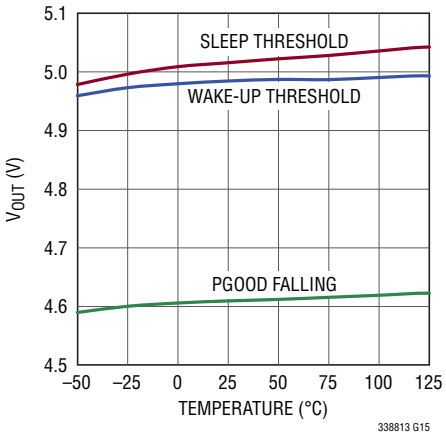
### 3.0V Output vs Temperature (LTC3388-3)



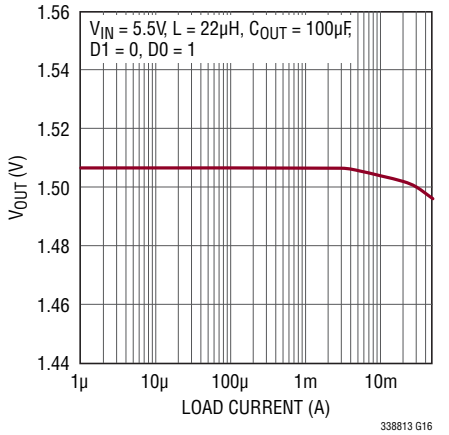

### 3.3V Output vs Temperature (LTC3388-3)



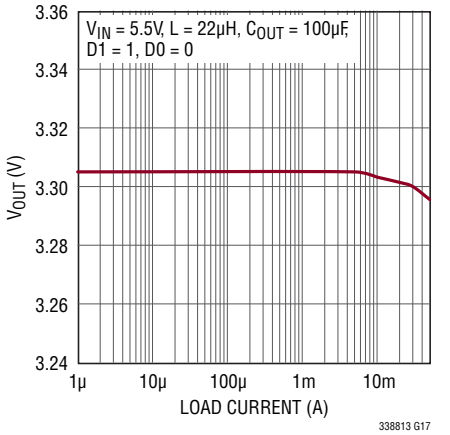

### 5.0V Output vs Temperature (LTC3388-3)



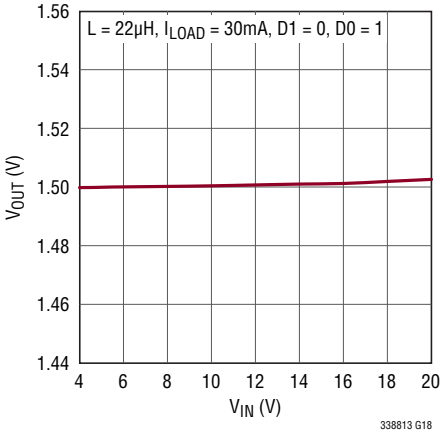

### VOUT Load Regulation (LTC3388-1)



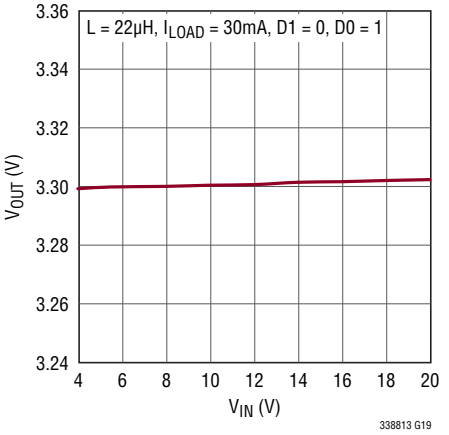

### VOUT Load Regulation (LTC3388-3)



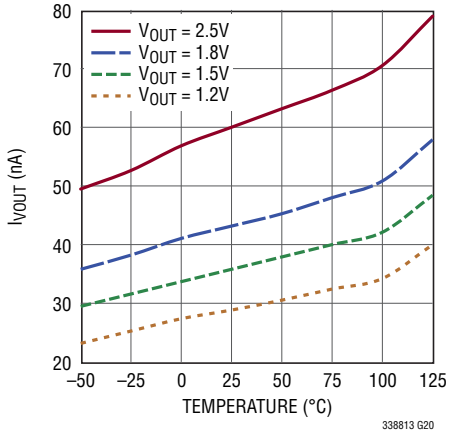

### VOUT Line Regulation (LTC3388-1)



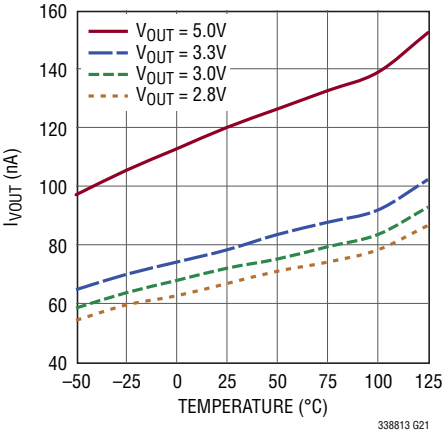

### VOUT Line Regulation (LTC3388-3)




### IVOUT vs Temperature (LTC3388-1)

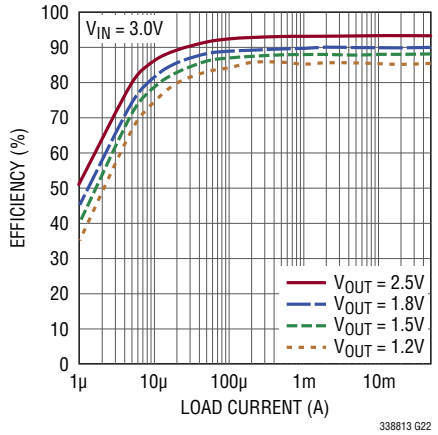



### IVOUT vs Temperature (LTC3388-3)

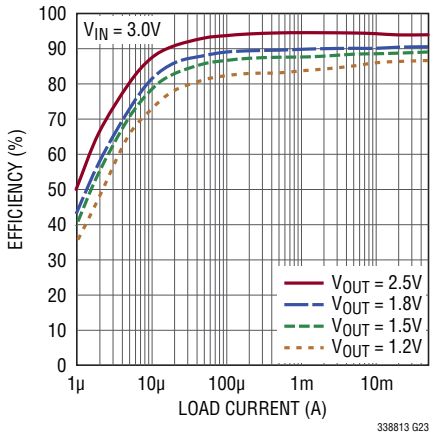


## TYPICAL PERFORMANCE CHARACTERISTICS

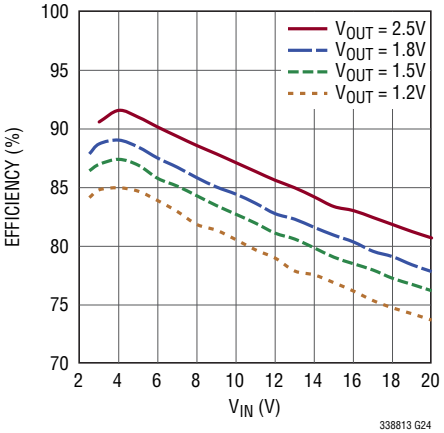
**Efficiency vs $I_{LOAD}$, L = 22µH (LTC3388-1)**



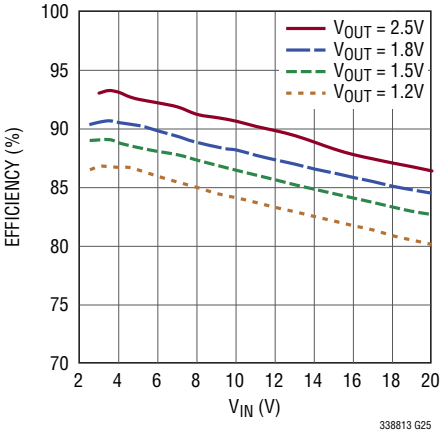

**Efficiency vs $I_{LOAD}$, L = 100µH (LTC3388-1)**



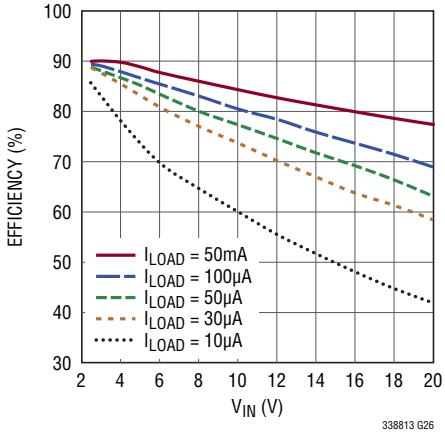

**Efficiency vs $V_{IN}$ for $I_{LOAD}$ = 50mA, L = 22µH (LTC3388-1)**



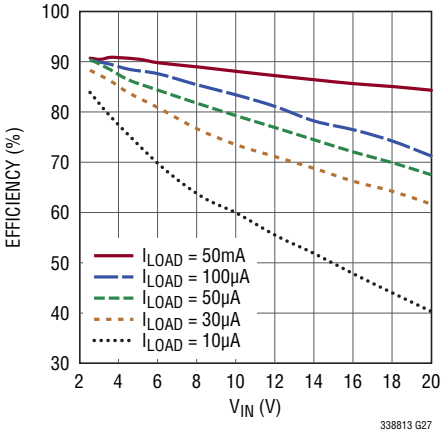

**Efficiency vs $V_{IN}$ for $I_{LOAD}$ = 50mA, L = 100µH (LTC3388-1)**




**Efficiency vs $V_{IN}$ for $V_{OUT}$ = 1.8V, L = 22µH (LTC3388-1)**

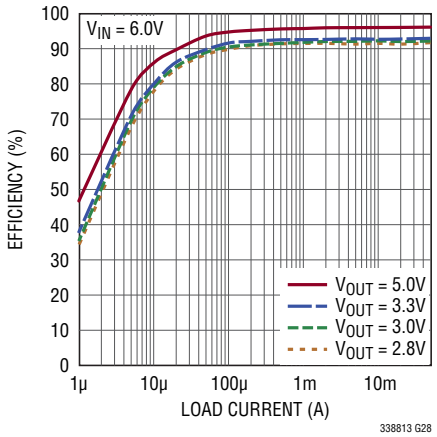



**Efficiency vs $V_{IN}$ for $V_{OUT}$ = 1.8V, L = 100µH (LTC3388-1)**

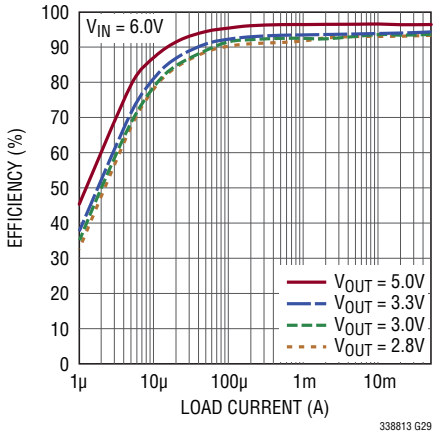


## TYPICAL PERFORMANCE CHARACTERISTICS

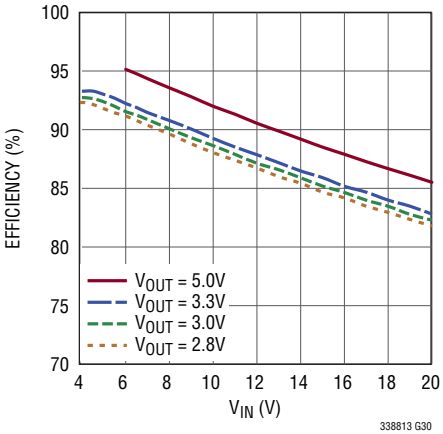
**Efficiency vs $I_{LOAD}$, L = 22µH (LTC3388-3)**



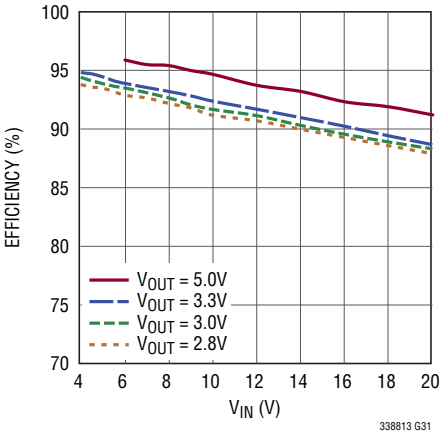

**Efficiency vs $I_{LOAD}$, L = 100µH (LTC3388-3)**



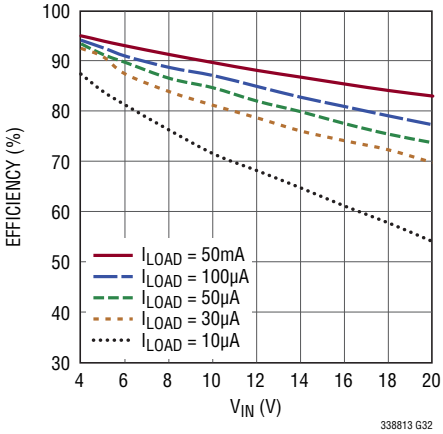

**Efficiency vs $V_{IN}$ for $I_{LOAD}$ = 50mA, L = 22µH (LTC3388-3)**



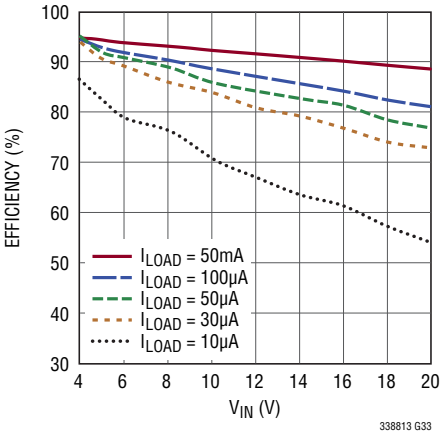

**Efficiency vs $V_{IN}$ for $I_{LOAD}$ = 50mA, L = 100µH (LTC3388-3)**




**Efficiency vs $V_{IN}$ for $V_{OUT}$ = 3.3V, L = 22µH (LTC3388-3)**




**Efficiency vs $V_{IN}$ for $V_{OUT}$ = 3.3V, L = 100µH (LTC3388-3)**



## PIN FUNCTIONS

**EN (Pin 1):** Enable Input. Logic level input referenced to $V_{IN2}$. A logic high on EN will enable the buck converter. Driving EN to $V_{IN2}$ will result in no additional quiescent current on $V_{IN}$. However, if EN is driven near $V_{IH}$ or $V_{IL}$ 40nA of additional quiescent current can appear on $V_{IN}$.

**STBY (Pin 2):** Standby Input. Logic level input referenced to $V_{IN2}$. A logic high on STBY will place the part in standby mode. Driving STBY to $V_{IN2}$ will result in no additional quiescent current on $V_{IN}$. However, if STBY is driven near $V_{IH}$ or $V_{IL}$ 40nA of additional quiescent current can appear on $V_{IN}$.

**CAP (Pin 3):** Internal rail referenced to $V_{IN}$ to serve as gate drive for buck PMOS switch. A 1µF capacitor should be connected between CAP and $V_{IN}$. This pin is not intended for use as an external system rail.

**$V_{IN}$ (Pin 4):** Input Voltage. A 2.2µF or larger capacitor should be connected from $V_{IN}$ to GND.

**SW (Pin 5):** Switch Pin for the Buck Switching Regulator. A 22µH or larger inductor should be connected from SW to $V_{OUT}$.

**$V_{OUT}$ (Pin 6):** Sense pin used to monitor the output voltage and adjust it through internal feedback.

**$V_{IN2}$ (Pin 7):** Internal low voltage rail to serve as gate drive for buck NMOS switch. Also serves as a logic high rail for output voltage select bits D0 and D1. A 4.7µF capacitor should be connected from $V_{IN2}$ to GND. This pin is not intended for use as an external system rail.

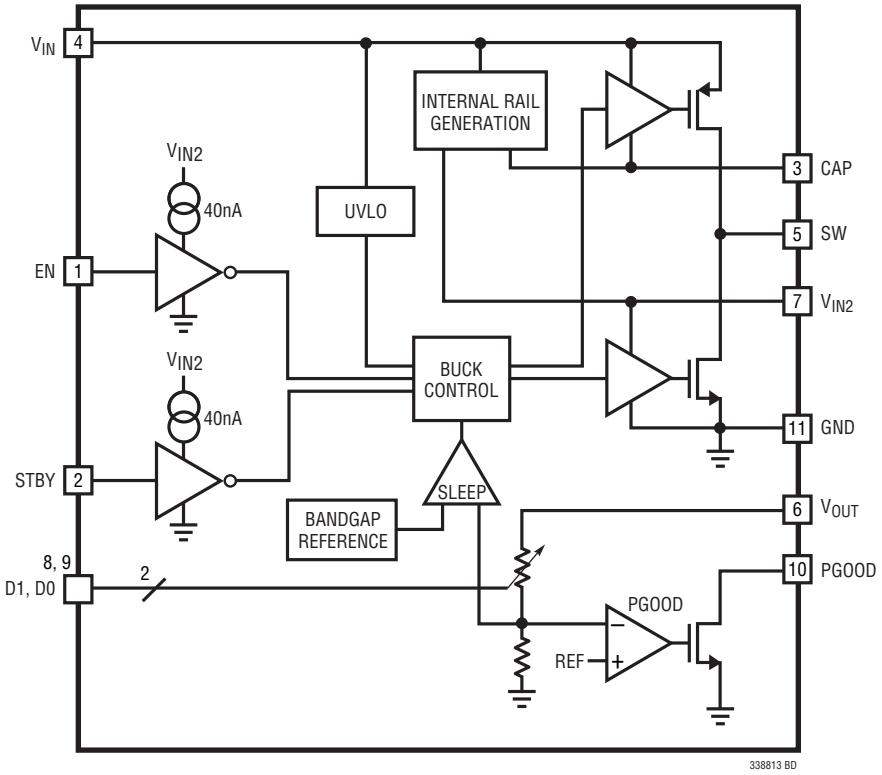
**D1 (Pin 8):** Output Voltage Select Bit. D1 should be tied high to $V_{IN2}$ or low to GND to select desired $V_{OUT}$ (see Table 1).

**D0 (Pin 9):** Output Voltage Select Bit. D0 should be tied high to $V_{IN2}$ or low to GND to select desired $V_{OUT}$ (see Table 1).

**PGOOD (Pin 10):** Power Good Open-Drain NMOS Output. The PGOOD pin is Hi-Z when $V_{OUT}$ is above 92% of the target value.

**GND (Exposed Pad Pin 11):** Ground. The exposed pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3388-1/LTC3388-3.

## BLOCK DIAGRAM



## OPERATION

The LTC3388-1/LTC3388-3 is an ultralow quiescent current power supply designed to maintain a regulated output voltage by means of a nanopower high efficiency synchronous buck regulator.

### Undervoltage Lockout (UVLO)

When the voltage on $V_{IN}$ rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. If $V_{IN}$ falls below the UVLO falling threshold the part will re-enter UVLO. In UVLO the quiescent current is approximately 400nA and the buck converter is disabled.

### Internal Rail Generation

Two internal rails, CAP and $V_{IN2}$, are generated from $V_{IN}$ and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the $V_{IN2}$ rail serves as logic high for EN, STBY, and output voltage select bits D0 and D1. The $V_{IN2}$ rail is regulated at 4.6V above GND while the CAP rail is regulated at 4.8V below $V_{IN}$. The $V_{IN2}$ and CAP rails are not intended to be used as external rails. Bypass capacitors are connected to the CAP and $V_{IN2}$ pins to serve as energy reservoirs for driving the buck switches. When $V_{IN}$ is below 4.6V, $V_{IN2}$ is equal to $V_{IN}$. CAP is at GND until $V_{IN}$ rises above 4.8V. Figure 1 shows the ideal $V_{IN}$, $V_{IN2}$ and CAP relationship.

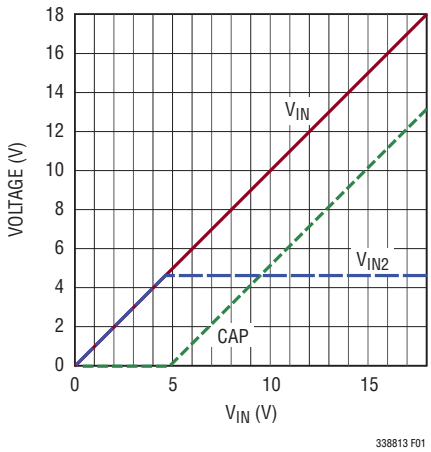



**Figure 1. Ideal $V_{IN}$, $V_{IN2}$ and CAP Relationship**

### Buck Operation

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the $V_{OUT}$ sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 150mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by $V_{IN}$, $V_{OUT}$, and the inductor value. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the buck output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 50mA of average load current when it is switching.

When the sleep comparator signals that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still flowing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode. The LTC3388-1/LTC3388-3 keeps the NMOS switch on during this time to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips, the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero.

Though the quiescent current when the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when the output voltage discharges to the sleep falling threshold. Thus, the buck operating quiescent current is averaged with the low sleep quiescent current. This allows the converter to remain very efficient at loads as low as 10µA.

## OPERATION

Four selectable voltages are available by tying the output select bits, D0 and D1, to GND or $V_{IN2}$. Table 1 shows the four D0/D1 codes and their corresponding output voltages as well as the difference in output voltages between the LTC3388-1 and LTC3388-3.

**Table 1. LTC3388-1/LTC3388-3 Output Voltage Selection**

| D1 | D0 | $V_{OUT}$ | $V_{OUT}$ Quiescent Current ($I_{VOUT}$) |
|---|---|---|---|
| 0 | 0 | 1.2V/2.8V | 28nA/66nA |
| 0 | 1 | 1.5V/3.0V | 36nA/72nA |
| 1 | 0 | 1.8V/3.3V | 43nA/78nA |
| 1 | 1 | 2.5V/5.0V | 60nA/120nA |

The internal feedback network draws a small amount of current from $V_{OUT}$ as listed in Table 1.

### Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of inductor current decreases, reducing the switching frequency of the current bursts. Further reduction in input supply voltage will eventually cause the PMOS to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the PMOS and the inductor.

### Power Good Comparator

A power good comparator causes the PGOOD pin to go Hi-Z the first time the converter reaches the sleep threshold of the programmed $V_{OUT}$, signaling that the output is in regulation. The PGOOD pin will remain Hi-Z until $V_{OUT}$ falls to 92% of the desired regulation voltage. Additionally, if PGOOD is high and $V_{IN}$ falls below the UVLO falling threshold, PGOOD will remain high until $V_{OUT}$ falls to 92% of the desired regulation point. This allows output energy to be used even if the input is lost. Figure 2 shows the behavior for $V_{OUT}$ = 1.8V and a 10µA load. At t = 2s $V_{IN}$ becomes high impedance and is discharged by the quiescent current of the LTC3388-1 and through servicing $V_{OUT}$. $V_{IN}$ crosses UVLO falling but PGOOD remains high until $V_{OUT}$ decreases to 92% of the desired regulation point.

This scenario is likely for cases in which the selected output voltage is below the UVLO falling threshold. If the input becomes high impedance and begins to fall it will be supported by the output through the body diode of the PMOS switch. For a high enough output voltage the part will not necessarily enter UVLO while $V_{OUT}$ remains PGOOD. This is always true for the output voltages available on the LTC3388-3.

The D0/D1 inputs can be switched while in regulation as shown in Figure 3. If $V_{OUT}$ is programmed to a voltage with a PGOOD falling threshold above the old $V_{OUT}$, PGOOD will transition low until the new regulation point is reached. When $V_{OUT}$ is programmed to a lower voltage, PGOOD will remain high through the transition.

The PGOOD pin is designed to drive a microprocessor or other chip I/O and is not intended to drive higher current loads such as an LED.

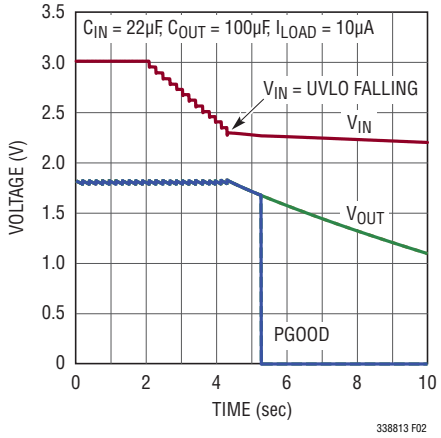



**Figure 2. PGOOD Operation During Transition to UVLO**

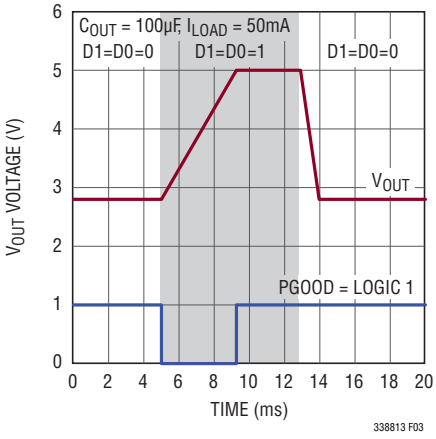



**Figure 3. PGOOD Operation During D0/D1 Transition**

## OPERATION

### Enable and Standby Modes

Two logic pins, EN and STBY, determine the operating mode of the LTC3388-1/LTC3388-3. When EN is high and STBY is low the synchronous buck converter is enabled and will regulate the output if the input voltage is above the programmed output voltage and above the UVLO threshold. If EN is low the buck converter circuitry is powered down to save quiescent current. The internal rail generation circuits are kept alive and the voltages at $V_{IN2}$ and CAP are maintained. When low, EN also shuts down the PGOOD circuitry and pulls the PGOOD pin low. If EN is high and the input falls below the UVLO threshold, the buck converter is shut down.

While enabled, the LTC3388-1/LTC3388-3 can be placed in standby mode by bringing STBY high. In standby mode the buck converter is disabled, eliminating the quiescent current used to run the buck circuitry. The PGOOD and sleep comparators are kept alive to maintain the state of the PGOOD pin.

The sleep comparator has lower quiescent current than the PGOOD comparator and when the LTC3388-1/LTC3388-3 is in sleep mode the PGOOD comparator is shut down and PGOOD is held high. The same occurs in standby mode. If the LTC3388-1/LTC3388-3 was in sleep before entering standby it will stay in sleep in standby, saving the quiescent current of the PGOOD comparator. If $V_{OUT}$ falls below the sleep falling threshold the PGOOD comparator will be enabled. If $V_{OUT}$ falls below the PGOOD falling threshold the PGOOD pin will be pulled low.

If STBY is driven high with EN low it will be ignored and the LTC3388-1/LTC3388-3 will remain shut down.

If EN and STBY are driven high but near $V_{IH}$ or low but near $V_{IL}$, additional quiescent current may appear on $V_{IN}$. This additional quiescent current is typically 40nA and depends on $V_{IN}$ and temperature. Driving EN or STBY to 0V or $V_{IN2}$ will prevent additional quiescent current on $V_{IN}$.

Figure 4 shows $V_{OUT}$ during a transition into and out of standby. While in standby, the buck is off and $V_{OUT}$ is quiet.

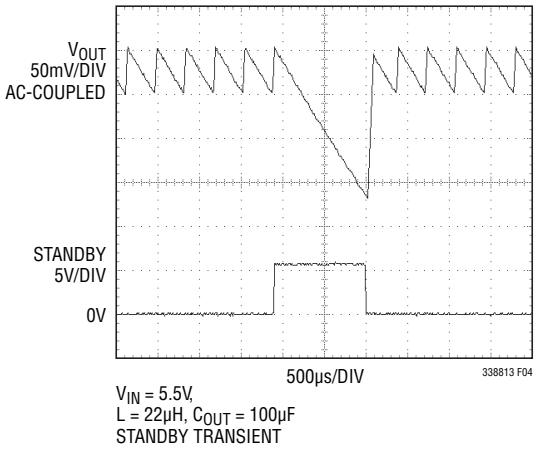



**Figure 4. LTC3388-3 Standby Transient, $V_{OUT}$ = 3.3V, $I_{LOAD}$ = 5mA**

## APPLICATIONS INFORMATION

### Introduction

The basic LTC3388-1/LTC3388-3 application circuit is shown on the front page. External components are selected based on the performance requirements of the application.

### Input Capacitor Selection

The input capacitor at $V_{IN}$ should be selected to adequately bypass the LTC3388-1/LTC3388-3 and filter the switching current presented by the buck regulator. The $V_{IN}$ capacitor should be rated to withstand the highest voltage ever present at $V_{IN}$. It should be placed as close as possible to the LTC3388-1/LTC3388-3 to force the high frequency switching current into a tight local loop to minimize EMI. A 2.2µF ceramic X7R or X5R capacitor should be adequate for bypassing.

High ripple current, high voltage rating, and low ESR make ceramic capacitors ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. A sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part.

For such applications with inductive source impedance, such as a long wire, a series RC network may be required in parallel with $C_{IN}$ to dampen the ringing of the input supply. Figure 5 shows this circuit and the typical values required to dampen the ringing. The RC resistor may be replaced by a single electrolytic capacitor that has an ESR equivalent to the needed series resistance of the network. See Application Note 88 for a complete discussion of this phenomenon.

### Output Capacitor Selection

The duration for which the regulator sleeps depends on the load current and the size of the output capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The DC sleep hysteresis window, $V_{HYST}$, is ±8mV and ±16mV around the programmed output voltage on the LTC3388-1 and LTC3388-3 respectively. Ideally this means that the sleep time is determined by the following equation:

$$t_{SLEEP} = C_{OUT} \frac{V_{HYST}}{I_{LOAD}}$$

This is true for output capacitors on the order of 100µF or larger, but as the output capacitor decreases towards 10µF delays in the internal sleep comparator along with the load current may result in the $V_{OUT}$ voltage slewing past the ±8mV/±16mV thresholds. This will lengthen the sleep time and increase $V_{OUT}$ ripple. A capacitor less than 10µF is not recommended as $V_{OUT}$ ripple could increase to an undesirable level.

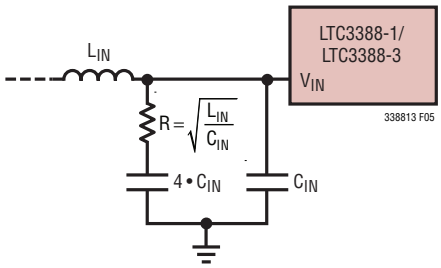



**Figure 5. Series RC to Reduce $V_{IN}$ Ringing**

## APPLICATIONS INFORMATION

If transient load currents above 50mA are required then a larger capacitor can be used at the output. This capacitor will be continuously discharged during a load condition and the capacitor can be sized for an acceptable drop in $V_{OUT}$:

$$C_{OUT} = (I_{LOAD} - I_{BUCK})\frac{t_{LOAD}}{V_{OUT}^{+} - V_{OUT}^{-}}$$

Here $V_{OUT}^{+}$ is the value of $V_{OUT}$ when PGOOD goes high and $V_{OUT}^{-}$ is the desired lower limit of $V_{OUT}$. $I_{BUCK}$ is the average current being delivered from the buck converter, typically $I_{PEAK}/2$.

A standard surface mount ceramic capacitor can be used for $C_{OUT}$, though some applications may be better suited to a low leakage aluminum electrolytic capacitor or a supercapacitor. These capacitors can be obtained from manufacturers such as Vishay, Illinois Capacitor, AVX, or CAP-XX.

### Inductor

The buck is optimized to work with an inductor of at least 22µH. This value represents a suitable trade-off between size and efficiency for typical applications. A larger inductor will benefit high voltage applications by increasing the on-time of the PMOS switch and improving efficiency by reducing gate charge loss. Choose an inductor with a DC current rating greater than 200mA. The DCR of the inductor can have an impact on efficiency as it is a source of loss. Trade-offs between price, size, and DCR should be evaluated. Table 2 lists several inductors that work well with the LTC3388-1/LTC3388-3.

**Table 2. Recommended Inductors for LTC3388-1/LTC3388-3**

| INDUCTOR TYPE | L (µH) | MAX $I_{DC}$ (mA) | MAX DCR (Ω) | SIZE in mm (L × W × H) | MANU-FACTURER |
|---|---|---|---|---|---|
| CDRH2D18/LDNP | 22 | 300 | 0.320 | 3.2 × 3.2 × 2.0 | Sumida |
| A997AS-220M | 22 | 390 | 0.440 | 4.0 × 4.0 × 1.8 | Toko |
| LPS5030-223MLC | 22 | 700 | 0.190 | 4.9 × 4.9 × 3.0 | Coilcraft |
| LPS4012-473MLC | 47 | 350 | 1.400 | 4.0 × 4.0 × 1.2 | Coilcraft |
| SLF7045T | 100 | 500 | 0.250 | 7.0 × 7.0 × 4.5 | TDK |

### $V_{IN2}$ and CAP Capacitors

A 1µF capacitor should be connected between $V_{IN}$ and CAP and a 4.7µF capacitor should be connected between $V_{IN2}$ and GND. These capacitors hold up the internal rails during buck switching and compensate the internal rail generation circuits. In applications where the input source is limited to less than 6V, the CAP pin can be tied to GND and the $V_{IN2}$ pin can be tied to $V_{IN}$ as shown in Figure 6. This circuit does not require the capacitors on $V_{IN2}$ and CAP, saving components and allowing a lower voltage rating for the single $V_{IN}$ capacitor.

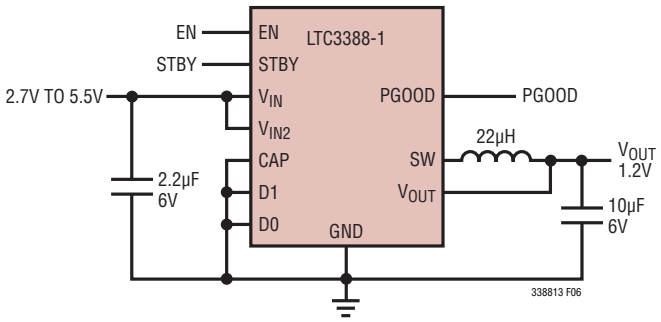



**Figure 6. Smallest Solution Size 1.2V Low Input Voltage Power Supply**

## APPLICATIONS INFORMATION

### Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (η1 + η 2 + η 3 + ...)

where η1, η2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses: 1) DC $V_{IN}$ operating current while active and in sleep, 2) MOSFET gate charge loss, and 3) $I^2R$ losses. The $V_{IN}$ operating current dominates the efficiency loss at very low load currents whereas the gate charge and $I^2R$ loss dominates the efficiency loss at medium to high load currents.

1. The DC $V_{IN}$ current is the average of the quiescent supply currents, given in the electrical characteristics, in the active and sleep modes. This can be estimated with the following equation:

$$I_{VIN(AVG)} = \frac{I_{LOAD}}{I_{BUCK}} I_{Q(ACTIVE)} + \left(1 - \frac{I_{LOAD}}{I_{BUCK}}\right) I_{Q(SLEEP)}$$

   where $I_{BUCK}$ is the average current being delivered from the buck converter, typically $I_{PEAK}/2$. For very light loads $I_{Q(SLEEP)}$ will dominate this loss term which is why the extremely low quiescent current in sleep of the LTC3388-1/LTC3388-3 is critical.

2. Internal MOSFET gate charge currents result from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from $V_{IN}$ to ground. The resulting dQ/dt is the current out of $V_{IN}$ that is typically larger than the DC bias current. Of course, this switching current only appears when the buck is on and is important at high load currents. Gate charge loss can be reduced by increasing the inductor, thereby reducing the switching frequency when the buck is active.

3. $I^2R$ losses are calculated from the resistances of the internal switches, $R_{SW}$, and the external inductor DCR. When switching, the average output current flowing through the inductor is "chopped" between the high side PMOS switch and the low side NMOS switch. Thus, the series resistance looking back into the switch pin is a function of the top and bottom switch on-resistance and the duty cycle (DC = $V_{OUT}/V_{IN}$) as follows:

$$R_{SW} = (R_{P,BUCK})DC + (R_{N,BUCK})(1 - DC)$$

   The on-resistance for both the top and bottom MOSFETs can be obtained from the curves in the Typical Performance Characteristics section. Thus, to obtain the $I^2R$ losses, simply add $R_{SW}$ to the DCR and multiply the result by the square of the average output current:

$$I^2R \text{ Loss} = I_O^2(R_{SW} + DCR)$$

   This loss term only occurs when the buck is operating and must be multiplied by the percentage of time the buck is operating versus sleeping or $I_{LOAD}/I_{BUCK}$ to see its overall effect.

Other losses, including $C_{IN}$ and $C_{OUT}$ ESR dissipative losses and inductor core losses, generally account for less than 2% of the total power loss.

## APPLICATIONS INFORMATION

### Interfacing with a Microprocessor

The PGOOD, STBY, and EN pins can be useful when powering a microprocessor from the LTC3388-1/LTC3388-3.

The PGOOD signal can be used to enable a sleeping microprocessor or other circuitry when $V_{OUT}$ reaches regulation, as shown in Figure 7. While active, a microprocessor may draw a small load when operating sensors, and then draw a large load to transmit data. Figure 7 shows the LTC3388-1/LTC3388-3 responding smoothly to such a load step.

The microprocessor or other circuitry may require a quiet supply for performing some functions. The STBY pin allows the microprocessor to place the LTC3388-1/LTC3388-3 into standby mode where the buck converter is inactive. Any ripple in the output voltage of the LTC3388-1/LTC3388-3 will cease and the output capacitor will support the load of the microprocessor and other circuitry. While in standby the output voltage will decrease as it's loaded. The output capacitor should be sized to minimize the decline.

The EN pin can be used to activate the LTC3388-1/LTC3388-3. For instance, in Figure 8 the LTC3388-1 is enabled by the PGOOD output of the LTC3588-1, a piezoelectric energy harvesting power supply, to create a 1.2V rail. The quiescent current that the LTC3388-1 draws will appear at the input of the LTC3588-1, reduced by the conversion ratio of the LTC3588-1 buck converter. Because the LTC3388-1 is driven by a 3.3V supply no capacitors are needed for the internal $V_{IN2}$ and CAP rails.

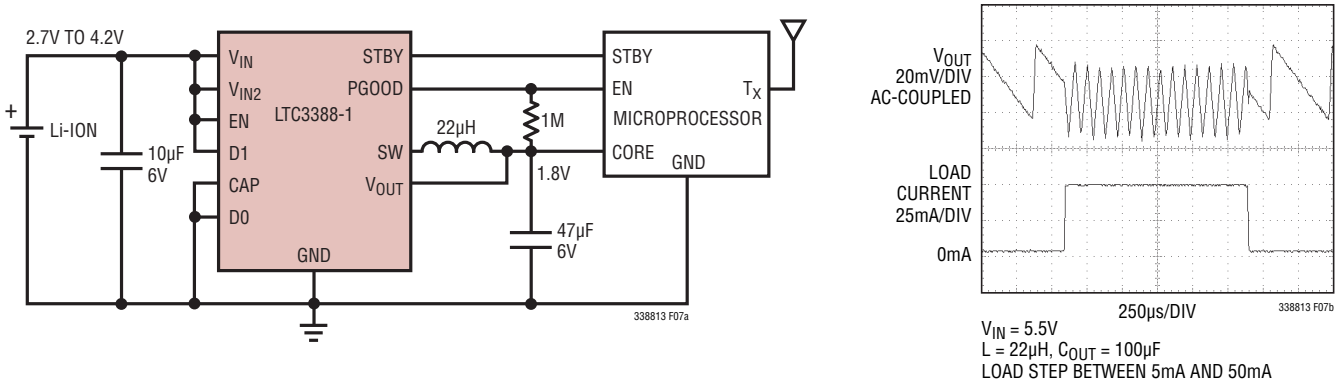



**Figure 7. 1.8V Step-Down Converter Powering a Microprocessor with a Wireless Transmitter and 45mA Load Step Response**

## APPLICATIONS INFORMATION

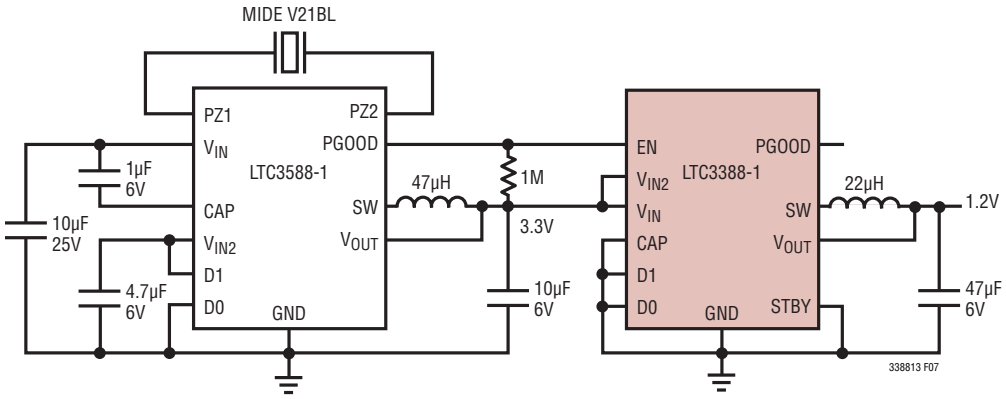
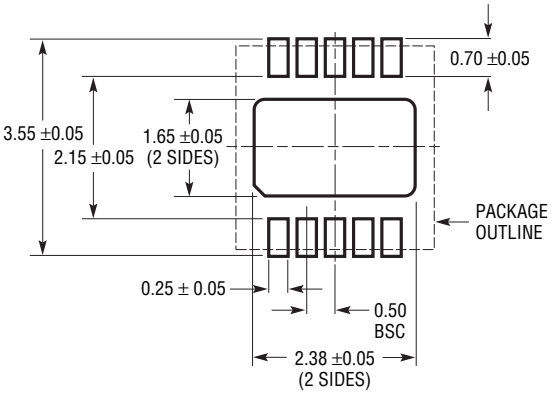



**Figure 8. Piezoelectric Energy Harvester and 1.2V Secondary Rail**

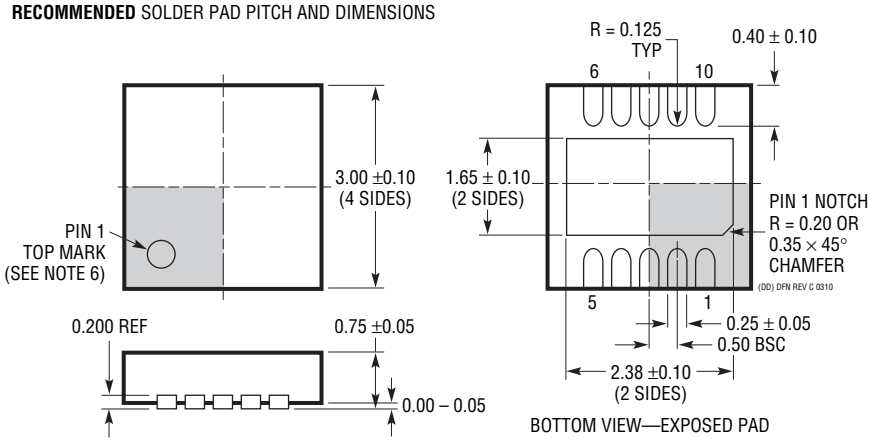
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**DD Package**
**10-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1699 Rev C)




**RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS



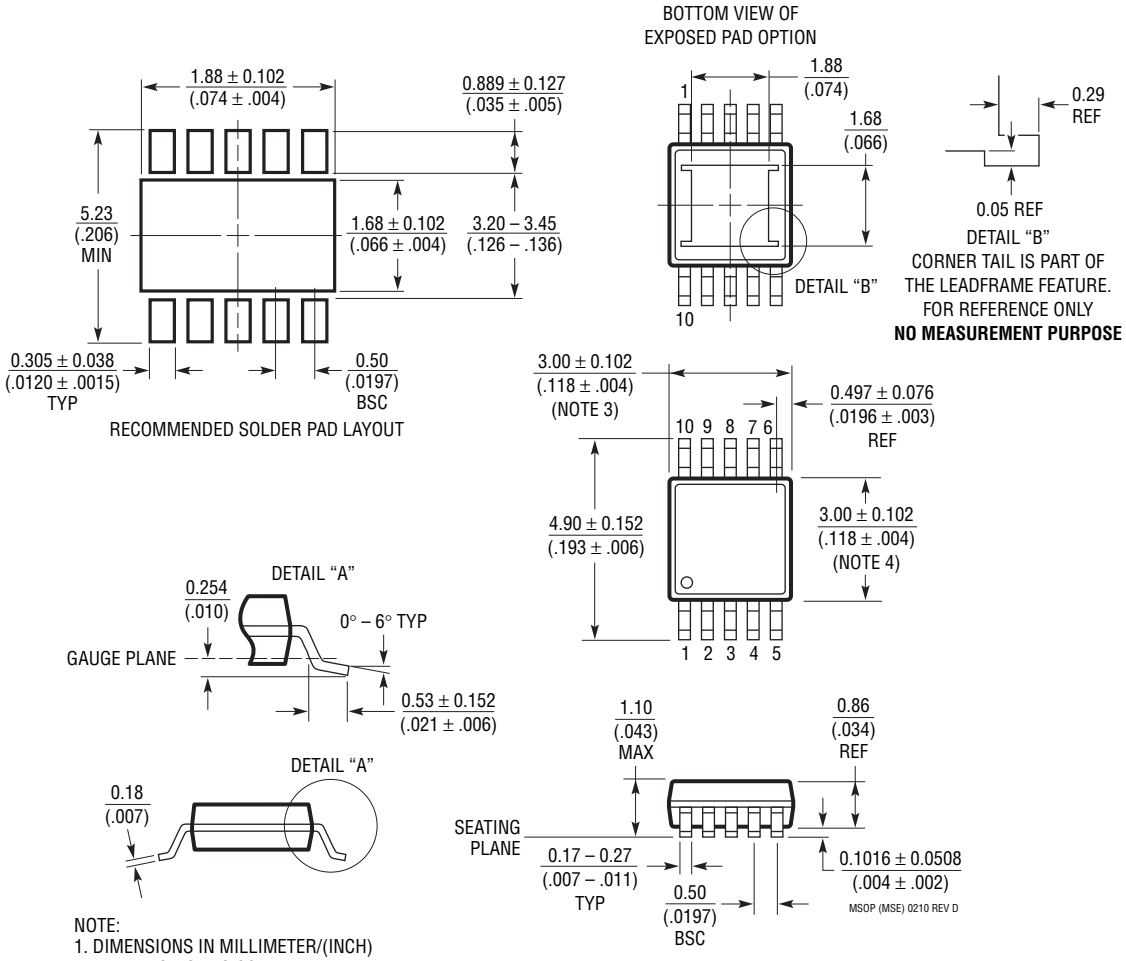

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**MSE Package**
**10-Lead Plastic MSOP, Exposed Die Pad**
(Reference LTC DWG # 05-08-1664 Rev D)




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 08/15 | Modified $C_{OUT}$ Equation | 15 |



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