1A, 2MHz Synchronous Step-Up DC/DC Converter in 2mm × 3mm DFN

FEATURES

- **Delivers 3.3V at 200mA from a Single Alkaline/ NiMH Cell or 3.3V at 400mA from Two Cells**
- **V_{IN} Start-Up Voltage: 700mV**
- **0.50V to 5.5V Input Range**
- **1.6V to 5.25V V_{OUT} Range**
- **Up to 94% Efficiency**
- **Output Disconnect**
- **2MHz Fixed Frequency Operation**
- **V_{IN} > V_{OUT} Operation**
- **Integrated Soft-Start**
- Current Mode Control with Internal Compensation
- Low Noise PWM Operation
- Internal Synchronous Rectifier
- Logic Controlled Shutdown: <1µA
- Anti-Ringing Control
- Low Profile (2mm × 3mm × 0.75mm) DFN Package

APPLICATIONS

- Medical Instruments
- Flash-Based MP3 Players
- Noise Canceling Headphones
- Wireless Mice
- Bluetooth Headsets

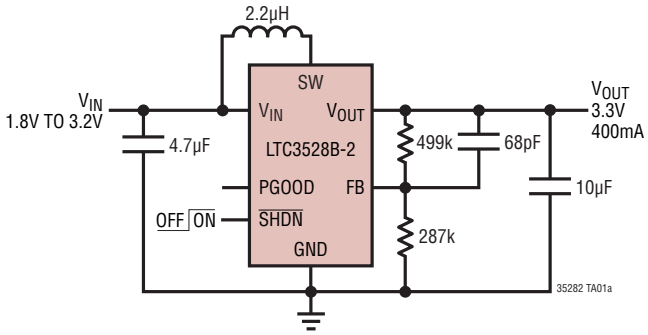
DESCRIPTION

The LTC®3528B-2 is a synchronous, fixed frequency step-up DC/DC converter with output disconnect. High efficiency synchronous rectification, in addition to a 700mV start-up voltage and operation down to 500mV once started, provides longer run-time for single or multiple cell battery-powered products.

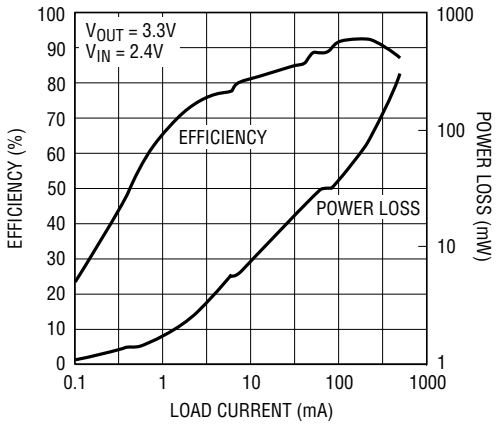
A switching frequency of 2MHz minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. The current mode PWM is internally compensated, simplifying the design process. The LTC3528B-2 features continuous switching at light loads. Anti-ringing circuitry reduces EMI by damping the inductor in discontinuous mode. Additional features include a low shutdown current, open-drain power good output, short-circuit protection and thermal overload protection.

The LTC3528B-2 is offered in an 8-lead 2mm × 3mm × 0.75mm DFN package.

TYPICAL APPLICATION



Efficiency and Power Loss

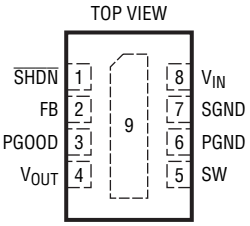


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 6V
SW Voltage
DC ..... –0.3V to 6V
Pulsed < 100ns ..... –0.3V to 7V
$\overline{SHDN}$, FB Voltage ..... –0.3V to 6V
V_{OUT} ..... –0.3V to 6V
PGOOD ..... –0.3V to 6V
Operating Junction Temperature Range
(Notes 2, 5) ..... –40°C to 125°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W (NOTE 6)
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3528BEDDB-2#PBF	LTC3528BEDDB-2#TRPBF	LDPB	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 1.2V, V_{OUT} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	I_{LOAD} = 1mA	●		0.70	0.88	V
Output Voltage Adjust Range	 T_A = 0°C to 85°C	● ●	1.7 1.6		5.25 5.25	V V
Feedback Voltage	(Note 7)	●	1.170	1.200	1.230	V
Feedback Input Current	V_{FB} = 1.3V			1	50	nA
Quiescent Current—Shutdown	$V_{\overline{SHDN}}$ = 0V, Not Including Switch Leakage, V_{OUT} = 0V			0.01	1	µA
Quiescent Current—Active	Measured on V_{OUT}, Nonswitching (Note 4)			300	500	µA
N-Channel MOSFET Switch Leakage Current	V_{SW} = 5V			0.1	10	µA
P-Channel MOSFET Switch Leakage Current	V_{SW} = 5V, V_{OUT} = 0V			0.1	10	µA
N-Channel MOSFET Switch On Resistance				0.175		Ω
P-Channel MOSFET Switch On Resistance				0.250		Ω
N-Channel MOSFET Current Limit		●	1.0	1.5		A
Current Limit Delay Time to Output	(Note 3)			60		ns
Maximum Duty Cycle	V_{FB} = 1.15V	●	87	92		%
Minimum Duty Cycle	V_{FB} = 1.3V	●			0	%
Frequency		●	1.8	2.0	2.4	MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 1.2V, V_{OUT} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Input High Voltage			0.88			V
$\overline{SHDN}$ Input Low Voltage					0.25	V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 1.2V			0.3	1	µA
PGOOD Threshold Percentage	Referenced to Feedback Voltage Falling		–7	–10	–13	%
PGOOD Low Voltage	I_{PGOOD} = 1mA V_{OUT} = 1.6V, I_{PGOOD} = 1mA			0.05 0.05	0.1 0.2	V V
PGOOD Leakage Current	V_{PGOOD} = 5.5V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3528B-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3528BE-2 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 76°C/W is the package thermal impedance.

Note 3: Specification is guaranteed by design and not 100% tested in production.

Note 4: Current measurements are made when the output is not switching.

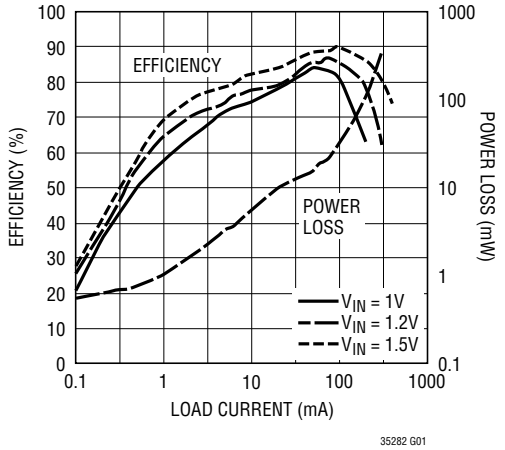
Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 6: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much higher than 76°C/W.

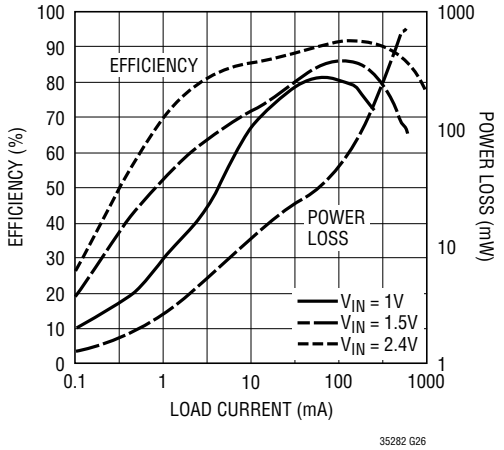
Note 7: The IC is tested in a feedback loop to make the measurement.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

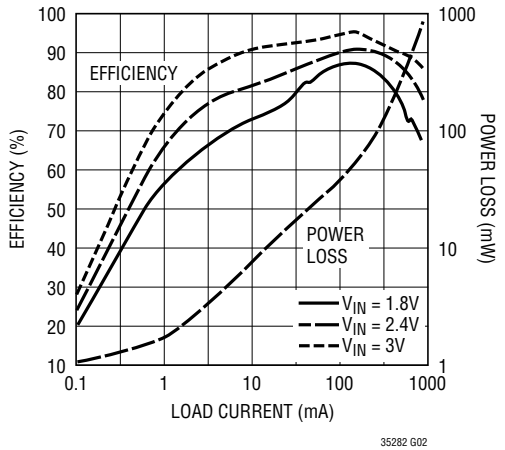
Efficiency vs Load Current and V_{IN} for V_{OUT} = 1.8V



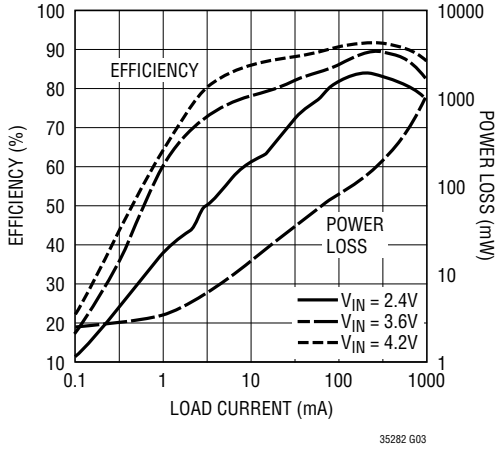
Efficiency vs Load Current and V_{IN} for V_{OUT} = 3V



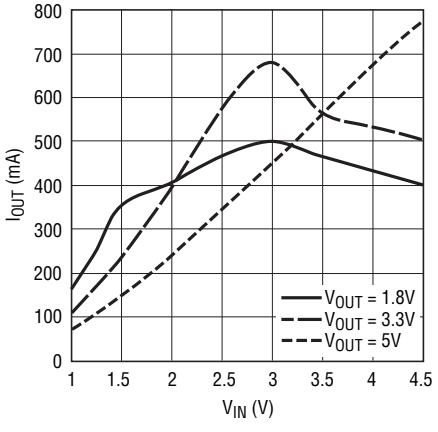
Efficiency vs Load Current and V_{IN} for V_{OUT} = 3.3V



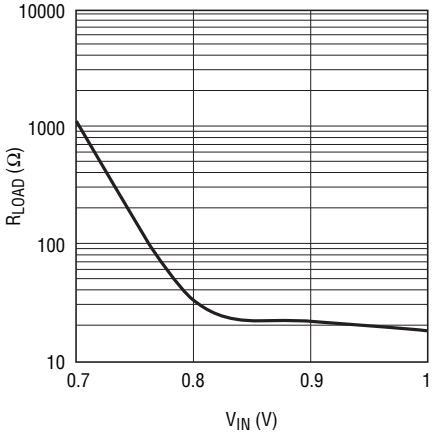
Efficiency vs Load Current and V_{IN} for V_{OUT} = 5V



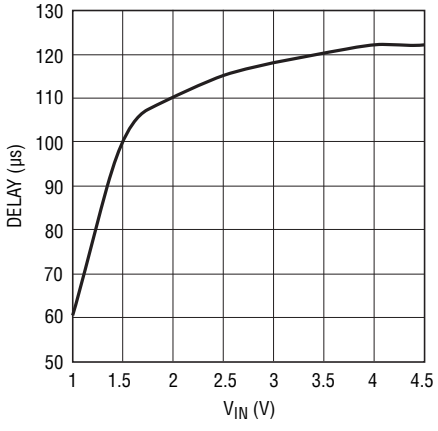
Maximum Output Current vs V_{IN}



Minimum Load Resistance During Start-Up vs V_{IN}

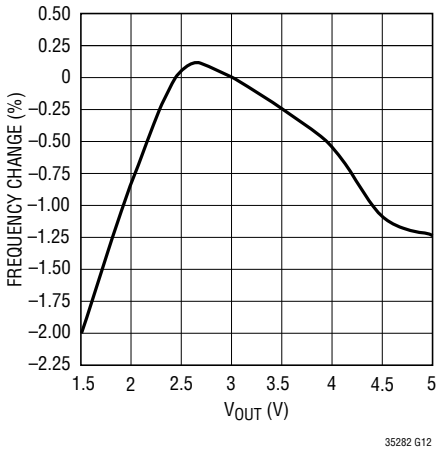


Start-Up Delay Time vs V_{IN}

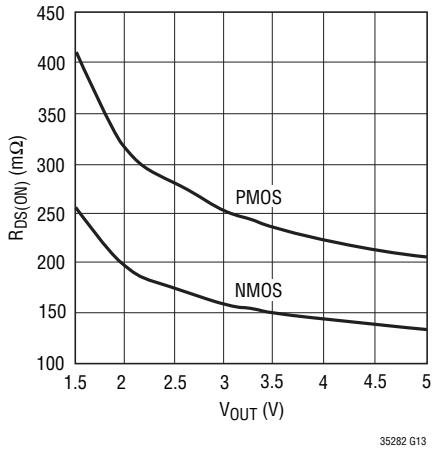


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

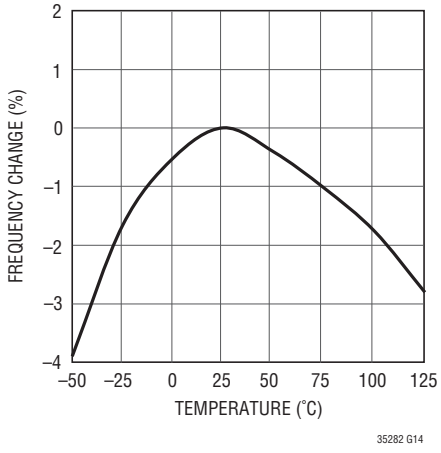
Oscillator Frequency Change vs V_{OUT}



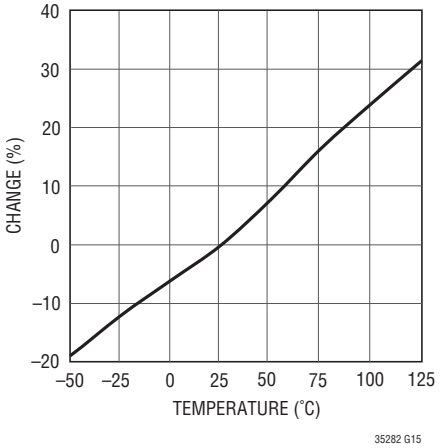
$R_{DS(ON)}$ vs V_{OUT}



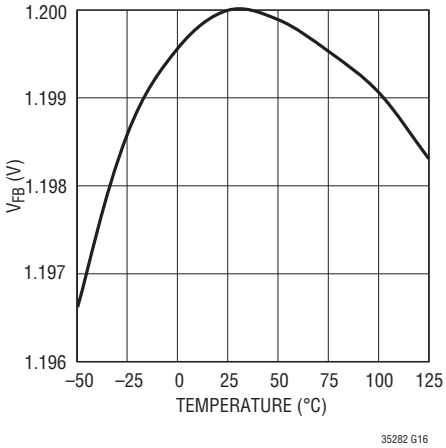
Oscillator Frequency Change vs Temperature



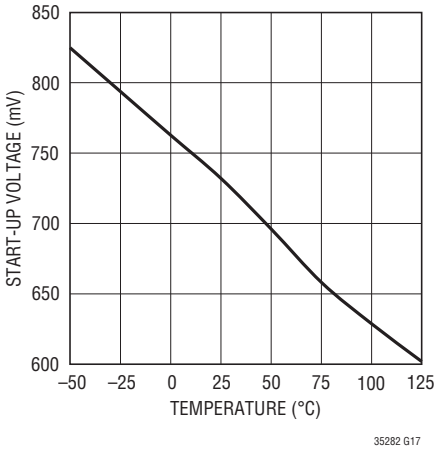
$R_{DS(ON)}$ Change vs Temperature



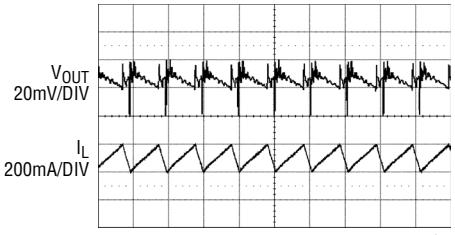
V_{FB} vs Temperature



Start-Up Voltage vs Temperature

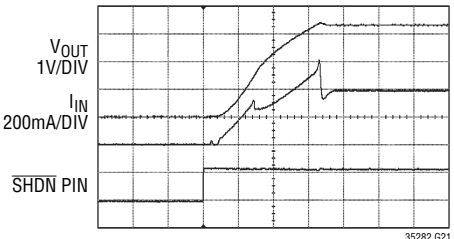


Fixed Frequency V_{OUT} Ripple and Inductor Current Waveforms



V_{IN} = 1.2V 500ns/DIV
V_{OUT} = 3.3V
C_{OUT} = 10µF
C_{FF} = 33pF
I_{OUT} = 100mA
L = 2.2µH

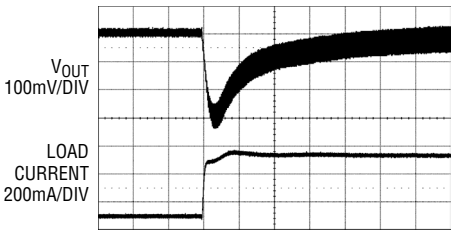
V_{OUT} and I_{IN} During Soft-Start



V_{IN} = 1.2V 200µs/DIV
V_{OUT} = 3.3V
C_{OUT} = 10µF
L = 2.2µH

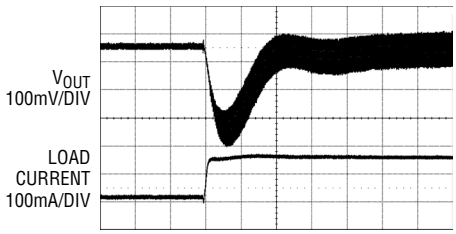
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Load Step Response (3.6V to 5V)



V_{IN} = 3.6V 20µs/DIV
V_{OUT} = 5V
C_{OUT} = 10µF
L = 2.2µH
LOAD CURRENT = 100mA TO 550mA

Load Step Response (1.2V to 3.3V)



V_{IN} = 1.2V 20µs/DIV
V_{OUT} = 3.3V
C_{OUT} = 10µF
L = 2.2µH
LOAD CURRENT = 20mA TO 170mA

PIN FUNCTIONS

$\overline{SHDN}$ (Pin 1): Logic Controlled Shutdown Input. There is an internal 4MΩ pull-down resistor on this pin.

- $\overline{SHDN}$ = High: Normal operation
- $\overline{SHDN}$ = Low: Shutdown, quiescent current < 1µA

FB (Pin 2): Feedback Input. Connect resistor divider tap to this pin. The output voltage can be adjusted from 1.6V to 5.25V by:

$$V_{OUT} = 1.20V \bullet \left(1 + \frac{R2}{R1}\right)$$

PGOOD (Pin 3): Power Good Comparator Output. This open-drain output is low when V_{FB} < 10% from its regulation voltage.

V_{OUT} (Pin 4): Output Voltage Sense and Drain Connection of the Internal Synchronous Rectifier. PCB trace length from V_{OUT} to the output filter capacitor (4.7µF minimum) should be as short and wide as possible.

SW (Pin 5): Switch Pin. Connect inductor between SW and V_{IN}. Keep PCB trace lengths as short and wide as possible to reduce EMI. If the inductor current falls to zero, or $\overline{SHDN}$ is low, an internal anti-ringing switch is connected from SW to V_{IN} to minimize EMI.

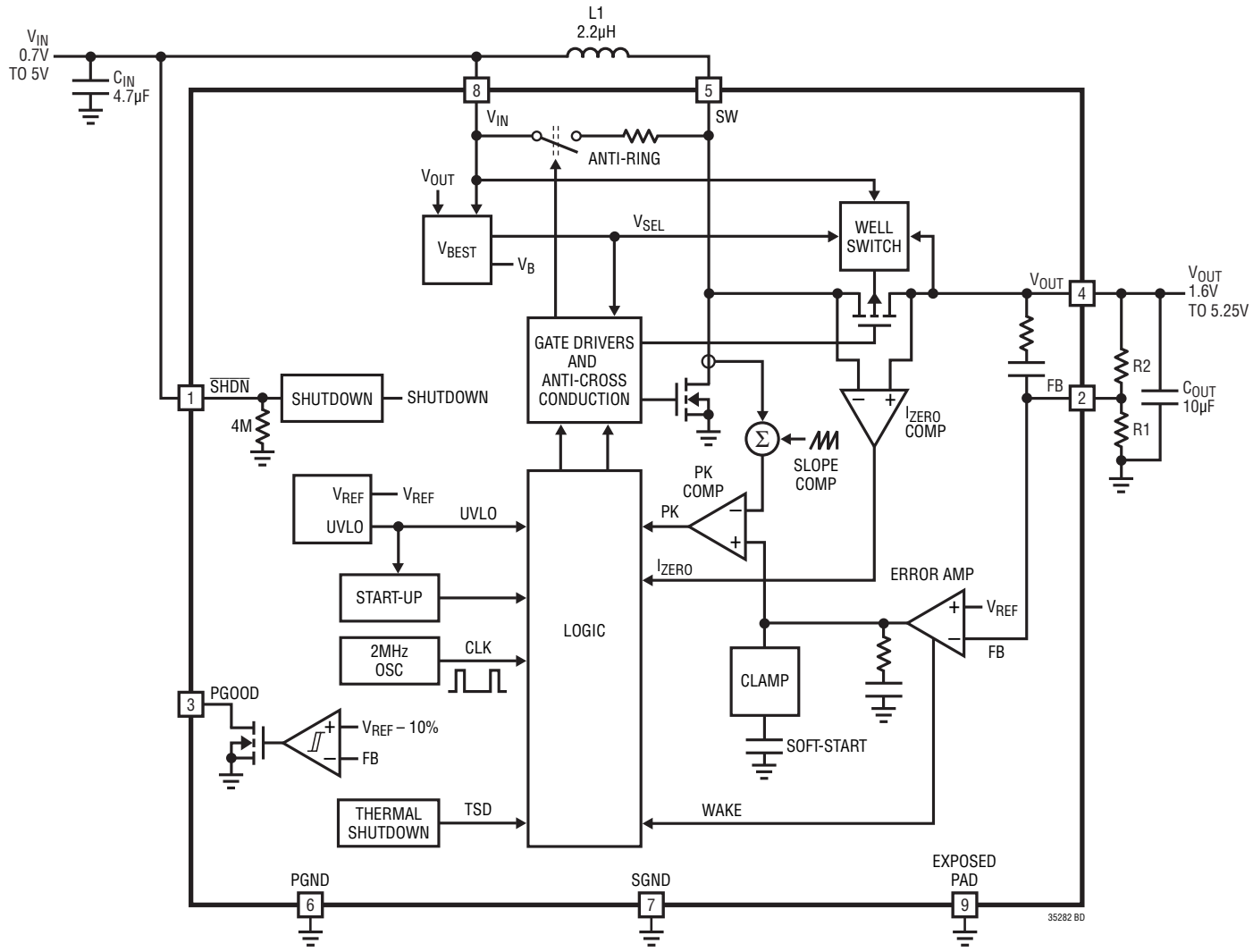
PGND (Pin 6): Power Ground. Provide a short direct PCB path between PGND and the (–) side of the input and output capacitors.

SGND (Pin 7): Signal Ground. Provide a short direct PCB path between SGND and the (–) side of the input and output capacitors.

V_{IN} (Pin 8): Battery Input Voltage. Connect a minimum of 1µF ceramic decoupling capacitor from this pin to ground.

GND (Exposed Pad Pin 9): The exposed pad must be soldered to the PCB ground plane. It serves as another ground connection and as a means of conducting heat away from the die.

BLOCK DIAGRAM



OPERATION (Refer to Block Diagram)

The LTC3528B-2 is a 2MHz synchronous boost converter housed in an 8-lead 3mm × 2mm DFN package. With the ability to start-up and operate from inputs less than 0.88V, the device features fixed frequency, current mode PWM control for exceptional line and load regulation. The current mode architecture with adaptive slope compensation provides excellent transient load response and requires minimal output filtering. Internal soft-start and internal loop compensation simplifies the design process while minimizing the number of external components.

With its low $R_{DS(ON)}$ and low gate charge internal N-channel MOSFET switch and P-channel MOSFET synchronous rectifier, the LTC3528-2 achieves high efficiency over a wide range of load current. The LTC3528B-2 features continuous PWM operation at 2MHz. At very light loads, the LTC3528B-2 will exhibit pulse-skip operation. Operation can be best understood by referring to the Block Diagram.

LOW VOLTAGE START-UP

The LTC3528B-2 includes an independent start-up oscillator designed to operate at an input voltage of 0.70V (typical). Soft-start and inrush current limiting are provided during start-up, as well as normal operating mode.

When either V_{IN} or V_{OUT} exceeds 1.6V typical, the IC enters normal operating mode. Once the output voltage exceeds the input by 0.24V, the IC powers itself from V_{OUT} instead of V_{IN}. At this point the internal circuitry has no dependency on the V_{IN} input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop as low as 0.5V. The limiting factor for the application becomes the availability of the power source to supply sufficient power to the output at the low voltages, and the maximum duty cycle, which is clamped at 92% typical. Note that at low input voltages, small voltage drops due to series resistance become critical, and greatly limit the power delivery capability of the converter.

LOW NOISE FIXED FREQUENCY OPERATION

Soft-Start

The LTC3528B-2 contains internal circuitry to provide soft-start operation. The internal soft-start circuitry slowly ramps the peak inductor current from zero to its peak value of 1.5A (typical), allowing start-up into heavy loads. The soft-start time is approximately 0.5ms. The soft-start circuitry is reset in the event of a commanded shutdown or a thermal shutdown.

Oscillator

An internal oscillator sets the frequency of operation to 2MHz.

Shutdown

The converter is shut down by pulling the $\overline{SHDN}$ pin below 0.25V, and activated by pulling $\overline{SHDN}$ above 0.88V. Although $\overline{SHDN}$ can be driven above V_{IN} or V_{OUT} (up to the absolute maximum rating) without damage, the LTC3528B-2 has a proprietary test mode that may be engaged if $\overline{SHDN}$ is held in the range of 0.5V to 1V higher than the greater of V_{IN} or V_{OUT}. If the test mode is engaged, normal PWM switching action is interrupted, which can cause undesirable operation in some applications. Therefore, in applications where $\overline{SHDN}$ may be driven above V_{IN}, a resistor divider or other means must be employed to keep the $\overline{SHDN}$ voltage below (V_{IN} + 0.4V) to prevent the possibility of the test mode being engaged. Please refer to Figure 1 for two possible implementations

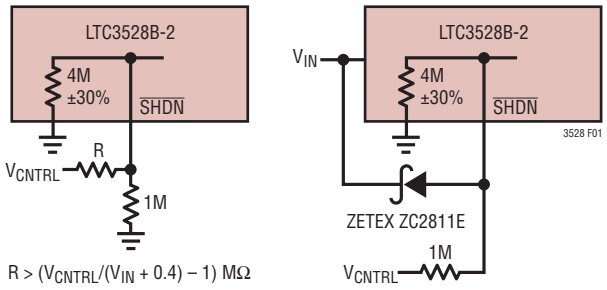


Figure 1. Recommended Shutdown Circuits when Driving $\overline{SHDN}$ Above V_{IN}

OPERATION (Refer to Block Diagram)

Error Amplifier

The error amplifier is a transconductance type. The noninverting input is internally connected to the 1.20V reference and the inverting input is connected to FB. Clamps limit the minimum and maximum error amp output voltage for improved large-signal transient response. Power converter control loop compensation is provided internally. A voltage divider from V_{OUT} to ground programs the output voltage via FB from 1.6V to 5.25V.

$$V_{OUT} = 1.20V \bullet \left(1 + \frac{R2}{R1}\right)$$

Current Sensing

Lossless current sensing converts the peak current signal of the N-channel MOSFET switch into a voltage which is summed with the internal slope compensation. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM.

Current Limit

The current limit comparator shuts off the N-channel MOSFET switch once its threshold is reached. The current limit comparator delay to output is typically 60ns. Peak switch current is limited to approximately 1.5A, independent of input or output voltage, unless V_{OUT} falls below 0.7V, in which case the current limit is cut in half.

Zero Current Comparator

The zero current comparator monitors the inductor current to the output and shuts off the synchronous rectifier when this current reduces to approximately 20mA. This prevents the inductor current from reversing in polarity, improving efficiency at light loads.

Synchronous Rectifier

To control inrush current and to prevent the inductor current from running away when V_{OUT} is close to V_{IN}, the P-channel MOSFET synchronous rectifier is only enabled when $V_{OUT} > (V_{IN} + 0.24V)$.

Anti-Ringing Control

The anti-ringing control connects a resistor across the inductor to prevent high frequency ringing on the SW pin during discontinuous current mode operation. The ringing of the resonant circuit formed by L and C_{SW} (capacitance on SW pin) is low energy, but can cause EMI radiation.

Output Disconnect

The LTC3528B-2 is designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifier. This allows for V_{OUT} to go to zero volts during shutdown, drawing no current from the input source. It also enables inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, a Schottky diode cannot be connected between SW and V_{OUT}. The output disconnect feature also allows V_{OUT} to be forced above the programmed regulation voltage, without any reverse current into a battery on V_{IN}.

Thermal Shutdown

If the die temperature exceeds 160°C, the LTC3528B-2 enters thermal shutdown. All switches will be turned off and the soft-start capacitor will be discharged. The device will be enabled again when the die temperature drops by approximately 15°C.

APPLICATIONS INFORMATION

V_{IN} > V_{OUT} OPERATION

The LTC3528B-2 maintains voltage regulation even when the input voltage is above the desired output voltage. Note that the efficiency is much lower in this mode, and the maximum output current capability will be less. Refer to the Typical Performance Characteristics.

SHORT-CIRCUIT PROTECTION

The LTC3528B-2 output disconnect feature allows an output short circuit while maintaining a maximum internally set current limit. To reduce power dissipation under short-circuit conditions, the peak switch current limit is reduced to 750mA (typical).

SCHOTTKY DIODE

Although not required, adding a Schottky diode from SW to V_{OUT} will improve efficiency by about 2%. Note that this defeats the output disconnect and short-circuit protection features.

PCB LAYOUT GUIDELINES

The high speed operation of the LTC3528B-2 demands careful attention to board layout. A careless layout will not produce the advertised performance. Figure 2 shows the recommended component placement. A large ground copper area with the package backside metal pad properly soldered will help to lower the chip temperature. A multi-layer board with a separate ground plane is ideal, but not absolutely necessary.

COMPONENT SELECTION

Inductor Selection

The LTC3528B-2 can utilize small surface mount chip inductors due to their fast 2MHz switching frequency. Inductor values between 1.5µH and 3.3µH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10µH will increase size while providing little improvement in output current capability.

The minimum inductance value is given by:

$$L > \frac{V_{IN(MIN)} \bullet \left(V_{OUT(MAX)} - V_{IN(MIN)}\right)}{2 \bullet Ripple \bullet V_{OUT(MAX)}} \ \mu H$$

where:

Ripple = Allowable inductor current ripple (amps peak-peak)

$V_{IN(MIN)}$ = Minimum input voltage

$V_{OUT(MAX)}$ = Maximum output voltage

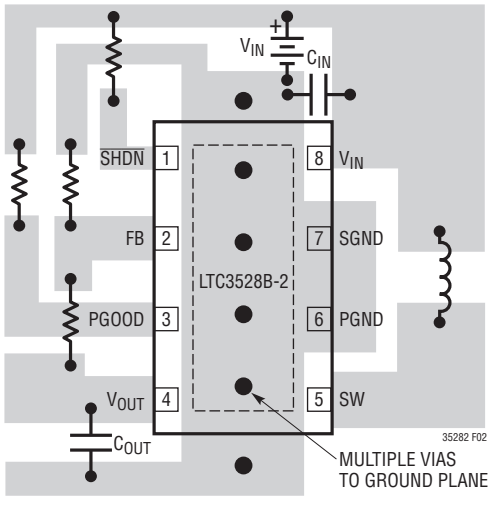


Figure 2. Recommended Component Placement for Single Layer Board

APPLICATIONS INFORMATION

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the I^2R power losses, and must be able to handle the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core area to support the peak inductor currents of 1.5A seen on the LTC3528B-2. To minimize radiated noise, use a shielded inductor. See Table 1 for suggested components and suppliers.

Table 1. Recommended Inductors

VENDOR	PART/STYLE
Coilcraft (847) 639-6400 www.coilcraft.com	DO1606T, MSS5131, MSS5121 MSS6122, MOS6020 ME3220, DO1608C 1812PS
Coiltronics	SD12, SD14, SD20 SD25, SD52
Sumida (847) 956-0666 www.sumida.com	CD43 CDC5D23B CDRH5D18
TDK	VLP, VLF VLCF, SLF, VLS
Toko (408) 432-8282 www.tokoam.com	D53, D62, D63 D73, D75
Wurth (201) 785-8800 www.we-online.com	WE-TPC type M, MH

Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 10µF to 22µF output capacitor is sufficient for most applications. Values larger than 22µF may be used to obtain extremely low output voltage ripple and improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used.

The internal loop compensation of the LTC3528B-2 is designed to be stable with output capacitor values of 10µF or greater. Although ceramic capacitors are recommended, low ESR tantalum capacitors may be used as well.

A small ceramic capacitor in parallel with a larger tantalum capacitor may be used in demanding applications which have large load transients. Another method of improving the transient response is to add a small feed-forward capacitor across the top resistor of the feedback divider (from V_{OUT} to FB). A typical value of 33pF will generally suffice.

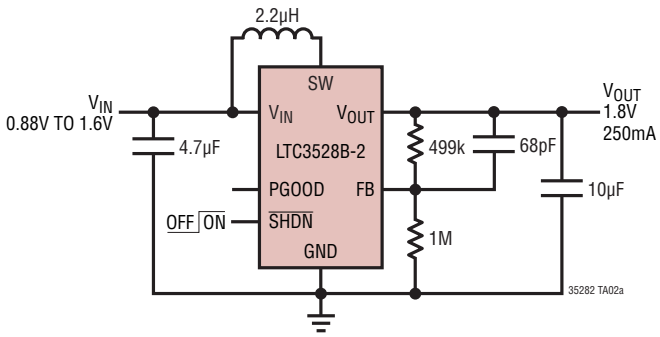
Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 10µF input capacitor is sufficient for most applications. Larger values may be used without limitations. Table 2 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers directly for detailed information on their selection of ceramic parts.

Table 2. Capacitor Vendor Information

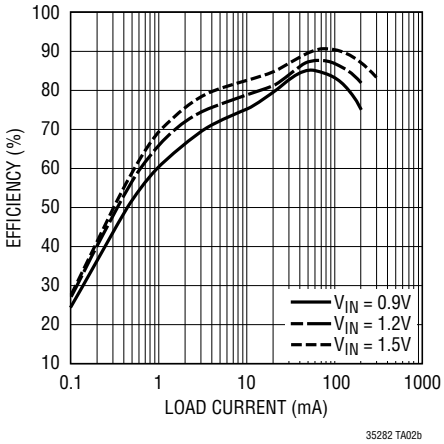
SUPPLIER	PHONE	WEBSITE
AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com
Taiyo-Yuden	(408) 573-4150	www.t-yuden.com
TDK	(847) 803-6100	www.component.tdk.com

TYPICAL APPLICATIONS

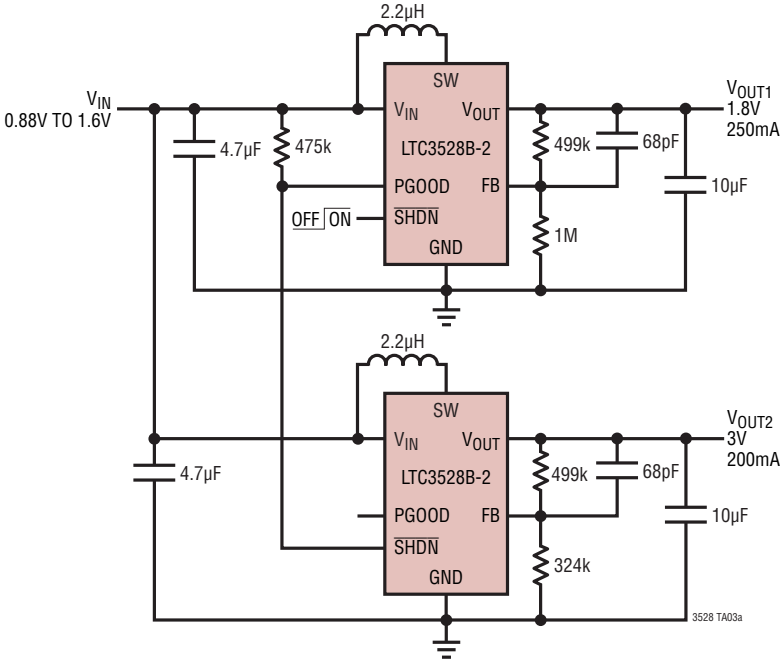
1 Cell to 1.8V



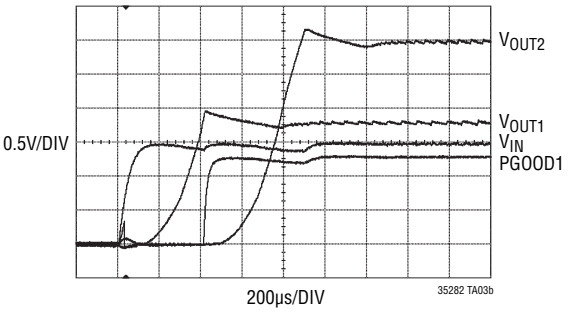
Efficiency



Dual 1 Cell to 1.8V, 3V Sequenced Supply

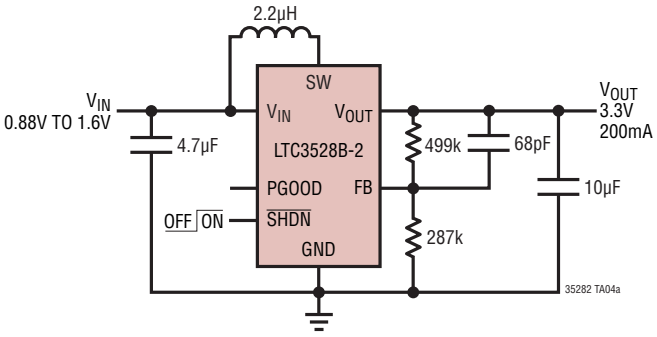


Output Voltage Sequencing

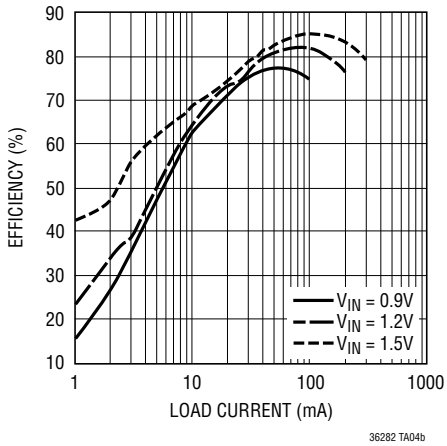


TYPICAL APPLICATIONS

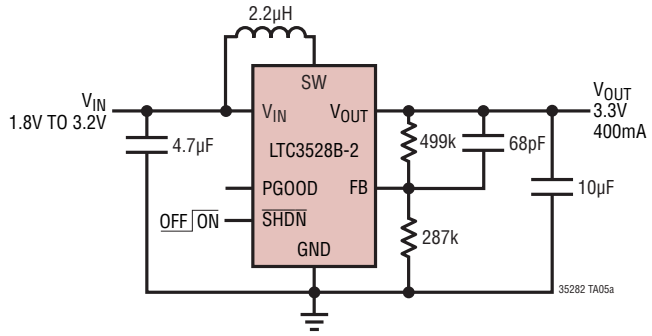
1 Cell to 3.3V



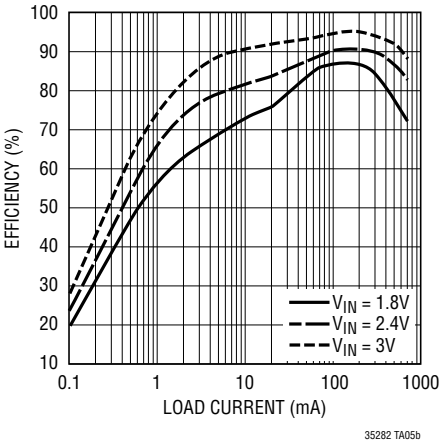
Efficiency



2 Cell to 3.3V

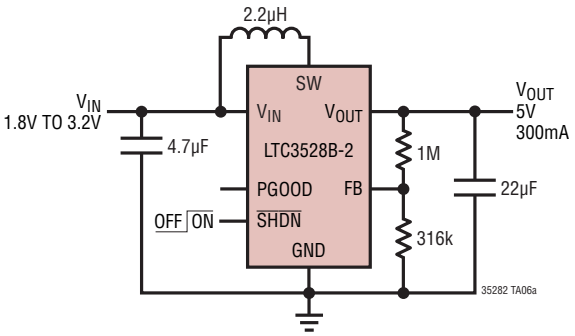


Efficiency



TYPICAL APPLICATIONS

2 Cell to 5V



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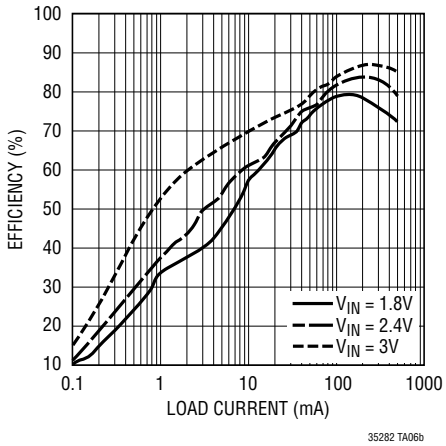
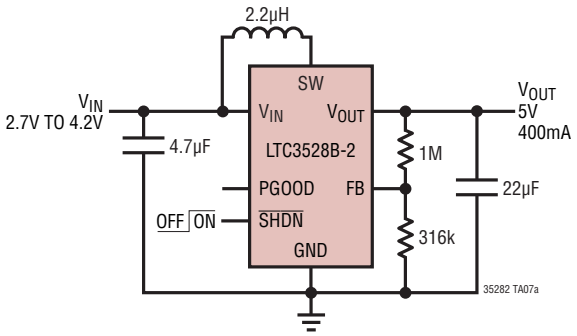
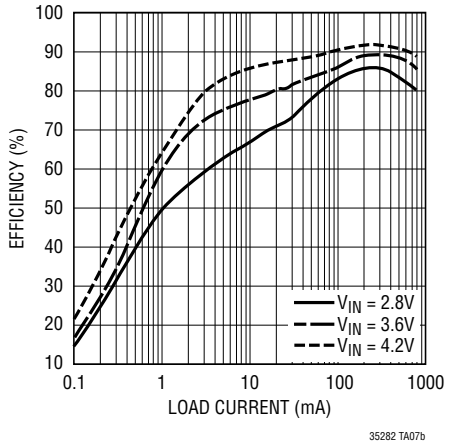


TYPICAL APPLICATIONS

Li-Ion to 5V

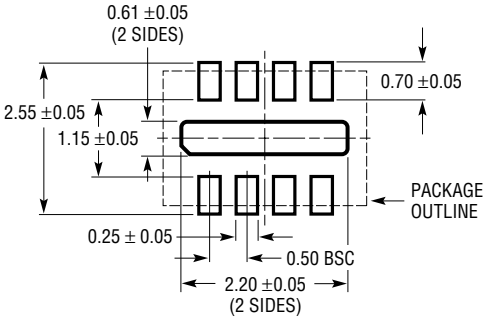


Efficiency

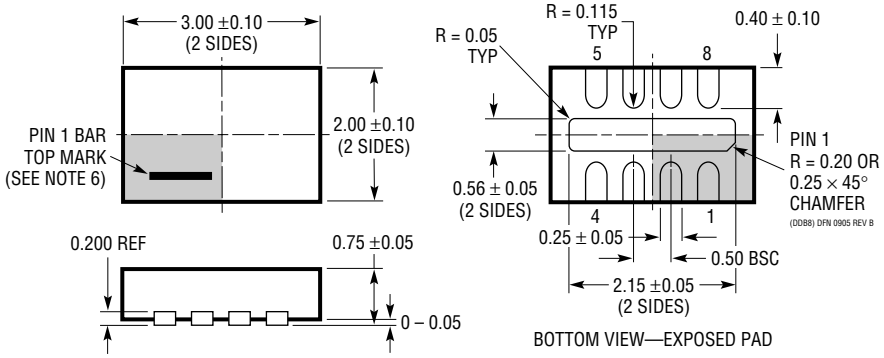


PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/11	Change to Operating Temperature Range	2
		Update to Note 2 reflected in Electrical Characteristics	2, 3
		Replaced graphs G14, G15, G16 and G17	5
		Operations section update Pin 9 to read GND	6
		Operations section update to Shutdown	8