Linear USB Battery Charger with Buck and Buck-Boost Regulators

FEATURES

Battery Charger

- **Standalone USB Charger**
- **Up to 950mA Charge Current Programmable via Single Resistor**
- HPWR Input Selects 20% or 100% of Programmed Charge Current
- NTC Input for Temperature Qualified Charging
- Internal Timer Termination
- Bad Battery Detection

Switching Regulators (Buck and Buck-Boost)

- **Up to 400mA Output Current per Regulator**
- **2.25MHz Constant-Frequency Operation**
- Power Saving Burst Mode® Operation
- Low Profile, 20-Lead, 3mm × 3mm QFN Package

APPLICATIONS

- SD/Flash-Based MP3 Players
- Low Power Handheld Applications

DESCRIPTION

The LTC®3558 is a USB battery charger with dual high efficiency switching regulators. The device is ideally suited to power single-cell Li-Ion/Polymer based handheld applications needing multiple supply rails.

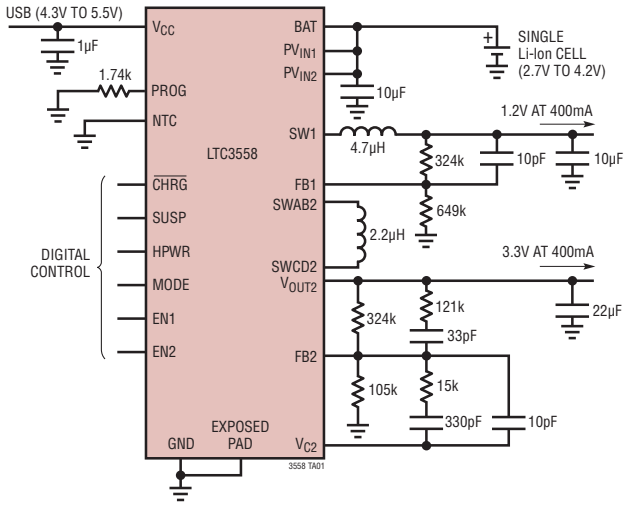
Battery charge current is programmed via the PROG pin and the HPWR pin with capability up to 950mA of current at the BAT pin. The $\overline{CHRG}$ pin allows battery status to be monitored continuously during the charging process. An internal timer controls charger termination.

The part includes monolithic synchronous buck and buck-boost regulators that can provide up to 400mA of output current each and operate at efficiencies greater than 90% over the entire Li-Ion/Polymer battery range. The buck-boost regulator can regulate its programmed output voltage at its rated deliverable current over the entire Li-Ion range without drop out, increasing battery runtime.

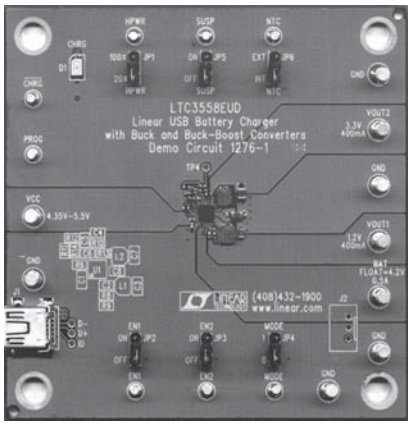
The LTC3558 is offered in a low profile (0.75mm), thermally enhanced, 20-lead (3mm × 3mm) QFN package.

TYPICAL APPLICATION

USB Charger Plus Buck Regulator and Buck-Boost Regulator



Demo Board

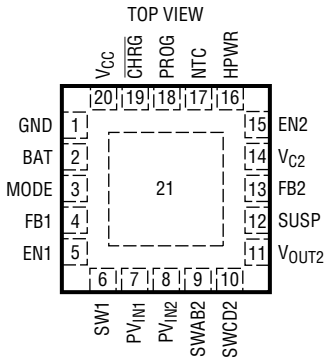


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} (Transient);
t < 1ms and Duty Cycle < 1%..... –0.3V to 7V
V_{CC} (Static) ..... –0.3V to 6V
BAT, CHRG ..... –0.3V to 6V
PROG, SUSP.....–0.3V to (V_{CC} + 0.3V)
HPWR, NTC.....–0.3V to Max (V_{CC}, BAT) + 0.3V
PROG Pin Current 1.25mA
BAT Pin Current 1A
PV_{IN1}, PV_{IN2} .....–0.3V to (BAT + 0.3V)
EN1, EN2, MODE, V_{OUT2} ..... –0.3V to 6V
FB1, SW1 ..... –0.3V to (PV_{IN1} + 0.3V) or 6V
FB2, V_{C2}, SWAB2 ..... –0.3V to (PV_{IN2} + 0.3V) or 6V
SWCD2 .....–0.3V to (V_{OUT2} + 0.3V) or 6V
I_{SW1} .....600mA DC
I_{SWAB2}, I_{SWCD2}, I_{VOUT2}.....750mA DC
Junction Temperature (Note 2) .....125°C
Operating Temperature Range (Note 3).... –40°C to 85°C
Storage Temperature..... –65°C to 125°C

PIN CONFIGURATION



UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3558EUD#PBF	LTC3558EUD#TRPBF	LDCD	20-Lead (3mm × 3mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, BAT = PV_{IN1} = PV_{IN2} = 3.6V, R_{PROG} = 1.74k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
V_{CC}	Input Supply Voltage		●	4.3		5.5	V
I_{VCC}	Battery Charger Quiescent Current (Note 4)	Standby Mode, Charge Terminated Suspend Mode, V_{SUSP} = 5V			285 8.5	400 17	µA µA
V_{FLOAT}	BAT Regulated Output Voltage	 0°C ≤ T_A ≤ 85°C		4.179 4.165	4.200 4.200	4.221 4.235	V V
I_{CHG}	Constant-Current Mode Charge Current	HPWR = 1 HPWR = 0	●	440 84	460 92	500 100	mA mA
I_{BAT}	Battery Drain Current	Standby Mode, Charger Terminated, EN1 = EN2 = 0 Shutdown, V_{CC} < V_{UVLO}, BAT = 4.2V, EN1 = EN2 = 0 Suspend Mode, SUSP = 5V, BAT = 4.2V, EN1 = EN2 = 0 V_{CC} = 0V, EN1 = EN2 = 1, MODE = 1, FB1 = FB2 = 0.85V, V_{OUT2} = 3.6V			–3.5 –2.5 –1.5 –50	–7 –4 –3 –100	µA µA µA µA
V_{UVLO}	Undervoltage Lockout Threshold	BAT = 3.5V, V_{CC} Rising		3.85	4	4.125	V
ΔV_{UVLO}	Undervoltage Lockout Hysteresis	BAT = 3.5V			200		mV
V_{DUVLO}	Differential Undervoltage Lockout Threshold	BAT = 4.05V, (V_{CC} – BAT) Falling		30	50	70	mV
ΔV_{DUVLO}	Differential Undervoltage Lockout Hysteresis	BAT = 4.05V			130		mV
V_{PROG}	PROG Pin Servo Voltage	HPWR = 1 HPWR = 0 BAT < V_{TRKL}			1.000 0.200 0.100		V V V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				800		mA/mA
I_{TRKL}	Trickle Charge Current	BAT < V_{TRKL}		36	46	56	mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.8	2.9	3	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				100		mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–95	–115	mV
t_{RECHRG}	Recharge Comparator Filter Time	BAT Falling			1.7		ms
t_{TERM}	Safety Timer Termination Period	BAT = V_{FLOAT}		3.5	4	4.5	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.4	0.5	0.6	Hour
$h_{C/10}$	End-of-Charge Indication Current Ratio	(Note 5)		0.085	0.1	0.11	mA/mA
$t_{C/10}$	End-of-Charge Comparator Filter Time	I_{BAT} Falling			2.2		ms
$R_{ON(CHG)}$	Battery Charger Power FET On-Resistance (Between V_{CC} and BAT)	I_{BAT} = 190mA			500		mΩ
T_{LIM}	Junction Temperature in Constant Temperature Mode				105		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising NTC Voltage Hysteresis		75	76.5 1.6	78	%V_{CC} %V_{CC}
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling NTC Voltage Hysteresis		33.4	34.9 1.6	36.4	%V_{CC} %V_{CC}
V_{DIS}	NTC Disable Threshold Voltage	Falling NTC Voltage Hysteresis	●	0.7	1.7 50	2.7	%V_{CC} mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{CC} = 5V		–1		1	µA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic (HPWR, SUSP, $\overline{CHRG}$, EN1, EN2, MODE)							
V_{IL}	Input Low Voltage	HPWR, SUSP, MODE, EN1, EN2 Pins				0.4	V
V_{IH}	Input High Voltage	HPWR, SUSP, MODE, EN1, EN2 Pins		1.2			V
R_{DN}	Logic Pin Pull-Down Resistance	HPWR, SUSP Pins	●	1.9	4	6.3	MΩ
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			100	250	mV
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Input Current	BAT = 4.5V, $V_{\overline{CHRG}}$ = 5V			0	1	µA
Buck Switching Regulator							
PV_{IN1}	Input Supply Voltage		●	2.7		4.2	V
I_{PVIN1}	Pulse Skip Input Current Burst Mode Current Shutdown Current Supply Current in UVLO	FB1 = 0.85V, MODE = 0 (Note 6) FB1 = 0.85V, MODE = 1 (Note 6) EN1 = 0 PV_{IN1} = PV_{IN2} = 2V	 ● 		220 35 0 4	400 50 2 8	µA µA µA µA
PV_{IN1} UVLO	PV_{IN1} Falling PV_{IN1} Rising		● ●	2.30	2.45 2.55	 2.70	V V
f_{OSC}	Switching Frequency	MODE = 0		1.91	2.25	2.59	MHz
I_{LIMSW1}	Peak PMOS Current Limit			550	800	1050	mA
V_{FB1}	Feedback Voltage	MODE = 0	●	780	800	820	mV
I_{FB1}	FB Input Current	FB1 = 0.85V		–50		50	nA
D_{MAX1}	Maximum Duty Cycle	FB1 = 0V	●	100			%
R_{PMOS1}	$R_{DS(ON)}$ of PMOS	I_{SW1} = 100mA			0.65		Ω
R_{NMOS1}	$R_{DS(ON)}$ of NMOS	I_{SW1} = –100mA			0.75		Ω
$R_{SW1(PD)}$	SW Pull-Down in Shutdown				13		kΩ
Buck-Boost Switching Regulator							
PV_{IN2}	Input Supply Voltage		●	2.7		4.2	V
I_{PVIN2}	PWM Input Current Burst Mode Input Current Shutdown Current Supply Current in UVLO	MODE = 0, I_{OUT} = 0A, FB2 = 0.85V (Note 6) MODE = 1, I_{OUT} = 0A, FB2 = 0.85V (Note 6) EN2 = 0, I_{OUT} = 0A PV_{IN1} = PV_{IN2} = 2V			220 20 0 4	400 30 1 8	µA µA µA µA
PV_{IN2} UVLO	PV_{IN2} Falling PV_{IN2} Rising		● ●	2.30	2.45 2.55	 2.70	V V
$V_{OUT2(LOW)}$	Minimum Regulated Buck-Boost V_{OUT}				2.65	2.75	V
$V_{OUT2(HIGH)}$	Maximum Regulated Buck-Boost V_{OUT}			5.45	5.60		V
I_{LIMF2}	Forward Current Limit (Switch A)	MODE = 0	●	580	700	820	mA
$I_{PEAK2(BURST)}$	Forward Current Limit (Switch A)	MODE = 1	●	180	250	320	mA
I_{LIMR2}	Reverse Current Limit (Switch D)	MODE = 0	●	325	450	575	mA
$I_{ZERO2(BURST)}$	Reverse Current Limit (Switch D)	MODE = 1	●	–35	0	35	mA
$I_{MAX2(BURST)}$	Maximum Deliverable Output Current in Burst Mode Operation	2.7V < PV_{IN2} < 4.2V 2.75V < V_{OUT2} < 5.5V		50			mA
V_{FB2}	Feedback Servo Voltage		●	780	800	820	mV
I_{FB2}	FB2 Input Current	FB2 = 0.85V		–50		50	nA
f_{OSC}	Switching Frequency	MODE = 0		1.91	2.25	2.59	MHz

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$R_{DSP(ON)}$	PMOS $R_{DS(ON)}$	V_{OUT} = 3.6V			0.6		Ω
$R_{DSN(ON)}$	NMOS $R_{DS(ON)}$				0.6		Ω
$I_{LEAK(P)}$	PMOS Switch Leakage	Switches A, D		–1		1	µA
$I_{LEAK(N)}$	NMOS Switch Leakage	Switches B, C		–1		1	µA
$DC_{BUCK(MAX)}$	Maximum Buck Duty Cycle	MODE = 0	●	100			%
$DC_{BOOST(MAX)}$	Maximum Boost Duty Cycle	MODE = 0			75		%
t_{SS2}	Soft-Start Time				0.5		ms
$R_{OUT(PD)}$	V_{OUT} Pull-Down in Shutdown				10		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

Note 3: The LTC3558E is guaranteed to meet specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

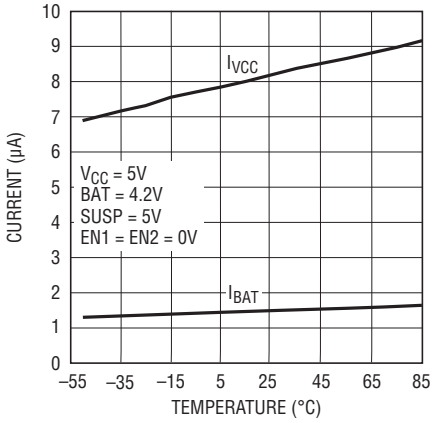
Note 4: V_{CC} supply current does not include current through the PROG pin or any current delivered to the BAT pin. Total input current is equal to this specification plus 1.00125 • I_{BAT} where I_{BAT} is the charge current.

Note 5: $I_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

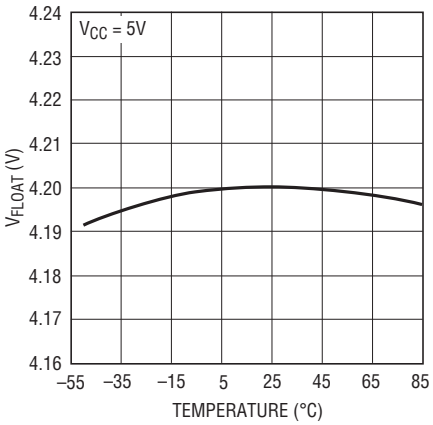
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Suspend State Supply and BAT Currents vs Temperature



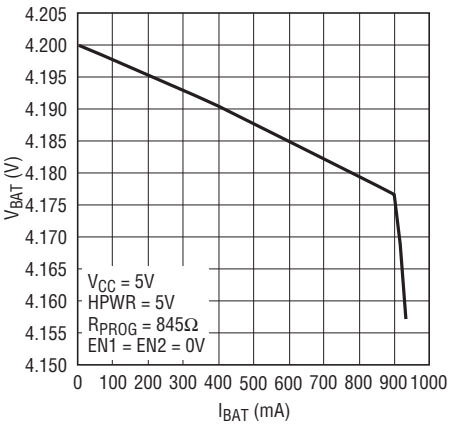
3558 G01

Battery Regulation (Float) Voltage vs Temperature



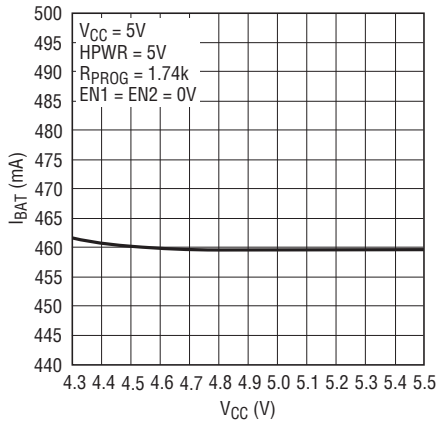
3558 G02

Battery Regulation (Float) Voltage vs Battery Charge Current, Constant-Voltage Charging



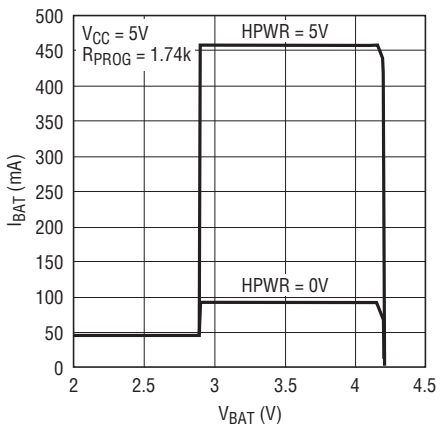
3558 G03

Battery Charge Current vs Supply Voltage



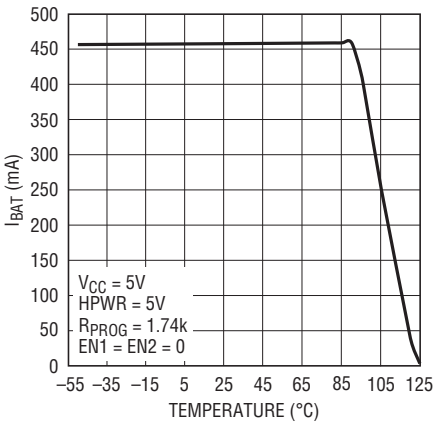
3558 G04

Battery Charge Current vs Battery Voltage



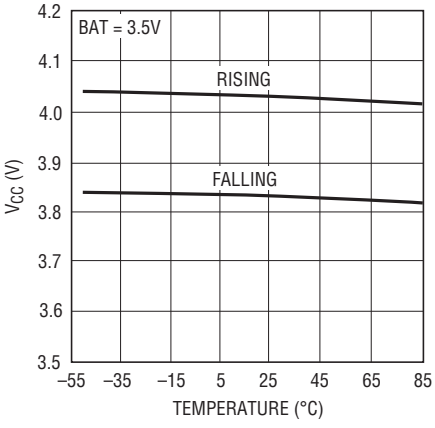
3558 G05

Battery Charge Current vs Ambient Temperature in Thermal Regulation



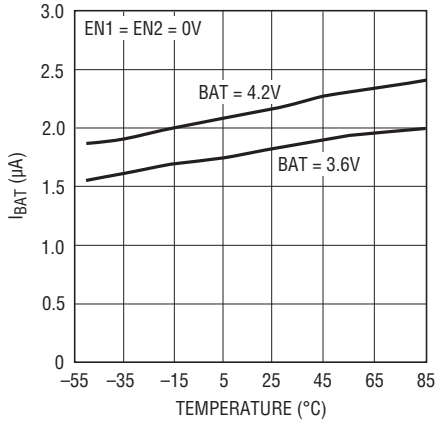
3558 G06

Battery Charger Undervoltage Lockout Threshold vs Temperature



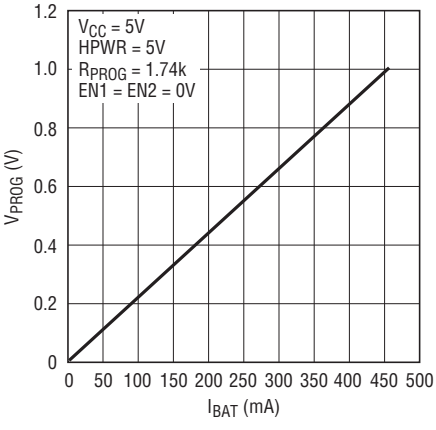
3558 G07

Battery Drain Current in Undervoltage Lockout vs Temperature



3558 G08

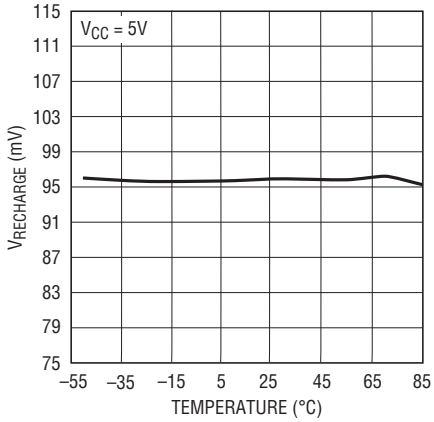
PROG Voltage vs Battery Charge Current



3558 G09

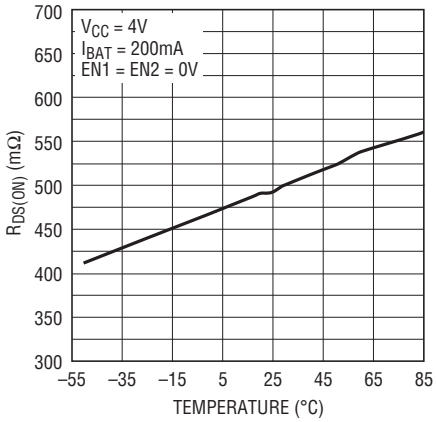
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Recharge Threshold vs Temperature



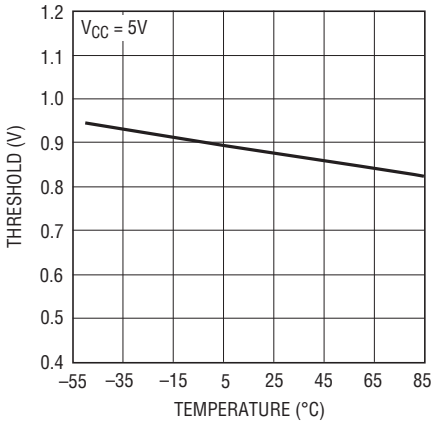
3558 G10

Battery Charger FET On-Resistance vs Temperature



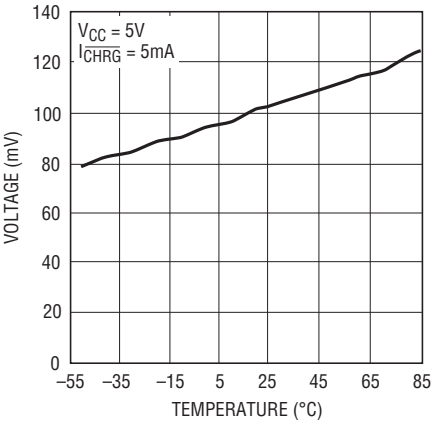
3558 G11

SUSP/HPWR Pin Rising Thresholds vs Temperature



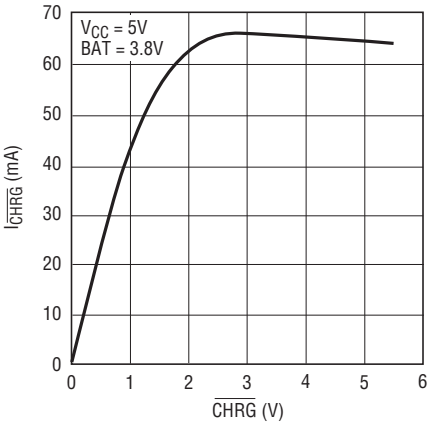
3558 G12

$\overline{CHRG}$ Pin Output Low Voltage vs Temperature



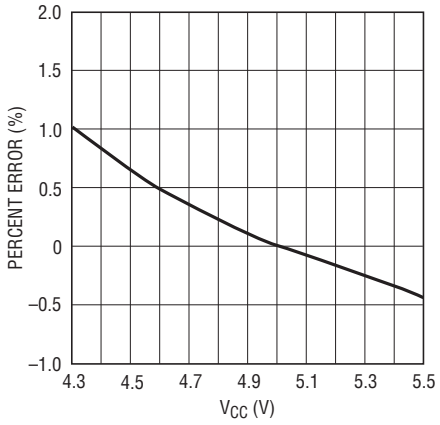
3558 G13

$\overline{CHRG}$ Pin I-V Curve



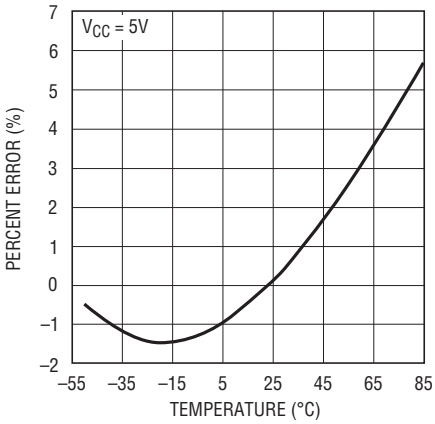
3558 G14

Timer Accuracy vs Supply Voltage



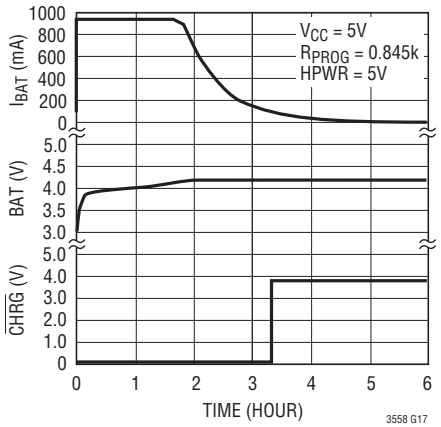
3558 G15

Timer Accuracy vs Temperature



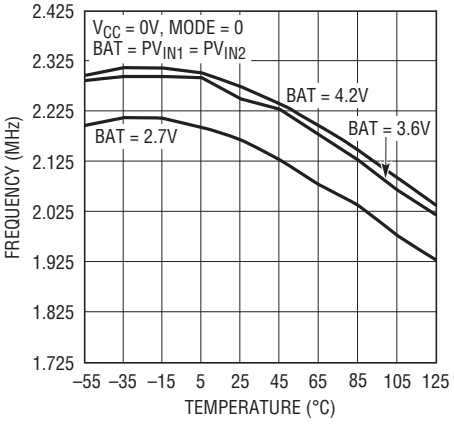
3558 G16

Complete Charge Cycle 2400mAh Battery



3558 G17

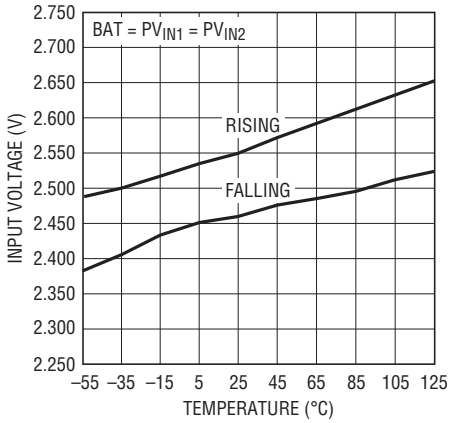
Buck and Buck-Boost Regulator Switching Frequency vs Temperature



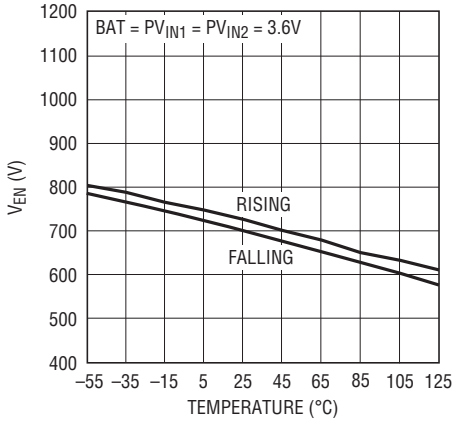
3558 G18

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

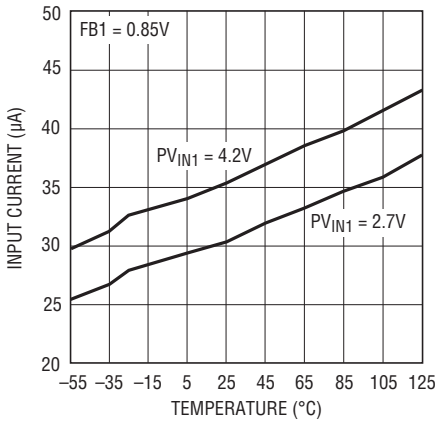
Buck and Buck-Boost Regulator Undervoltage Thresholds vs Temperature



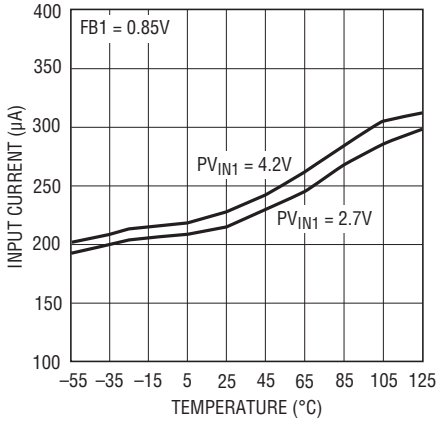
Buck and Buck-Boost Regulator Enable Thresholds vs Temperature



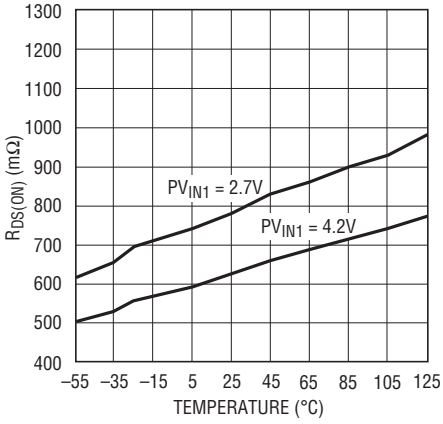
Buck Regulator Input Current vs Temperature, Burst Mode Operation



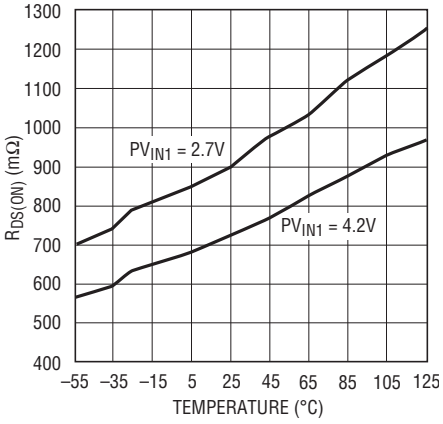
Buck Regulator Input Current vs Temperature, Pulse Skip Mode



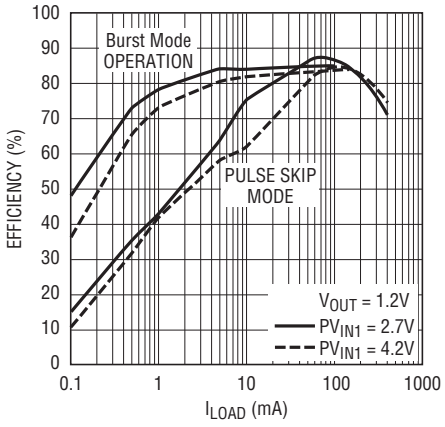
Buck Regulator PMOS $R_{DS(ON)}$ vs Temperature



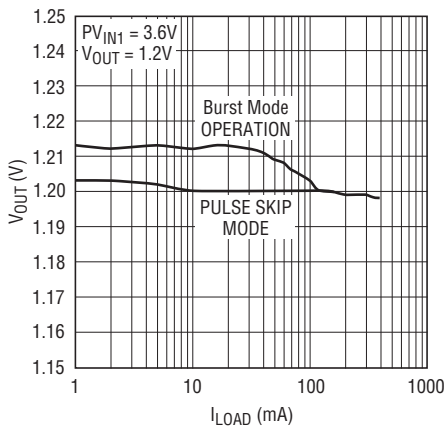
Buck Regulator NMOS $R_{DS(ON)}$ vs Temperature



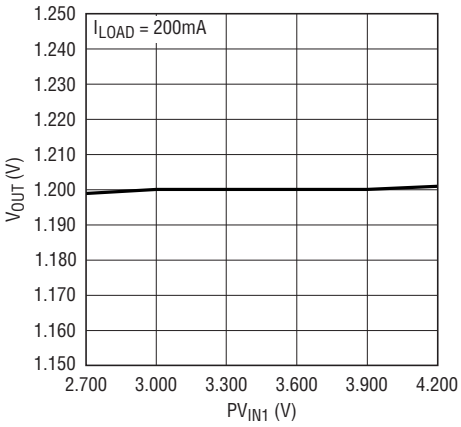
Buck Regulator Efficiency vs I_{LOAD}



Buck Regulator Load Regulation

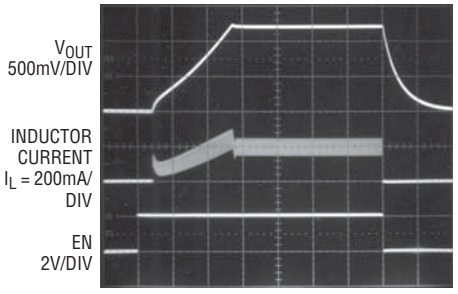


Buck Regulator Line Regulation



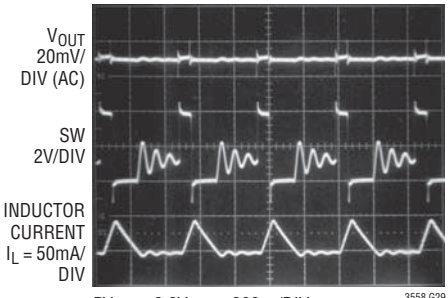
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Buck Regulator Start-Up Transient



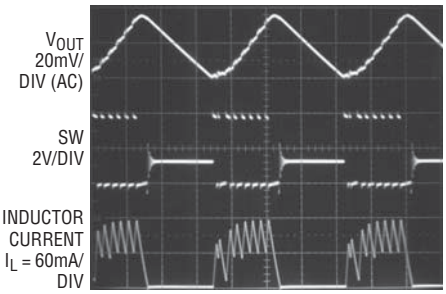
PV_{IN1} = 3.8V 50µs/DIV
PULSE SKIP MODE
LOAD = 6Ω

Buck Regulator Pulse Skip Mode Operation



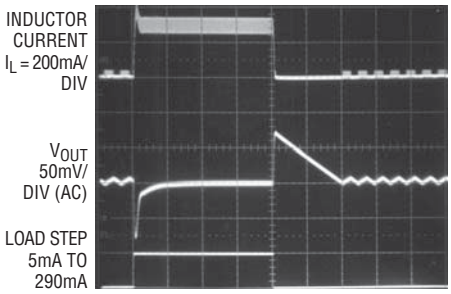
PV_{IN1} = 3.8V 200ns/DIV
LOAD = 10mA

Buck Regulator Burst Mode Operation



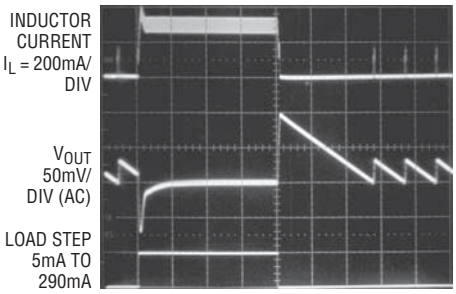
PV_{IN1} = 3.8V 2µs/DIV
LOAD = 60mA

Buck Regulator Transient Response, Pulse Skip Mode



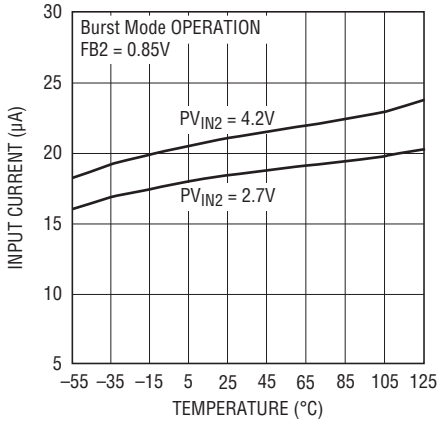
PV_{IN1} = 3.8V 50µs/DIV

Buck Regulator Transient Response, Burst Mode Operation

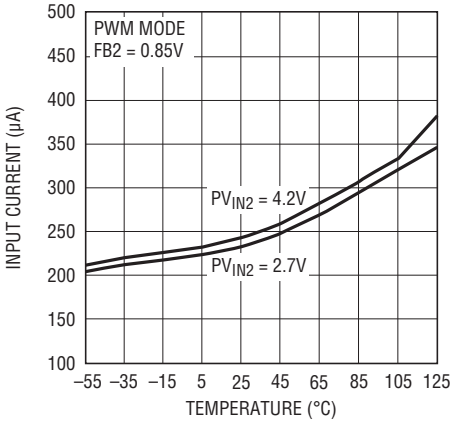


PV_{IN1} = 3.8V 50µs/DIV

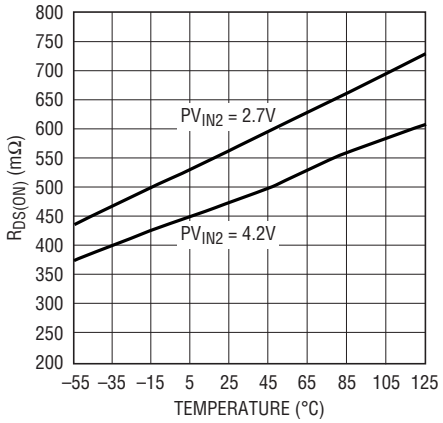
Buck-Boost Regulator Input Current vs Temperature



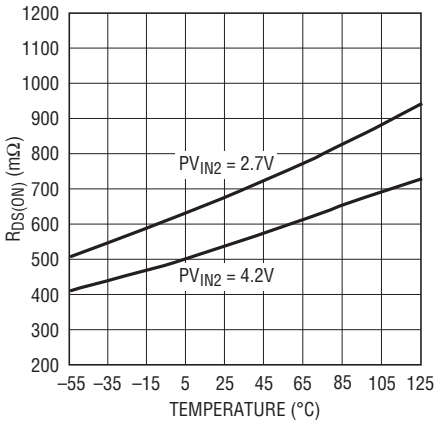
Buck-Boost Regulator Input Current vs Temperature



Buck-Boost Regulator PMOS $R_{DS(ON)}$ vs Temperature

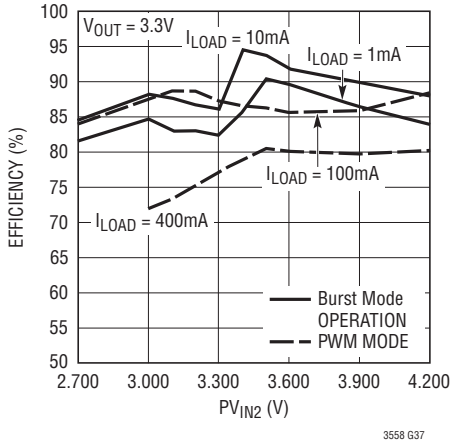


Buck-Boost Regulator NMOS $R_{DS(ON)}$ vs Temperature

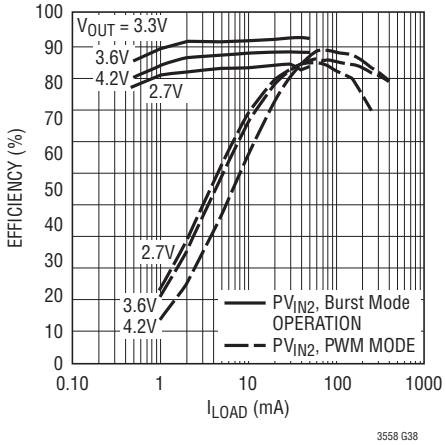


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

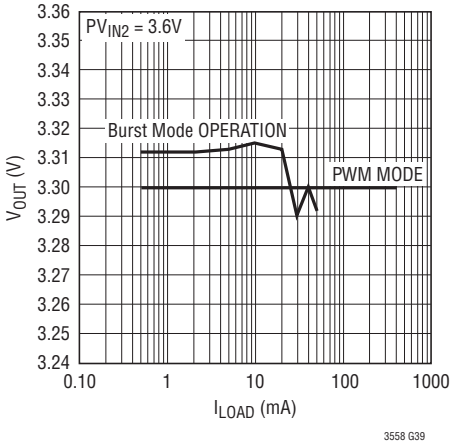
Buck-Boost Regulator Efficiency vs Input Voltage



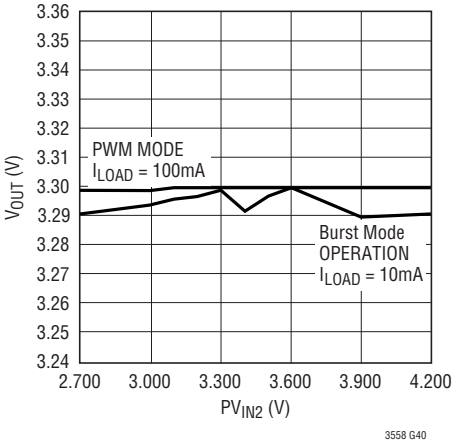
Buck-Boost Efficiency vs Load Current



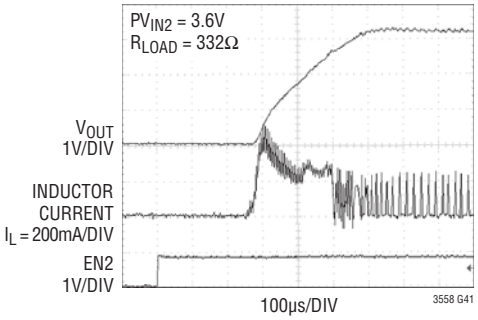
Buck-Boost Regulator Load Regulation



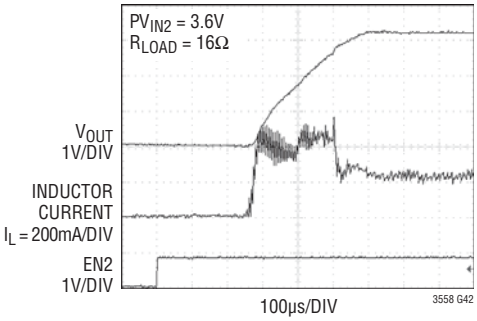
Buck-Boost Regulator Line Regulation



Buck-Boost Regulator Start-Up Transient, Burst Mode Operation



Buck-Boost Regulator Start-Up Transient, PWM Mode



PIN FUNCTIONS

GND (Pin 1): Ground. Connect to Exposed Pad (Pin 21).

BAT (Pin 2): Charge Current Output. Provides charge current to the battery and regulates final float voltage to 4.2V.

MODE (Pin 3): MODE Pin for Switching Regulators. When held high, both regulators operate in Burst Mode Operation. When held low, the buck regulator operates in pulse skip mode and the buck-boost regulator operates in PWM mode. This pin is a high impedance input; do not float.

FB1 (Pin 4): Buck Regulator Feedback Voltage Pin. Receives feedback by a resistor divider connected across the output.

EN1 (Pin 5): Enable Input Pin for the Buck Regulator. This pin is a high impedance input; do not float. Active high.

SW1 (Pin 6): Buck Regulator Switching Node. External inductor connects to this node.

PV_{IN1} (Pin 7): Input Supply Pin for Buck Regulator. Connect to BAT and PV_{IN2}. A single 10µF input decoupling capacitor to GND is required.

PV_{IN2} (Pin 8): Input Supply Pin for Buck-Boost Regulator. Connect to BAT and PV_{IN1}. A single 10µF input decoupling capacitor to GND is required.

SWAB2 (Pin 9): Switch Node for Buck-Boost Regulator Connected to the Internal Power Switches A and B. External inductor connects between this node and SWCD2.

SWCD2 (Pin 10): Switch Node for Buck-Boost Regulator Connected to the Internal Power Switches C and D. External inductor connects between this node and SWAB2.

V_{OUT2} (Pin 11): Regulated Output Voltage for Buck-Boost Regulator.

SUSP (Pin 12): Suspend Battery Charging Operation. A voltage greater than 1.2V on this pin puts the battery charger in suspend mode, disables the charger and resets the termination timer. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

FB2 (Pin 13): Buck-Boost Regulator Feedback Voltage Pin. Receives feedback by a resistor divider connected across the output.

V_{C2} (Pin 14): Output of the Error Amplifier and Voltage Compensation Node for the Buck-Boost Regulator. External Type I or Type III compensation (to FB2) connects to this pin.

EN2 (Pin 15): Enable Input Pin for the Buck-Boost Regulator. This pin is a high impedance input; do not float. Active high.

HPWR (Pin 16): High Current Battery Charging Enabled. A voltage greater than 1.2V at this pin programs the BAT pin current at 100% of the maximum programmed charge current. A voltage less than 0.4V sets the BAT pin current to 20% of the maximum programmed charge current. When used with a 1.74k PROG resistor, this pin can toggle between low power and high power modes per USB specification. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

NTC (Pin 17): Input to the NTC Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery pack to determine if the battery is too hot or too cold to charge. If the battery temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from V_{CC} to NTC and a thermistor is required from NTC to ground. To disable the NTC function, the NTC pin should be tied to ground.

PROG (Pin 18): Charge Current Program and Charge Current Monitor Pin. Charge current is programmed by connecting a resistor from PROG to ground. When charging in constant-current mode, the PROG pin servos to 1V if the HPWR pin is pulled high, or 200mV if the HPWR pin is pulled low. The voltage on this pin always represents the BAT pin current through the following formula:

$$I_{BAT} = \frac{PROG \bullet 800}{R_{PROG}}$$

$\overline{CHRG}$ (Pin 19): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ charging, not charging (i.e., the charge current is less than one-tenth

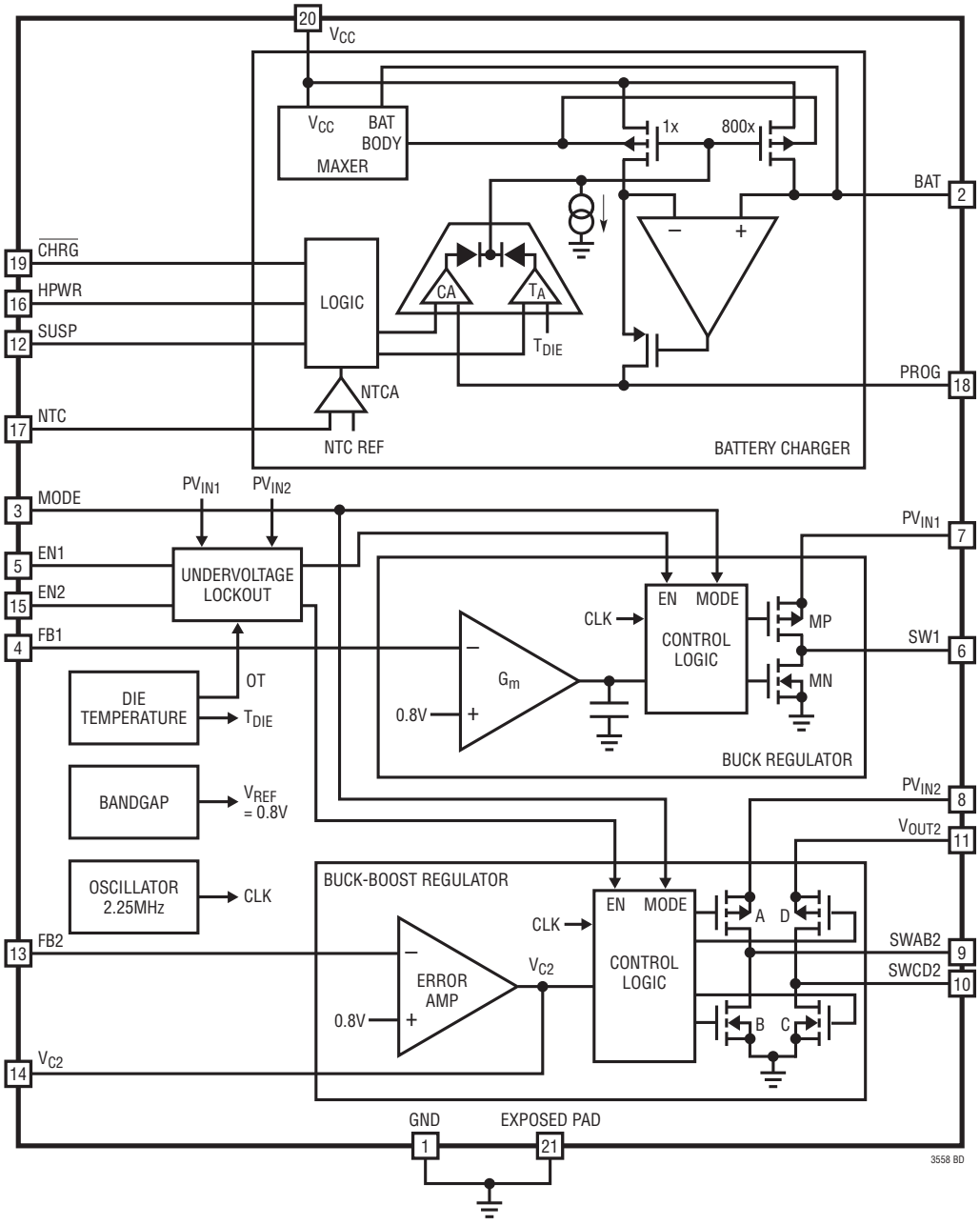
PIN FUNCTIONS

of the full-scale charge current), unresponsive battery (i.e., the battery voltage remains below 2.9V after one half hour of charging) and battery temperature out of range. $\overline{CHRG}$ requires a pull-up resistor and/or LED to provide indication.

V_{CC} (Pin 20): Battery Charger Input. A 1µF decoupling capacitor to GND is recommended.

Exposed Pad (Pin 21): Ground. The Exposed Pad must be soldered to PCB ground to provide electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3558 is a linear battery charger with a monolithic synchronous buck regulator and a monolithic synchronous buck-boost regulator. The buck regulator is internally compensated and needs no external compensation components.

The battery charger employs a constant-current, constant-voltage charging algorithm and is capable of charging a single Li-Ion battery at charging currents up to 950mA. The user can program the maximum charging current available at the BAT pin via a single PROG resistor. The actual BAT pin current is set by the status of the HPWR pin.

For proper operation, the BAT, PV_{IN1} and PV_{IN2} pins must be tied together, as shown in Figure 1. Current being delivered at the BAT pin is 500mA. Both switching regulators are enabled. The sum of the average input currents drawn by both switching regulators is 200mA. This makes the effective battery charging current only 300mA. If the HPWR pin were tied LO, the BAT pin current would be 100mA. With the switching regulator conditions unchanged, this would cause the battery to discharge at 100mA.

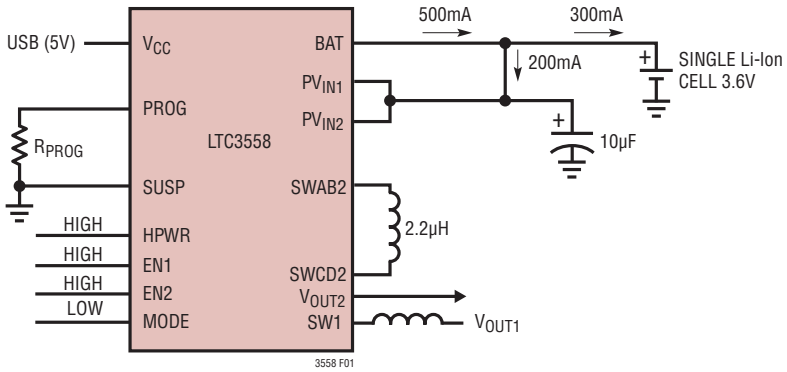


Figure 1. For Proper Operation, the BAT, PV_{IN1} and PV_{IN2} Pins Must Be Tied Together

APPLICATIONS INFORMATION

Battery Charger Introduction

The LTC3558 has a linear battery charger designed to charge single-cell lithium-ion batteries. The charger uses a constant-current/constant-voltage charge algorithm with a charge current programmable up to 950mA. Additional features include automatic recharge, an internal termination timer, low-battery trickle charge conditioning, bad-battery detection, and a thermistor sensor input for out of temperature charge pausing.

Furthermore, the battery charger is capable of operating from a USB power source. In this application, charge current can be programmed to a maximum of 100mA or 500mA per USB power specifications.

Input Current vs Charge Current

The battery charger regulates the total current delivered to the BAT pin; this is the charge current. To calculate the total input current (i.e., the total current drawn from the V_{CC} pin), it is necessary to sum the battery charge current, charger quiescent current and PROG pin current.

Undervoltage Lockout (UVLO)

The undervoltage lockout circuit monitors the input voltage (V_{CC}) and disables the battery charger until V_{CC} rises above V_{UVLO} (typically 4V). 200mV of hysteresis prevents oscillations around the trip point. In addition, a differential undervoltage lockout circuit disables the battery charger

APPLICATIONS INFORMATION

when V_{CC} falls to within V_{DUVLO} (typically 50mV) of the BAT voltage.

Suspend Mode

The battery charger can also be disabled by pulling the SUSP pin above 1.2V. In suspend mode, the battery drain current is reduced to 1.5µA and the input current is reduced to 8.5µA.

Charge Cycle Overview

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.9V, an automatic trickle charge feature sets the battery charge current to 10% of the full-scale value.

Once the battery voltage is above 2.9V, the battery charger begins charging in constant-current mode. When the battery voltage approaches the 4.2V required to maintain a full charge, otherwise known as the float voltage, the charge current begins to decrease as the battery charger switches into constant-voltage mode.

Trickle Charge and Defective Battery Detection

Any time the battery voltage is below V_{TRKL}, the charger goes into trickle charge mode and reduces the charge current to 10% of the full-scale current. If the battery voltage remains below V_{TRKL} for more than 1/2 hour, the charger latches the bad-battery state, automatically terminates, and indicates via the $\overline{CHRG}$ pin that the battery was unresponsive. If for any reason the battery voltage rises above V_{TRKL}, the charger will resume charging. Since the charger has latched the bad-battery state, if the battery voltage then falls below V_{TRKL} again but without rising past V_{RECHRG} first, the charger will immediately assume that the battery is defective. To reset the charger (i.e., when the dead battery is replaced with a new battery), simply remove the input voltage and reapply it or put the part in and out of suspend mode.

Charge Termination

The battery charger has a built-in safety timer that sets the total charge time for 4 hours. Once the battery voltage rises above V_{RECHRG} (typically 4.105V) and the charger enters constant-voltage mode, the 4-hour timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off, drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.105V). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, it will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.7ms. The charge cycle and safety timer will also restart if the V_{CC} UVLO or DUVLO cycles low and then high (e.g., V_{CC} is removed and then replaced) or the charger enters and then exits suspend mode.

Programming Charge Current

The PROG pin serves both as a charge current program pin, and as a charge current monitor pin. By design, the PROG pin current is 1/800th of the battery charge current. Therefore, connecting a resistor from PROG to ground programs the charge current while measuring the PROG pin voltage allows the user to calculate the charge current.

Full-scale charge current is defined as 100% of the constant-current mode charge current programmed by the PROG resistor. In constant-current mode, the PROG pin servos to 1V if HPWR is high, which corresponds to charging at the full-scale charge current, or 200mV if HPWR is low, which corresponds to charging at 20% of the full-scale charge current. Thus, the full-scale charge current and desired program resistor for a given full-scale charge current are calculated using the following equations:

$$I_{CHG} = \frac{800V}{R_{PROG}}$$

$$R_{PROG} = \frac{800V}{I_{CHG}}$$

APPLICATIONS INFORMATION

In any mode, the actual battery current can be determined by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{PROG}{R_{PROG}} \bullet 800$$

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 115°C. Thermal regulation protects the battery charger from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC3558 or external components. The benefit of the LTC3558 battery charger thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ charging, not charging, unresponsive battery and battery temperature out of range.

The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. The $\overline{CHRG}$ pin, which is an open-drain output, can drive an indicator LED through a current limiting resistor for human interfacing, or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either a low for charging, a high for not charging, or it is switched at high frequency (35kHz) to indicate the two possible faults: unresponsive battery and battery temperature out of range.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When the charge current has dropped to below 10% of the full-scale current, the $\overline{CHRG}$ pin is released (high impedance). If a fault occurs after the $\overline{CHRG}$ pin is released, the pin remains high impedance. However, if a fault occurs before the $\overline{CHRG}$ pin is released, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking". Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for microprocessor recognition.

Table 1 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 1. $\overline{CHRG}$ Output Pin

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLE
Charging	0Hz	0 Hz (Lo-Z)	100%
I_{BAT} < C/10	0Hz	0 Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	6.25%, 93.75%
Bad Battery	35kHz	6.1Hz at 50%	12.5%, 87.5%

An NTC fault is represented by a 35kHz pulse train whose duty cycle alternates between 6.25% and 93.75% at a 1.5Hz rate. A human will easily recognize the 1.5Hz rate as a "slow" blinking which indicates the out of range battery temperature while a microprocessor will be able to decode either the 6.25% or 93.75% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below V_{TRKL} for over 1/2 hour), the $\overline{CHRG}$ pin gives the battery fault indication. For this fault, a human would easily recognize the frantic 6.1Hz "fast" blinking of the LED while a microprocessor would be able to decode either the 12.5% or 87.5% duty cycles as a bad battery fault.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and take a new duty cycle reading.

APPLICATIONS INFORMATION

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 3.

To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and ground, and a bias resistor, R_{NOM}, from V_{CC} to NTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). A 100k thermistor is recommended since thermistor current is not measured by the battery charger and its current will have to be considered for compliance with USB specifications.

The battery charger will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k (for a Vishay "Curve 1" thermistor, this corresponds to approximately 40°C). If the battery charger is in constant-voltage mode, the safety timer will pause until the thermistor indicates a return to a valid temperature.

As the temperature drops, the resistance of the NTC thermistor rises. The battery charger is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For a Vishay "Curve 1" thermistor, this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

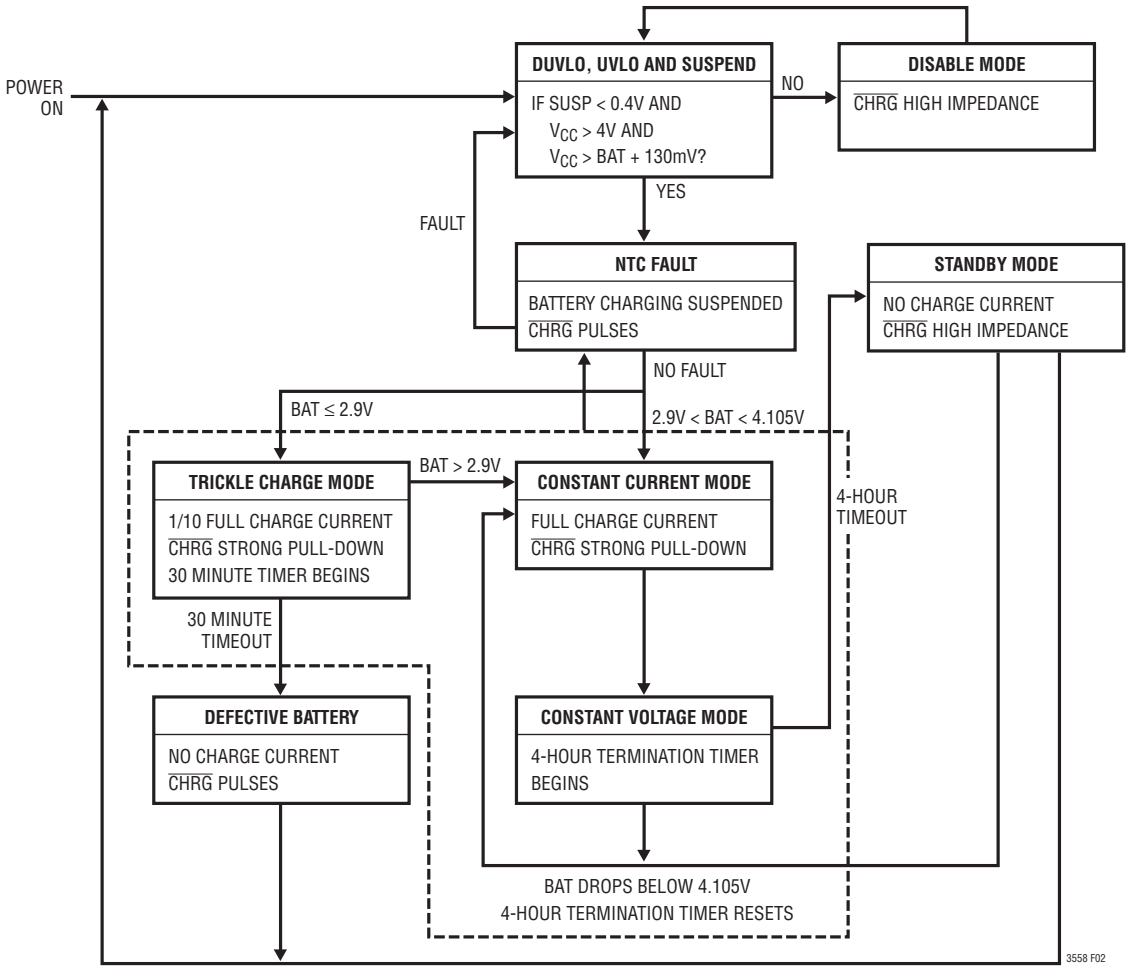


Figure 2. State Diagram of Battery Charger Operation

APPLICATIONS INFORMATION

Alternate NTC Thermistors and Biasing

The battery charger provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to the NTC pin. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay "Curve 1" thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay "Curve 1" resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT} = Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 3)

R1 = Optional temperature range adjustment resistor (see Figure 4)

The trip points for the battery charger's temperature qualification are internally programmed at 0.349 • V_{CC} for the hot threshold and 0.765 • V_{CC} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM} + R_{NTC|HOT}} \bullet V_{CC} = 0.349 \bullet V_{CC}$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM} + R_{NTC|COLD}} \bullet V_{CC} = 0.765 \bullet V_{CC}$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.536 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.25 \bullet R_{NOM}$$

By setting R_{NOM} equal to R25, the above equations result in r_{HOT} = 0.536 and r_{COLD} = 3.25. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the desired hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set

APPLICATIONS INFORMATION

to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 4. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k.

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 4 and results in an upper trip point of 45°C and a lower trip point of 0°C.

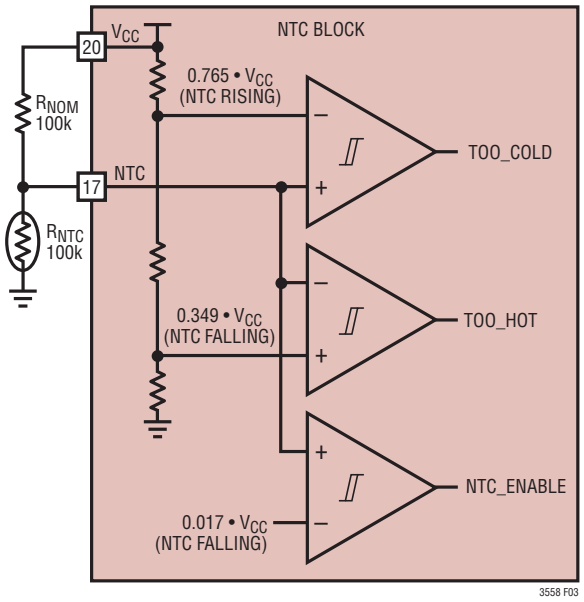


Figure 3. Typical NTC Thermistor Circuit

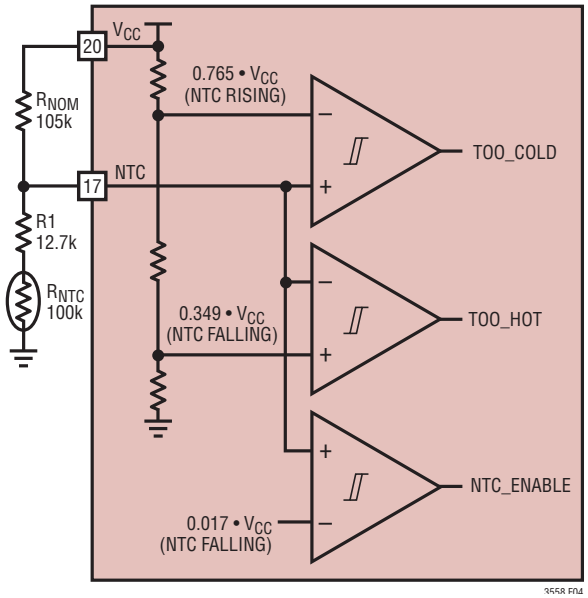


Figure 4. NTC Thermistor Circuit with Additional Bias Resistor

APPLICATIONS INFORMATION

USB and Wall Adapter Power

Although the battery charger is designed to draw power from a USB port to charge Li-Ion batteries, a wall adapter can also be used. Figure 5 shows an example of how to combine wall adapter and USB power inputs. A P-channel MOSFET, MP1, is used to prevent back conduction into the USB port when a wall adapter is present and Schottky diode, D1, is used to prevent USB power loss through the 1k pull-down resistor.

Typically, a wall adapter can supply significantly more current than the 500mA-limited USB port. Therefore, an N-channel MOSFET, MN1, and an extra program resistor are used to increase the maximum charge current to 950mA when the wall adapter is present.

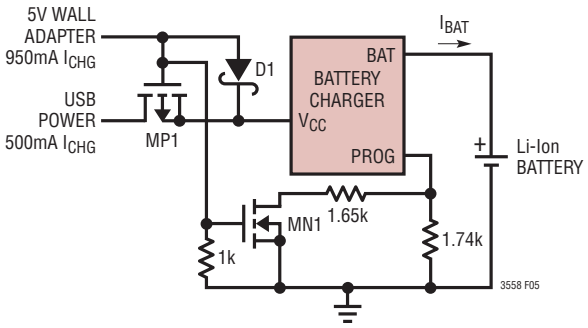


Figure 5. Combining Wall Adapter and USB Power

Power Dissipation

The conditions that cause the LTC3558 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. For high charge currents, the LTC3558 power dissipation is approximately:

$$P_D = (V_{CC} - V_{BAT}) \bullet I_{BAT}$$

where P_D is the power dissipated, V_{CC} is the input supply voltage, V_{BAT} is the battery voltage, and I_{BAT} is the charge current. It is not necessary to perform any worst-case power dissipation scenarios because the LTC3558 will automatically reduce the charge current to maintain the die temperature at approximately 105°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 105°C - P_D\theta_{JA}$$

$$T_A = 105°C - (V_{CC} - V_{BAT}) \bullet I_{BAT} \bullet \theta_{JA}$$

Example: Consider an LTC3558 operating from a USB port providing 500mA to a 3.5V Li-Ion battery. The ambient temperature above which the LTC3558 will begin to reduce the 500mA charge current is approximately:

$$T_A = 105°C - (5V - 3.5V) \bullet (500mA) \bullet 68°C/W$$

$$T_A = 105°C - 0.75W \bullet 68°C/W = 105°C - 51°C$$

$$T_A = 54°C$$

The LTC3558 can be used above 70°C, but the charge current will be reduced from 500mA. The approximate current at a given ambient temperature can be calculated:

$$I_{BAT} = \frac{105°C - T_A}{(V_{CC} - V_{BAT}) \bullet \theta_{JA}}$$

Using the previous example with an ambient temperature of 88°C, the charge current will be reduced to approximately:

$$I_{BAT} = \frac{105°C - 88°C}{(5V - 3.5V) \bullet 68°C/W} = \frac{17°C}{102°C/A}$$

$$I_{BAT} = 167mA$$

Furthermore, the voltage at the PROG pin will change proportionally with the charge current as discussed in the Programming Charge Current section.

It is important to remember that LTC3558 applications do not need to be designed for worst-case thermal conditions since the IC will automatically reduce power dissipation when the junction temperature reaches approximately 105°C.

APPLICATIONS INFORMATION

Battery Charger Stability Considerations

The LTC3558 battery charger contains two control loops: the constant-voltage and constant-current loops. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1.5µF from BAT to GND. Furthermore, a 4.7µF capacitor with a 0.2Ω to 1Ω series resistor from BAT to GND is required to keep ripple voltage low when the battery is disconnected.

High value capacitors with very low ESR (especially ceramic) reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant-current mode, the PROG pin is in the feedback loop, not the battery. Because of the additional pole created by the PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 25K. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 10^5 \bullet C_{PROG}}$$

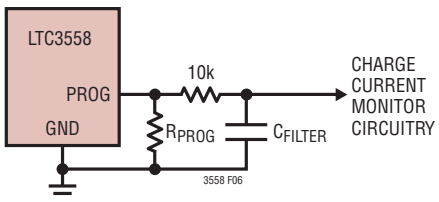


Figure 6. Isolated Capacitive Load on PROG Pin and Filtering

Average, rather than instantaneous, battery current may be of interest to the user. For example, if a switching power supply operating in low-current mode is connected in parallel with the battery, the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses. In such a case, a simple RC filter can be used on the PROG pin to measure the average battery current as shown in Figure 6. A 10k resistor has been added between the PROG pin and the filter capacitor to ensure stability.

USB Inrush Limiting

When a USB cable is plugged into a portable product, the inductance of the cable and the high-Q ceramic input capacitor form an L-C resonant circuit. If there is not much impedance in the cable, it is possible for the voltage at the input of the product to reach as high as twice the USB voltage (~10V) before it settles out. In fact, due to the high voltage coefficient of many ceramic capacitors (a nonlinearity), the voltage may even exceed twice the USB voltage. To prevent excessive voltage from damaging the LTC3558 during a hot insertion, the soft connect circuit in Figure 7 can be employed.

In the circuit of Figure 7, capacitor C1 holds MP1 off when the cable is first connected. Eventually C1 begins to charge up to the USB input voltage applying increasing gate support to MP1. The long time constant of R1 and C1 prevents the current from building up in the cable too fast thus dampening out any resonant overshoot.

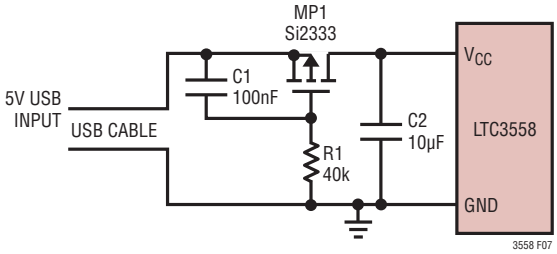


Figure 7. USB Soft Connect Circuit

APPLICATIONS INFORMATION

Buck Switching Regulator General Information

The LTC3558 contains a 2.25MHz constant-frequency current mode buck switching regulator that can provide up to 400mA. The switcher can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry. The regulator supports 100% duty cycle operation (dropout mode) when the input voltage drops very close to the output voltage and is also capable of operating in Burst Mode operation for highest efficiencies at light loads (Burst Mode operation is pin selectable). The buck switching regulator also includes soft-start to limit inrush current when powering on, short-circuit current protection, and switch node slew limiting circuitry to reduce radiated EMI.

A MODE pin sets the buck switching regulator in Burst Mode operation or pulse skip operating mode. The regulator is enabled individually through its enable pin. The buck regulator input supply (PV_{IN1}) should be connected to the battery pin (BAT) and PV_{IN2}. This allows the undervoltage lockout circuit on the BAT pin to disable the buck regulators when the BAT voltage drops below 2.45V. Do not drive the buck switching regulator from a voltage other than BAT. A 10µF decoupling capacitor from the PV_{IN1} pin to GND is recommended.

Buck Switching Regulator Output Voltage Programming

The buck switching regulator can be programmed for output voltages greater than 0.8V. The output voltage for the buck switching regulator is programmed using a resistor divider from the switching regulator output connected to its feedback pin (FB1), as shown in Figure 8, such that:

$$V_{OUT} = 0.8(1 + R1/R2)$$

Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response if so desired by the user.

Buck Switching Regulator Operating Modes

The buck switching regulator includes two possible operating modes to meet the noise/power needs of a variety of applications.

In pulse skip mode, an internal latch is set at the start of every cycle, which turns on the main P-channel MOSFET

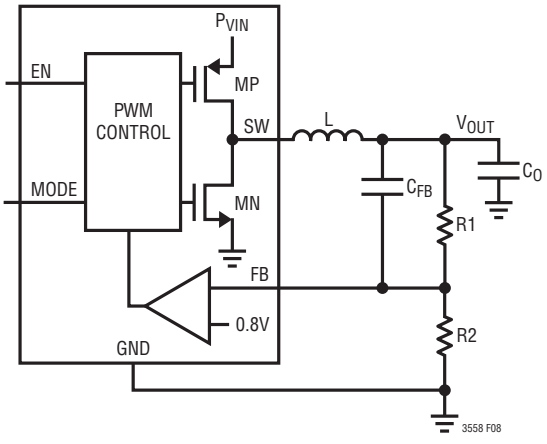


Figure 8. Buck Converter Application Circuit

APPLICATIONS INFORMATION

switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch, which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the buck switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse skip mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW1) goes high impedance and the switch node voltage will "ring". This is discontinuous operation, and is normal behavior for a switching regulator. At very light loads in pulse skip mode, the buck switching regulator will automatically skip pulses as needed to maintain output regulation. At high duty cycle ($V_{OUT} > PV_{IN1}/2$) in pulse skip mode, it is possible for the inductor current to reverse causing the buck converter to switch continuously. Regulation and low noise operation are maintained but the input supply current will increase to a couple mA due to the continuous gate switching.

During Burst Mode operation, the buck switching regulator automatically switches between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads the buck switching regulator controls the inductor current directly and use a hysteretic control loop to minimize both noise and switching losses. During Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The buck switching regulator then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the switching regulator's circuitry is powered down, helping conserve battery power. When the output voltage drops below a pre-determined value, the buck switching regulator circuitry is powered on and another burst cycle begins. The sleep time decreases as the load current increases. Beyond a certain load current point (about 1/4 rated output load current) the buck switching regulator will switch to a low noise constant-frequency PWM mode of operation, much the same as pulse skip operation at high loads. For applications that can tolerate some output ripple at low output currents, Burst Mode operation provides better efficiency than pulse skip at light loads.

The buck switching regulator allows mode transition on-the-fly, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed. Burst Mode operation is set by driving the MODE pin high, while pulse skip mode is achieved by driving the MODE pin low.

Buck Switching Regulator in Shutdown

The buck switching regulator is in shutdown when not enabled for operation. In shutdown, all circuitry in the buck switching regulator is disconnected from the regulator input supply, leaving only a few nanoamps of leakage pulled to ground through a 13k resistor on the switch (SW1) pin when in shutdown.

Buck Switching Regulator Dropout Operation

It is possible for the buck switching regulator's input voltage to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

APPLICATIONS INFORMATION

Buck Switching Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each switching regulator over a 500µs period. This allows an output to rise slowly, helping minimize the battery in-rush current required to charge up the regulator's output capacitor. A soft-start cycle occurs when the buck switcher first turns on, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes using the MODE pin. This allows seamless output operation when transitioning between operating modes.

Buck Switching Regulator Switching Slew Rate Control

The buck switching regulator contains circuitry to limit the slew rate of the switch node (SW1). This circuitry is designed to transition the switch node over a period of a couple of nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency.

Buck Switching Regulator Low Supply Operation

An undervoltage lockout (UVLO) circuit on PV_{IN1} shuts down the step-down switching regulators when BAT drops below 2.45V. This UVLO prevents the buck switching regulator from operating at low supply voltages where loss of regulation or other undesirable operation may occur.

Buck Switching Regulator Inductor Selection

The buck switching regulator is designed to work with inductors in the range of 2.2µH to 10µH, but for most applications a 4.7µH inductor is suggested. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current which improves transient response time. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output efficiency is reduced about 2% for every 100mΩ series resistance at 400mA load current, and about 2% for every 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition the inductor should be rated to handle the maximum peak current specified for the buck regulators.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance, and any radiated EMI requirements than on what the buck regulator requires to operate.

The inductor value also has an effect on Burst Mode operation. Lower inductor values will cause Burst Mode switching frequency to increase.

APPLICATIONS INFORMATION

Table 2 shows several inductors that work well with the LTC3558 buck switching regulator. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Buck Switching Regulator Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at switching regulator outputs as well as the switching regulator input supply. Ceramic capacitor dielectrics are a compromise between high dielectric constant and stability versus temperature and versus DC bias voltage. The X5R/X7R dielectrics offer the best compromise with high dielectric constant and acceptable performance over temperature and under bias. Do not use Y5V dielectrics. A 10µF output capacitor is sufficient for most applications. For good transient response and stability the output capacitor should retain at least 4µF of capacitance over operating temperature and bias voltage. The buck switching regulator input supply should be bypassed with a 10µF capacitor. Consult manufacturer for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (< 1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 3 shows a list of several ceramic capacitor manufacturers.

Table 3: Recommended Ceramic Capacitor Manufacturers

AVX	(803) 448-9411	www.avxcorp.com
Murata	(714) 852-2001	www.murata.com
Taiyo Yuden	(408) 537-4150	www.t-yuden.com
TDK	(888) 835-6646	www.tdk.com

Table 2. Recommended Inductors for Buck Switching Regulators

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
DE2818C DE2812C	4.7 4.7	1.25 1.15	72* 130*	3 × 2.8 × 1.8 3 × 2.8 × 1.2	Toko www.toko.com
CDRH3D16	4.7	0.9	110	4 × 4 × 1.8	Sumida www.sumida.com
SD3118 SD3112	4.7 4.7	1.3 0.8	162 246	3.1 × 3.1 × 1.8 3.1 × 3.1 × 1.2	Cooper www.cooperet.com
LPS3015	4.7	1.1	200	3 × 3 × 1.5	Coilcraft www.coilcraft.com

*Typical DCR

APPLICATIONS INFORMATION

Buck-Boost Switching Regulator

The LTC3558 contains a 2.25MHz constant-frequency, voltage mode, buck-boost switching regulator. The regulator provides up to 400mA of output load current. The buck-boost switching regulator can be programmed for a minimum output voltage of 2.75V and can be used to power a microcontroller core, microcontroller I/O, memory, disk drive, or other logic circuitry. To suit a variety of applications, different mode functions allow the user to trade off noise for efficiency. Two modes are available to control the operation of the buck-boost regulator. At moderate to heavy loads, the constant-frequency PWM mode provides the least noise switching solution. At lighter loads, Burst Mode operation may be selected. Regulation is maintained by an error amplifier that compares the divided output voltage with a reference and adjusts the compensation voltage accordingly until the FB2 voltage has stabilized at 0.8V. The buck-boost switching regulator also includes soft-start to limit inrush current and voltage overshoot when powering on, short-circuit current protection, and switch node slew limiting circuitry for reduced radiated EMI.

Buck-Boost Regulator PWM Operating Mode

In PWM mode, the voltage seen at the feedback node is compared to a 0.8V reference. From the feedback voltage, an error amplifier generates an error signal seen at the V_{C2} pin. This error signal controls PWM waveforms that modulate switches A (input PMOS), B (input NMOS), C (output NMOS), and D (output PMOS). Switches A and B operate synchronously, as do switches C and D. If the input voltage is significantly greater than the programmed output voltage, then the regulator will operate in buck mode. In this case, switches A and B will be modulated, with switch D always on (and switch C always off), to step-down the input voltage to the programmed output. If the input voltage is significantly less than the programmed output voltage, then the converter will operate in boost mode. In this case, switches C and D are modulated, with switch A always on (and switch B always off), to step up the input voltage to the programmed output. If the input voltage is close to the programmed output voltage, then the converter will operate in four-switch mode. While operating in four-switch mode, switches turn on as per the following sequence: switches A and D $\rightarrow$ switches A and C $\rightarrow$ switches B and D $\rightarrow$ switches A and D.

Buck-Boost Regulator Burst Mode Operation

In Burst Mode operation, the switching regulator uses a hysteretic feedback voltage algorithm to control the output voltage. By limiting FET switching and using a hysteretic control loop switching losses are greatly reduced. In this mode, output current is limited to 50mA. While in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The buck-boost converter then goes into a SLEEP state, during which the output capacitor provides the load current. The output capacitor is charged by charging the inductor until the input current reaches 250mA typical, and then discharging the inductor until the reverse current reaches 0mA typical. This process of bursting current is repeated until the feedback voltage has charged to the reference voltage plus 6mV (806mV typical). In the SLEEP state, most of the regulator's circuitry is powered down, helping to conserve battery power. When the feedback voltage drops below the reference voltage minus 6mV (794mV typical), the switching regulator circuitry is powered on and another burst cycle begins. The duration for which the regulator operates in SLEEP depends on the load current and output capacitor value. The SLEEP time decreases as the load current increases. The maximum deliverable load current in Burst Mode operation is 50mA typical. The buck-boost regulator may not enter SLEEP if the load current is greater than 50mA. If the load current increases beyond this point while in Burst Mode operation, the output may lose regulation. Burst Mode operation provides a significant improvement in efficiency at light loads at the expense of higher output ripple when compared to PWM mode. For many noise-sensitive systems, Burst Mode operation might be undesirable at certain times (i.e., during a transmit or receive cycle of a wireless device), but highly desirable at others (i.e., when the device is in low power standby mode).

APPLICATIONS INFORMATION

Buck-Boost Switching Regulator Output Voltage Programming

The buck-boost switching regulator can be programmed for output voltages greater than 2.75V and less than 5.45V. To program the output voltage, a resistor divider is connected between V_{OUT2} and the feedback node (FB2) as shown in Figure 9. The output voltage is given by $V_{OUT2} = 0.8(1 + R1/R2)$.

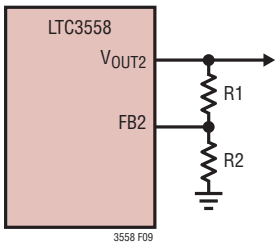


Figure 9. Programming the Buck-Boost Output Voltage Requires a Resistor Divider Connected Between V_{OUT2} and FB2

Closing the Feedback Loop

The LTC3558 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck-boost), but is usually no greater than 20. The output filter exhibits a double pole response given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature in boost mode is the right-half plane zero (RHP), and is given by:

$$f_{RHPZ} = \frac{PV_{IN2}^{2}}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT2}} Hz$$

The loop gain is typically rolled off before the RHP zero frequency.

A simple Type I compensation network, as shown in Figure 10, can be incorporated to stabilize the loop, but at the cost of reduced bandwidth and slower transient response. To ensure proper phase margin, the loop requires to be crossed over a decade before the LC double pole.

The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{P1}} Hz$$

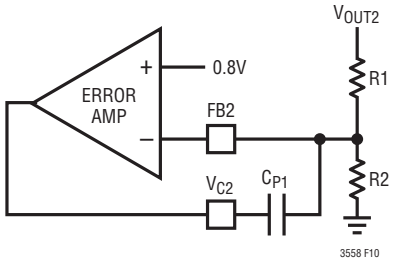


Figure 10. Error Amplifier with Type I Compensation

APPLICATIONS INFORMATION

Most applications demand an improved transient response to allow a smaller output filter capacitor. To achieve a higher bandwidth, Type III compensation is required. Two zeros are required to compensate for the double-pole response. Type III compensation also reduces any V_{OUT2} overshoot seen during a start-up condition. A Type III compensation circuit is shown in Figure 11 and yields the following transfer function:

$$\frac{V_{C2}}{V_{OUT2}} = \frac{1}{R1(C1+C2)} \bullet \frac{(1+sR2C2)[1+s(R1+R3)C3]}{s\left[1+sR2(C1||C2)\right](1+sR3C3)}$$

A Type III compensation network attempts to introduce a phase bump at a higher frequency than the LC double pole. This allows the system to cross unity gain after the LC double pole, and achieve a higher bandwidth. While attempting to cross over after the LC double pole, the system must still cross over before the boost right-half plane zero. If unity gain is not reached sufficiently before the right-half plane zero, then the –180° of phase lag from the LC double pole combined with the –90° of phase lag from the right-half plane zero will result in negating the phase bump of the compensator.

The compensator zeros should be placed either before or only slightly after the LC double pole such that their positive phase contributions offset the –180° that occurs at the filter double pole. If they are placed at too low of a frequency, they will introduce too much gain to the system and the crossover frequency will be too high. The two high frequency poles should be placed such that the system crosses unity gain during the phase bump introduced by the zeros and before the boost right-half plane zero and such that the compensator bandwidth is less than the bandwidth of the error amp (typically 900kHz). If the gain of the compensation network is ever greater than the gain of the error amplifier, then the error amplifier no longer acts as an ideal op amp, and another pole will be introduced at the same point.

Recommended Type III compensation components for a 3.3V output are:

R1: 324kΩ

R_{FB}: 105kΩ

C1: 10pF

R2: 15kΩ

C2: 330pF

R3: 121kΩ

C3: 33pF

C_{OUT}: 22µF

L_{OUT}: 2.2µH

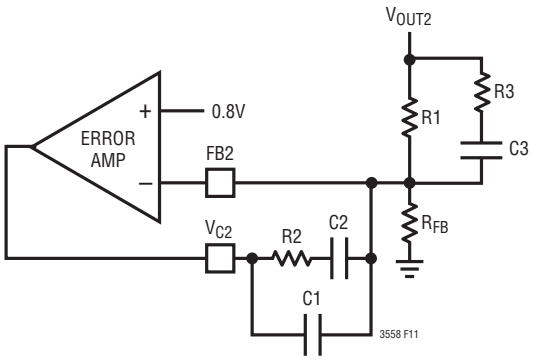


Figure 11. Error Amplifier with Type III Compensation

APPLICATIONS INFORMATION

Input Current Limit

The input current limit comparator will shut the input PMOS switch off once current exceeds 700mA typical. Before the switch current limit, the average current limit amp (620mA typical) will source current into the feedback pin to drop the output voltage. The input current limit also protects against a short-circuit condition at the V_{OUT2} pin.

Reverse Current Limit

The reverse current limit comparator will shut the output PMOS switch off once current returning from the output exceeds 450mA typical.

Output Overvoltage Protection

If the feedback node were inadvertently shorted to ground, then the output would increase indefinitely with the maximum current that could be sourced from the input supply. The buck-boost regulator protects against this by shutting off the input PMOS if the output voltage exceeds a 5.75V maximum.

Buck-Boost Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the reference voltage over a 500µs typical period. A soft-start cycle occurs whenever the buck-boost is enabled, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes. This allows seamless output operation when transitioning between Burst Mode operation and PWM mode operation.

Buck-Boost Switching Regulator Inductor Selection

The buck-boost switching regulator is designed to work with inductors in the range of 1µH to 5µH. For most applications, a 2.2µH inductor will suffice. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time. To maximize efficiency, choose an inductor with a low DC resistance and a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition, the inductor current should be rated to handle up to the peak current specified for the buck-boost regulator.

The inductor value also affects Burst Mode operation. Lower inductor values will cause Burst Mode switching frequencies to increase.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses and will not give the best efficiency.

Table 4 shows some inductors that work well with the buck-boost regulator. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 4. Recommended Inductors for the Buck-Boost Switching Regulator.

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
DB3018C	2.4	1.31	80	3.8 × 3.8 × 1.4	Toko
D312C	2.2	1.14	140	3.6 × 3.6 × 1.2	www.toko.com
DE2812C	2	1.4	81	3 × 3.2 × 1.2	
DE2812C	2.7	1.2	87	3 × 3.2 × 1.2	
CDRH3D16	2.2	1.2	72	4 × 4 × 1.8	Sumida www.sumida.com
SD12	2.2	1.8	74	5.2 × 5.2 × 1.2	Cooper www.cooperet.com

*Typical DCR

APPLICATIONS INFORMATION

Buck-Boost Switching Regulator Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at both the buck-boost regulator input (PV_{IN2}) and the output (V_{OUT2}). It is recommended that the input be bypassed with a 10µF capacitor. The output should be bypassed with at least a 10µF capacitor if using Type I compensation and 22µF if using Type III compensation.

The same selection criteria apply for the buck-boost regulator input and output capacitors as described in the Buck Switching Regulator Input/Output Capacitor Selection section.

PCB Layout Considerations

In order to deliver maximum charge current under all conditions, it is critical that the backside of the LTC3558 be soldered to the PC board ground.

The LTC3558 has dual switching regulators. As with all switching regulators, care must be taken while laying out a PC board and placing components. The input decoupling capacitors, the output capacitor and the inductors must all be placed as close to the pins as possible and on the same side of the board as the LTC3558. All connections must also be made on the same layer. Place a local unbroken ground plane below these components. Avoid routing noisy high frequency lines such as those that connect to switch pins over or parallel to lines that drive high impedance inputs.

TYPICAL APPLICATIONS

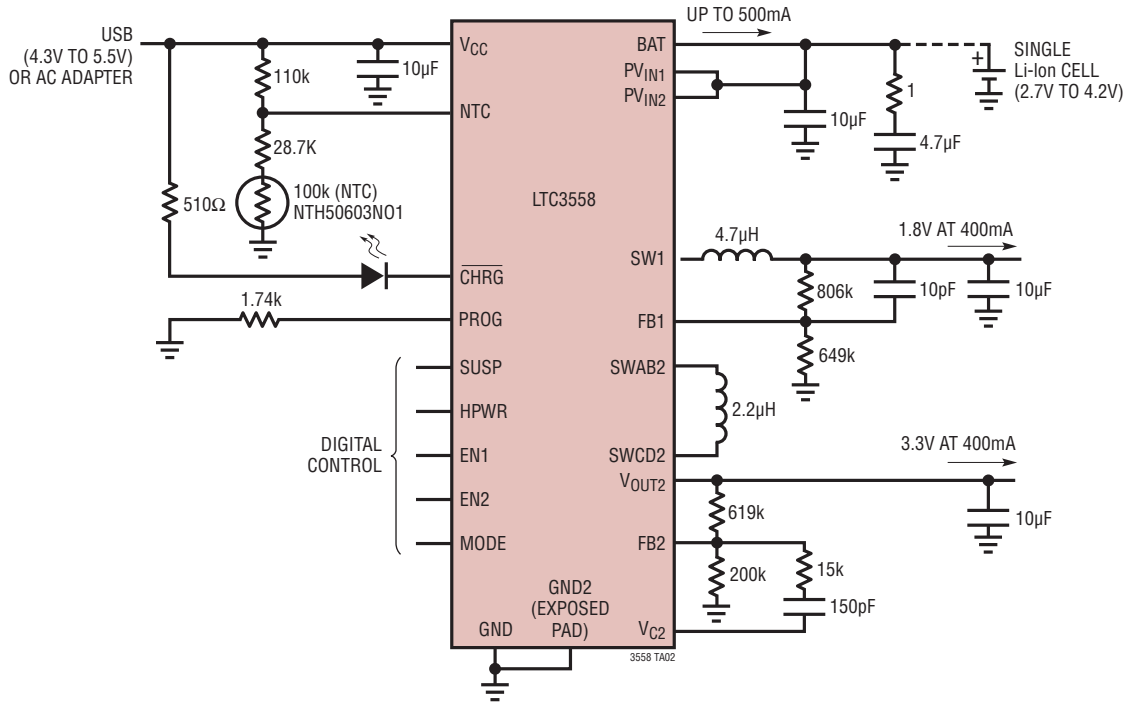


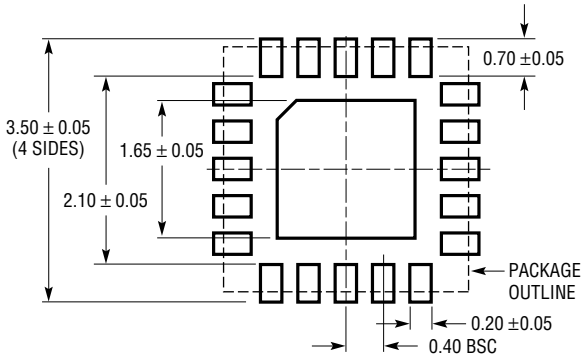
Figure 12. Li-Ion to 3.3V at 400mA, 1.8V at 400mA and USB-Compatible Battery Charger

As shown in Figure 12, the LTC3558 can be operated with no battery connected to the BAT pin. A 1Ω resistor in series with a 4.7µF capacitor at the BAT pin ensures battery charger stability. 10µF V_{CC} decoupling capacitors are required for proper operation of the DC/DC converters. A three-resistor bias network for NTC sets hot and cold trip points at approximately 55°C and 0°C.

The battery can be charged with up to 950mA of charge current when powered from a 5V wall adaptor, as shown in Figure 13. $\overline{CHRG}$ has a LED to provide a user with a visual indication of battery charge status. The buck-boost regulator starts up only after V_{OUT1} is up to approximately 0.7V. This provides a sequencing function which may be desirable in applications where a microprocessor needs to be powered up before peripherals. A Type III compensation network improves the transient response of the buck-boost switching regulator.

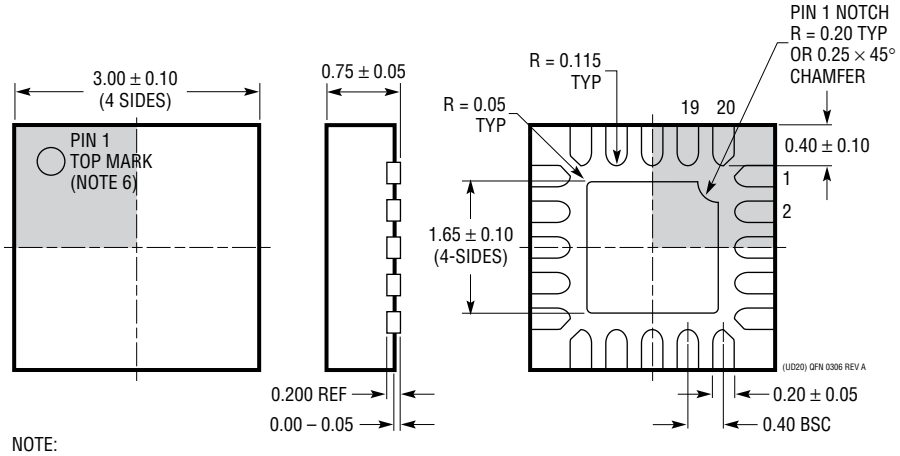
PACKAGE DESCRIPTION

UD Package
20-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1720 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE