Nanopower Energy Harvesting Power Supply with 14V Minimum V_{IN}

FEATURES

- **1500nA Input Quiescent Current (Output in Regulation – No Load, V_{IN} = 18V)**
- **830nA Input Quiescent Current in UVLO, V_{IN} = 12V**
- **14V to 20V Input Operating Range**
- **Integrated Low-Loss Full-Wave Bridge Rectifier**
- **16V UVLO Improves Power Utilization from High Voltage Current Limited Inputs**
- **Up to 100mA of Output Current**
- High Efficiency Integrated Hysteretic Buck DC/DC
- Selectable Output Voltages: 3.45V, 4.1V, 4.5V, 5.0V
- Input Protective Shunt – Up to 25mA Pull-Down at $V_{IN} \geq 20V$
- Available in 10-Lead MSE and 3mm × 3mm DFN Packages

APPLICATIONS

- Piezoelectric Energy Harvesting
- Electro-Mechanical Energy Harvesting
- Low Power Battery Charging
- Wireless HVAC Sensors
- Mobile Asset Tracking
- Tire Pressure Sensors
- Battery Replacement for Industrial Sensors

DESCRIPTION

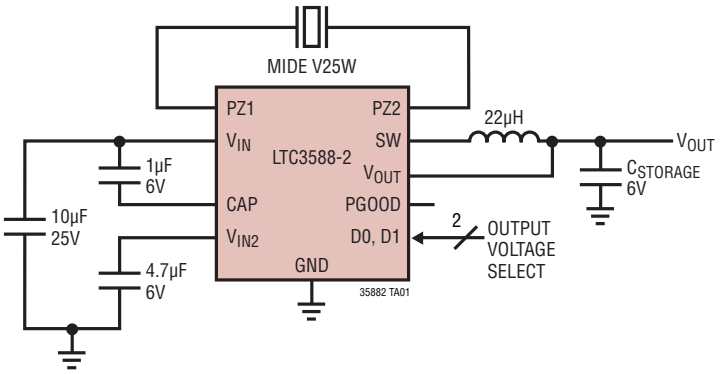
The LTC®3588-2 integrates a low-loss full-wave bridge rectifier with a high efficiency buck converter to form a complete energy harvesting solution optimized for high output impedance energy sources such as piezoelectric, solar, or magnetic transducers.

An ultralow quiescent current undervoltage lockout (UVLO) mode with a 16V rising threshold enables efficient energy extraction from sources with high open circuit voltages. This energy is transferred from the input capacitor to the output via a high efficiency synchronous buck regulator. The 16V UVLO threshold also allows for input to output current multiplication through the buck regulator. The buck features a sleep state that minimizes both input and output quiescent currents while in regulation.

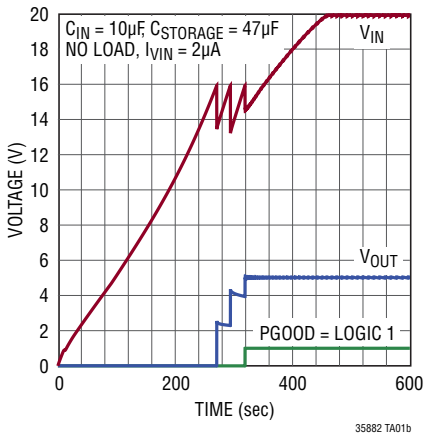
Four output voltages of 3.45V, 4.1V, 4.5V and 5.0V are pin selectable with up to 100mA of continuous output current, and suit Li-Ion and $LiFePO_4$ batteries as well as supercapacitors. An input protective shunt set at 20V provides overvoltage protection.

TYPICAL APPLICATION

High Voltage Piezoelectric Energy Harvesting Power Supply



LTC3588-2 5.0V Regulator Start-Up Profile



ABSOLUTE MAXIMUM RATINGS (Note 1)

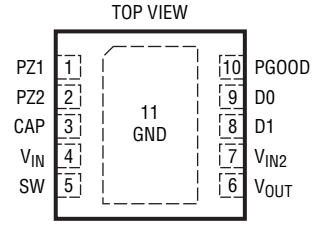
V_{IN}
- Low Impedance Source ..... –0.3V to 18V*
- Current Fed, I_{SW} = 0A ..... 25mA†

PZ1, PZ2 ..... 0V to V_{IN}
D0, D1 ..... –0.3V to [Lesser of (V_{IN2} + 0.3V) or 6V]
CAP ..... [Higher of –0.3V or (V_{IN} – 6V)] to V_{IN}
V_{IN2} ..... –0.3V to [Lesser of (V_{IN} + 0.3V) or 6V]

* V_{IN} has an internal 20V clamp
† For t < 1ms and Duty Cycle < 1%,
Absolute Maximum Continuous Current = 5mA

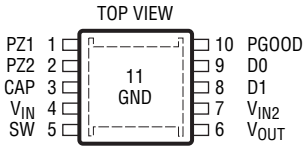
V_{OUT} ..... –0.3V to [Lesser of (V_{IN} + 0.3V) or 6V]
PGOOD ..... –0.3V to [Lesser of (V_{OUT} + 0.3V) or 6V]
I_{PZ1}, I_{PZ2} ..... ±50mA
I_{SW} 350mA
Operating Junction Temperature Range
(Notes 2, 3) ..... –40 to 125°C
Storage Temperature Range ..... –65 to 125°C
Lead Temperature (Soldering, 10 sec)
MSE Only ..... 300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 7.5°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3588EDD-2#PBF	LTC3588EDD-2#TRPBF	LFYK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3588IDD-2#PBF	LTC3588IDD-2#TRPBF	LFYK	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3588EMSE-2#PBF	LTC3588EMSE-2#TRPBF	LTFYM	10-Lead Plastic MSOP	–40°C to 125°C
LTC3588IMSE-2#PBF	LTC3588IMSE-2#TRPBF	LTFYM	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). V_{IN} = 18V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	Low Impedance Source on V_{IN}	●			18.0	V
I_Q	V_{IN} Quiescent Current						
	UVLO	V_{IN} = 12V, Not PGOOD			830	1400	nA
	Buck Enabled, Sleeping	V_{IN} = 18V			1500	2500	nA
	Buck Enabled, Not Sleeping	I_{SW} = 0A (Note 4)			150	250	µA
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising	●		16.0	17.0	V
		V_{IN} Falling	●	13.0	14.0		V
V_{SHUNT}	V_{IN} Shunt Regulator Voltage	I_{VIN} = 1mA		18.8	20.0	21.2	V
I_{SHUNT}	Maximum Protective Shunt Current	1ms Duration		25			mA
	Internal Bridge Rectifier Loss ($\lvert V_{PZ1} - V_{PZ2} \rvert - V_{IN}$)	I_{BRIDGE} = 10µA		350	400	450	mV
	Internal Bridge Rectifier Reverse Leakage Current	$V_{REVERSE}$ = 18V				20	nA
	Internal Bridge Rectifier Reverse Breakdown Voltage	$I_{REVERSE}$ = 1µA		V_{SHUNT}	30		V
V_{OUT}	Regulated Output Voltage	3.45V Output Selected					
		Sleep Threshold	●		3.466	3.554	V
		Wake-Up Threshold	●	3.346	3.434		V
		4.1V Output Selected					
		Sleep Threshold	●		4.116	4.221	V
		Wake-Up Threshold	●	3.979	4.084		V
		4.5V Output Selected					
		Sleep Threshold	●		4.516	4.646	V
		Wake-Up Threshold	●	4.354	4.484		V
		5.0V Output Selected					
		Sleep Threshold	●		5.016	5.175	V
		Wake-Up Threshold	●	4.825	4.984		V
	PGOOD Falling Threshold	As a Percentage of the Selected V_{OUT}		83	92		%
I_{VOUT}	Output Quiescent Current	V_{OUT} = 5.0V			125	250	nA
I_{PEAK}	Buck Peak Switch Current			200	260	350	mA
I_{BUCK}	Available Buck Output Current			100			mA
R_P	Buck PMOS Switch On-Resistance				1.1		Ω
R_N	Buck NMOS Switch On-Resistance				1.3		Ω
	Max Buck Duty Cycle		●	100			%
$V_{IH(D0, D1)}$	D0/D1 Input High Voltage		●	1.2			V
$V_{IL(D0, D1)}$	D0/D1 Input Low Voltage		●			0.4	V
$I_{IH(D0, D1)}$	D0/D1 Input High Current					10	nA
$I_{IL(D0, D1)}$	D0/D1 Input Low Current					10	nA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

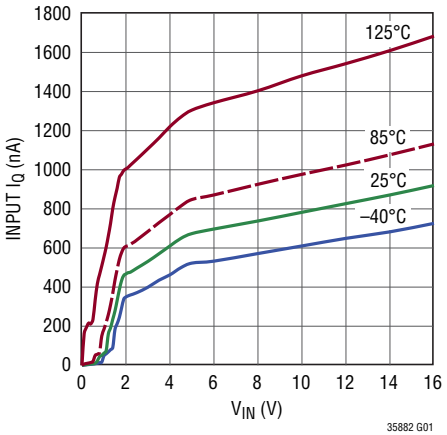
Note 2: The LTC3588E-2 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3588E-2 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3588I-2 is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

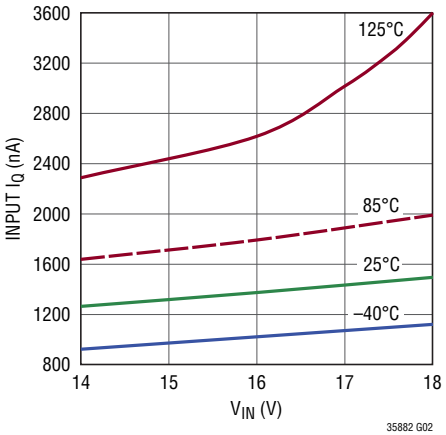
Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

TYPICAL PERFORMANCE CHARACTERISTICS

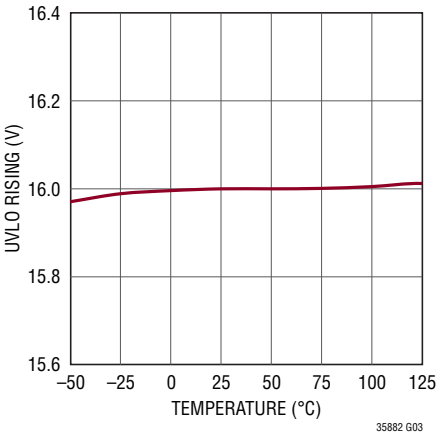
Input I_Q in UVLO vs V_{IN}



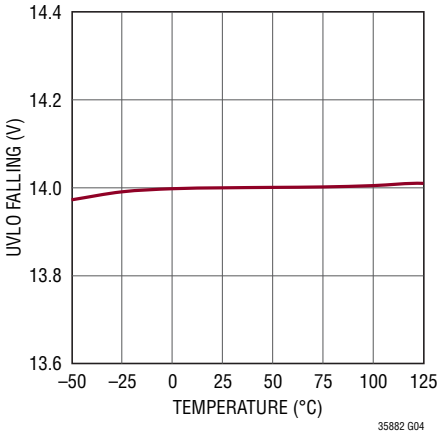
Input I_Q in Sleep vs V_{IN}



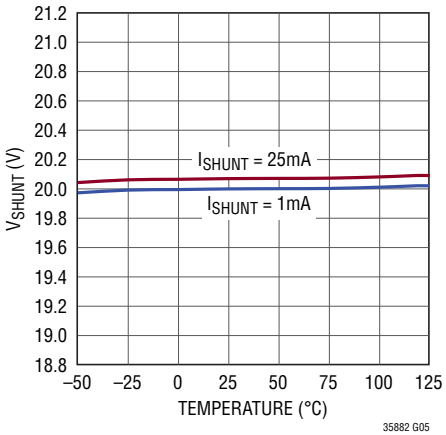
UVLO Rising vs Temperature



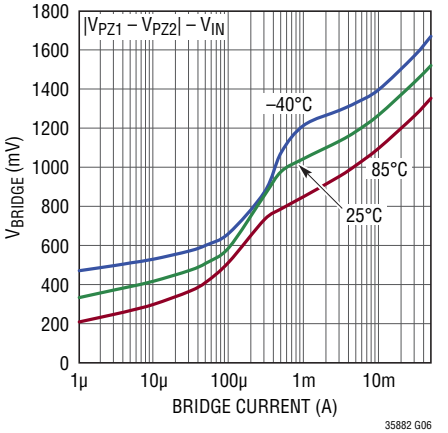
UVLO Falling vs Temperature



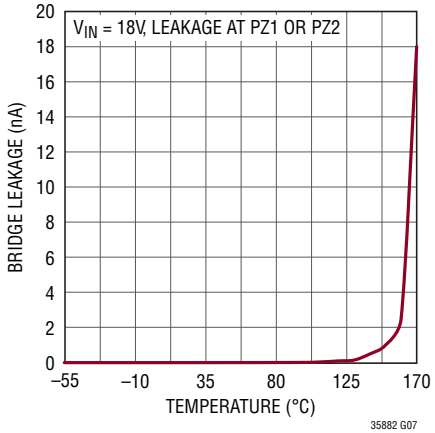
V_{SHUNT} vs Temperature



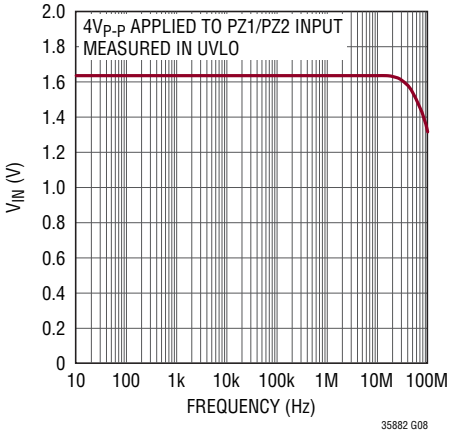
Total Bridge Rectifier Drop vs Bridge Current



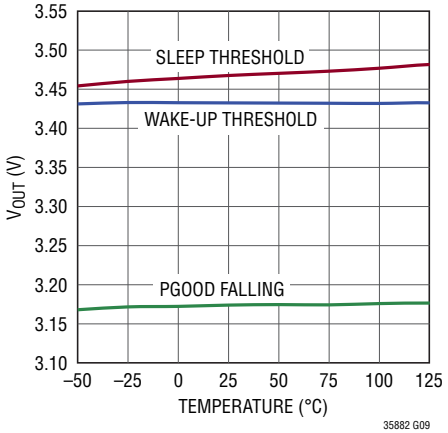
Bridge Leakage vs Temperature



Bridge Frequency Response

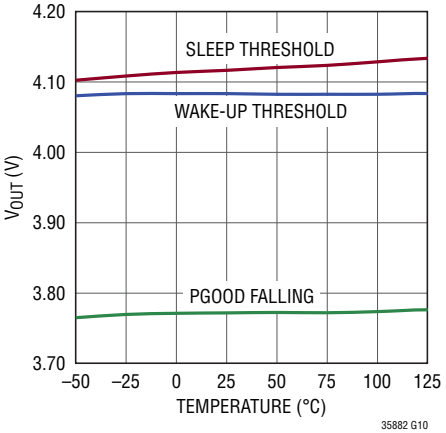


3.45V Output vs Temperature

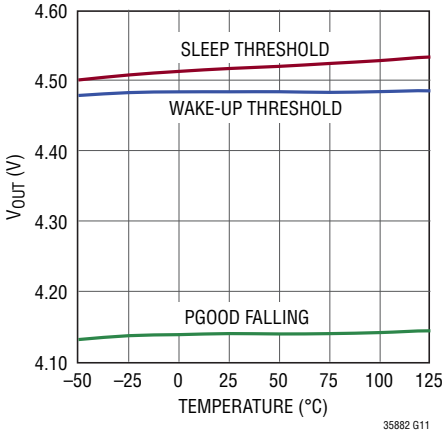


TYPICAL PERFORMANCE CHARACTERISTICS

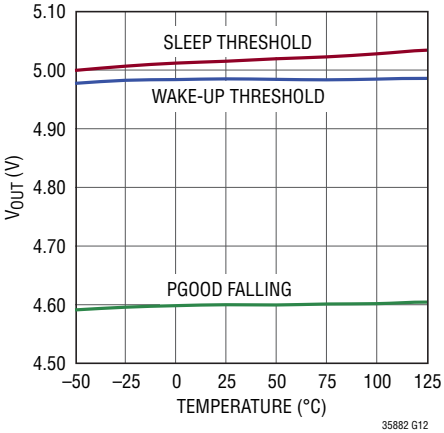
4.1V Output vs Temperature



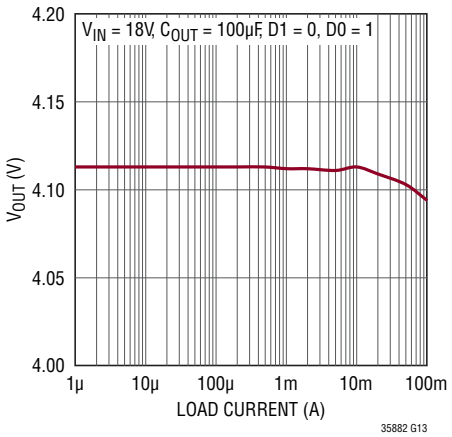
4.5V Output vs Temperature



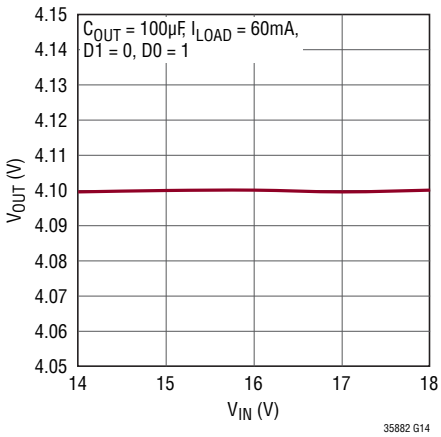
5.0V Output vs Temperature



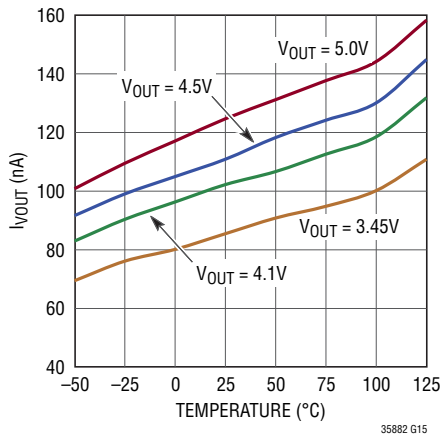
V_{OUT} Load Regulation



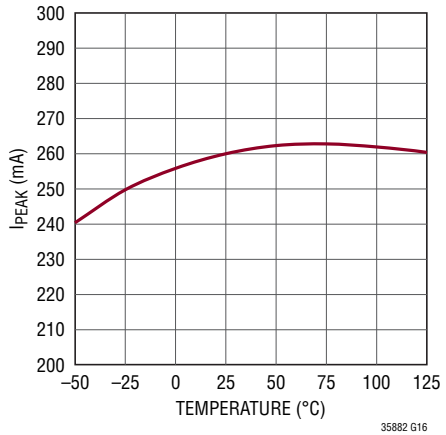
V_{OUT} Line Regulation



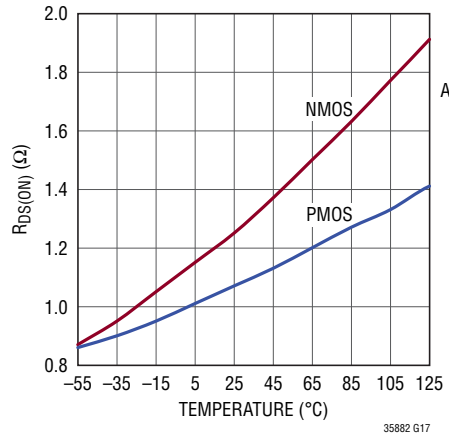
I_{VOUT} vs Temperature



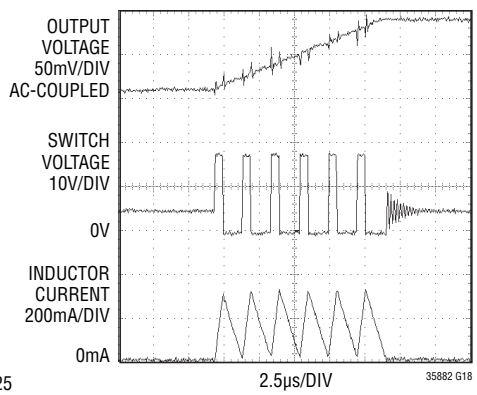
I_{PEAK} vs Temperature



$R_{DS(ON)}$ of PMOS/NMOS vs Temperature



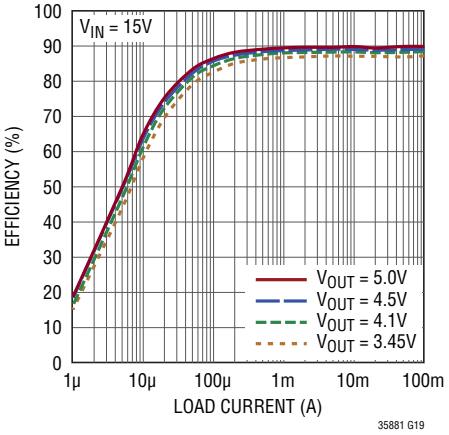
Operating Waveforms



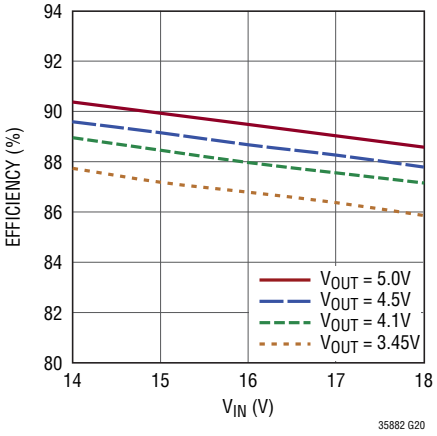
V_{IN} = 18V, V_{OUT} = 5.0V
I_{LOAD} = 1mA
L = 22µH, C_{OUT} = 47µF

TYPICAL PERFORMANCE CHARACTERISTICS

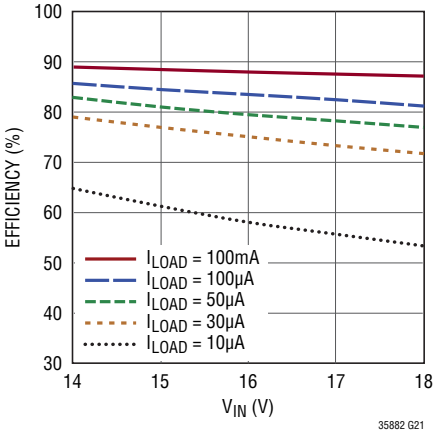
Efficiency vs I_{LOAD}, L = 22µH



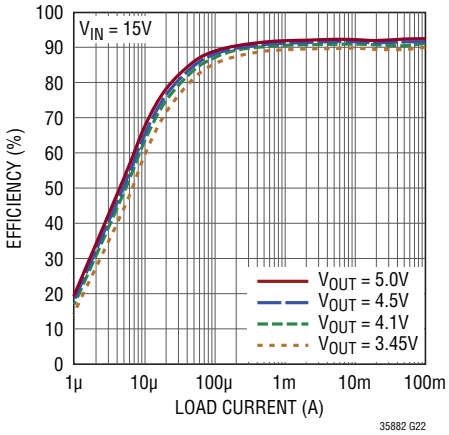
Efficiency vs V_{IN} for I_{LOAD} = 100mA, L = 22µH



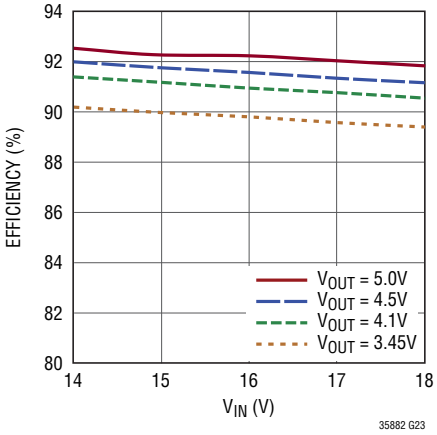
Efficiency vs V_{IN} for V_{OUT} = 4.1V, L = 22µH



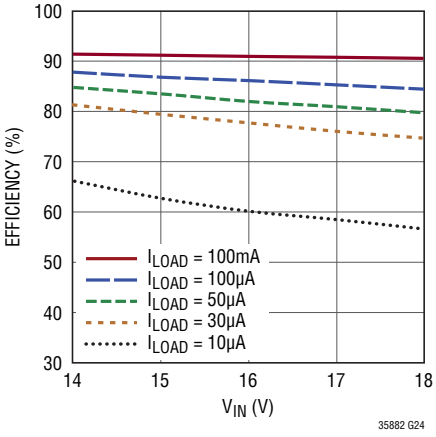
Efficiency vs I_{LOAD}, L = 100µH



Efficiency vs V_{IN} for I_{LOAD} = 100mA, L = 100µH



Efficiency vs V_{IN} for V_{OUT} = 4.1V, L = 100µH



PIN FUNCTIONS

PZ1 (Pin 1): Input connection for piezoelectric element or other AC source (used in conjunction with PZ2).

PZ2 (Pin 2): Input connection for piezoelectric element or other AC source (used in conjunction with PZ1).

CAP (Pin 3): Internal rail referenced to V_{IN} to serve as gate drive for buck PMOS switch. A 1µF capacitor should be connected between CAP and V_{IN}. This pin is not intended for use as an external system rail.

V_{IN} (Pin 4): Rectified Input Voltage. A capacitor on this pin serves as an energy reservoir and input supply for the buck regulator. The V_{IN} voltage is internally clamped to a maximum of 20V (typical).

SW (Pin 5): Switch Pin for the Buck Switching Regulator. A 22µH or larger inductor should be connected from SW to V_{OUT}.

V_{OUT} (Pin 6): Sense pin used to monitor the output voltage and adjust it through internal feedback.

V_{IN2} (Pin 7): Internal low voltage rail to serve as gate drive for buck NMOS switch. Also serves as a logic high rail for output voltage select bits D0 and D1. A 4.7µF capacitor should be connected from V_{IN2} to GND. This pin is not intended for use as an external system rail.

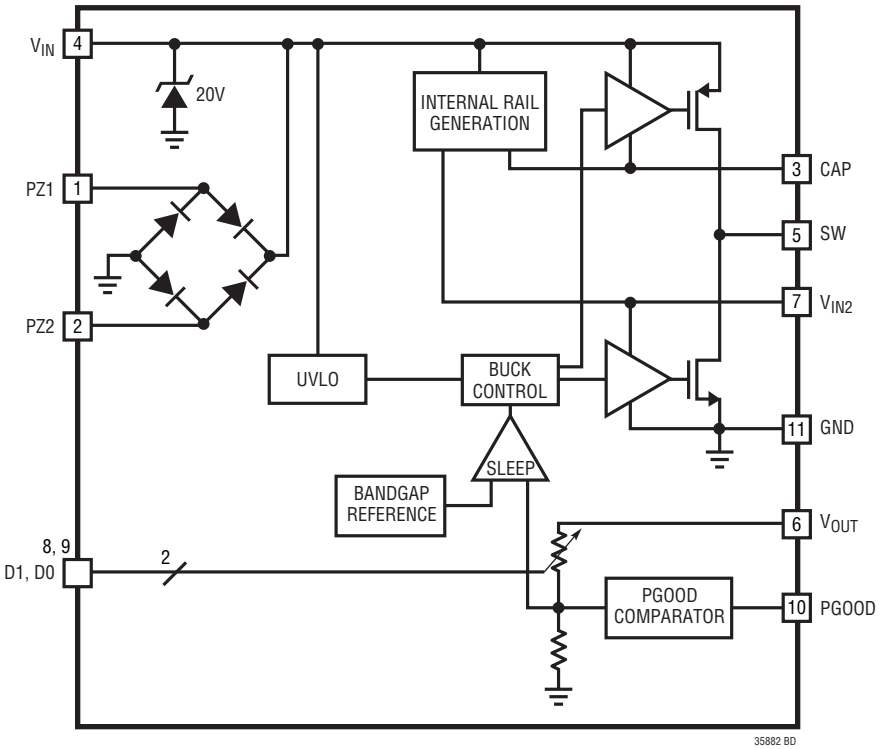
D1 (Pin 8): Output Voltage Select Bit. D1 should be tied high to V_{IN2} or low to GND to select desired V_{OUT} (see Table 1).

D0 (Pin 9): Output Voltage Select Bit. D0 should be tied high to V_{IN2} or low to GND to select desired V_{OUT} (see Table 1).

PGOOD (Pin 10): Power good output is logic high when V_{OUT} is above 92% of the target value. The logic high is referenced to the V_{OUT} rail.

GND (Exposed Pad Pin 11): Ground. The Exposed Pad should be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3588-2.

BLOCK DIAGRAM



OPERATION

The LTC3588-2 is an ultralow quiescent current power supply designed specifically for energy harvesting and/or low current step-down applications. The part is designed to interface directly to a piezoelectric or alternative A/C power source, rectify a voltage waveform and store harvested energy on an external capacitor, bleed off any excess power via an internal shunt regulator, and maintain a regulated output voltage by means of a nanopower high efficiency synchronous buck regulator.

Internal Bridge Rectifier

The LTC3588-2 has an internal full-wave bridge rectifier accessible via the differential PZ1 and PZ2 inputs that rectifies AC inputs such as those from a piezoelectric element. The rectified output is stored on a capacitor at the V_{IN} pin and can be used as an energy reservoir for the buck converter. The low-loss bridge rectifier has a total drop of about 400mV with typical piezo generated currents (~10µA). The bridge is capable of carrying up to 50mA. One side of the bridge can be operated as a single-ended DC input. PZ1 and PZ2 should never be shorted together when the bridge is in use.

Undervoltage Lockout (UVLO)

When the voltage on V_{IN} rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. A wide (~2V) UVLO hysteresis window allows a portion of the energy stored on the input capacitor to be transferred to the output capacitor by the buck. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled. Extremely low quiescent current (830nA typical, V_{IN} = 12V) in UVLO allows energy to accumulate on the input capacitor in situations where energy must be harvested from low power sources.

Internal Rail Generation

Two internal rails, CAP and V_{IN2}, are generated from V_{IN} and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the V_{IN2} rail serves as logic high for output voltage select bits D0 and D1. The V_{IN2} rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below V_{IN}. These are not intended to be used as external rails. Bypass capacitors are connected to the CAP and V_{IN2} pins to serve as energy reservoirs for driving the buck switches. When V_{IN} is below 4.8V, V_{IN2} is equal to V_{IN} and CAP is held at GND. Figure 1 shows the ideal V_{IN}, V_{IN2} and CAP relationship.

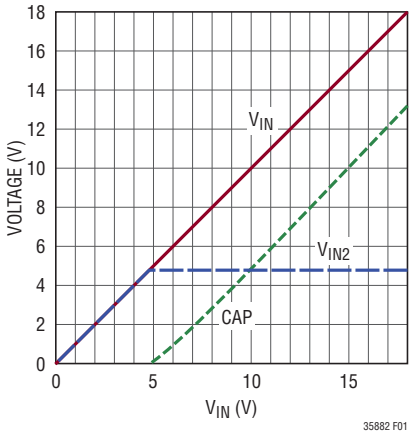


Figure 1. Ideal V_{IN}, V_{IN2} and CAP Relationship

Buck Operation

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the V_{OUT} sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to 260mA through an internal PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by V_{IN}, V_{OUT}, and the inductor value. If the input voltage falls below the UVLO falling threshold before the output voltage reaches regulation, the buck converter will shut off and will not be turned on until the input voltage again rises above the UVLO rising threshold. During this time the output voltage will be loaded by approximately 100nA. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the buck output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA of average current to the output when it is switching.

OPERATION

When the sleep comparator signals that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still flowing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode. The LTC3588-2 keeps the NMOS switch on during this time to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero.

Though the quiescent current when the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when sufficient energy has been accumulated in the input capacitor and the length of time the converter needs to transfer energy to the output is much less than the time it takes to accumulate energy. Thus, the buck operating quiescent current is averaged over a long period of time so that the total average quiescent current is low. This feature accommodates sources that harvest small amounts of ambient energy.

Four selectable voltages are available by tying the output select bits, D0 and D1, to GND or V_{IN2}. Table 1 shows the four D0/D1 codes and their corresponding output voltages.

Table 1. Output Voltage Selection

D1	D0	V_{OUT}	V_{OUT} QUIESCENT CURRENT (I_{VOUT})
0	0	3.45V	86nA
0	1	4.1V	101nA
1	0	4.5V	111nA
1	1	5.0V	125nA

The internal feedback network draws a small amount of current from V_{OUT} as listed in Table 1.

Power Good Comparator

A power good comparator produces a logic high referenced to V_{OUT} on the PGOOD pin the first time the converter reaches the sleep threshold of the programmed V_{OUT}, signaling that the output is in regulation. The PGOOD pin will remain high until V_{OUT} falls to 92% of the desired regulation voltage. Several sleep cycles may occur during this time. Additionally, if PGOOD is high and V_{IN} falls below the UVLO falling threshold, PGOOD will remain high until V_{OUT} falls to 92% of the desired regulation point. This allows output energy to be used even if the input is lost. Figure 2 shows the behavior for V_{OUT} = 5V and a 10µA load. At t = 2s V_{IN} becomes high impedance and is discharged by the quiescent current of the LTC3588-2 and through servicing V_{OUT} which is discharged by its own leakage current. V_{IN} crosses UVLO falling but PGOOD remains high until V_{OUT} decreases to 92% of the desired regulation point. The PGOOD pin is designed to drive a microprocessor or other chip I/O and is not intended to drive higher current loads such as an LED.

The D0/D1 inputs can be switched while in regulation as shown in Figure 3. If V_{OUT} is programmed to a voltage with a PGOOD falling threshold above the old V_{OUT}, PGOOD will

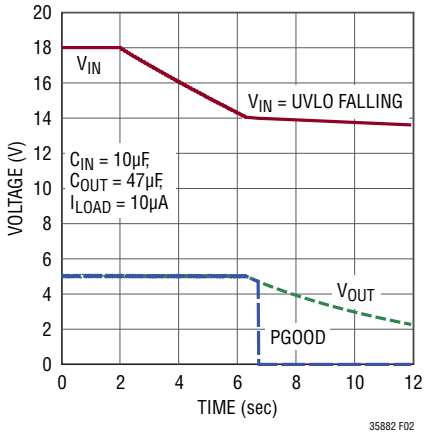


Figure 2. PGOOD Operation During Transition to UVLO

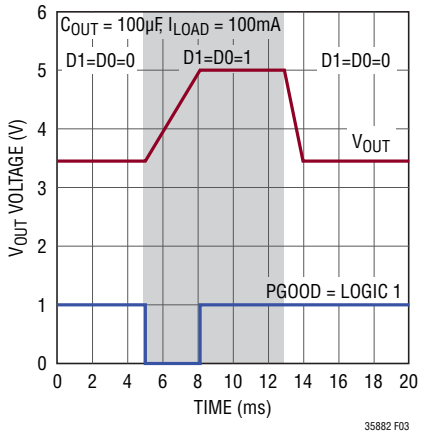


Figure 3. PGOOD Operation During D0/D1 Transition

OPERATION

transition low until the new regulation point is reached. When V_{OUT} is programmed to a lower voltage, PGOOD will remain high through the transition.

Energy Storage

Harvested energy can be stored on the input capacitor or the output capacitor. The high UVLO threshold takes advantage of the fact that energy storage on a capacitor is proportional to the square of the capacitor voltage. After the output voltage is brought into regulation any excess energy is stored on the input capacitor and its voltage increases. When a load exists at the output the buck can efficiently transfer energy stored at a high voltage to the regulated output. While energy storage at the input utilizes the high voltage at the input, the load current is limited to what the buck converter can supply. If larger loads need to be serviced the output capacitor can be sized to support a larger current for some duration. For example, a current burst could begin when PGOOD goes high and would continuously deplete the output capacitor until PGOOD went low.

The output voltages available on the LTC3588-2 are particularly suited to Li-Ion and $LiFePO_4$ batteries as well as supercapacitors for applications where energy storage at the output is desired.

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Introduction

The LTC3588-2 harvests ambient vibrational energy through a piezoelectric element in its primary application. Common piezoelectric elements are PZT (lead zirconate titanate) ceramics, PVDF (polyvinylidene fluoride) polymers, or other composites. Ceramic piezoelectric elements exhibit a piezoelectric effect when the crystal structure of the ceramic is compressed and internal dipole movement produces a voltage. Polymer elements comprised of long-chain molecules produce a voltage when flexed as molecules repel each other. Ceramics are often used under direct pressure while a polymer can be flexed more readily. A wide range of piezoelectric elements are available and produce a variety of open-circuit voltages and short-circuit currents. Typically the open-circuit voltage and short-circuit currents increase with available vibrational energy as shown in Figure 4. Piezoelectric elements can be placed in series or in parallel to achieve desired open-circuit voltages.

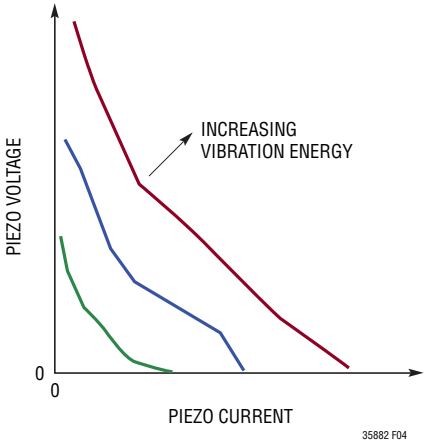

Figure 4. Typical Piezoelectric Load Lines

The LTC3588-2 is well-suited to a piezoelectric energy harvesting application. The 20V input protective shunt can accommodate a variety of piezoelectric elements. The low quiescent current of the LTC3588-2 enables efficient energy accumulation from piezoelectric elements which can have short-circuit currents on the order of tens of microamps. Piezoelectric elements can be obtained from manufacturers listed in Table 2.

Table 2. Piezoelectric Element Manufacturers

Advanced Cerametrics	www.advancedcerametrics.com
Piezo Systems	www.piezo.com
Measurement Specialties	www.meas-spec.com
PI (Physik Instrumente)	www.pi-usa.us
MIDE Technology Corporation	www.mide.com
Morgan Technical Ceramics	www.morganelectroceramics.com

APPLICATIONS INFORMATION

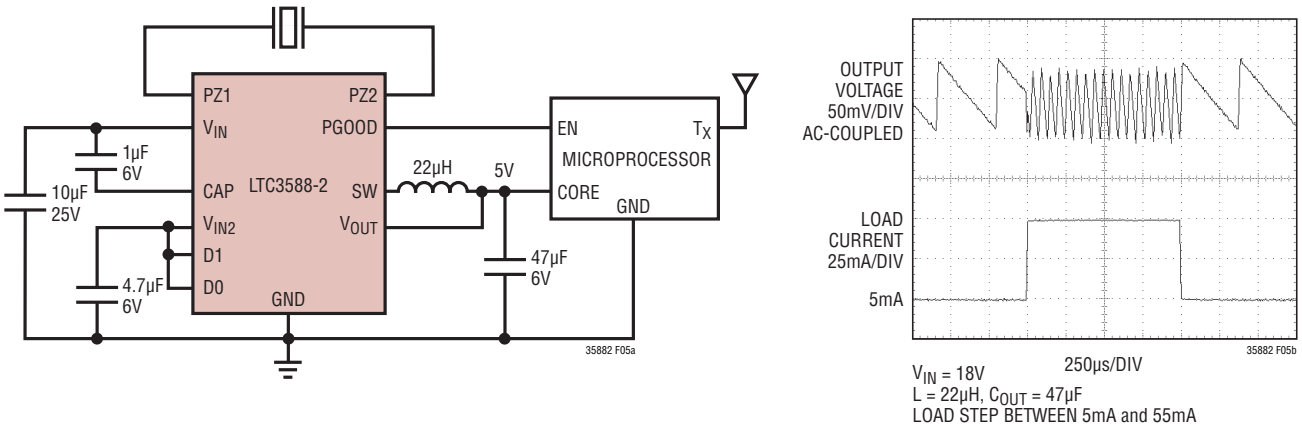

Figure 5. 5V Piezoelectric Energy Harvester Powering a Microprocessor with a Wireless Transmitter and 50mA Load Step Response

The LTC3588-2 will gather energy and convert it to a useable output voltage to power microprocessors, wireless sensors, and wireless transmission components. Such a wireless sensor application may require much more peak power than a piezoelectric element can produce. However, the LTC3588-2 accumulates energy over a long period of time to enable efficient use for short power bursts. For continuous operation, these bursts must occur with a low duty cycle such that the total output energy during the burst does not exceed the average source power integrated over an energy accumulation cycle. For piezoelectric inputs the time between cycles could be minutes, hours, or longer depending on the selected capacitor values and the nature of the vibration source.

PGOOD Signal

The PGOOD signal can be used to enable a sleeping microprocessor or other circuitry when V_{OUT} reaches regulation, as shown in Figure 5. Typically V_{IN} will be somewhere between the UVLO thresholds at this time and a load could only be supported by the output capacitor. Alternatively, waiting a period of time after PGOOD goes high would let the input capacitor accumulate more energy allowing load current to be maintained longer as the buck efficiently transfers that energy to the output. While active, a microprocessor may draw a small load when operating sensors, and then draw a large load to transmit data. Figure 5 shows the LTC3588-2 responding smoothly to such a load step.

Input and Output Capacitor Selection

The input and output capacitors should be selected based on the energy needs and load requirements of the application. In every case the V_{IN} capacitor should be rated to withstand the highest voltage ever present at V_{IN}. For 100mA or smaller loads, storing energy at the input takes advantage of the high voltage input since the buck can deliver 100mA average load current efficiently to the output. The input capacitor should then be sized to store enough energy to provide output power for the length of time required. This may involve using a large capacitor, letting V_{IN} charge to a high voltage, or both. Enough energy should be stored on the input so that the buck does not reach the UVLO falling threshold which would halt energy transfer to the output. In general:

$$P_{LOAD} t_{LOAD} = \frac{1}{2} \eta C_{IN} \left(V_{IN}^2 - V_{UVLO(FALLING)}^2 \right)$$

$$V_{UVLO(FALLING)} \leq V_{IN} \leq V_{SHUNT}$$

The above equation can be used to size the input capacitor to meet the power requirements of the output for an application with continuous input energy. Here η is the average efficiency of the buck converter over the input range and V_{IN} is the input voltage when the buck begins to switch. This equation may overestimate the input capacitor necessary since load current can deplete the output capacitor all the way to the lower PGOOD threshold. It also assumes that the input source charging has a negligible

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effect during this time. For applications where the output must reach regulation on a single UVLO cycle, the energy required to charge the output capacitor must be taken into account when sizing C_{IN}.

The duration for which the regulator sleeps depends on the load current and the size of the output capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The DC sleep hysteresis window is ±16mV around the programmed output voltage. Ideally this means that the sleep time is determined by the following equation:

$$t_{SLEEP} = C_{OUT} \frac{32mV}{I_{LOAD}}$$

This is true for output capacitors on the order of 100µF or larger, but as the output capacitor decreases towards 10µF delays in the internal sleep comparator along with the load current may result in the V_{OUT} voltage slewing past the ±16mV thresholds. This will lengthen the sleep time and increase V_{OUT} ripple. A capacitor less than 10µF is not recommended as V_{OUT} ripple could increase to an undesirable level.

If transient load currents above 100mA are required then a larger capacitor can be used at the output. This capacitor will be continuously discharged during a load condition and the capacitor can be sized for an acceptable drop in V_{OUT}:

$$C_{OUT} = (I_{LOAD} - I_{BUCK}) \frac{t_{LOAD}}{V_{OUT}^{+} - V_{OUT}^{-}}$$

Here V_{OUT}^{+} is the value of V_{OUT} when PGOOD goes high and V_{OUT}^{-} is the desired lower limit of V_{OUT}. I_{BUCK} is the average current being delivered from the buck converter, typically $I_{PEAK}/2$.

A standard surface mount ceramic capacitor can be used for C_{OUT}, though some applications may be better suited to a low leakage aluminum electrolytic capacitor or a supercapacitor. These capacitors can be obtained from manufacturers such as Vishay, Illinois Capacitor, AVX, or CAP-XX.

Inductor

The buck is optimized to work with a 22µH inductor. Inductor values greater than 22µH may yield benefits in some applications. For example, a larger inductor will benefit high voltage applications by increasing the on-time of the PMOS switch and improving efficiency by reducing gate charge loss. Choose an inductor with a DC current rating greater than 350mA. The DCR of the inductor can have an impact on efficiency as it is a source of loss. Trade-offs between price, size, and DCR should be evaluated. Table 3 lists several inductors that work well with the LTC3588-2.

Table 3. Recommended Inductors for LTC3588-2

INDUCTOR TYPE	L (µH)	MAX I_{DC} (mA)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
A997AS-220M	22	390	0.440	4.0 × 4.0 × 1.8	Toko
LPS5030-223MLC	22	700	0.190	4.9 × 4.9 × 3.0	Coilcraft
LPS4012-473MLC	47	350	1.400	4.0 × 4.0 × 1.2	Coilcraft
SLF7045T	100	500	0.250	7.0 × 7.0 × 4.8	TDK

V_{IN2} and CAP Capacitors

A 1µF capacitor should be connected between V_{IN} and CAP and a 4.7µF capacitor should be connected between V_{IN2} and GND. These capacitors hold up the internal rails during buck switching and compensate the internal rail generation circuits.

Additional Applications with Piezo Inputs

The versatile LTC3588-2 can be used in a variety of configurations. Figure 6 shows a single piezo source powering two LTC3588-2s simultaneously, providing capability for multiple rail systems. As the piezo provides input power both V_{IN} rails will initially come up together, but when one output starts drawing power, only its corresponding V_{IN} will fall as the bridges of each LTC3588-2 provide isolation. Input piezo energy will then be directed to this lower voltage capacitor until both V_{IN} rails are again equal. This configuration is expandable to any number of LTC3588-2s powered by a single piezo as long as the piezo can support the sum total of the quiescent currents from each LTC3588-2.

APPLICATIONS INFORMATION

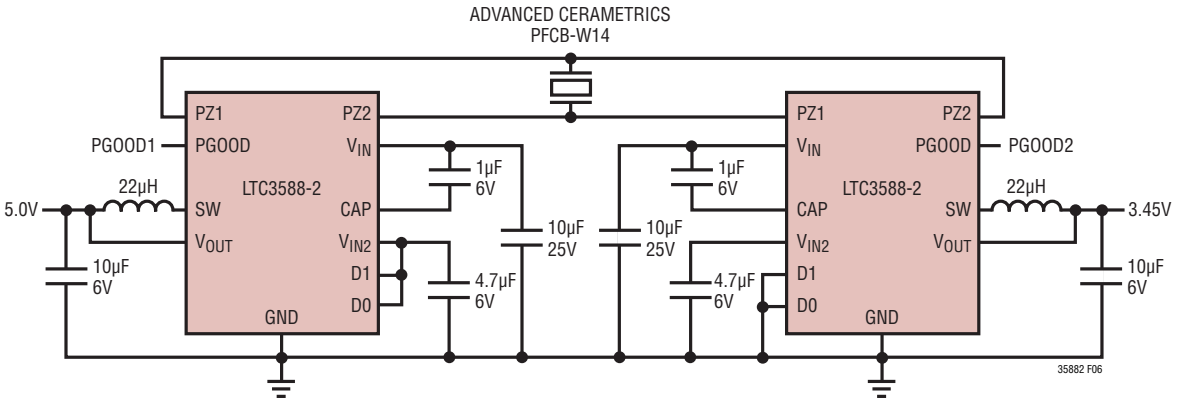
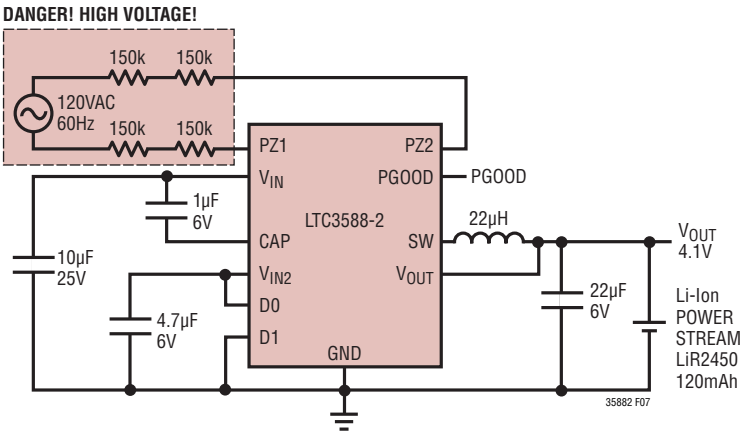


Figure 6. Dual Rail Power Supply with Single Piezo



DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS! BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION. ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.

Figure 7. AC Line Powered 4.1V Li-Ion Battery Charger

Alternate Power Sources

The LTC3588-2 is not limited to use with piezoelectric elements but can accommodate a wide variety of input sources depending on the type of ambient energy available. Figure 7 shows the LTC3588-2 internal bridge rectifier connected to the AC line in series with four 150k current limiting resistors. This is a high voltage application and minimum spacing between the line, neutral, and any high voltage components should be maintained per the applicable UL specification. For general off-line applications refer to UL regulation 1012.

Figure 8 shows an application where copper panels are placed near a standard fluorescent room light to capacitively harvest energy from the electric field around the light. The

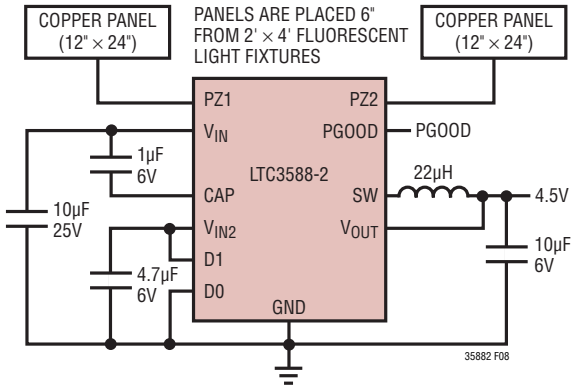


Figure 8. Electric Field Energy Harvester

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frequency of the emission will be 120Hz for magnetic ballasts but could be higher if the light uses electronic ballast. The LTC3588-2 bridge rectifier can handle a wide range of input frequencies.

Figure 9 shows the LTC3588-2 powered by a 48V communications line. In this example, 1mA is the maximum current that is allowed to be drawn. The 28k current limiting resistor sets this current as the LTC3588-2 will shunt V_{IN} at 20V. The advantage of this scheme is that the current at the output is multiplied by the ratio of V_{IN} to V_{OUT} (less the loss in the buck converter). This is useful in cases where greater current is needed at the output than is available at the input. The high UVLO of 16V prevents any start-up issue as there is already a good multiplication factor at that level. This same technique can be extended to AC source that also have limited current available at the input.

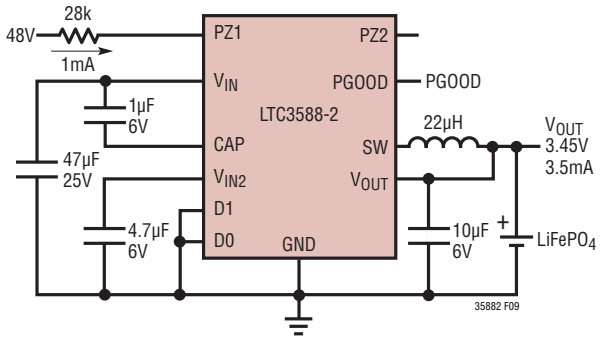
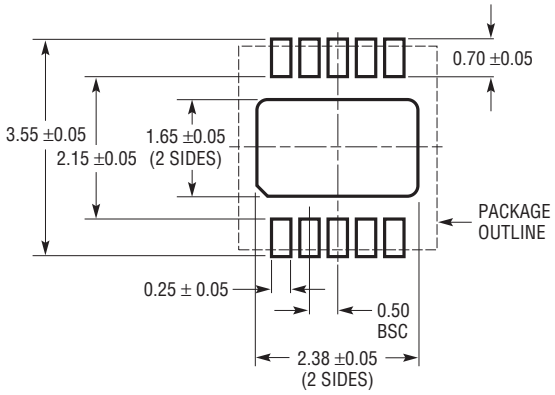


Figure 9. Current Fed 3.45V $LiFePO_4$ Battery Charger

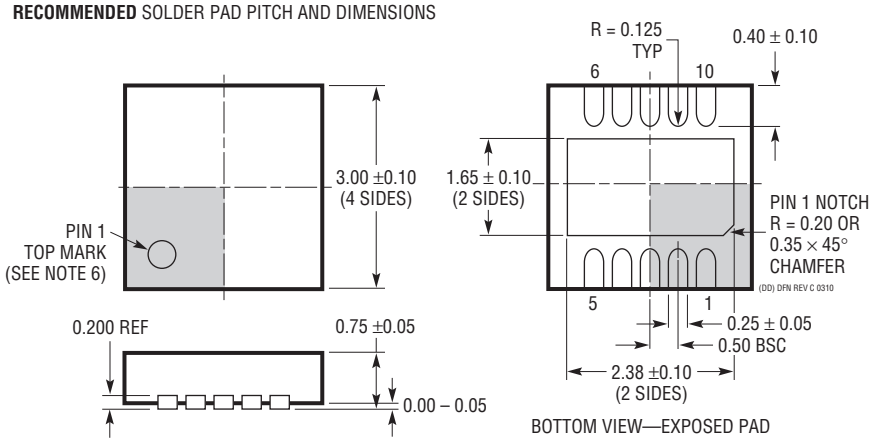
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



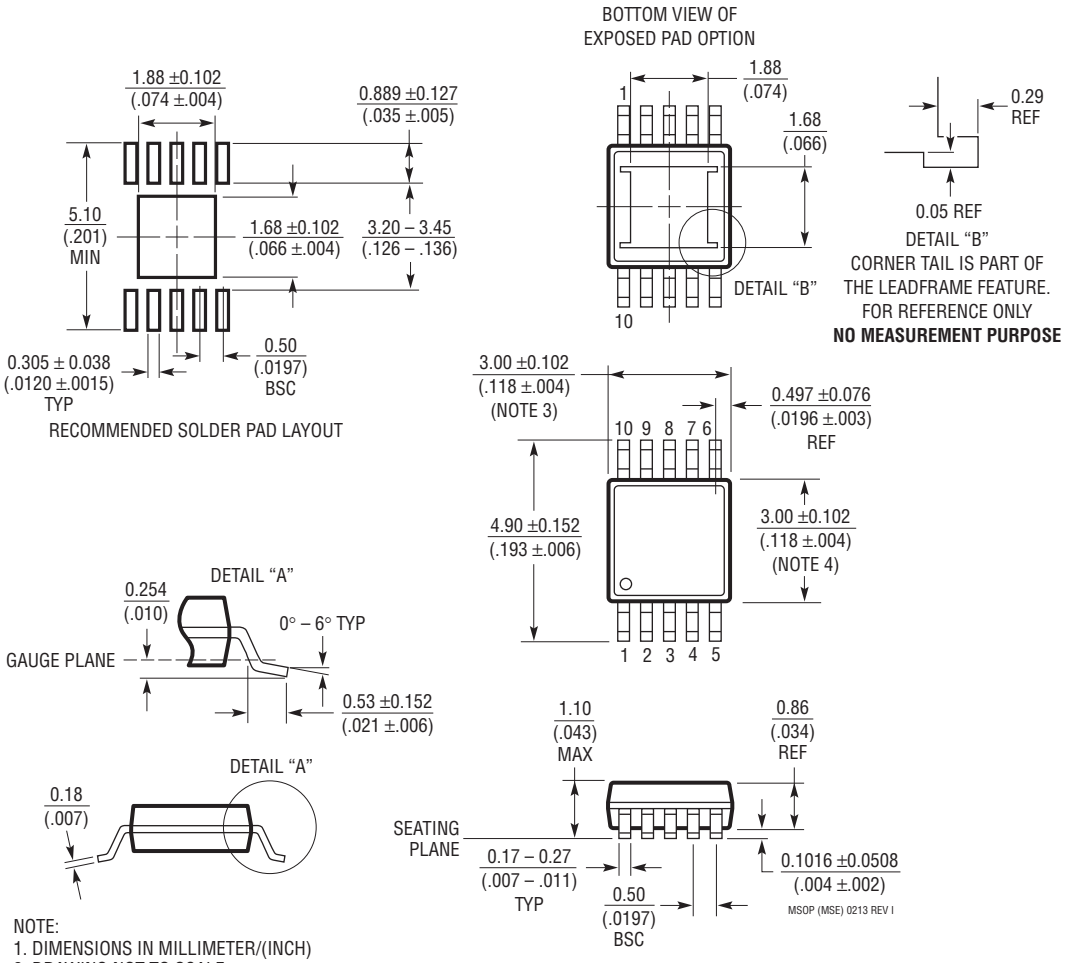
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev I)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	5/11	Add brackets to Absolute Maximum Ratings for V_{OUT} and PGOOD.	2
		Replace MS package description to the correct MSE package description.	15
		Add to Related Parts section and order parts by part number.	16
B	7/14	Clarified title and Description	1
		Clarified x-axis label on Figure 1	8
		Clarified Figure 8	14
		Clarified Related Parts list	18
C	8/15	Modified C_{OUT} Equation	12