Highly Integrated Portable Product PMIC

FEATURES

- **Full Featured Li-Ion/Polymer Charger/PowerPath™ Controller with Instant-On Operation**
- **Triple Adjustable High Efficiency Step-Down Switching Regulators (800mA, 500mA, 500mA I_{OUT})**
- **I^2C Adjustable SW Slew Rates for EMI Reduction**
- **High Temperature Battery Voltage Reduction Improves Safety and Reliability**
- Overvoltage Protection Controller for USB (V_{BUS})/Wall Inputs Provide Protection to 30V
- 1.5A Maximum Charge Current with Thermal Limiting
- Battery Float Voltage: 4.2V
- Pushbutton ON/OFF Control with System Reset
- Dual 150mA Current Limited LDOs
- Start-Up Timing Compatible with SiRF Atlas IV Processor
- Small 4mm × 7mm 44-Pin QFN Package

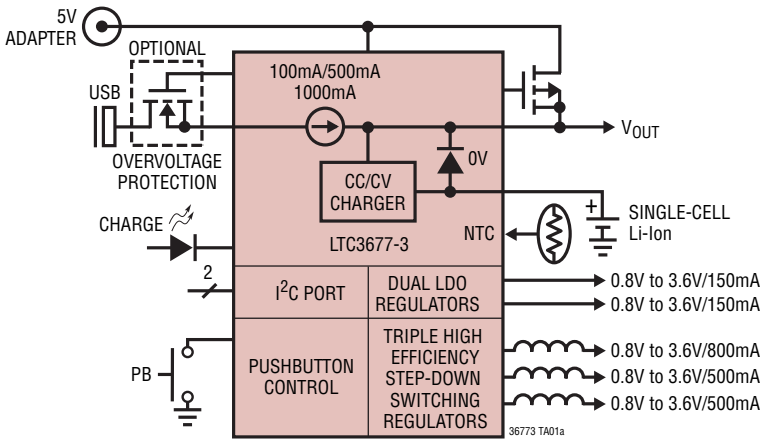
APPLICATIONS

- PNDs, DMB/DVB-H, Digital/Satellite Radio, Media Players
- Portable Industrial/Medical Products
- Other USB-Based Handheld Products

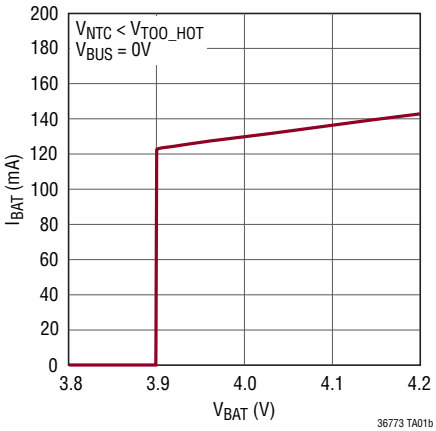
DESCRIPTION

The LTC®3677-3 is a highly integrated power management IC for single-cell Li-Ion/Polymer battery applications. It includes a PowerPath manager with automatic load prioritization, a battery charger, an ideal diode, input overvoltage protection and numerous other internal protection features. The LTC3677-3 is designed to accurately charge from current limited supplies such as USB by automatically reducing charge current such that the sum of the load current and the charge current does not exceed the programmed input current limit (100mA or 500mA modes). The LTC3677-3 reduces the battery voltage at elevated temperatures to improve safety and reliability. The three step-down switching regulators and two LDOs provide a wide range of available supplies. The LTC3677-3 also includes a pushbutton input to control power sequencing and system reset. The LTC3677-3 has pushbutton timing and sequencing designed to support the SiRF Atlas IV processor. The LTC3677-3 is available in a low profile 4mm × 7mm × 0.75mm 44-pin QFN package.

TYPICAL APPLICATION



High Temperature BAT Discharge



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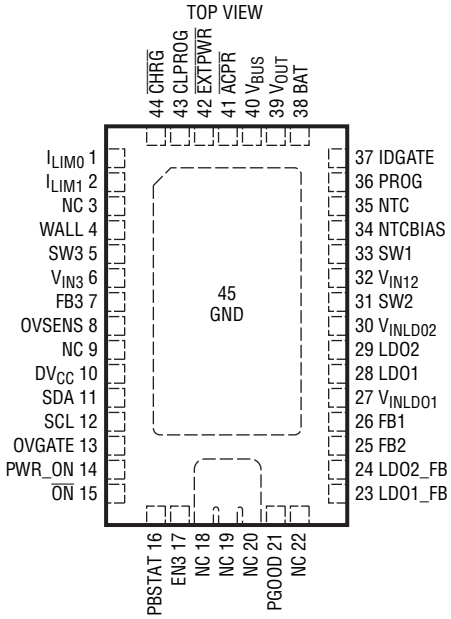
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{BUS}, V_{OUT}, V_{IN12}, V_{IN3}, V_{INLDO1}, V_{INLDO2}, WALL
t < 1ms and Duty Cycle < 1% ..... –0.3V to 7V
Steady State ..... –0.3V to 6V
$\overline{CHRG}$, BAT, PWR_ON, $\overline{EXTPWR}$, PBSTAT, PGOOD, FB1, FB2, FB3, LDO1, LDO1_FB, LDO2, LDO2_FB, DV_{CC}, SCL, SDA, EN3 ..... –0.3V to 6V
NTC, PROG, CLPROG, $\overline{ON}$, I_{LIM0}, I_{LIM1} (Note 4) ..... –0.3V to V_{CC} + 0.3V
I_{VBUS}, I_{VOUT}, I_{BAT}, Continuous (Note 16) 2A
I_{SW3}, Continuous (Note 16) 850mA
I_{SW2}, I_{SW1}, Continuous (Note 16) 600mA
I_{LDO1}, I_{LDO2}, Continuous (Note 16) 200mA
$I_{\overline{CHRG}}$, $I_{\overline{ACPR}}$, $I_{\overline{EXTPWR}}$, I_{PBSTAT}, I_{PGOOD} 75mA
I_{OVSENS} 10mA
I_{CLPROG}, I_{PROG} 2mA
Operating Junction Temperature Range (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature ..... 110°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UFF PACKAGE
44-LEAD (7mm × 4mm) PLASTIC QFN

T_{JMAX} = 110°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 45) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3677EUFF-3#PBF	LTC3677EUFF-3#TRPBF	36773	44-Lead (4mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

Power Manager. The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{BUS} = 5V, V_{BAT} = 3.8V, I_{LIM0} = I_{LIM1} = 5V, WALL = 0V, V_{INLDO2} = V_{INLDO1} = V_{IN12} = V_{IN3} = V_{OUT}, R_{PROG} = 2k, R_{CLPROG} = 2.1k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
I_{BUS_LIM}	Total Input Current (Note 5)	I_{LIM0} = 5V, I_{LIM1} = 5V (1x Mode) I_{LIM0} = 0V, I_{LIM1} = 0V (5x Mode) I_{LIM0} = 0V, I_{LIM1} = 5V (10x Mode)	● ● ●	80 450 900	90 475 950	100 500 1000	mA mA mA
I_{BUSQ}	Input Quiescent Current, POFF State	1x, 5x, 10x Modes I_{LIM0} = 5V, I_{LIM1} = 0V (Suspend Mode)			0.42 0.05	 0.1	mA mA
h_{CLPROG}	Ratio of Measured V_{BUS} Current to CLPROG Program Current				1000		mA/mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x Mode 5x Mode 10x Mode			0.2 1.0 2.0		V V V
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.5	3.8 3.7	3.9 	V V
V_{DUVLO}	V_{BUS} to V_{OUT} Differential Undervoltage Lockout	Rising Threshold Falling Threshold			50 –50	100 	mV mV
R_{ON_ILIM}	Input Current Limit Power FET On-Resistance (Between V_{BUS} and V_{OUT})				200		mΩ
Battery Charger							
V_{FLOAT}	V_{BAT} Regulated Output Voltage	LTC3677-3 LTC3677-3, 0 ≤ T_J ≤ 85°C		4.179 4.165	4.200 4.200	4.221 4.235	V V
I_{CHG}	Constant-Current Mode Charge Current IC Not in Thermal Limit	R_{PROG} = 1k, Input Current Limit = 2A R_{PROG} = 2k, Input Current Limit = 1A R_{PROG} = 5k, Input Current Limit = 0.4A	● ● ●	950 465 180	1000 500 200	1050 535 220	mA mA mA
I_{BATQ_OFF}	Battery-Drain Current, POFF State, Buck3 Disabled, No Load (Note 14)	V_{BAT} = 4.3V, Charger Time Out V_{BUS} = 0V			6 55	27 100	µA µA
I_{BATQ_ON}	Battery-Drain Current, PON State, Buck3 Enabled (Notes 10, 14)	V_{BUS} = 0V, I_{OUT} = 0µA, No Load On Supplies, Burst Mode® Operation			130	200	µA
$V_{PROG,CHG}$	PROG Pin Servo Voltage	V_{BAT} > V_{TRKL}			1.000		V
$V_{PROG,TRKL}$	PROG Pin Servo Voltage in Trickle Charge	V_{BAT} < V_{TRKL}			0.100		V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1000		mA/mA
I_{TRKL}	Trickle Charge Current	V_{BAT} < V_{TRKL}		40	50	60	mA
V_{TRKL}	Trickle Charge Rising Threshold Trickle Charge Falling Threshold	V_{BAT} Rising V_{BAT} Falling		 2.5	2.9 2.75	3.0 	V V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts when V_{BAT} = V_{FLOAT} – 50mV		3.2	4	4.8	Hour
t_{BADBAT}	Bad Battery Termination Time	V_{BAT} < V_{TRKL}		0.4	0.5	0.6	Hour
$h_{C/10}$	End-of-Charge Indication Current Ratio	(Note 6)		0.085	0.1	0.11	mA/mA
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)				200		mΩ
T_{LIM}	Junction Temperature in Constant-Temperature Mode				110		°C

ELECTRICAL CHARACTERISTICS

Power Manager. The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{BUS} = 5V, V_{BAT} = 3.8V, I_{LIM0} = I_{LIM1} = 5V, WALL = 0V, V_{INLDO2} = V_{INLDO1} = V_{IN12} = V_{IN3} = V_{OUT}, R_{PROG} = 2k, R_{CLPROG} = 2.1k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC, Battery Discharge Protection							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising NTC Voltage Hysteresis		75	76 1.3	77	$\%V_{NTCBIAS}$ $\%V_{NTCBIAS}$
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling NTC Voltage Hysteresis		34	35 1.3	36	$\%V_{NTCBIAS}$ $\%V_{NTCBIAS}$
V_{TOO_HOT}	NTC Discharge Threshold Voltage	Falling NTC Voltage Hysteresis		24.5	25.5 50	26.5	$\%V_{NTCBIAS}$ mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{BUS} = 5V		–50		50	nA
$I_{BAT2HOT}$	BAT Discharge Current	V_{BAT} = 4.1V, NTC < V_{TOO_HOT}			170		mA
$V_{BAT2HOT}$	BAT Discharge Threshold	I_{BAT} < 0.1mA, NTC < V_{TOO_HOT}			3.9		V
Ideal Diode							
V_{FWD}	Forward Voltage Detection	I_{OUT} = 10mA		5	15	25	mV
$R_{DROPOUT}$	Diode On-Resistance, Dropout	I_{OUT} = 200mA			200		mΩ
I_{MAX}	Diode Current Limit	(Note 7)			3.6		A
Overvoltage Protection							
$V_{OVCUTOFF}$	Overvoltage Protection Threshold	Rising Threshold, R_{OVSENS} = 6.2k		6.10	6.35	6.70	V
V_{OVGATE}	OVGATE Output Voltage	Input Below $V_{OVCUTOFF}$ Input Above $V_{OVCUTOFF}$			1.88 • V_{OVSENS} 0	12	V V
$I_{OVSENSQ}$	OVSENS Quiescent Current	V_{OVSENS} = 5V			40		µA
t_{RISE}	OVGATE Time to Reach Regulation	C_{OVGATE} = 1nF			2.5		ms
Wall Adapter and High Voltage Buck Output Control							
$V_{\overline{ACPR}}$	$\overline{ACPR}$ Pin Output High Voltage $\overline{ACPR}$ Pin Output Low Voltage	$I_{\overline{ACPR}}$ = 0.1mA $I_{\overline{ACPR}}$ = 1mA		V_{OUT} – 0.3	V_{OUT} 0	 0.3	V V
V_W	Absolute Wall Input Threshold Voltage	V_{WALL} Rising V_{WALL} Falling		 3.1	4.3 3.2	4.45	V V
ΔV_W	Differential Wall Input Threshold Voltage	V_{WALL} – V_{BAT} Falling V_{WALL} – V_{BAT} Rising		0	25 75	 100	mV mV
I_{QWALL}	Wall Operating Quiescent Current	I_{WALL} + I_{VOUT}, I_{BAT} = 0mA, WALL = V_{OUT} = 5V			440		µA
Logic (I_{LIM0}, I_{LIM1} and $\overline{CHRG}$)							
V_{IL}	Input Low Voltage	I_{LIM0}, I_{LIM1}				0.4	V
V_{IH}	Input High Voltage	I_{LIM0}, I_{LIM1}		1.2			V
I_{PD}	Static Pull-Down Current	I_{LIM0}, I_{LIM1}; V_{PIN} = 1V			2		µA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 10mA			0.15	0.4	V
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Input Current	V_{BAT} = 4.5V, $V_{\overline{CHRG}}$ = 5V			0	1	µA

ELECTRICAL CHARACTERISTICS

I²C Interface. The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. DV_{CC} = 3.3V, V_{OUT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DV_{CC}	Input Supply Voltage			1.6		5.5	V
I_{DVCC}	DV_{CC} Supply Current	SCL = 400kHz SCL = SDA = 0kHz				10 1	µA µA
$V_{DVCC,UVLO}$	DV_{CC} UVLO				1.0		V
V_{IH}	Input High Voltage				50	70	$\%DV_{CC}$
V_{IL}	Input Low Voltage			30	50		$\%DV_{CC}$
I_{IH}	Input High Leakage Current	SDA = SCL = DV_{CC} = 5.5V		–1		1	µA
I_{IL}	Input Low Leakage Current	SDA = SCL = 0V, DV_{CC} = 5.5V		–1		1	µA
V_{OL}	SDA Output Low Voltage	I_{SDA} = 3mA				0.4	V
Timing Characteristics (Note 8) (All Values Are Referenced to V_{IH} and V_{IL})							
f_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	Low Period of the SCL Clock			1.3			µs
t_{HIGH}	High Period of the SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Set-Up Time for a Repeated Start Condition			0.6			µs
$t_{SU,STO}$	Stop Condition Set-Up Time			0.6			µs
$t_{HD,DATO}$	Output Data Hold Time			0		900	ns
$t_{HD,DATI}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Set-Up Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns

ELECTRICAL CHARACTERISTICS

Step-Down Switching Regulators. The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{OUT} = V_{IN12} = V_{IN3} = 3.8V, all regulators enabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Down Switching Regulators (Buck1, Buck2 and Buck3)							
V_{IN12}, V_{IN3}	Input Supply Voltage	(Note 9)	●	2.7		5.5	V
V_{OUT} UVLO	V_{OUT} Falling V_{OUT} Rising	V_{IN12} and V_{IN3} Connected to V_{OUT} Through Low Impedance. Switching Regulators Are Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
f_{OSC}	Oscillator Frequency			1.91	2.25	2.59	MHz
800mA Step-Down Switching Regulator 3 (Buck3-Enabled via EN3, Disabled in PDN and POFF States)							
I_{VIN3Q}	Pulse-Skipping Mode Input Current	(Note 10)			100		µA
	Burst Mode Operation Input Current	(Note 10)			20	35	µA
	Shutdown Input Current	EN3 = 0			0.01	1	µA
I_{LIM3}	Peak P-Channel MOSFET Current Limit	(Note 7)		1000	1400	1700	mA
V_{FB3}	Feedback Voltage	Pulse-Skipping Mode Burst Mode Operation	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB3}	FB3 Input Current	(Note 10)		–0.05		0.05	µA
D3	Max Duty Cycle	FB3 = 0V		100			%
R_{P3}	$R_{DS(ON)}$ of P-Channel MOSFET				0.3		Ω
R_{N3}	$R_{DS(ON)}$ of N-Channel MOSFET				0.4		Ω
R_{SW3_PD}	SW3 Pull-Down in Shutdown	EN3 = 0			10		kΩ
$V_{IL,EN3}$	EN3 Input Low Voltage					0.4	V
$V_{IH,EN3}$	EN3 Input High Voltage			1.2			V
500mA Step-Down Switching Regulator 2 (Buck2-Pushbutton Enabled, Third in Sequence)							
I_{VIN12Q}	Pulse-Skipping Mode Input Current	(Note 10)			100		µA
	Burst Mode Operation Input Current	(Note 10)			20		µA
	Shutdown Input Current	POFF State			0.01	1	µA
I_{LIM2}	Peak P-Channel MOSFET Current Limit	(Note 7)		650	900	1200	mA
V_{FB2}	Feedback Voltage	Pulse-Skipping Mode Burst Mode Operation	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB2}	FB2 Input Current	(Note 10)		–0.05		0.05	µA
D2	Max Duty Cycle	FB2 = 0V		100			%
R_{P2}	$R_{DS(ON)}$ of P-Channel MOSFET	I_{SW2} = 100mA			0.6		Ω
R_{N2}	$R_{DS(ON)}$ of N-Channel MOSFET	I_{SW2} = –100mA			0.6		Ω
R_{SW2_PD}	SW2 Pull-Down in Shutdown	POFF State			10		kΩ
500mA Step-Down Switching Regulator 1 (Buck1-Pushbutton Enabled, Second in Sequence)							
I_{VIN12Q}	Pulse-Skipping Mode Input Current	(Note 10)			100		µA
	Burst Mode Operation Input Current	(Note 10)			20		µA
	Shutdown Input Current				0.01	1	µA
I_{LIM1}	Peak P-Channel MOSFET Current Limit	(Note 7)		650	900	1200	mA
V_{FB1}	Feedback Voltage	Pulse-Skipping Mode Burst Mode Operation	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB1}	FB1 Input Current	(Note 10)		–0.05		0.05	µA
D1	Max Duty Cycle	FB1 = 0V		100			%
R_{P1}	$R_{DS(ON)}$ of P-Channel MOSFET	I_{SW1} = 100mA			0.6		Ω
R_{N1}	$R_{DS(ON)}$ of N-Channel MOSFET	I_{SW1} = –100mA			0.6		Ω
R_{SW1_PD}	SW1 Pull-Down in Shutdown	POFF State			10		kΩ

ELECTRICAL CHARACTERISTICS

LDO Regulators. The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{INLDO1} = V_{INLDO2} = V_{OUT} = 3.8V, LDO1 and LDO2 enabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator 1 (LDO1-Always On)							
V_{INLDO1}	Input Voltage Range	$V_{INLDO1} \le V_{OUT}$ + 0.3V	●	1.65		5.5	V
V_{OUT_UVLO}	V_{OUT} Falling V_{OUT} Rising	LDO1 Is Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
V_{LDO1_FB}	LDO1_FB Regulated Feedback Voltage	I_{LDO1} = 1mA	●	0.78	0.8	0.82	V
	LDO1_FB Line Regulation (Note 11)	I_{LDO1} = 1mA, V_{IN} = 1.65V to 5.5V			0.4		mV/V
	LDO1_FB Load Regulation (Note 11)	I_{LDO1} = 1mA to 150mA			5		µV/mA
I_{LDO1_OC}	Available Output Current		●	150			mA
I_{LDO1_SC}	Short-Circuit Output Current (Note 7)				270		mA
V_{DROP1}	Dropout Voltage (Note 12)	I_{LDO1} = 150mA, V_{INLDO1} = 3.6V I_{LDO1} = 150mA, V_{INLDO1} = 2.5V I_{LDO1} = 75mA, V_{INLDO1} = 1.8V			160 200 170	260 320 280	mV mV mV
R_{LDO1_PD}	Output Pull-Down Resistance in Shutdown	LDO1 Disabled			10		kΩ
I_{LDO_FB1}	LDO_FB1 Input Current			–50		50	nA
LDO Regulator 2 (LDO2-Pushbutton Enabled, First in Sequence)							
V_{INLDO2}	Input Voltage Range	$V_{INLDO2} \le V_{OUT}$ + 0.3V	●	1.65		5.5	V
V_{OUT_UVLO}	V_{OUT} Falling V_{OUT} Rising	LDO2 is Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
V_{LDO2_FB}	LDO2_FB Regulated Output Voltage	I_{LDO2} = 1mA	●	0.78	0.8	0.82	V
	LDO2_FB Line Regulation (Note 11)	I_{LDO2} = 1mA, V_{IN} = 1.65V to 5.5V			0.4		mV/V
	LDO2_FB Load Regulation (Note 11)	I_{LDO2} = 1mA to 150mA			5		µV/mA
I_{LDO2_OC}	Available Output Current		●	150			mA
I_{LDO2_SC}	Short-Circuit Output Current (Note 7)				270		mA
V_{DROP2}	Dropout Voltage (Note 12)	I_{LDO2} = 150mA, V_{INLDO2} = 3.6V I_{LDO2} = 150mA, V_{INLDO2} = 2.5V I_{LDO1} = 75mA, V_{INLDO1} = 1.8V			160 200 170	260 320 280	mV mV mV
R_{LDO2_PD}	Output Pull-Down Resistance in Shutdown	LDO2 Disabled			14		kΩ
I_{LDO_FB2}	LDO_FB2 Input Current			–50		50	nA

ELECTRICAL CHARACTERISTICS

Pushbutton Controller. The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{OUT} = 3.8V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Pushbutton Pin ($\overline{ON}$)							
V_{OUT}	Pushbutton Operating Supply Range	(Note 9)	●	2.7		5.5	V
V_{OUT} UVLO	V_{OUT} Falling V_{OUT} Rising	Pushbutton is Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	2.9	V V
$V_{\overline{ON}\_TH}$	$\overline{ON}$ Threshold Rising $\overline{ON}$ Threshold Falling			0.4	0.8 0.7	1.2	V V
$I_{\overline{ON}}$	$\overline{ON}$ Input Current	$V_{\overline{ON}} = V_{OUT}$ $V_{\overline{ON}} = 0V$		–1 –4	–9	1 –14	µA µA
Power-On Input Pin (PWR_ON)							
V_{PWR_ON}	PWR_ON Threshold Rising PWR_ON Threshold Falling			0.4	0.8 0.7	1.2	V V
I_{PWR_ON}	PWR_ON Input Current	V_{PWR_ON} = 3V		–1		1	µA
Status Output Pins (PBSTAT, $\overline{EXTPWR}$, PGOOD)							
I_{PBSTAT}	PBSTAT Output High Leakage Current	V_{PBSTAT} = 3V		–1		1	µA
V_{PBSTAT}	PBSTAT Output Low Voltage	I_{PBSTAT} = 3mA			0.1	0.4	V
$I_{\overline{EXTPWR}}$	$\overline{EXTPWR}$ Pin Input Current	$V_{\overline{EXTPWR}}$ = 3V			0	1	µA
$V_{\overline{EXTPWR}}$	$\overline{EXTPWR}$ Pin Output Low Voltage	$I_{\overline{EXTPWR}}$ = 2mA			0.15	0.4	V
I_{PGOOD}	PGOOD Output High Leakage Current	V_{PGOOD} = 3V		–1		1	µA
V_{PGOOD}	PGOOD Output Low Voltage	I_{PGOOD} = 3mA			0.1	0.4	V
$V_{THPGOOD}$	PGOOD Threshold Voltage	(Note 13)			–8		%
Pushbutton Timing Parameters							
$t_{\overline{ON}\_PBSTAT1}$	$\overline{ON}$ Low Time to PBSTAT Low				50		ms
$t_{\overline{ON}\_PBSTAT2}$	$\overline{ON}$ High to PBSTAT High	PBSTAT Low > t_{PBSTAT_PW}			900		µs
t_{PBSTAT_PW}	PBSTAT Minimum Pulse Width			40	50		ms
$t_{\overline{ON}\_PUP}$	$\overline{ON}$ Low Time for Power-Up				50		ms
$t_{\overline{ON}\_RST}$	$\overline{ON}$ Low to PGOOD Reset Low			12	14	16.5	Seconds
$t_{\overline{ON}\_RST\_PW}$	PGOOD Reset Low Pulse Width				1.8		ms
t_{PUP_PDN}	Minimum Time from Power Up to Down				1		Seconds
t_{PDN_PUP}	Minimum Time from Power Down to Up				1		Seconds
t_{PWR_ONH}	PWR_ON High to Power-Up				50		ms
t_{PWR_ONL}	PWR_ON Low to Power-Down				50		ms
t_{PWR_ONBK1}	PWR_ON Power-Up Blanking	PWR_ON Low Recognized from Power-Up			1		Seconds
t_{PWR_ONBK2}	PWR_ON Power-Down Blanking	PWR_ON High Recognized from Power-Down			1		Seconds
t_{PGOODH}	From Regulation to PGOOD High	Buck1, 2 and LDO1 Within PGOOD Threshold			230		ms
t_{PGOODL}	Bucks Disabled to PGOOD Low	Bucks Disabled			44		µs
t_{LDO2_BK1}	LDO2 Enable to Buck Enable			12.5	14.5	17.5	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3677-3 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: This IC includes over temperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

ELECTRICAL CHARACTERISTICS

Note 4: V_{CC} is the greater of V_{BUS}, V_{OUT} or BAT.

Note 5: Total input current is the sum of quiescent current, I_{BUSQ}, and measured current given by $V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$.

Note 6: $h_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

Note 7: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation or failure.

Note 8: The serial port is tested at rated operating frequency. Timing parameters are tested and/or guaranteed by design.

Note 9: V_{OUT} not in UVLO.

Note 10: Buck FB high, not switching.

Note 11: Measured with the LDO running unity gain with output tied to feedback pin.

Note 12: Dropout voltage is the minimum input to output voltage differential needed for an LDO to maintain regulation at a specified output current. When an LDO is in dropout, its output voltage will be equal to $V_{IN} - V_{DROP}$.

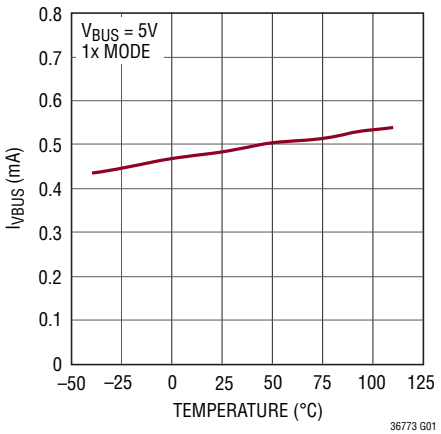
Note 13: PGOOD threshold is expressed as a percentage difference from the Buck1, Buck2 and LDO1 regulation voltages. The threshold is measured from Buck1, Buck2 and LDO1 output rising.

Note 14: The I_{BATQ} specifications represent the total battery load assuming V_{INLDO1}, V_{INLDO2}, V_{IN12} and V_{IN3} are tied directly to V_{OUT}.

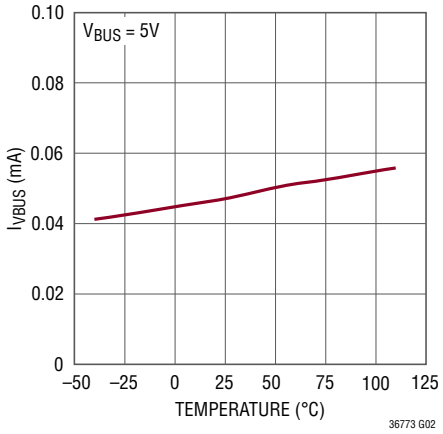
Note 15: Long-term current density rating for the part.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified

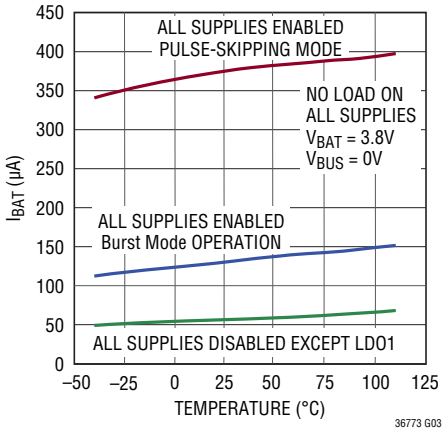
Input Supply Current vs Temperature



Input Supply Current vs Temperature (Suspend Mode)

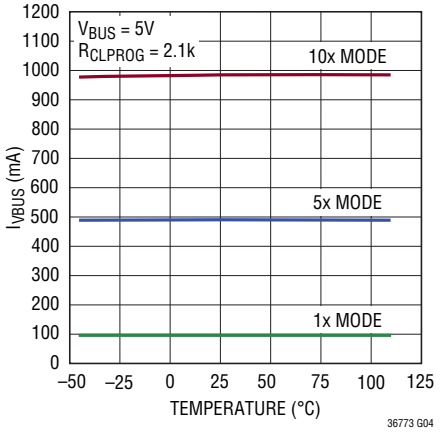


Battery-Drain Current vs Temperature

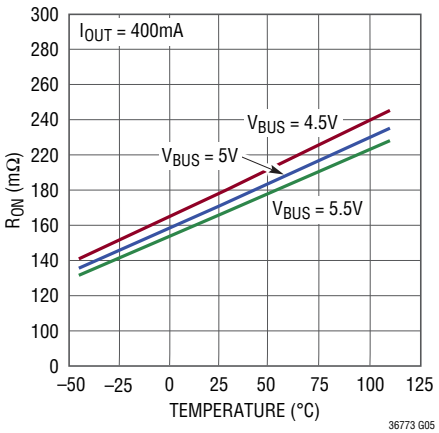


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified

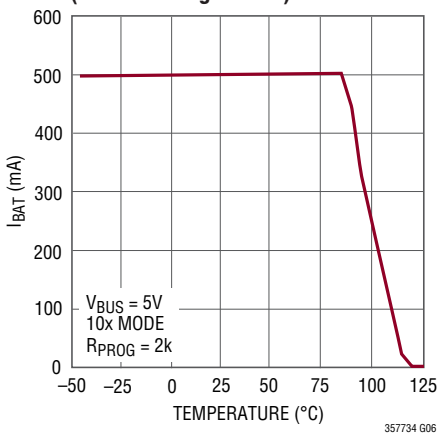
Input Current Limit vs Temperature



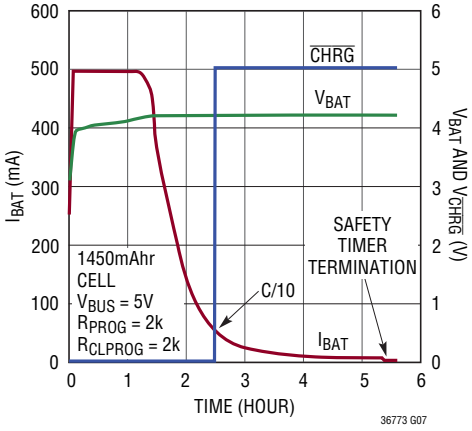
Input R_{ON} vs Temperature



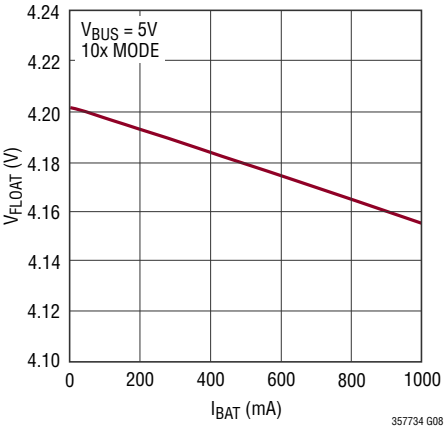
Charge Current vs Temperature (Thermal Regulation)



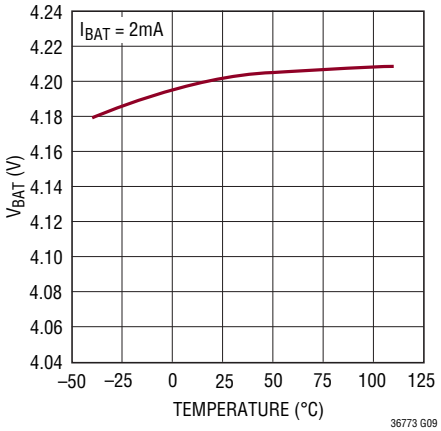
Battery Current and Voltage vs Time



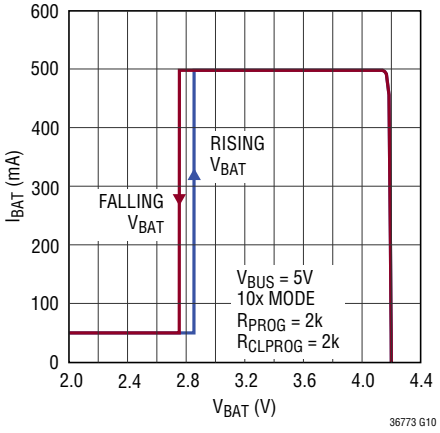
Battery Float Voltage Load Regulation



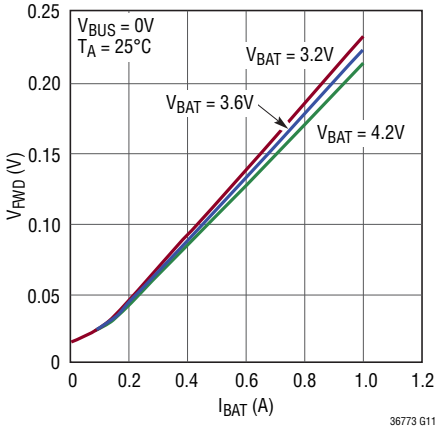
Battery Regulation (Float) Voltage vs Temperature



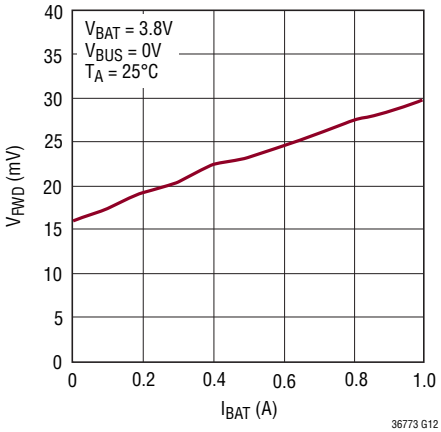
I_{BAT} vs V_{BAT}



Forward Voltage vs Ideal Diode Current (No External FET)

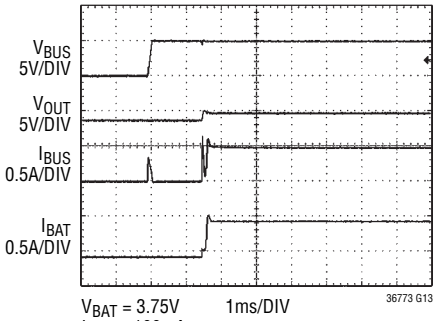


Forward Voltage vs Ideal Diode Current (with Si2333DS External FET)



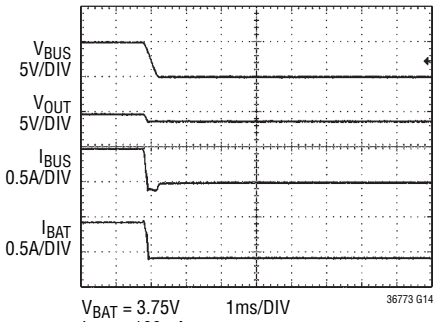
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified

Input Connect Waveform



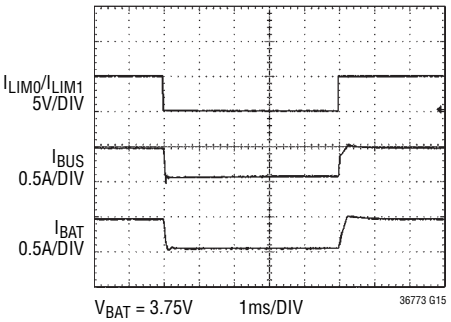
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Input Disconnect Waveform



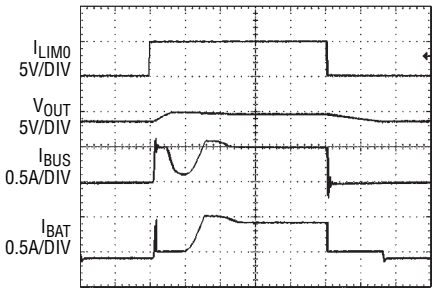
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Switching from 1x to 5x Mode



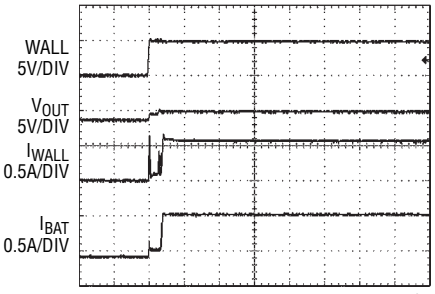
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 50mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Switching from Suspend Mode to 5x Mode



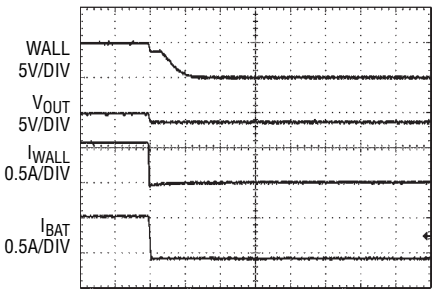
V_{BAT} = 3.75V 100µs/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k
I_{LIM1} = 5V

WALL Connect Waveform



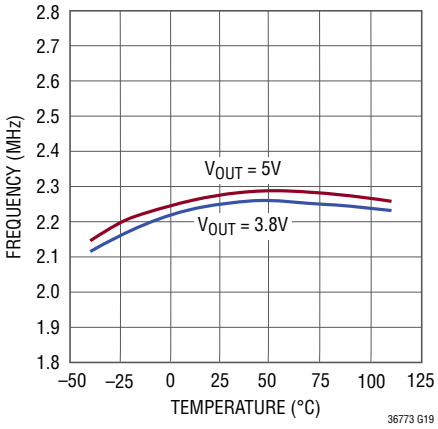
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 2k

WALL Disconnect Waveform

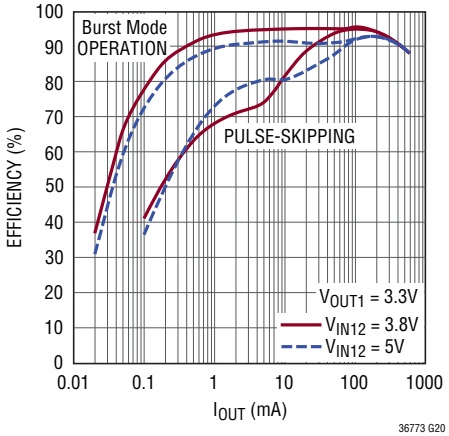


V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 2k

Oscillator Frequency vs Temperature

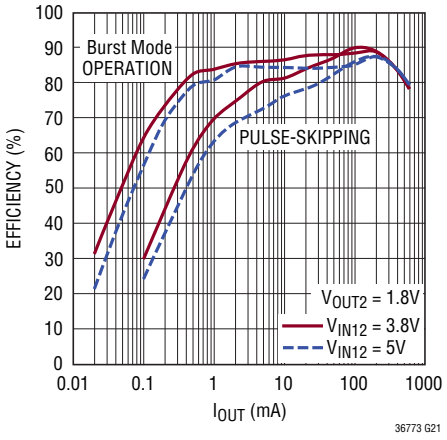


Step-Down Switching Regulator 1 3.3V Output Efficiency vs I_{OUT1}

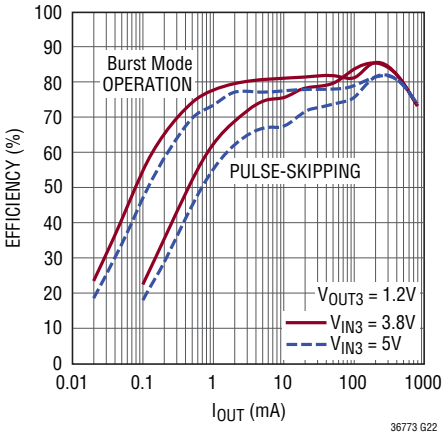


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified

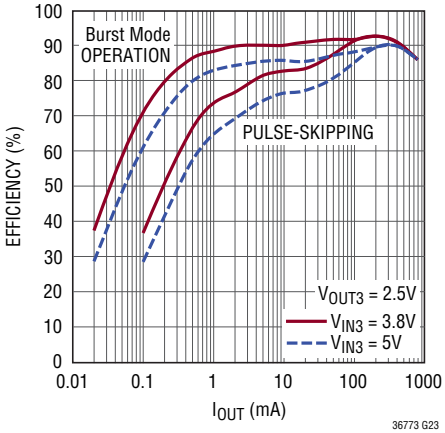
Step-Down Switching Regulator 2 1.8V Output Efficiency vs I_{OUT2}



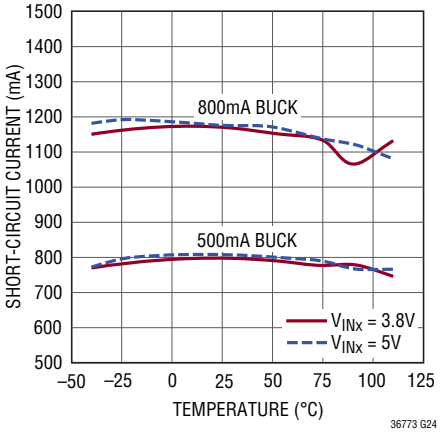
Step-Down Switching Regulator 3 1.2V Output Efficiency vs I_{OUT3}



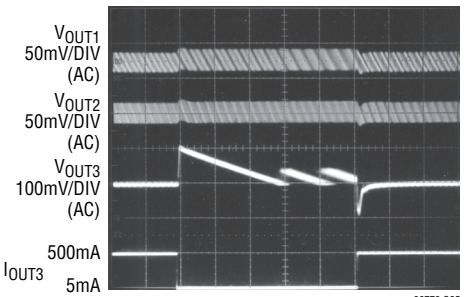
Step-Down Switching Regulator 3 2.5V Output Efficiency



Step-Down Switching Regulator Short-Circuit Current vs Temperature

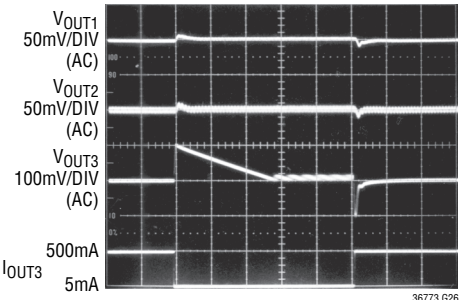


Step-Down Switching Regulator Output Transient (Burst Mode Operation)



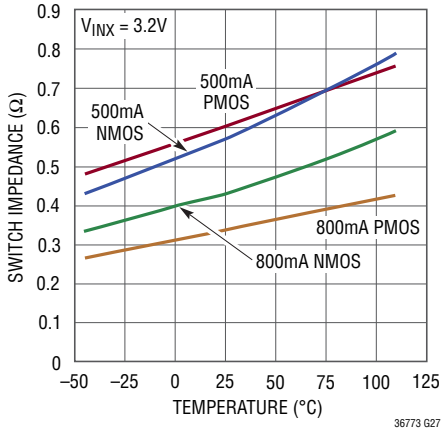
V_{OUT1} = 3.3V 50µs/DIV
I_{OUT1} = 10mA
V_{OUT2} = 1.8V
I_{OUT2} = 20mA
V_{OUT3} = 1.2V
V_{OUT} = V_{BAT} = 3.8V

Step-Down Switching Regulator Output Transient (Pulse-Skipping)

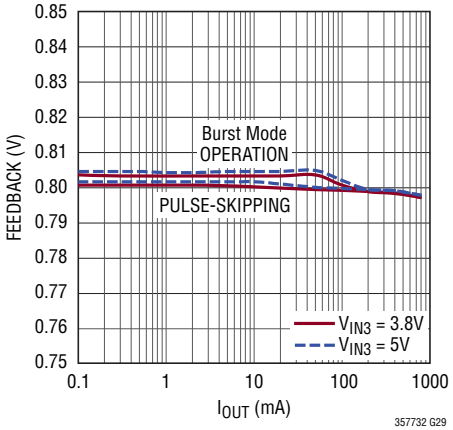


V_{OUT1} = 3.3V 50µs/DIV
I_{OUT1} = 30mA
V_{OUT2} = 1.8V
I_{OUT2} = 20mA
V_{OUT3} = 1.2V
V_{OUT} = V_{BAT} = 3.8V

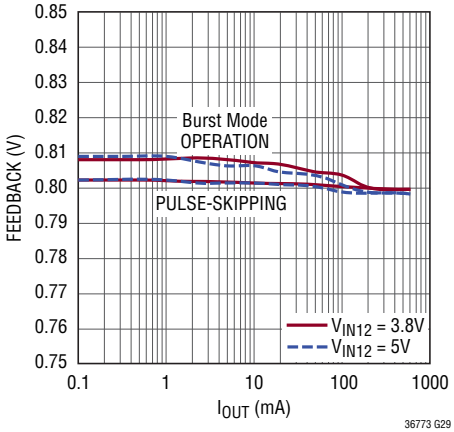
Step-Down Switching Regulator Switch Impedance vs Temperature



800mA Step-Down Switching Regulator Feedback Voltage vs Output Current

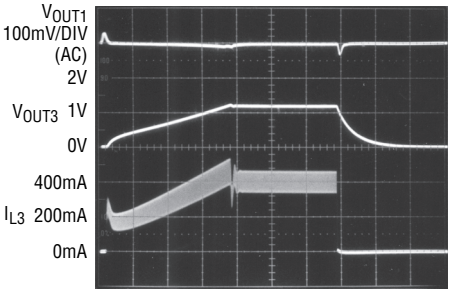


500mA Step-Down Switching Regulator Feedback Voltage vs Output Current



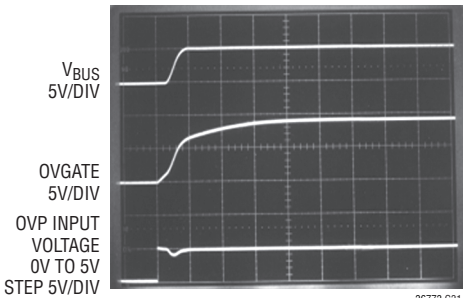
TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified

Step-Down Switching Regulator 3 Soft-Start and Shutdown



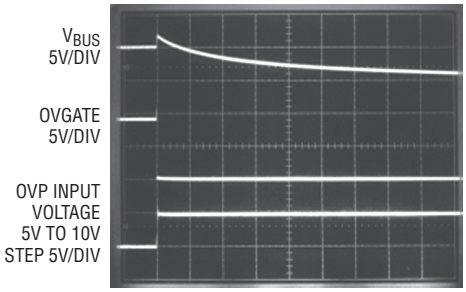
V_{OUT1} = 1.8V
I_{OUT1} = 100mA
R_{OUT3} = 3Ω
50µs/DIV

OVP Connection Waveform



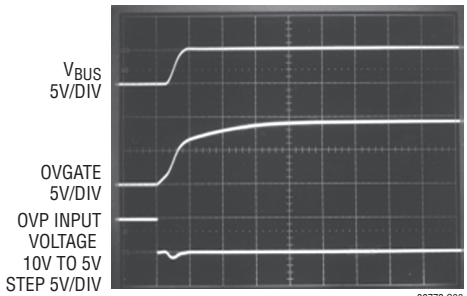
500µs/DIV

OVP Protection Waveform



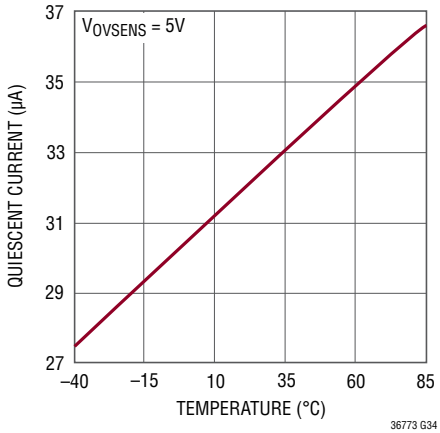
500µs/DIV

OVP Reconnection Waveform

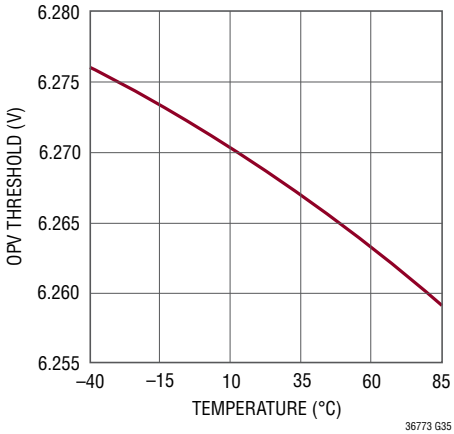


500µs/DIV

OVSENS Quiescent Current vs Temperature

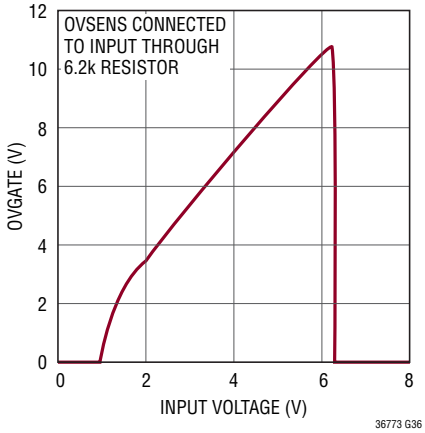


Rising Overvoltage Threshold vs Temperature

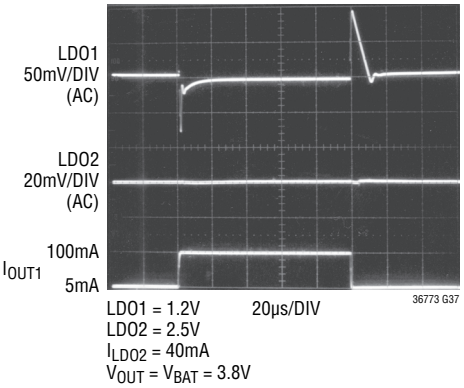


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C unless otherwise specified

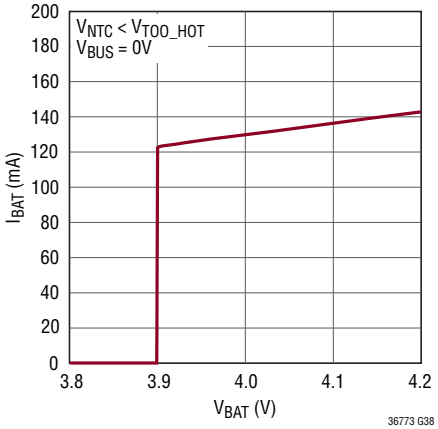
OVGATE vs OVSENS



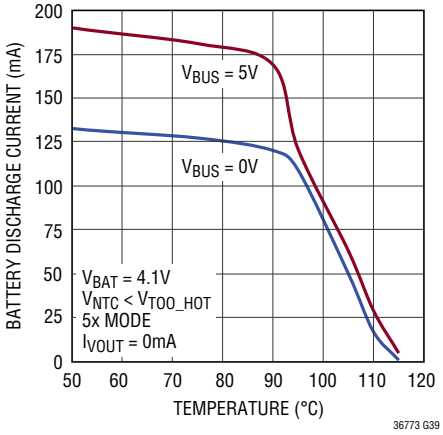
LDO Load Step



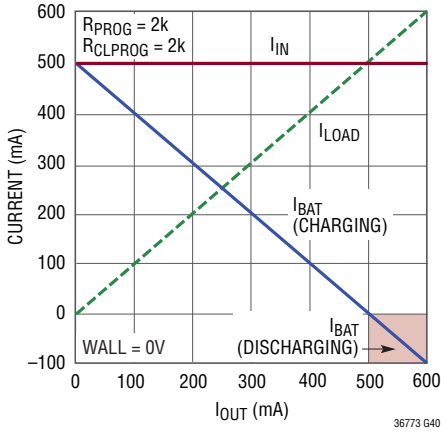
Too Hot BAT Discharge



Battery Discharge vs Temperature



Input and Battery Current vs Output Current



PIN FUNCTIONS

I_{LIM0}, I_{LIM1} (Pins 1, 2): Input Current Control Pins. I_{LIM0} and I_{LIM1} control the input current limit. See Table 1 in the USB PowerPath Controller section. Both pins are pulled low by a weak current sink.

NC (Pins 3, 9, 18, 19, 20, 22): No Connect. This pin has no function and may be floated or connected to ground.

WALL (Pin 4): Wall Adapter Present Input. Pulling this pin above 4.3V will disconnect the power path from V_{BUS} to V_{OUT}. The $\overline{ACPR}$ pin will also be pulled low to indicate that a wall adapter has been detected.

SW3 (Pin 5): Power Transmission (Switch) Pin for Step-Down Switching Regulator 3 (Buck3).

V_{IN3} (Pin 6): Power Input for Step-Down Switching Regulator 3. This pin should be connected to V_{OUT}.

FB3 (Pin 7): Feedback Input for Step-Down Switching Regulator 3 (Buck3). This pin servos to a fixed voltage of 0.8V when the control loop is complete.

OVSENSE (Pin 8): Overvoltage Protection Sense Input. OVSENSE should be connected through a 6.2k resistor to the input power connector and the drain of an external

PIN FUNCTIONS

N-channel MOSFET pass transistor. When the voltage on this pin exceeds a preset level, the OVGATE pin will be pulled to GND to disable the pass transistor and protect downstream circuitry.

DV_{CC} (Pin 10): Supply Voltage for I^2C Lines. This pin sets the logic reference level of the LTC3677-3. A UVLO circuit on the DV_{CC} pin forces all registers to all 0s whenever DV_{CC} is <1V. Bypass to GND with a 0.1µF capacitor.

SDA (Pin 11): I^2C Data Input. Serial data is shifted one bit per clock to control the LTC3677-3. The logic level for SDA is referenced to DV_{CC}.

SCL (Pin 12): I^2C Clock Input. The logic level for SCL is referenced to DV_{CC}.

OVGATE (Pin 13): Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOSFET pass transistor. The source of the transistor should be connected to V_{BUS} and the drain should be connected to the product's DC input connector. In the absence of an overvoltage condition, this pin is connected to an internal charge pump capable of creating sufficient overdrive to fully enhance this transistor. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage. OVGATE works in conjunction with OVSENSE to provide this protection.

PWR_ON (Pin 14): Logic Input Used to Keep Buck1, Buck2 and LDO2 Enabled After Power-Up. May also be used to enable regulators directly (sequence = LDO2 → Buck1 → Buck2). See the Pushbutton Interface Operation section for more information.

$\overline{ON}$ (Pin 15): Pushbutton Input. A weak internal pull-up forces $\overline{ON}$ high when left floating. A normally open push-button is connected from $\overline{ON}$ to ground to force a low state on this pin.

PBSTAT (Pin 16): Open-drain output is a debounced and buffered version of $\overline{ON}$ to be used for processor interrupts.

EN3 (Pin 17): Enable Pin for Step-Down Switching Regulator 3 (Buck3).

PGOOD (Pin 21): Open-Drain Output. PGOOD indicates that Buck1, Buck2 and LDO1 are within 8% of final regulation value. There is a 230ms delay from all regulators reaching regulation and PGOOD going high.

LDO1_FB (Pin 23): Feedback Voltage Input for Low Dropout Linear Regulator 1 (LDO1). LDO1 output voltage is set using an external resistor divider between LDO1 and LDO1_FB.

LDO2_FB (Pin 24): Feedback Voltage Input for Low Dropout Linear Regulator 2 (LDO2). LDO2 output voltage is set using an external resistor divider between LDO2 and LDO2_FB.

FB2 (Pin 25): Feedback Input for Step-Down Switching Regulator 2 (Buck2). This pin servos to a fixed voltage of 0.8V when the control loop is complete.

FB1 (Pin 26): Feedback Input for Step-Down Switching Regulator 1 (Buck1). This pin servos to a fixed voltage of 0.8V when the control loop is complete.

V_{INLDO1} (Pin 27): Input Supply of Low Dropout Linear Regulator 1 (LDO1). This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO1 (Pin 28): Output of Low Dropout Linear Regulator 1. LDO1 is an always-on LDO and will be enabled whenever the part is not in V_{OUT} UVLO. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO2 (Pin 29): Output of Low Dropout Linear Regulator 2. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{INLDO2} (Pin 30): Input Supply of Low Dropout Linear Regulator 2 (LDO2). This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

SW2 (Pin 31): Power Transmission (Switch) Pin for Step-Down Switching Regulator 2 (Buck2).

V_{IN12} (Pin 32): Power Input for Step-Down Switching Regulators 1 and 2. This pin will generally be connected to V_{OUT}.

SW1 (Pin 33): Power Transmission (Switch) Pin for Step-Down Switching Regulator 1 (Buck1).

NTCBIAS (Pin 34): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

PIN FUNCTIONS

NTC (Pin 35): The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it drops back into range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground.

PROG (Pin 36): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current:

$$I_{CHG} = \frac{1000V}{R_{PROG}} (A)$$

If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current.

IDGATE (Pin 37): Ideal Diode Gate Connection. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. It is important to maintain high impedance on this pin and minimize all leakage paths.

BAT (Pin 38): Single-Cell Li-Ion Battery Pin. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger.

V_{OUT} (Pin 39): Output Voltage of the PowerPath Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3677-3 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted input current from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor.

V_{BUS} (Pin 40): USB Input Voltage. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

$\overline{ACPR}$ (Pin 41): Wall Adapter Present Output (Active Low). A low on this pin indicates that the wall adapter input comparator has had its input pulled above its input threshold (typically 4.3V). This pin can be used to drive the gate of an external P-channel MOSFET to provide power to V_{OUT} from a power source other than a USB port.

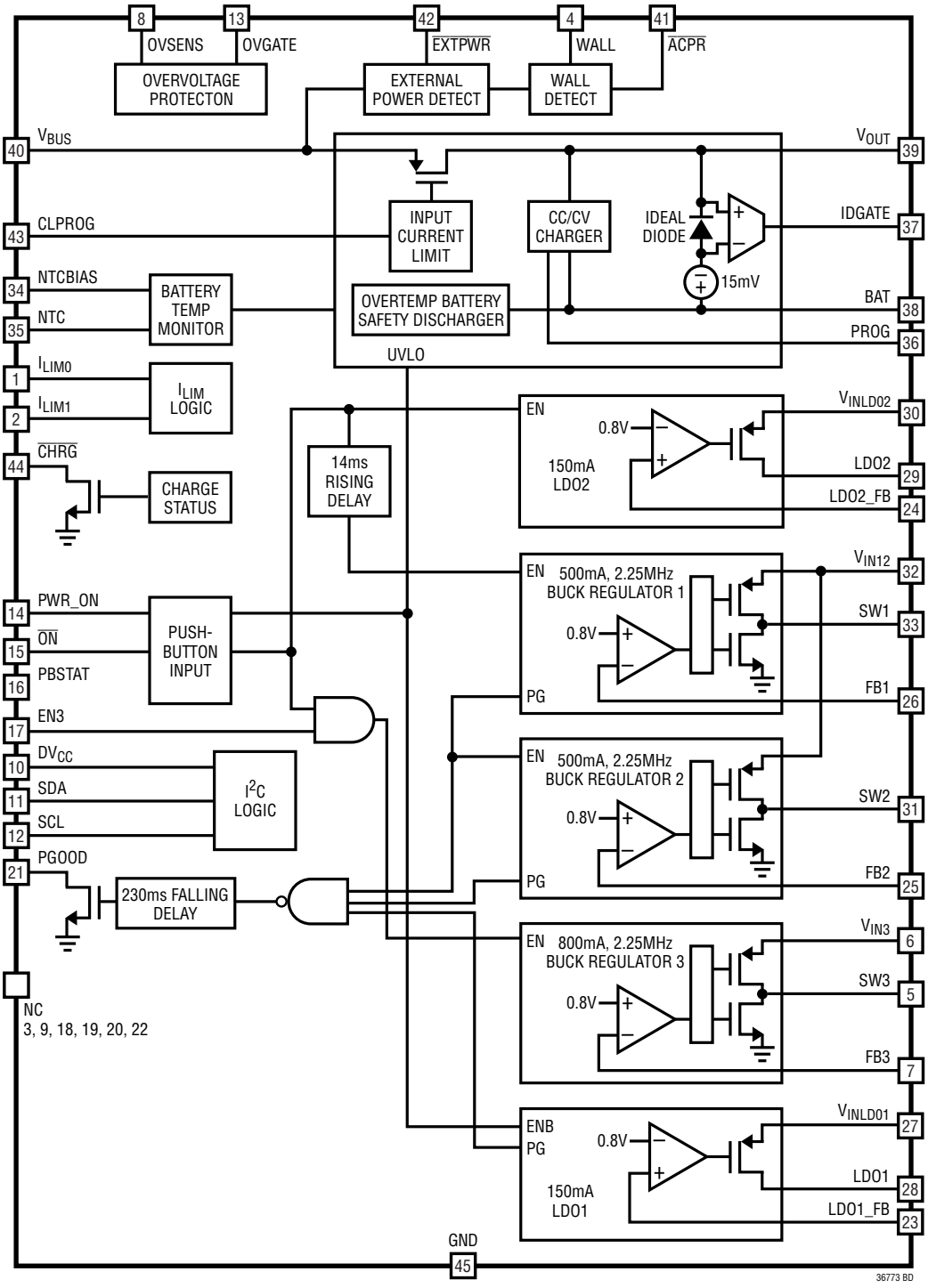
$\overline{EXTPWR}$ (Pin 42): External Power Present Output (Active Low, Open-Drain Output). A low on this pin indicates that external power is present at either the V_{BUS} or WALL input. For $\overline{EXTPWR}$ to signal V_{BUS} present, V_{BUS} must exceed the V_{BUS} undervoltage lockout threshold. For $\overline{EXTPWR}$ to signal WALL present, WALL must exceed the absolute and differential WALL input thresholds. The $\overline{EXTPWR}$ signal is independent of the I_{LIM1} and I_{LIM0} pins. Thus, it is possible to have the input current limit circuitry in suspend with $\overline{EXTPWR}$ showing a valid charging level on V_{BUS}.

CLPROG (Pin 43): Input Current Program and Input Current Monitor Pin. A resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin (i.e., the input current limit). A precise fraction of the input current, h_{CLPROG}, is sent to the CLPROG pin. The input PowerPath delivers current until the CLPROG pin reaches 2V (10x mode), 1V (5x mode) or 0.2V (1x mode). Therefore, the current drawn from V_{BUS} will be limited to an amount given by h_{CLPROG} and R_{CLPROG}. In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

$\overline{CHRG}$ (Pin 44): Open-Drain Charge Status Output. The $\overline{CHRG}$ pin indicates the status of the battery charger. If $\overline{CHRG}$ is high then the charger is near the float voltage (charge current less than 1/10th programmed charge current) or charging is complete and charger is disabled. A low on $\overline{CHRG}$ indicates that the charger is enabled. For more information see the Charge Status Indication section.

GND (Exposed Pad Pin 45): The exposed package pad is ground and must be soldered to PCB ground for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

PowerPath OPERATION

Introduction

The LTC3677-3 is highly integrated power management IC that includes the following features:

– PowerPath controller
– Battery charger
– Ideal diode
– Input overvoltage protection
– Pushbutton controller
– Three step-down switching regulators
– Two low dropout linear regulators

Designed specifically for USB applications, the PowerPath controller incorporates a precision input current limit which communicates with the battery charger to ensure that input current does not violate the USB average input current specification. The ideal diode from BAT to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}. The LTC3677-3 also has the ability to receive power from a wall adapter or other non-current-limited power source. Such a power supply can be connected to the V_{OUT} pin of the LTC3677-3 through an external device such as a power Schottky or FET, as shown in Figure 1. The LTC3677-3 has the unique ability to use the output, which is powered by an external supply, to charge the battery while providing power to the load. A comparator on the WALL pin is configured to detect the presence of the wall adapter and shut off the connection to the USB. This prevents reverse conduction from V_{OUT} to V_{BUS} when a wall adapter is present.

The LTC3677-3 also includes a pushbutton input to control the power sequencing of two synchronous step-down switching regulators (Buck1 and Buck2), a low dropout regulator (LDO2) and system reset. The three 2.25MHz constant-frequency current mode step-down switching regulators provide 500mA, 500mA and 800mA each and

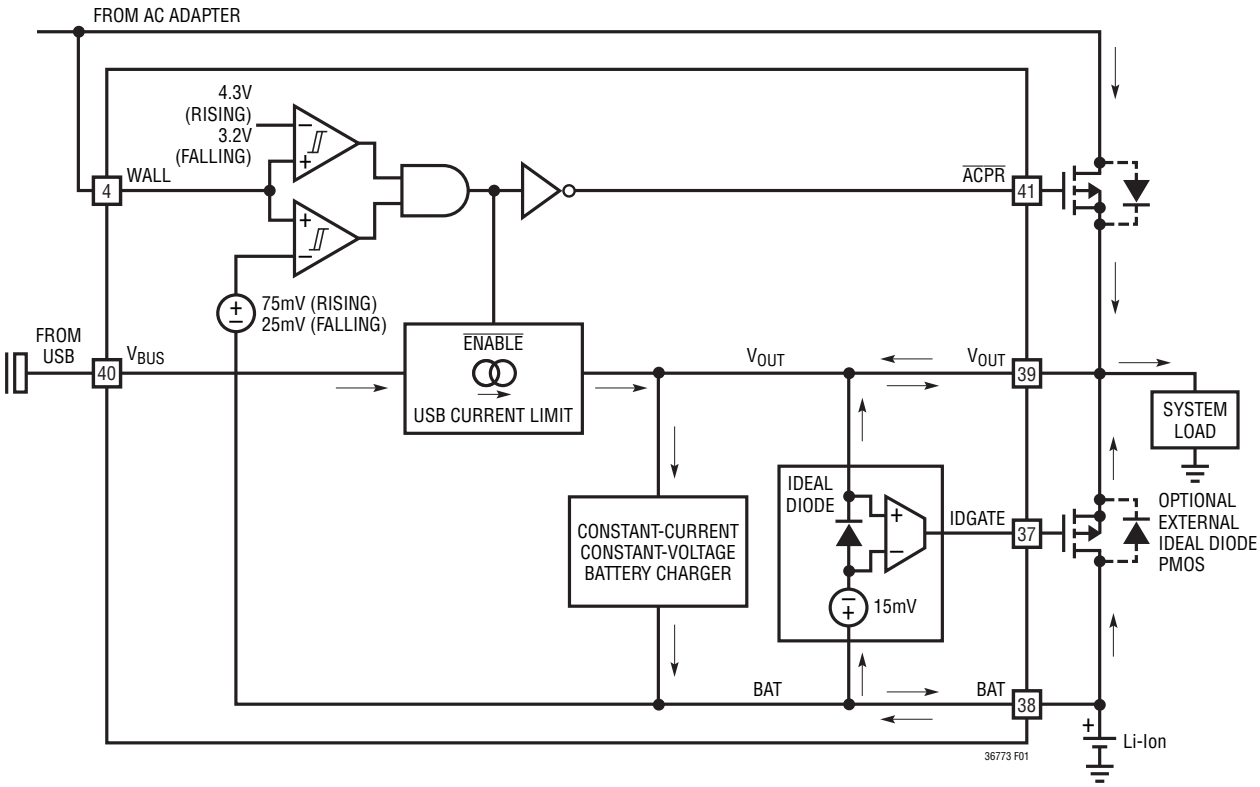


Figure 1. Simplified PowerPath Block Diagram

OPERATION

support 100% duty cycle operation as well as operating in Burst Mode operation for high efficiency at light load. No external compensation components are required for the switching regulators. The two low dropout regulators can output up to 150mA.

All regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry.

USB PowerPath Controller

The input current limit and charge control circuits of the LTC3677-3 is designed to limit input current as well as control battery charge current as a function of I_{VOUT}. V_{OUT} drives the combination of the external load, the three step-down switching regulators, two LDOs and the battery charger.

If the combined load does not exceed the programmed input current limit, V_{OUT} will be connected to V_{BUS} through an internal 200mΩ P-channel MOSFET. If the combined load at V_{OUT} exceeds the programmed input current limit, the battery charger will reduce its charge current by the amount necessary to enable the external load to be satisfied while maintaining the programmed input current. Even if the battery charge current is set to exceed the allowable USB current, the average input current USB specification will not be violated. Furthermore, load current at V_{OUT} will always be prioritized and only excess available current will be used to charge the battery. The current out of the CLPROG pin is a fraction ($1/h_{CLPROG}$) of the V_{BUS} current. When a programming resistor is connected from CLPROG to GND, the voltage on CLPROG represents the input current:

$$I_{VBUS} = I_{BUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet h_{CLPROG}$$

where I_{BUSQ} and h_{CLPROG} are given in the Electrical Characteristics table.

The input current limit is programmed by the I_{LIM0} and I_{LIM1} pins. The LTC3677-3 can be configured to limit input current to one of several possible settings as well as be deactivated (USB suspend). The input current limit will be set by the appropriate servo voltage and the resistor on CLPROG according to the following expression:

$$I_{VBUS} = I_{BUSQ} + \frac{0.2V}{R_{CLPROG}} \bullet h_{CLPROG} \left(1x\ Mode\right)$$

$$I_{VBUS} = I_{BUSQ} + \frac{1V}{R_{CLPROG}} \bullet h_{CLPROG} \left(5x\ Mode\right)$$

$$I_{VBUS} = I_{BUSQ} + \frac{2V}{R_{CLPROG}} \bullet h_{CLPROG} \left(10x\ Mode\right)$$

Under worst-case conditions, the USB specification for average input current will not be violated with an R_{CLPROG} resistor of 2.1k or greater. Table 1 shows the available settings for the I_{LIM0} and I_{LIM1} pins:

Table 1. Controlled Input Current Limit

I_{LIM1}	I_{LIM0}	$I_{BUS(LIM)}$
1	1	100mA (1x)
1	0	1A (10x)
0	1	Suspend
0	0	500mA (5x)

Notice that when I_{LIM0} is low and I_{LIM1} is high, the input current limit is set to a higher current limit for increased charging and current availability at V_{OUT}. This mode is typically used when there is a higher power, non-USB source available at the V_{BUS} pin.

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Ideal Diode from BAT to V_{OUT}

The LTC3677-3 has an internal ideal diode as well as a controller for an optional external ideal diode. Both the internal and the external ideal diodes respond quickly whenever V_{OUT} drops below BAT. If the load increases beyond the input current limit, additional current will be pulled from the battery via the ideal diodes. Furthermore, if power to V_{BUS} (USB) or V_{OUT} (external wall power or high voltage regulator) is removed, then all of the application power will be provided by the battery via the ideal diodes. The ideal diodes are fast enough to keep V_{OUT} from dropping significantly below V_{BAT} with just the recommended output capacitor (see Figure 2). The ideal diode consists of a precision amplifier that enables an on-chip P-channel MOSFET whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 200mΩ. If this is sufficient for the application, then no external components are necessary. However, if lower resistance is needed, an external P-channel MOSFET can be added from BAT to V_{OUT}. The IDGATE pin of the LTC3677-3 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET having extremely low on-resistance.

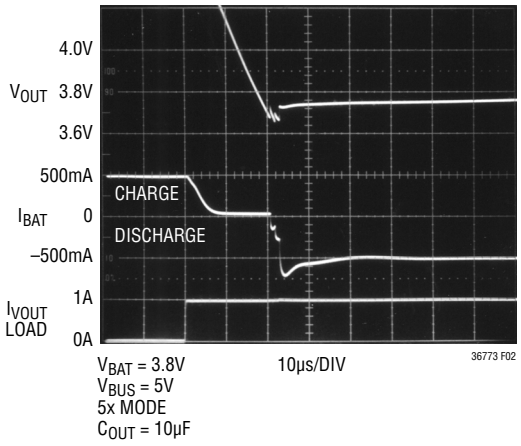

Figure 2. Ideal Diode Transient Response

Using the WALL Pin to Detect the Presence of an External Power Source

The WALL input pin can be used to identify the presence of an external power source (particularly one that is not subject to a fixed current limit like the USB V_{BUS} input). Typically, such a power supply would be a 5V wall adapter output or the low voltage output of a high voltage buck regulator. When the wall adapter output (or buck regulator output) is connected directly to the WALL pin, and the voltage exceeds the WALL pin threshold, the USB power path (from V_{BUS} to V_{OUT}) will be disconnected. Furthermore, the $\overline{ACPR}$ pin will be pulled low. In order for the presence of an external power supply to be acknowledged, both of the following conditions must be satisfied:

1. The WALL pin voltage must exceed approximately 4.3V.
2. The WALL pin voltage must be greater than 75mV above the BAT pin voltage.

The input power path (between V_{BUS} and V_{OUT}) is re-enabled and the $\overline{ACPR}$ pin is pulled high when either of the following conditions is met:

1. The WALL pin voltage falls to within 25mV of the BAT pin voltage.
2. The WALL pin voltage falls below 3.2V.

Each of these thresholds is suitably filtered in time to prevent transient glitches on the WALL pin from falsely triggering an event.

Suspend Mode

When I_{LIM0} is pulled high and I_{LIM1} is pulled low the LTC3677-3 enters suspend mode to comply with the USB specification. In this mode, the power path between V_{BUS} and V_{OUT} is put in a high impedance state to reduce the V_{BUS} input current to 50µA. If no other power source is available to drive WALL and V_{OUT}, the system load connected to V_{OUT} is supplied through the ideal diodes connected to BAT.

OPERATION

V_{BUS} Undervoltage Lockout (UVLO) and Undervoltage Current Limit (UVCL)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the input current limit circuitry off until V_{BUS} rises above the rising UVLO threshold (3.8V) and at least 50mV above V_{OUT}. Hysteresis on the UVLO turns off the input current limit if V_{BUS} drops below 3.7V or 50mV below V_{OUT}. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode. To minimize the possibility of oscillation in and out of UVLO when using resistive input supplies, the input current limit is reduced as V_{BUS} falls below 4.45V (typ).

Battery Charger

The LTC3677-3 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out of temperature charge pausing. When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates. Once the battery voltage is above 2.85V, the battery charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1000V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional current will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the battery voltage approaches the float voltage, the charge current begins to decrease as the LTC3677-3 enters constant-voltage mode. Once the battery charger detects that it has entered constant-voltage mode, the four hour safety timer is started. After the safety timer expires, charging of the battery will terminate and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.1V for LTC3677-3). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, the timer will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.3ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS}, is removed and then replaced).

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1000th of the battery charge current is delivered to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1000 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1000V}{I_{CHG}},\ I_{CHG} = \frac{1000V}{R_{PROG}}$$

OPERATION

In either the constant-current or constant-voltage charging modes, the PROG pin voltage will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input current available and prioritization with the system load drawn from V_{OUT}.

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC3677-3 from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC3677-3 or external components. The benefit of the LTC3677-3 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing. When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the charger enters constant-voltage mode and the charge current has dropped to one-tenth of the programmed value, the $\overline{CHRG}$ pin is released (high impedance). The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3677-3 is in input current limit. This prevents false end-of-charge indications due to insufficient power available to the battery charger. Even though charging is stopped during an NTC fault the $\overline{CHRG}$ pin will stay low indicating that charging is not complete.

Battery Charger Stability Considerations

The LTC3677-3's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 4.7µF capacitor in series with a 0.2Ω to 1Ω resistor from BAT to GND is required to keep ripple voltage low when the battery is disconnected.

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

NTC Thermistor and Battery Voltage Reduction

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from NTCBIAS to NTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). The LTC3677-3 will

OPERATION

pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k (for a Vishay curve 1 thermistor, this corresponds to approximately 40°C). If the battery charger is in constant-voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3677-3 is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For a Vishay curve 1 thermistor this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. The typical NTC circuit is shown in Figure 3.

To improve safety and reliability the battery voltage is reduced when the battery temperature becomes excessively high. When the resistance of the NTC thermistor drops to about 0.35 times the value of R25 or approximately 35k (for a Vishay curve 1 thermistor, this corresponds to approximately 50°C) the NTC enables circuitry to monitor the battery voltage. If the battery voltage is above the battery discharge threshold (about 3.9V) then the battery discharge circuitry is enabled and draws about 140mA from the battery when V_{BUS} = 0V and about 180mA when V_{BUS} = 5V. The battery discharge current is disabled below the battery discharge threshold.

When the charger is disabled an internal watchdog timer samples the NTC thermistor for about 150µs every 150ms and will enable the battery monitoring circuitry if the battery temperature exceeds the NTC TOO_HOT threshold. If adding a capacitor to the NTC pin for filtering the time constant must be much less than 150µs so that the NTC pin can settle to its final value during the sampling period. A time constant less than 10µs is recommended. Once the battery monitoring circuitry is enabled it will remain enabled and monitoring the battery voltage until the battery temperature falls back below the discharge temperature threshold. The battery discharge circuitry is only enabled if the battery voltage is greater than the battery discharge threshold.

Alternate NTC Thermistors and Biasing

The LTC3677-3 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay curve 1 thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value

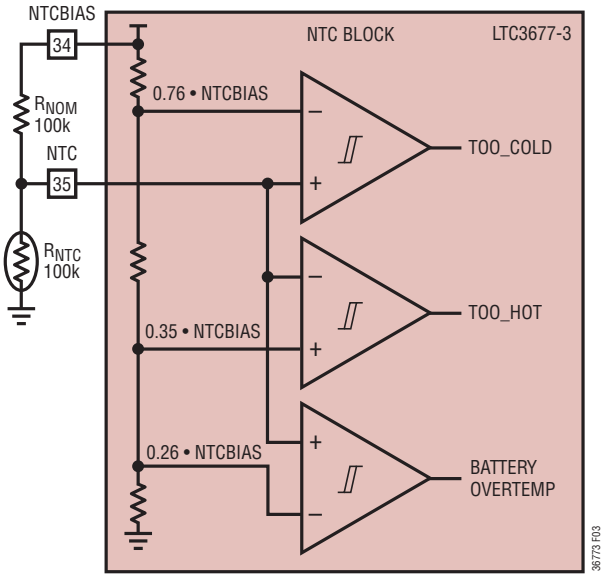

Figure 3. Typical NTC Thermistor Circuit

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or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay curve 1 resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT} = Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 3)

R1 = Optional temperature range adjustment resistor (see Figure 4)

The trip points for the LTC3677-3's temperature qualification are internally programmed at 0.35 • V_{NTC} for the hot threshold and 0.76 • V_{NTC} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM}+R_{NTC|HOT}} \bullet NTCBIAS = 0.35 \bullet NTCBIAS$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM}+R_{NTC|COLD}} \bullet NTCBIAS = 0.76 \bullet NTCBIAS$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.538 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.17 \bullet R_{NOM}$$

By setting R_{NOM} equal to R25, the above equations result in r_{HOT} = 0.538 and r_{COLD} = 3.17. Referencing these ratios to the Vishay resistance-temperature curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.538} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.17} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the *desired* hot and cold trip points. Note that these equations

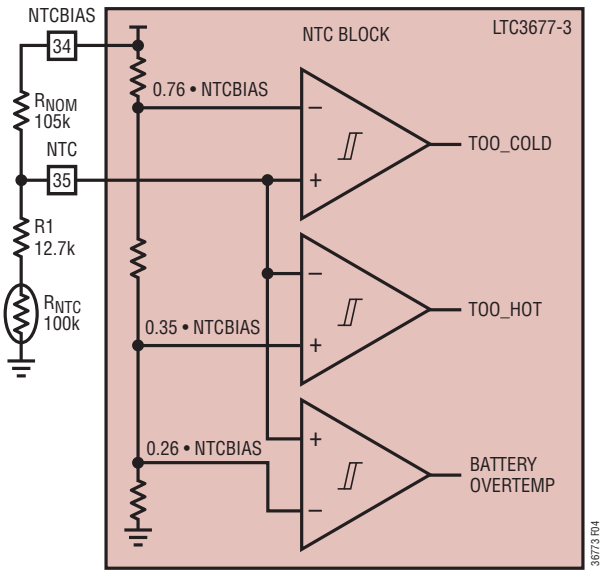

Figure 4. NTC Thermistor Circuit with Additional Bias Resistor

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are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC.

Consider an example where a 60°C hot trip point is desired. From the Vishay curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in temperature gain of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 4. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k.

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 4 and results in an upper trip point of 45°C and a lower trip point of 0°C.

Overvoltage Protection (OVP)

The LTC3677-3 can protect itself from the inadvertent application of excessive voltage to V_{BUS} or WALL with just two external components: an N-channel MOSFET and a 6.2k resistor. The maximum safe overvoltage magnitude will be determined by the choice of the external N-channel MOSFET and its associated drain breakdown voltage.

The overvoltage protection module consists of two pins. The first, OVSENS, is used to measure the externally applied voltage through an external resistor. The second, OVGATE, is an output used to drive the gate pin of an external FET. The voltage at OVSENS will be lower than the OVP input voltage by (I_{OVSENS} • 6.2kΩ) due to the OVP circuit's quiescent current. The OVP input will be 200mV to 400mV higher than OVSENS under normal operating conditions. When OVSENS is below 6V, an internal charge pump will drive OVGATE to approximately 1.88 • OVSENS. This will enhance the N-channel MOSFET and provide a low impedance connection to V_{BUS} or WALL which will, in turn, power the LTC3677-3. If OVSENS should rise above 6V (6.35V OVP input) due to a fault or use of an incorrect wall adapter, OVGATE will be pulled to GND, disabling the external FET to protect downstream circuitry. When the voltage drops below 6V again, the external FET will be re-enabled.

In an overvoltage condition, the OVSENS pin will be clamped at 6V. The external 6.2k resistor must be sized appropriately to dissipate the resultant power. For example, a 1/10W 6.2k resistor can have at most $\sqrt{P_{MAX} \bullet 6.2k} = 24V$ applied across its terminals. With the 6V at OVSENS, the maximum overvoltage magnitude that this resistor can withstand is 30V. A 1/4W 6.2k resistor raises this value to 45V.

The charge pump output on OVGATE has limited output drive capability. Care must be taken to avoid leakage on this pin, as it may adversely affect operation.

OPERATION

Dual Input Overvoltage Protection

It is possible to protect both V_{BUS} and WALL from overvoltage damage with several additional components, as shown in Figure 5. Schottky diodes D1 and D2 pass the larger of V1 and V2 to R1 and OVSENS. If either V1 or V2 exceeds 6V plus $V_{F(SCHOTTKY)}$, OVGATE will be pulled to GND and both the WALL and USB inputs will be protected. Each input is protected up to the drain-source breakdown, BVDSS, of MN1 and MN2. R1 must also be rated for the power dissipated during maximum overvoltage. See the Overvoltage Protection section for an explanation of this calculation. Table 2 shows some N-channel MOSFETs that maybe suitable for overvoltage protection.

Table 2. Recommended Overvoltage FETs

N-CHANNEL MOSFET	BVDSS	R_{ON}	PACKAGE
Si1472DH	30V	82mΩ	SC70-6
Si2302ADS	20V	60mΩ	SOT-23
Si2306BDS	30V	65mΩ	SOT-23
Si2316BDS	30V	80mΩ	SOT-23
IRLML2502	20V	35mΩ	SOT-23

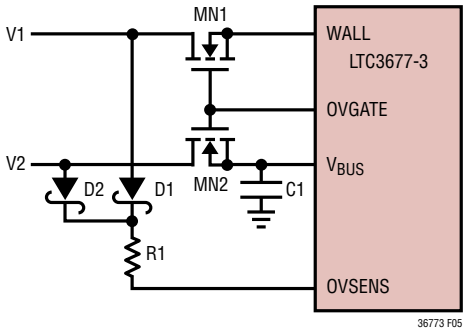
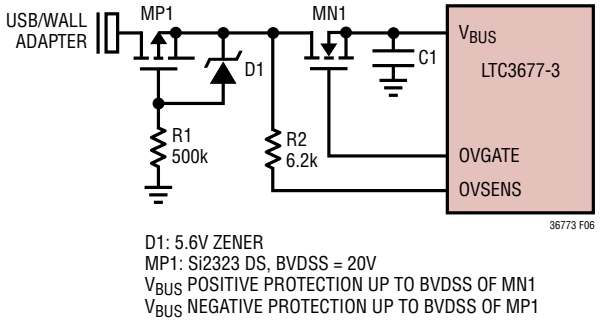


Figure 5. Dual Input Overvoltage Protection

Reverse Input Voltage Protection

The LTC3677-3 can also be easily protected against the application of reverse voltage as shown in Figure 6. D1 and R1 are necessary to limit the maximum VGS seen by MP1 during positive overvoltage events. D1's breakdown voltage must be safely below MP1's BVGS. The circuit shown in Figure 6 offers forward voltage protection up to MN1's BVDSS and reverse voltage protection up to MP1's BVDSS.



D1: 5.6V ZENER
MP1: Si2323 DS, BVDSS = 20V
V_{BUS} POSITIVE PROTECTION UP TO BVDSS OF MN1
V_{BUS} NEGATIVE PROTECTION UP TO BVDSS OF MP1

Figure 6. Dual Polarity Voltage Protection

LOW DROPOUT LINEAR REGULATOR OPERATION

LDO Operation and Voltage Programming

The LTC3677-3 contains two 150mA adjustable output LDO regulators. The first LDO (LDO1) is always on and will be enabled whenever V_{OUT} is greater than V_{OUT} UVLO. The second LDO (LDO2) is controlled by the pushbutton and is the first supply to sequence up in response to pushbutton application. Both LDOs are disabled when V_{OUT} is less than V_{OUT} UVLO and LDO2 is further disabled when the pushbutton circuity is in the power down or power off states. Both LDOs contain a soft-start function to limit inrush current when enabled. The soft-start function works by ramping up the LDO reference over a 200µs period (typical) when the LDO is enabled.

When disabled all LDO circuitry is powered off leaving only a few nanoamps of leakage current on the LDO supply. Both LDO outputs are individually pulled to ground through internal resistors when disabled.

OPERATION

The power good status bits of LDO1 and LDO2 are available in I²C through the read-back registers PGLDO[1] and PGLDO[2] for LDO1 and LDO2 respectively. The power good comparators for both LDOs are sampled when the I²C port receives the correct I²C read address.

Figure 7 shows the LDO application circuit. The full-scale output voltage for each LDO is programmed using a resistor divider from the LDO output (LDO1 or LDO2) connected to the feedback pins (LDO1_FB or LDO2_FB) such that:

$$V_{LDOx} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

For stability, each LDO output must be bypassed to ground with a minimum 1µF ceramic capacitor (C_{OUT}).

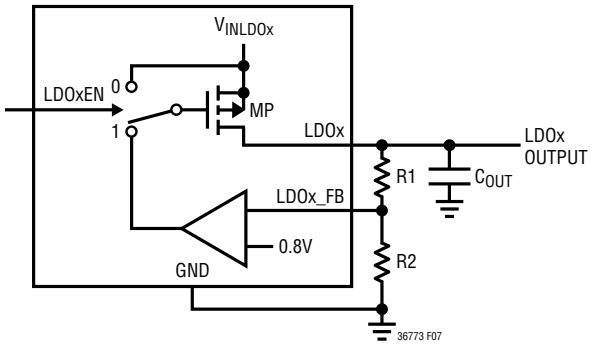


Figure 7. LDO Application Circuit

STEP-DOWN SWITCHING REGULATOR OPERATION

Introduction

The LTC3677-3 includes three 2.25MHz constant-frequency current mode step-down switching regulators providing 500mA, 500mA and 800mA each. All step-down switching regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry. All step-down switching regulators support 100% duty cycle operation (low dropout mode) when the input voltage drops very close to the output voltage and are also capable of Burst Mode operation for highest efficiencies at light loads. Burst Mode operation is individually selectable for each step-down switching regulator through the I²C register bits BK1BRST, BK2BRST and BK3BRST. The step-down switching regulators also include soft-start to limit inrush current when powering on, short-circuit current protection, and switch node slew limiting circuitry to reduce EMI radiation. No external compensation components are required for the switching regulators. Switching regulators 1 and 2 (Buck1 and Buck2) are sequenced up and down together through the pushbutton interface (see the Pushbutton Interface section for more information), while Buck3 has an individual enable pin (EN3) that is active when the pushbutton is in the power-up or power-on states. Buck3 is disabled in the power down and power off states. It is recommended that the step-down switching regulator input supplies (V_{IN12} and V_{IN3}) be connected to the system supply pin (V_{OUT}). This is recommended because the undervoltage lockout circuit on the V_{OUT} pin (V_{OUT} UVLO) disables the step-down switching regulators when the V_{OUT} voltage drops below the V_{OUT} UVLO threshold. If driving the step-down switching regulator input supplies from a voltage other than V_{OUT} the regulators should not be operated outside the specified operating range as operation is not guaranteed beyond this range.

Output Voltage Programming

Figure 8 shows the step-down switching regulator application circuit. The full-scale output voltage for each step-down switching regulator is programmed using a resistor divider from the step-down switching regulator output connected to the feedback pins (FB1, FB2 and FB3) such that:

$$V_{OUTx} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

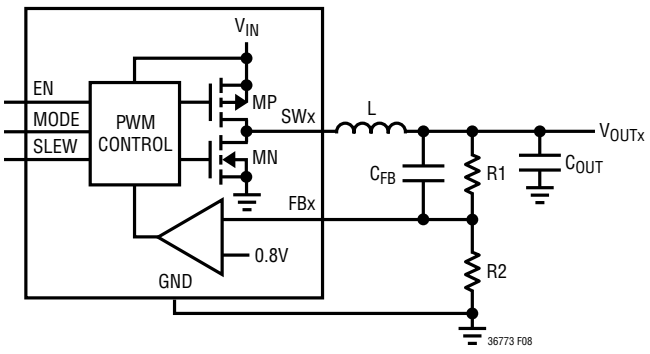


Figure 8. Step-Down Switching Regulator Application Circuit

OPERATION

Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

Operating Modes

The step-down switching regulators include two possible operating modes to meet the noise/power needs of a variety of applications. In pulse-skipping mode, an internal latch is set at the start of every cycle, which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch, which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the step-down switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse-skipping mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW1, SW2 or SW3) goes high impedance and the switch node voltage will ring. This is discontinuous operation, and is normal behavior for a switching regulator. At very light loads in pulse-skipping mode, the step-down switching regulators will automatically skip pulses as needed to maintain output regulation. At high duty cycle (V_{OUTX} approaching V_{INX}) it is possible for the inductor current to reverse at light loads causing the stepped down switching regulator to operate continuously. When operating continuously, regulation and low noise output voltage are maintained, but input operating current will increase to a few milliamps.

In Burst Mode operation, the step-down switching regulators automatically switch between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads the step-down switching regulators control the inductor current directly and use a hysteretic control loop to minimize both noise and switching losses. While operating in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down switching regulator then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the switching regulator's circuitry is powered down, helping conserve battery power. When the output voltage drops below a pre-determined value, the step-down switching regulator circuitry is powered on and another burst cycle begins. The sleep time decreases as the load current increases. Beyond a certain load current point (about 1/4 rated output load current) the step-down switching regulators will switch to a low noise constant-frequency PWM mode of operation, much the same as pulse-skipping operation at high loads.

For applications that can tolerate some output ripple at low output currents, Burst Mode operation provides better efficiency than pulse-skipping at light loads. The step-down switching regulators allow mode transition on-the-fly, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed. Burst Mode operation is individually selectable for each step-down switching regulator through the I^2C register bits BK1BRST, BK2BRST and BK3BRST.

Shutdown

The step-down switching regulators (Buck1, Buck2 and Buck3) are shut down when the pushbutton circuitry is in the power-down or power-off state. Step-down switching regulator 3 (Buck3) can also be shut down by bringing the EN3 input low. In shutdown all circuitry in the step-down switching regulator is disconnected from the switching regulator input supply leaving only a few nanoamps of leakage current. The step-down switching regulator outputs are individually pulled to ground through internal 10k resistors on the switch pin (SW1, SW2 or SW3) when in shutdown.

OPERATION

Dropout Operation

It is possible for a step-down switching regulator's input voltage to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the P-Channel MOSFET switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each step-down switching regulator over a 500µs period. This allows each output to rise slowly, helping minimize inrush current required to charge up the switching regulator output capacitor. A soft-start cycle occurs whenever a given switching regulator is enabled. A soft-start cycle is not triggered by changing operating modes. This allows seamless output transition when actively changing between operating modes.

Slew Rate Control

The step-down switching regulators contain patented circuitry to limit the slew rate of the switch node (SW1, SW2 and SW3). This new circuitry is designed to transition the switch node over a period of a few nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency. Since slowing the slew rate of the switch nodes causes efficiency loss, the slew rate of the step-down switching regulators is adjustable via the I^2C registers SLEWCTL1 and SLEWCTL2. This allows the user to optimize efficiency or EMI as necessary with four different slew rate settings. The power up default is the fastest slew rate (highest efficiency) setting. Figures 9 and 10 show the efficiency and power loss graph for Buck3 programmed for 1.2V and 2.5V outputs. Note that the power loss curves remain fairly constant for both graphs yet changing the slew rate has a larger effect on the 1.2V output efficiency. This is mainly because for a given output current the 2.5V output is delivering more than 2x the power than the 1.2V output. Efficiency will always decrease and show more variation to slew rate as the programmed output voltage is decreased.

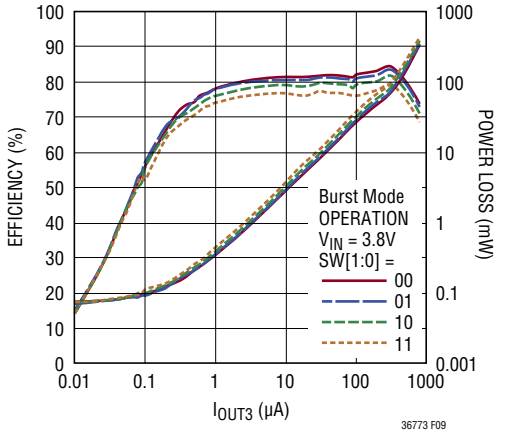


Figure 9. V_{OUT3} (1.2V) Efficiency and Power Loss vs I_{OUT3}

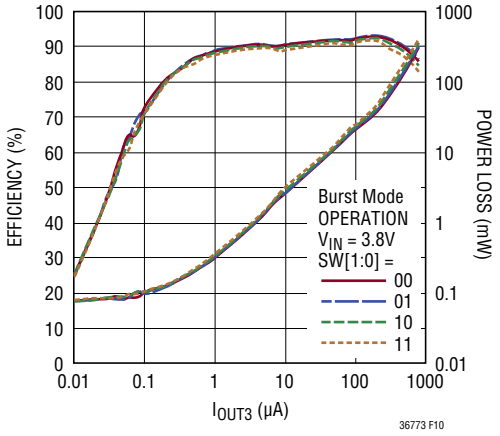


Figure 10. V_{OUT3} (2.5V) Efficiency and Power Loss vs I_{OUT3}

OPERATION

Low Supply Operation

An undervoltage lockout circuit on V_{OUT} (V_{OUT} UVLO) shuts down the step-down switching regulators when V_{OUT} drops below about 2.7V. It is recommended that the step-down switching regulator input supplies (V_{IN12}, V_{IN3}) be connected to the power path output (V_{OUT}) directly. This UVLO prevents the step-down switching regulators from operating at low supply voltages where loss of regulation or other undesirable operation may occur. If driving the step-down switching regulator input supplies from a voltage other than the V_{OUT} pin, the regulators should not be operated outside the specified operating range as operation is not guaranteed beyond this range.

Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler. The step-down switching regulators are designed to work with inductors in the range of 2.2µH to 10µH. For most applications a 4.7µH inductor is suggested for step-down switching regulators providing up to 500mA of output current while a 3.3µH inductor is suggested for step-down switching regulators providing up to 800mA. Larger value inductors reduce ripple current, which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time, but will reduce the available output current. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resistance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters. Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The

Table 3. Recommended Inductors for Step-Down Switching Regulators

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
DB318C	4.7	1.07	0.1	3.8 × 3.8 × 1.8	Toko
	3.3	1.20	0.07	3.8 × 3.8 × 1.8	www.toko.com
D312C	4.7	0.79	0.24	3.6 × 3.6 × 1.2	
	3.3	0.90	0.20	3.6 × 3.6 × 1.2	
DE2812C	4.7	1.15	0.13*	3.0 × 2.8 × 1.2	
	3.3	1.37	0.105*	3.0 × 2.8 × 1.2	
CDRH3D16	4.7	0.9	0.11	4 × 4 × 1.8	Sumida
	3.3	1.1	0.085	4 × 4 × 1.8	www.sumida.com
CDRH2D11	4.7	0.5	0.17	3.2 × 3.2 × 1.2	
	3.3	0.6	0.123	3.2 × 3.2 × 1.2	
CLS4D09	4.7	0.75	0.19	4.9 × 4.9 × 1	
SD3118	4.7	1.3	0.162	3.1 × 3.1 × 1.8	Cooper
	3.3	1.59	0.113	3.1 × 3.1 × 1.8	www.cooperet.com
SD3112	4.7	0.8	0.246	3.1 × 3.1 × 1.2	
	3.3	0.97	0.165	3.1 × 3.1 × 1.2	
SD12	4.7	1.29	0.117*	5.2 × 5.2 × 1.2	
	3.3	1.42	0.104*	5.2 × 5.2 × 1.2	
SD10	4.7	1.08	0.153*	5.2 × 5.2 × 1.0	
	3.3	1.31	0.108*	5.2 × 5.2 × 1.0	
LPS3015	4.7	1.1	0.2	3.0 × 3.0 × 1.5	Coil Craft
	3.3	1.3	0.13	3.0 × 3.0 × 1.5	www.coilcraft.com

*Typical DCR

OPERATION

choice of which style inductor to use often depends more on the price versus size, performance, and any radiated EMI requirements than on what the step-down switching regulators requires to operate. The inductor value also has an effect on Burst Mode operation. Lower inductor values will cause Burst Mode switching frequency to increase. Table 3 shows several inductors that work well with the step-down switching regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at both step-down switching regulator outputs as well as at each step-down switching regulator input supply. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for the step-down switching regulator outputs. For good transient response and stability the output capacitor for step-down switching regulators should retain at least 4µF of capacitance over operating temperature and bias voltage. Each switching regulator input supply should be bypassed with a 2.2µF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 4 shows a list of several ceramic capacitor manufacturers.

Table 4. Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

I²C OPERATION

I²C Interface

The LTC3677-3 may communicate with a bus master using the standard I²C 2-wire interface. The timing diagram in Figure 11 shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC3677-3 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I²C serial port is cleared and registers are set to the default configuration of all zeros.

I²C Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

I²C START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC3677-3, the master may transmit a STOP condition which commands the LTC3677-3 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH. The bus is then free for communication with another I²C device.

I²C Byte Format

Each byte sent to or received from the LTC3677-3 must be 8 bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC3677-3 most significant bit (MSB) first.

OPERATION

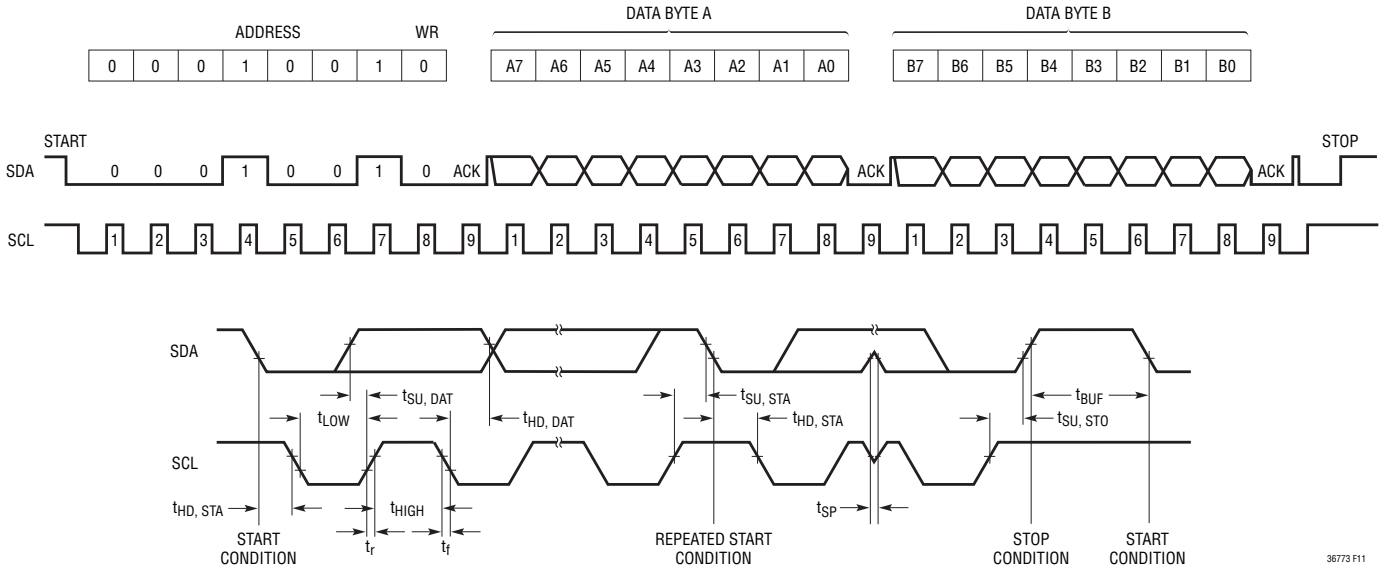


Figure 11. I²C Timing Diagram

I²C Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC3677-3 is written to (write address), it acknowledges its write address as well as the subsequent two data bytes. When read from (read address), the LTC3677-3 acknowledges its read address only. The bus master should acknowledge receipt of information from the LTC3677-3.

An acknowledge (active LOW) generated by the LTC3677-3 lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock cycle. The LTC3677-3 pulls down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC3677-3 is read from, it releases the SDA line so that the master may acknowledge receipt of the data. Since the LTC3677-3 only transmits one byte of data, a master not acknowledging the data sent by the LTC3677-3 has no I²C specific consequence on the operation of the I²C port.

I²C Slave Address

The LTC3677-3 responds to a 7-bit address which has been factory programmed to b'0001001[R/W]'. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC3677-3 and 1 when reading data from it. Considering the address an 8-bit word, then the write address is 0x12 and the read address is 0x13. The LTC3677-3 will acknowledge both its read and write address.

I²C Sub-Addressed Writing

The LTC3677-3 has one command register for control input. It is accessed by the I²C port via a sub-addressed writing system.

Each write cycle of the LTC3677-3 consists of exactly three bytes. The first byte is always the LTC3677-3's write address. The second byte represents the LTC3677-3's sub-address. The sub-address is a pointer which directs the subsequent data byte within the LTC3677-3. The third byte consists of the data to be written to the location pointed to by the sub-address. The LTC3677-3 contains control registers at only sub-address location 0x00. Sub-addresses outside 0x00 should not be written to as they access functionality not available in the LTC3677-3.

OPERATION

I²C Bus Write Operation

The master initiates communication with the LTC3677-3 with a START condition and the LTC3677-3's write address. If the address matches that of the LTC3677-3, the LTC3677-3 returns an acknowledge. The master should then deliver the sub-address. Again the LTC3677-3 acknowledges and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC3677-3. This procedure must be repeated for each sub-address that requires new data. After one or more cycles of [ADDRESS][SUB-ADDRESS][DATA], the master may terminate the communication with a STOP condition. Alternatively, a REPEAT-START condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3677-3 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC3677-3 will update its command latches with the data that it received.

I²C Bus Read Operation

The bus master reads the status of the LTC3677-3 with a START condition followed by the LTC3677-3 read address. If the read address matches that of the LTC3677-3, the LTC3677-3 returns an acknowledge. Following the acknowledgement of their read address, the LTC3677-3 returns one bit of status information for each of the next 8 clock cycles. A STOP command is not required for the bus read operation.

I²C Input Data

There is one byte of data that can be written to on the LTC3677-3. The byte is accessed through the sub-address 0x00. At first power application (V_{BUS}, WALL or BAT) all bits default to 0. Additionally, all bits are cleared to 0 when DV_{CC} drops below its undervoltage lock out or if the pushbutton enters the power down (PDN) state.

Table 5 shows the byte of data that can be written to at sub-address 0x00. This byte of data is referred to as the buck control register.

Table 5. Buck Control Register

BUCK CONTROL REGISTER		**ADDRESS:** 00010010 **SUB-ADDRESS:** 00000000
BIT	**NAME**	**FUNCTION**
B0	N/A	Not Used—No Effect On Operation
B1	N/A	Not Used—No Effect On Operation
B2	BK1BRST	Buck1 Burst Mode Enable
B3	BK2BRST	Buck2 Burst Mode Enable
B4	BK3BRST	Buck2 Burst Mode Enable
B5	SLEWCTL1	Buck SW Slew Rate: 00 = 1ns, 01 = 2ns, 10 = 4ns, 11 = 8ns
B6	SLEWCTL2	
B7	N/A	Not Used—No Effect On Operation

Bits B2, B3, and B4 set the operating modes of the step-down switching regulators (bucks). Writing a 1 to any of these three registers will put that respective buck converter in the high efficiency Burst Mode operation, while a 0 will enable the low noise pulse-skipping mode of operation.

The B5 and B6 bits adjust the slew rate of all SW pins together so they all slew at the same rate. It is recommended that the fastest slew rate (B6:B5 = 00) be used unless EMI is an issue in the application as slower slew rates cause reduced efficiency.

I²C Output Data

One status byte may be read from the LTC3677-3, as shown in Table 6. A 1 read back in the any of the bit posi-

OPERATION

tions indicates that the condition is true. For example, 1 read back from bit A3 indicate that LDO1 is enabled and regulating correctly. A status read from the LTC3677-3 captures the status information when the LTC3677-3 acknowledge its read address.

Table 6. I²C READ Register

STATUS REGISTER		ADDRESS: 00010011 SUB-ADDRESS: None
BIT	**NAME**	**FUNCTION**
A0	CHARGE	Charge Status (1 = Charging)
A1	STAT[0]	STAT[1:0]; 00 = No Fault 01 = TOO COLD/HOT 10 = BATTERY OVERTEMP 11 = BATTERY FAULT
A2	STAT[1]	
A3	PGLDO[1]	LDO1 Power Good
A4	PGLDO[2]	LDO2 Power Good
A5	PGBCK[1]	Buck1 Power Good
A6	PGBCK[2]	Buck2 Power Good
A7	PGBCK[3]	Buck3 Power Good

Bit A7 shows the power good status of Buck3. A 1 indicates that Buck3 is enabled and is regulating correctly. A 0 indicates that either Buck3 is not enabled, or that the Buck3 is enabled, but is out of regulation by more than 8%.

Bit A6 shows the power good status of Buck2. A 1 indicates that Buck2 is enabled and is regulating correctly. A 0 indicates that either Buck2 is not enabled, or that the Buck2 is enabled, but is out of regulation by more than 8%.

Bit A5 shows the power good status of Buck1. A 1 indicates that Buck1 is enabled and is regulating correctly. A 0 indicates that either Buck1 is not enabled, or that the Buck1 is enabled, but is out of regulation by more than 8%.

Bit A4 shows the power good status of LDO2. A 1 indicates that LDO2 is enabled and is regulating correctly. A 0 indicates that either LDO2 is not enabled, or that the LDO2 is enabled, but is out of regulation by more than 8%.

Bit A3 shows the power good status of LDO1. A 1 indicates that LDO1 is enabled and is regulating correctly. A 0 indicates that either LDO1 is not enabled, or that the LDO1 is enabled, but is out of regulation by more than 8%.

Bits A2 and A1 indicate the fault status of the charger measurement circuit and are decoded in Table 6. The too cold/hot state indicates that the thermistor temperature is out of the valid charging range (either below 0°C or above 40°C for a curve 1 thermistor) and that charging has paused until the battery returns to valid charging temperature. The battery overtemperature state indicates that the battery's thermistor has reached a critical temperature (about 50°C for a curve 1 thermistor) and that long-term battery capacity may be seriously compromised if the condition persists. The battery fault state indicates that an attempt was made to charge a low battery (typically < 2.85V) but that the low voltage condition persisted for more than 1/2 hour. In this case charging has terminated.

Bit A0 indicates the status of the battery charger. A 1 indicates that the charger is enabled and is in the constant-current charge state. In this case the battery is being charged unless the NTC thermistor is outside its valid charge range in which case charging is temporarily suspended but not complete. Charging will continue once the battery has returned to a valid charging temperature. A 0 in bit A0 indicates that charger has reached end-of-charge ($h_{C/10}$) and is near V_{FLOAT} or that charging has been terminated. Charging can be terminated by reaching the end of the charge timer or by a battery fault as described previously.

OPERATION

PUSHBUTTON INTERFACE OPERATION

State Diagram/Operation

Figure 13 shows the LTC3677-3 pushbutton state diagram. Upon first application of power (V_{BUS}, WALL or BAT) an internal power-on reset (POR) signal places the pushbutton circuitry into the power-off (POFF) state. The following events cause the state machine to transition out of POFF into the power-up (PUP) state:

1) $\overline{ON}$ input LOW for 50ms (PB50MS)

2) PWR_ON input going HIGH (PWR_ON)

Upon entering the PUP state, the pushbutton circuitry will sequence up LDO2, Buck1 and Buck2 in that order. One second after entering the PUP state, the pushbutton circuitry will transition into the power-on (PON) state. Note that the PWR_ON input must be brought HIGH before entering the PON state if the part is to remain in the PON state. Buck3 can be enabled through the EN3 input once the pushbutton is in the PUP or PON states.

PWR_ON going LOW, or V_{OUT} dropping to its undervoltage lockout (V_{OUT} UVLO) threshold will cause the state machine to leave the PON state and enter the power-down (PDN) state. The PDN state resets the I^2C registers as well as disables Buck1, Buck2 and LDO2 together. Buck3 is also disabled in the PDN and POFF states. The one second delay before leaving the power-down state allows the supplies to power down completely before they can be re-enabled.

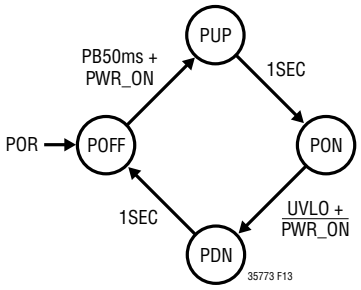


Figure 12. Pushbutton State Diagram

PBSTAT Operation

PBSTAT goes LOW 50ms after the initial pushbutton application ($\overline{ON}$ LOW) and will stay low for 50ms minimum. PBSTAT will go HIGH coincident with $\overline{ON}$ going HIGH unless $\overline{ON}$ goes HIGH before the 50ms minimum LOW time.

Hard Reset and PGOOD Operation

The hard reset event is generated by pressing and holding the pushbutton ($\overline{ON}$ input LOW) for 14 seconds. For a valid hard reset event to occur the initial pushbutton application must start in the PUP or PON state. This avoids causing a hard reset from occurring if the user hangs on the pushbutton during initial power-up. If a valid hard reset event is present then the PGOOD output will transition LOW for about 1.8ms to allow the microprocessor to reset. The hard reset event does not affect the operating state or regulator operation.

The PGOOD pin is an open-drain output used to indicate that Buck1, Buck2 and LDO1 are enabled and have reached their final regulation voltage. A 230ms delay is included from the time Buck1, Buck2 and LDO1 reach 92% of their regulation value to allow a system controller ample time to reset itself. PGOOD is an open-drain output and requires a pull-up resistor to an appropriate power source. Optimally the pull-up resistor is connected to the output of Buck1, Buck2 or LDO2 so that power is not dissipated while the regulators are disabled.

Pushbutton Operation and V_{OUT} UVLO

As stated earlier V_{OUT} dropping to its UVLO threshold will cause the pushbutton to leave the power-on state and enter the power-down state, thus powering down Buck1, Buck2, Buck3 and LDO2. Additionally, LDO1 is disabled when in UVLO. Thus, all LTC3677-3 supplies are disabled and remain disabled as long as the V_{OUT} UVLO condition exists. It is not possible to power up any of the LTC3677-3 generated supplies while V_{OUT} is below the V_{OUT} UVLO threshold.

OPERATION

Power-Up via Pushbutton Timing

The timing diagram, Figure 13, shows the LTC3677-3 powering up through application of the external pushbutton. For this example the pushbutton circuitry starts in the POFF state with V_{OUT} not in UVLO and Buck1, Buck2 and LDO2 disabled. Pushbutton application ($\overline{ON}$ LOW) for 50ms transitions the pushbutton circuitry into the PUP state which sequences up LDO2, Buck1 and Buck2 in that order. PWR_ON must be driven HIGH before the 1 second PUP period is over to keep supplies up. If PWR_ON is LOW or goes LOW after the 1 second PUP period Buck1, Buck2, and LDO2 will be shut down together. PGOOD is asserted once Buck1, Buck2 and LDO1 are within 8% of their regulation voltage for 230ms.

Buck3 can be enabled and disabled at any time via EN3 once in the PUP or PON states. The PWR_ON input can be driven via a µP/µC or by one of the sequenced outputs through a high impedance (100kΩ typ). PBSTAT goes LOW 50ms after the initial pushbutton application and will stay LOW for 50ms minimum. PBSTAT will go HIGH coincident with $\overline{ON}$ going HIGH unless $\overline{ON}$ goes HIGH before the 50ms minimum LOW time.

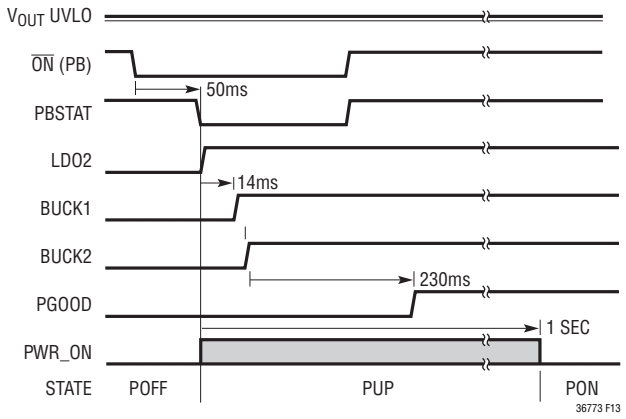


Figure 13. Power-Up via Pushbutton

Power-Up via PWR_ON Timing

The timing diagram, Figure 14, shows the LTC3677-3 powering up by driving PWR_ON HIGH. For this example the pushbutton circuitry starts in the POFF state with V_{OUT} not in UVLO and Buck1, Buck2 and LDO2 disabled. 50ms after PWR_ON goes HIGH the pushbutton circuitry transitions into the PUP state which sequences up LDO2, Buck1 and Buck2 in that order. PWR_ON must be driven high before the 1 second PUP period is over to keep supplies up. If PWR_ON is LOW or goes LOW after the 1 second PUP period Buck1, Buck2 and LDO2 will be shut down together. PGOOD is asserted once Buck1, Buck2 and LD01 are within 8% of their regulation voltage for 230ms.

Buck3 can be enabled and disabled at any time via EN3 once in the PUP or PON states.

Powering up via PWR_ON is useful for applications containing an always on microcontroller. This allows the microcontroller to power the application up and down for house keeping and other activities outside the user's control.

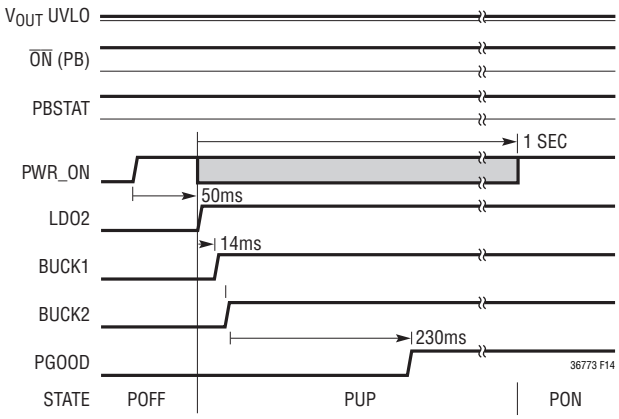


Figure 14. Power-Up via PWR_ON

OPERATION

Power Down via Pushbutton Timing

The timing diagram, Figure 15, shows the LTC3677-3 powering down by µC/µP control. For this example the pushbutton circuitry starts in the PON state with V_{OUT} not in UVLO and Buck1, Buck2 and LDO2 enabled. In this case the pushbutton is applied ($\overline{ON}$ LOW) for at least 50ms, which generates a low impedance on the PBSTAT output. After receiving the PBSTAT the µC/µP will drive the PWR_ON input LOW. 50ms after PWR_ON goes LOW the pushbutton circuitry will enter the PDN state. Buck1, Buck2 and LDO2 are disabled together upon entering the PDN state. After entering the PDN state, a 1 second wait time is initiated before entering the POFF state. During this 1 second time $\overline{ON}$ and PWR_ON inputs are ignored to allow all LTC3677-3 generated supplies to go LOW.

Upon entering the PDN state Buck3 is disabled and the I^2C registers are cleared. Holding $\overline{ON}$ LOW through the 1 second power-down period will not cause a power-up event at end of the 1 second period. The $\overline{ON}$ input must be brought HIGH following the power-down event and then go LOW again to establish a valid power-up event.

V_{OUT} UVLO Power-Down Timing

If V_{OUT} drops below the V_{OUT} UVLO threshold, the pushbutton circuitry will transition from the PON state to the PDN state. Buck1, Buck2 and LDO2 are disabled together upon entering the PDN state. After entering the PDN state, a 1 second wait time is initiated before entering the POFF state. During this 1 second time $\overline{ON}$ and PWR_ON inputs are ignored to allow all LTC3677-3 generated supplies to go LOW.

Upon entering the PDN state the Buck3 is disabled and the I^2C registers are cleared. LDO1 is also disabled by the V_{OUT} UVLO and stays disabled as long as the V_{OUT} UVLO condition remains. Note that it is not possible to sequence any of the supplies up while the V_{OUT} UVLO condition exists. LDO1 will be re-enabled when the V_{OUT} UVLO condition is removed. The other supplies will remain disabled until a valid power-up pushbutton event takes place.

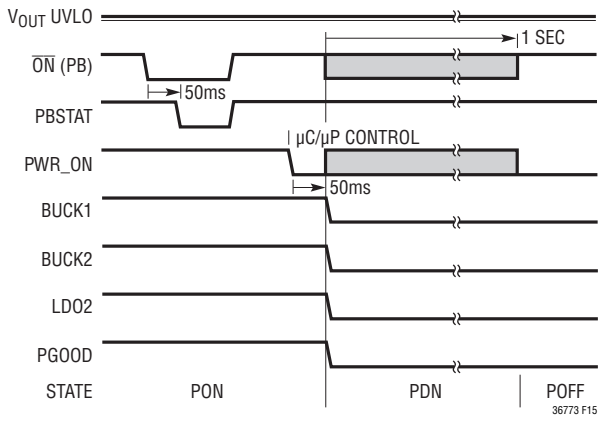


Figure 15. Power-Down via Pushbutton

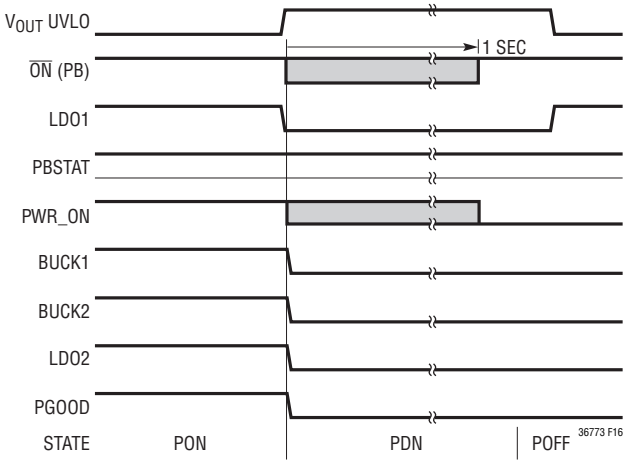


Figure 16. V_{OUT} UVLO Power-Down

OPERATION

Hard Reset Timing

Hard reset provides a way to reset the µC/µP in case of a software lockup. To initiate a hard reset, the pushbutton is pressed ($\overline{ON}$ LOW) and held for greater than 14 seconds. Once the hard reset time is exceeded the PGOOD input will go LOW for 1.8ms which resets the µC/µP. Operation of the enabled supplies is not effected by the hard reset event. All enabled supplies should remain in regulation and operating correctly assuming specified operating conditions are met (i.e., no shorted supplies, etc).

There are only two methods to power down the LTC3677-3 supplies: 1) PWR_ON goes LOW; 2) V_{OUT} drops below the V_{OUT} UVLO threshold. If the µC/µP controls shutdown by bringing PWR_ON LOW, it is possible that the application can hang with all supplies enabled if the µC/µP fails to reset correctly on hard reset. In this case the battery will continue to be drained until V_{OUT} drops below the V_{OUT} UVLO threshold, or the user intervenes to shut down the application manually. The application can be shut down manually by removing the battery and any external supplies, or by providing a suicide button that will bring PWR_ON LOW when pressed.

Power-Up Sequencing

Figure 18 shows the actual power-up sequencing of the LTC3677-3. Buck1, Buck2 and LDO2 are all initially disabled (0V). Once the pushbutton has been applied ($\overline{ON}$ LOW) for 50ms PBSTAT goes LOW and LDO2 is enabled. Once enabled, LDO2 slews up and enters regulation. The actual slew rate is controlled by the soft-start function of LDO2 which ramps the LDO reference up over a 200µs period typically. After a 14ms delay from LDO2 being enabled, Buck1 is enabled and slews up into regulation. When Buck1 is within about 8% of final regulation, Buck2 is enabled and slews up into regulation. The bucks also have a soft-start function to limit inrush current at start-up. 230ms after Buck2 is within 8% of final regulation, the PGOOD output will go high impedance (not shown in Figure 18). The regulators in Figure 18 are slewing up with nominal output capacitors and no load. Adding a load or increasing output capacitance on any of the outputs will reduce the slew rate and lengthen the time it takes the regulator to get into regulation.

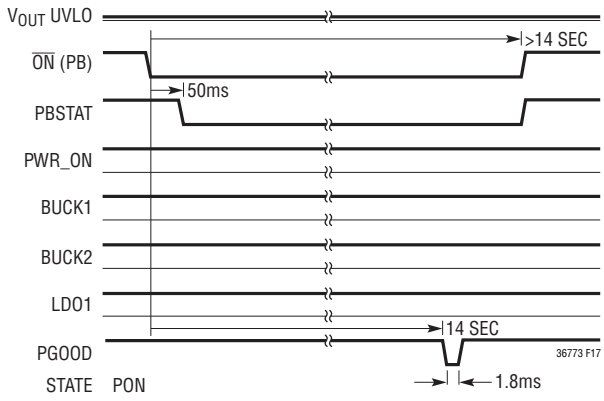


Figure 17. Hard Reset Timing

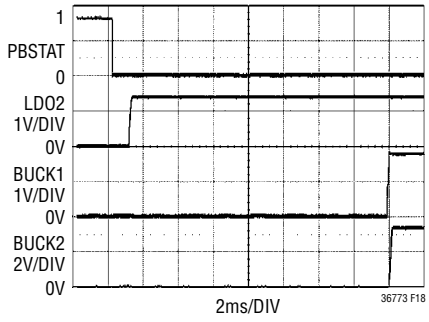


Figure 18. Power-Up Sequencing

OPERATION

LAYOUT AND THERMAL CONSIDERATIONS

Printed Circuit Board Power Dissipation

In order to be able to deliver maximum charge current under all conditions, it is critical that the exposed ground pad on the backside of the LTC3677-3 package be soldered to a ground plane on the board. Correctly soldered to 2500mm^2 ground plane on a double-sided 1oz copper board the LTC3677-3 has a thermal resistance (θ_{JA}) of approximately 45°C/W. Failure to make good thermal contact between the exposed pad on the backside of the package and a adequately sized ground plane will result in thermal resistances far greater than 45°C/W.

The conditions that cause the LTC3677-3 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the part. For high charge currents with a wall adapter applied to V_{OUT}, the LTC3677-3 power dissipation is approximately:

$$P_D = (V_{OUT} - BAT) \bullet I_{BAT} + P_{DREGS}$$

where P_D is the total power dissipated, V_{OUT} is the supply voltage, BAT is the battery voltage and I_{BAT} is the battery charge current. P_{DREGS} is the sum of power dissipated on-chip by the step-down switching, and LDO regulators.

The power dissipated by a step-down switching regulator can be estimated as follows:

$$P_{D(SWx)} = \left(OUTx \bullet I_{OUTx}\right) \bullet \frac{100 - Eff}{100}$$

where OUTx is the programmed output voltage, I_{OUTx} is the load current and Eff is the % efficiency which can be measured or looked up on an efficiency table for the programmed output voltage.

The power dissipated on chip by a LDO regulator can be estimated as follows:

$$P_{DLDOx} = (V_{INLDOx} - LDOx) \bullet I_{LDOx}$$

where LDOx is the programmed output voltage, VI_{NLDOx} is the LDO supply voltage and I_{LDOx} is the LDO output load current. Note that if the LDO supply is connected to one of the buck output, then its supply current must be added to the buck regulator load current for calculating the buck power loss.

Thus the power dissipated by all regulators is:

$$P_{DREGS} = P_{DSW1} + P_{DSW2} + P_{DSW3} + P_{DLDO1} + P_{DLDO2}$$

It is not necessary to perform any worst-case power dissipation scenarios because the LTC3677-3 will automatically reduce the charge current to maintain the die temperature at approximately 110°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 110°C - P_D \bullet \theta_{JA}$$

Example: Consider the LTC3677-3 operating from a wall adapter with 5V (V_{OUT}) providing 1A (I_{BAT}) to charge a Li-Ion battery at 3.3V (BAT). Also assume P_{DREGS} = 0.3W, so the total power dissipation is:

$$P_D = (5V - 3.3V) \bullet 1A + 0.3W = 2W$$

The ambient temperature above which the LTC3677-3 begins to reduce the 1A charge current, is approximately

$$T_A = 110°C - 2W \bullet 45°C/W = 20°C$$

The LTC3677-3 can be used above 20°C, but the charge current will be reduced below 1A. The charge current at a given ambient temperature can be approximated by:

$$P_D = \frac{110°C - T_A}{\theta_{JA}} = \left(V_{OUT} - BAT\right) \bullet I_{BAT} + P_{D(REGS)}$$

Thus:

$$I_{BAT} = \frac{\left(110°C - T_A\right)}{\theta_{JA} - P_{D(REGS)}} \over V_{OUT} - BAT$$

OPERATION

Consider the previous example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{BAT} = \frac{\frac{110°C - 55°C}{45°C/W} - 0.3W}{5V - 3.3V}$$

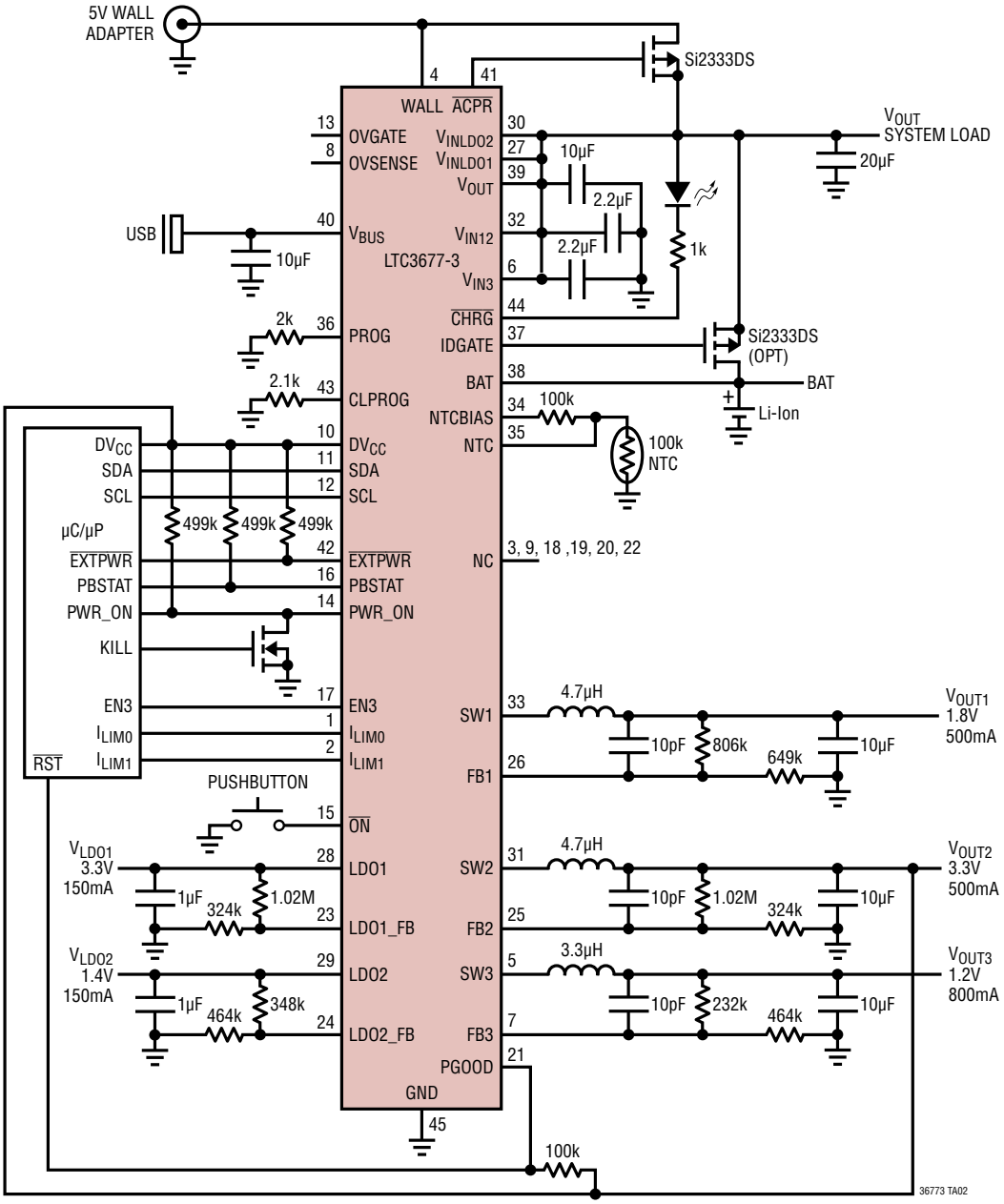
$$I_{BAT} = \frac{1.22 - 0.3W}{1.7V} = 542mA$$

Printed Circuit Board Layout

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3677-3:

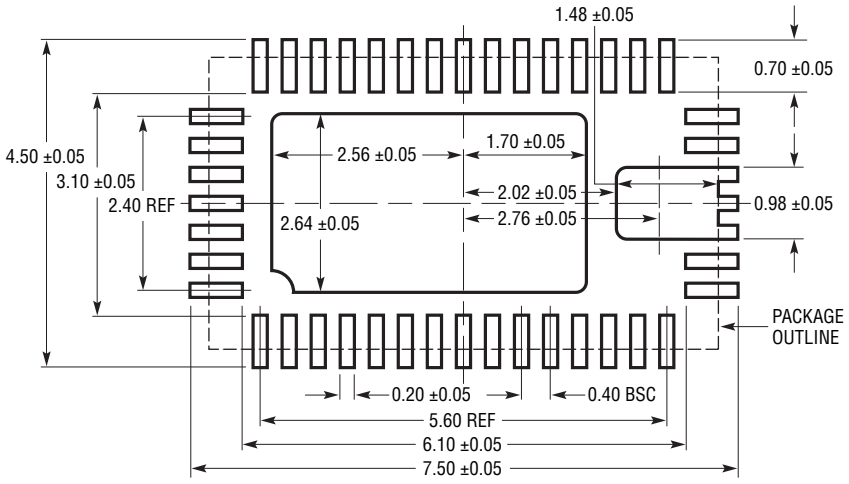
1. The exposed pad of the package (Pin 45) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. The step-down switching regulator input supply pins (V_{IN12} and V_{IN3}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It's important to minimizing inductance from these capacitors to the pins of the LTC3677-3. Connect V_{IN12} and V_{IN3} to V_{OUT} through a short low impedance trace.
3. The switching power traces connecting SW1, SW2, and SW3 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, sensitive nodes such as the feedback nodes (FBx and LDOx_FB) should be kept far away or shielded from the switching nodes or poor performance could result.
4. Connections between the step-down switching regulator inductors and their respective output capacitors should be kept as short as possible. The GND side of the output capacitors should connect directly to the thermal ground plane of the part.
5. Keep the buck feedback pin traces (FB1, FB2, and FB3) as short as possible. Minimize any parasitic capacitance between the feedback traces and any switching node (i.e., SW1, SW2, SW3, and logic signals). If necessary shield the feedback nodes with a GND trace.
6. Connections between the LTC3677-3 power path pins (V_{BUS} and V_{OUT}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part.

TYPICAL APPLICATION

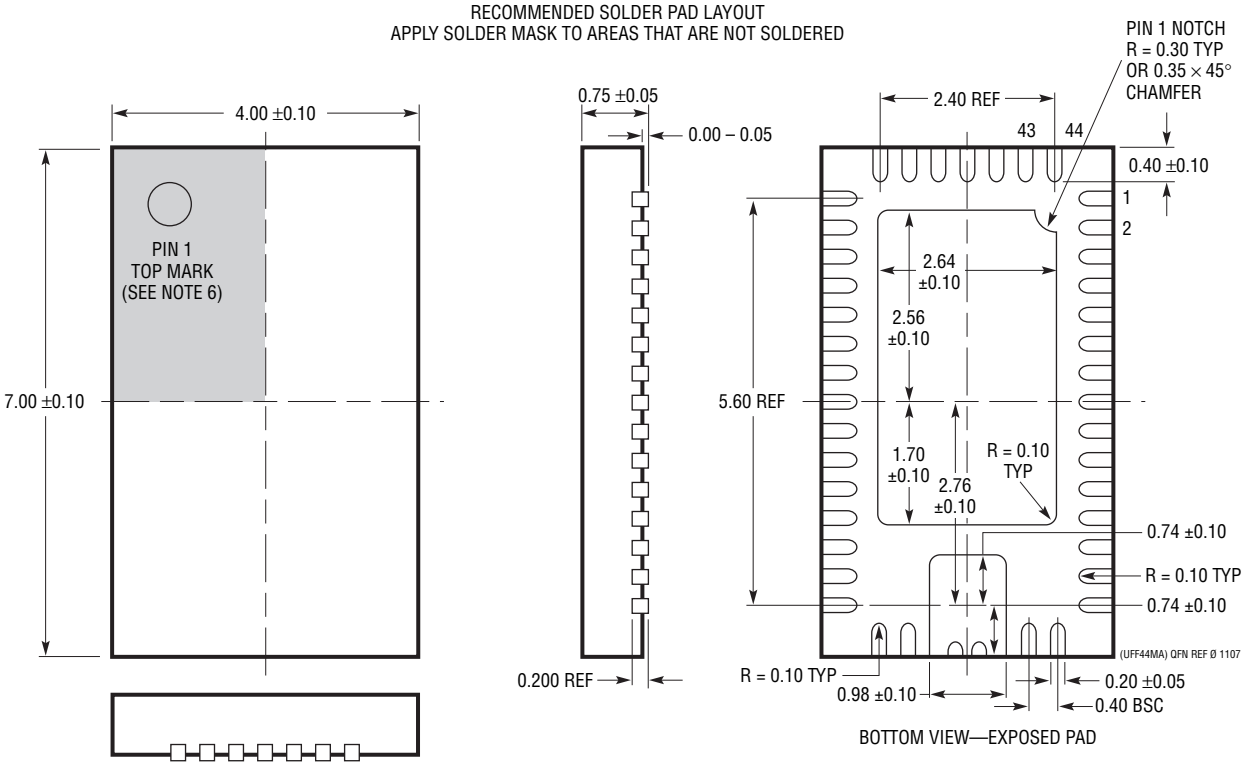


PACKAGE DESCRIPTION

UFF Package
Variation: UFFMA
44-Lead Plastic QFN (4mm × 7mm)
(Reference LTC DWG # 05-08-1762 Rev Ø)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE