Fast 2-Phase, No R_{SENSE}™, Synchronous DC/DC Controller with Tracking/Sequencing

FEATURES

- **PolyPhase® Valley Current Mode Controller**
- **Synchronizable to an External Clock with PLL**
- **Coincident or Ratiometric Tracking**
- **Sense Resistor Optional**
- **2% to 90% Duty Cycle at 200kHz**
- **$t_{ON(MIN)}$ < 100ns**
- **True Remote Sensing Differential Amplifier**
- High Efficiency at Both Light and Heavy Loads
- Power Good Output Voltage Monitor
- 0.6V ±1% Reference
- Adjustable Current Limit
- Programmable Soft-Start and Operating Frequency
- Output Overvoltage Protection
- Optional Short-Circuit Shutdown Timer
- Available in 32-Lead (5mm × 5mm) QFN and 36-Lead SSOP Packages

APPLICATIONS

- Notebook Computers
- Power Supply for DSP, ASIC, Graphic Processors

DESCRIPTION

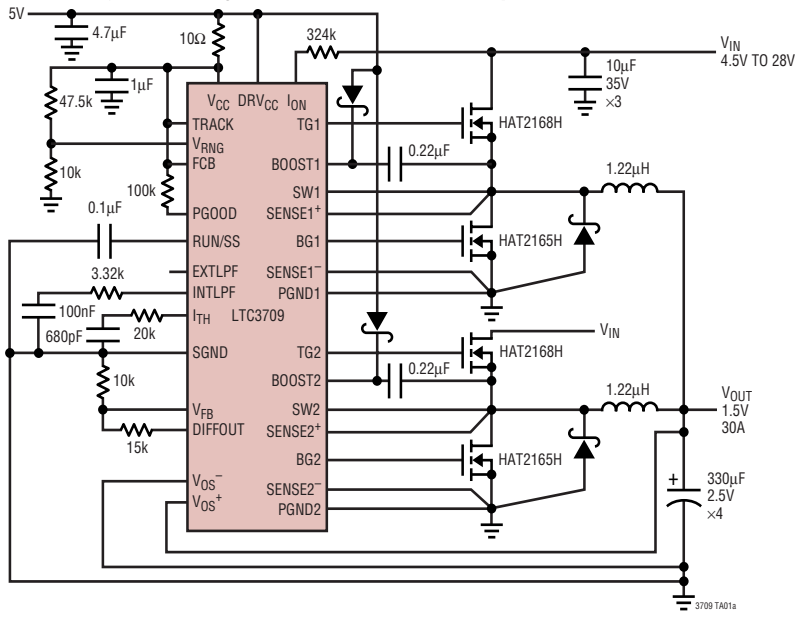
The LTC®3709 is a single output, dual phase, synchronous step-down switching regulator. The controller uses a constant on-time, valley current control architecture to deliver very low duty cycles without requiring a sense resistor. Operating frequency is selected by an external resistor and is compensated for variations in input supply voltage. An internal phase-lock loop allows the LTC3709 to be synchronized to an external clock.

A TRACK pin is provided for tracking or sequencing the output voltage among several LTC3709 chips or an LTC3709 and other DC/DC regulators. Soft-start is accomplished using an external timing capacitor.

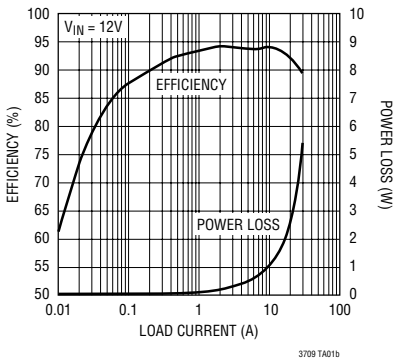
Fault protection is provided by an output overvoltage comparator and an optional short-circuit shutdown timer. The current limit level is user programmable. A wide supply range allows voltages as high as 31V to step down as low as 0.6V.

TYPICAL APPLICATION

High Efficiency Dual Phase 1.5V/30A Step-Down Converter



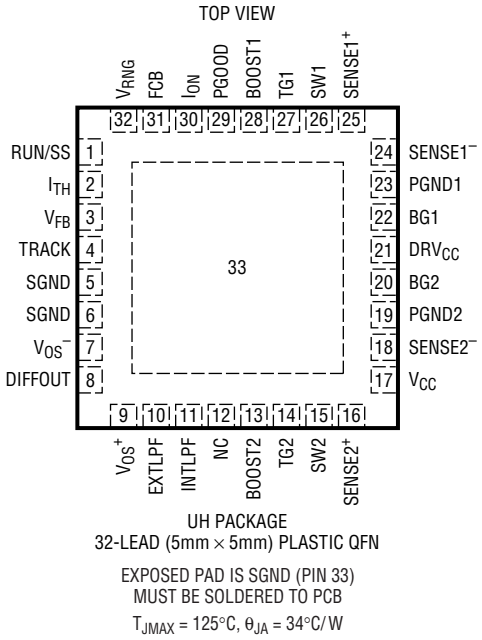
Efficiency and Power Loss



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{CC}, DRV_{CC}) ..... 7V to –0.3V
Boosted Topside Driver Supply Voltage
(BOOST1, BOOST2) ..... 37V to –0.3V
Switch Voltage (SW1, 2) ..... 31V to –1V
$SENSE1^+$, $SENSE2^+$ Voltages ..... 31V to –1V
$SENSE1^–$, $SENSE2^–$ Voltages ..... 10V to –0.3V
I_{ON} Voltage ..... 31V to –0.3V
(BOOST – SW) Voltages ..... 7V to –0.3V
RUN/SS, PGOOD Voltages ..... 7V to –0.3V
TRACK Voltage ..... 7V to –0.3V
V_{RNG} Voltage ..... V_{CC} + 0.3V to –0.3V
I_{TH} Voltage ..... 2.7V to –0.3V
V_{FB} Voltage ..... 2.7V to –0.3V
INTLPF, EXTLPF Voltages ..... 2.7V to –0.3V
V_{OS}^+, $V_{OS}^–$ Voltages ..... 7V to –0.3V
FCB Voltage ..... 7V to –0.3V
Operating Temperature Range (Note 4) .. –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range
UH Package ..... –65°C to 125°C
G Package ..... –65°C to 150°C

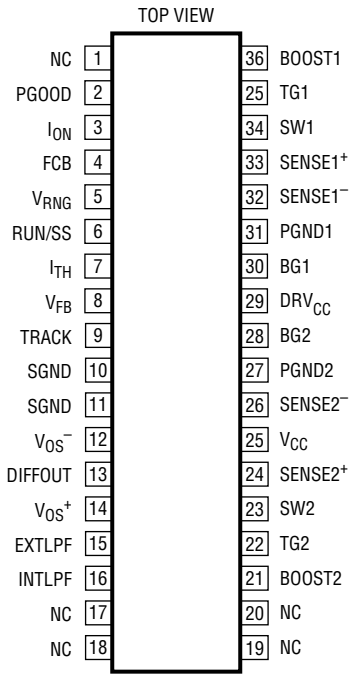
PACKAGE/ORDER INFORMATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

EXPOSED PAD IS SGND (PIN 33)
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 34°C/W



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER	UH PART MARKING
LTC3709EUH	3709

ORDER PART NUMBER	LTC3709EG

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = DRV_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
I_Q	Input DC Supply Current Normal Shutdown				 2.4 25	 3 65	 mA µA
I_{FB}	FB Pin Input Current	I_{TH} = 1.2V (Note 3)			–35	–60	nA
V_{FB}	Feedback Voltage	I_{TH} = 1.2V (Note 3)	●	0.594	0.600	0.606	V
$\Delta V_{FB(LINEREG)}$	Feedback Voltage Line Regulation	V_{CC} = 4.5V to 6.5V (Note 3)			0.02		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	I_{TH} = 0.5V to 2V (Note 3)			–0.12	–0.2	%
$g_{m(EA)}$	Error Amplifier Transconductance	I_{TH} = 1.2V (Note 3)		1.3	1.45	1.6	mS
t_{ON}	On-Time	I_{ON} = 180µA, V_{FCB} = 0V I_{ON} = 90µA, V_{FCB} = 0V		90 180	116 233	140 280	ns ns
$t_{ON(MIN)}$	Minimum On-Time	I_{ON} = 540µA			45	100	ns
$t_{OFF(MIN)}$	Minimum Off-Time	I_{ON} = 90µA			250	350	ns
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{RNG} = 1V V_{RNG} = 0V V_{RNG} = V_{CC}		124 86 177	144 101 202	166 119 234	mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold	V_{RNG} = 1V V_{RNG} = 0V V_{RNG} = V_{CC}			–60 –40 –80		mV mV mV
$\Delta V_{FB(OV)}$	Overvoltage Fault Threshold			8.5	10	12.5	%
$\Delta V_{FB(UV)}$	Undervoltage Fault Threshold			–8.5	–10	–12.5	%
$V_{RUN/SS(ON)}$	RUN Pin Start Threshold		●	0.8	1.4	2	V
$V_{RUN/SS(LE)}$	RUN Pin Latchoff Enable Threshold	RUN/SS Pin Rising			3		V
$V_{RUN/SS(LT)}$	RUN Pin Latchoff Threshold	RUN/SS Pin Falling			2.3		V
$I_{RUN/SS(C)}$	Soft-Start Charge Current			–0.5	–1.2	–3	µA
$I_{RUN/SS(D)}$	Soft-Start Discharge Current			0.8	2	4	µA
UVLO	Undervoltage Lockout	V_{CC} Falling			3.9	4.2	V
$UVLO_{(HYS)}$	Undervoltage Lockout Hysteresis	Measured at V_{CC} Pin			0.2	0.35	V
TG R_{UP}	TG Driver Pull-Up On-Resistance	TG High (Note 5)			2		Ω
TG R_{DOWN}	TG Driver Pull-Down On-Resistance	TG Low (Note 5)			1.5		Ω
BG R_{UP}	BG Driver Pull-Up On-Resistance	BG High (Note 5)			3		Ω
BG R_{DOWN}	BG Driver Pull-Down On-Resistance	BG Low (Note 5)			1.5		Ω
Tracking							
I_{TRACK}	TRACK Pin Input Current	I_{TH} = 1.2V, V_{TRACK} = 0.2V (Note 3)			–100	–150	nA
$V_{FB(TRACK)}$	Feedback Voltage at Tracking	V_{TRACK} = 0.1V, I_{TH} = 1.2V (Note 3) V_{TRACK} = 0.3V, I_{TH} = 1.2V (Note 3) V_{TRACK} = 0.5V, I_{TH} = 1.2V (Note 3)		90 290 490	100 300 500	110 310 510	mV mV mV
PGOOD Output							
ΔV_{FBH}	PGOOD Upper Threshold	V_{FB} Rising		8.5	10	12.5	%
ΔV_{FBL}	PGOOD Lower Threshold	V_{FB} Falling		–8.5	–10	–12.5	%
PG Delay	PGOOD Delay	V_{FB} Rising		100			µs
$\Delta V_{FB(HYS)}$	PGOOD Hysteresis	V_{FB} Returning			3.5		%
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 7V				±1	µA
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.2	0.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = DRV_{CC} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Lock Loop						
I_{INTPLL_SOURCE}	Internal PLL Sourcing Current			20		µA
I_{INTPLL_SINK}	Internal PLL Sinking Current			–20		µA
I_{EXTPLL_SOURCE}	External PLL Sourcing Current			20		µA
I_{EXTPLL_SINK}	External PLL Sinking Current			–20		µA
$V_{FCB(DC)}$	Forced Continuous Threshold	Measured with a DC Voltage at FCB Pin	1.9	2.1	2.3	V
$V_{FCB(AC)}$	Clock Input Threshold	Measured with a AC Pulse at FCB Pin	1	1.5	2	V
$t_{ON(PLL)1}$	t_{ON1} Modulation Range by External PLL Up Modulation Down Modulation	 I_{ON1} = 180µA, V_{EXTPLL} = 1.8V I_{ON1} = 180µA, V_{EXTPLL} = 0.6V	 186	 233 58	 80	 ns ns
$t_{ON(PLL)2}$	t_{ON2} Modulation Range by Internal PLL Up Modulation Down Modulation	 I_{ON2} = 180µA, V_{INTPLL} = 1.8V I_{ON2} = 180µA, V_{INTPLL} = 0.6V	 186	 233 58	 80	 ns ns
Differential Amplifier						
A_V	Differential Gain		0.995	1.000	1.005	V/V
V_{OS}	Input Offset Voltage	$IN^+ = IN^- = 1.2V$, I_{OUT} = 1mA, Input Referred; Gain = 1		0.5	7	mV
CM	Common Mode Input Voltage Range	I_{OUT} = 1mA	0		5	V
CMRR	Common Mode Rejection Ratio	$0V < IN^+ = IN^- < 5V$, I_{OUT} = 1mA, Input Referred	45	70		dB
I_{CL}	Output Current		10	40		mA
GBP	Gain Bandwidth Product	I_{OUT} = 1mA		2		MHz
SR	Slew Rate	R_L = 2k		5		V/µs
$V_{O(MAX)}$	Maximum High Output Voltage	I_{OUT} = 1mA	V_{CC} – 1.2	V_{CC} – 0.8		V
R_{IN}	Input Resistance	Measured at IN^+ Pin		80		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

LTC3709EUH: $T_J = T_A + (P_D \bullet 34°C/W)$

LTC3709EG: $T_J = T_A + (P_D \bullet 95°C/W)$

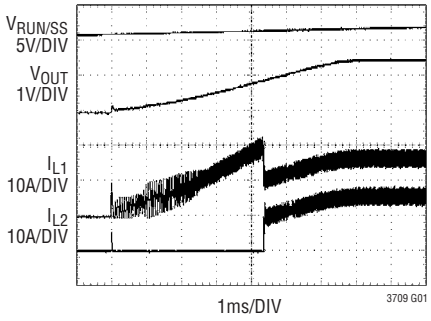
Note 3: The LTC3709 is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: The LTC3709E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

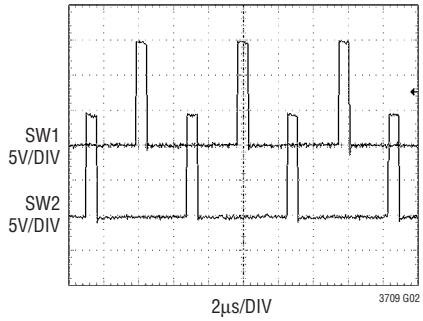
Note 5: $R_{DS(ON)}$ limit is guaranteed by design and/or correlation to static test.

TYPICAL PERFORMANCE CHARACTERISTICS

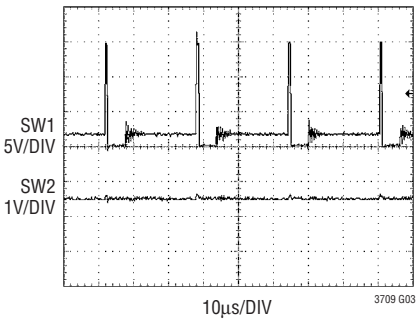
Start-Up



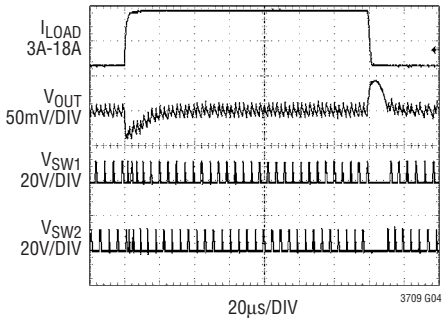
Continuous Current Mode (CCM)



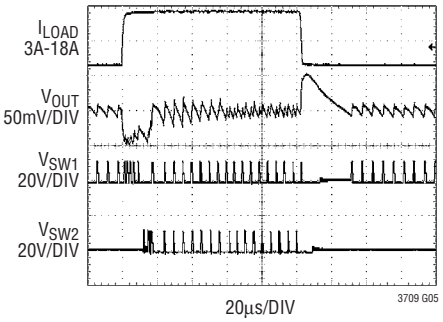
Discontinuous Current Mode (DCM)



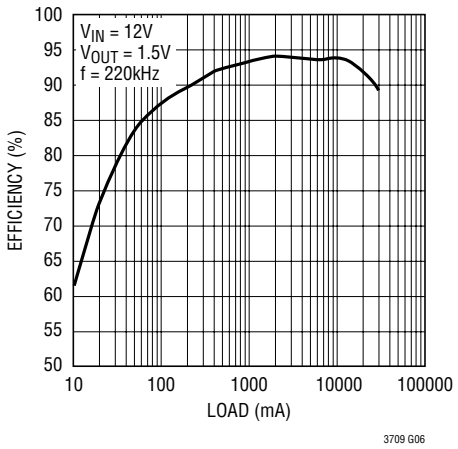
Transient Response (CCM)



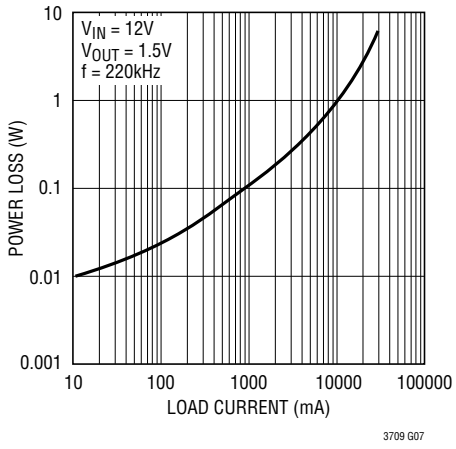
Transient Response (DCM)



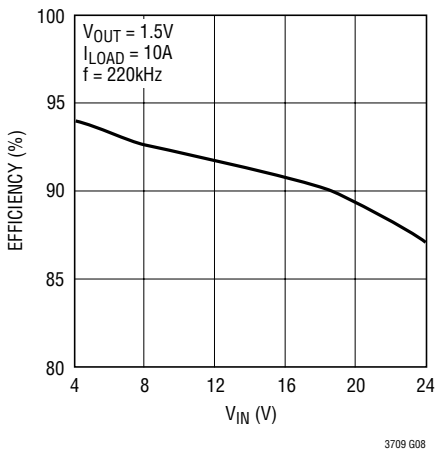
Efficiency vs Load Current



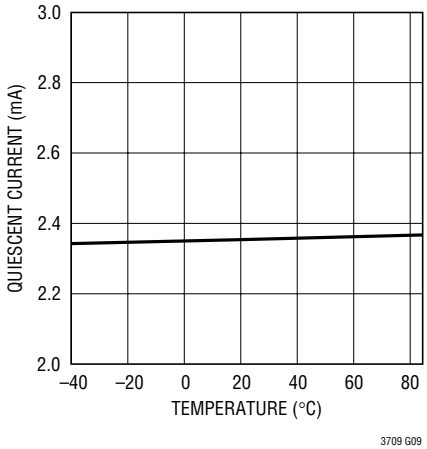
Power Loss vs Load Current



Efficiency vs V_{IN}

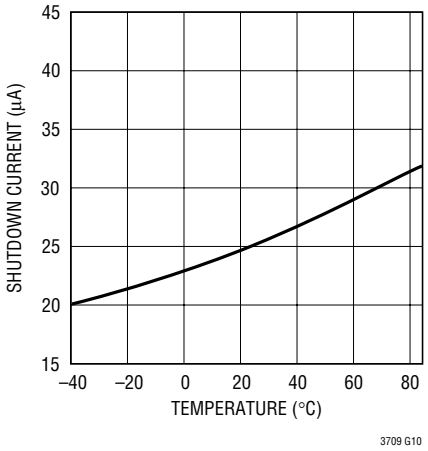


Quiescent Current at V_{CC} = 5V



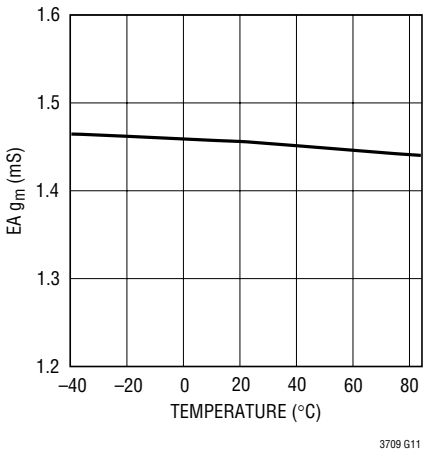
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Current at V_{CC} = 5V



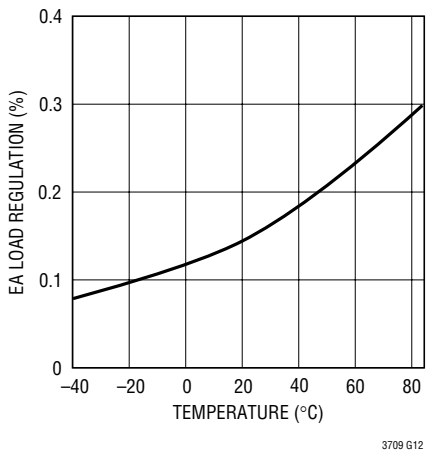
3709 G10

Error Amplifier g_m



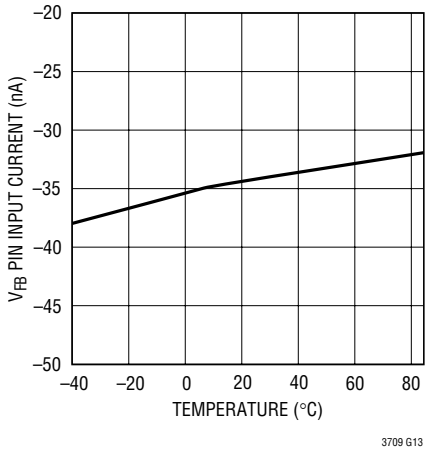
3709 G11

EA Load Regulation



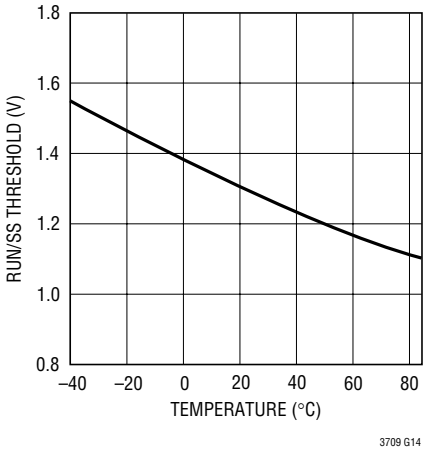
3709 G12

V_{FB} Pin Input Current



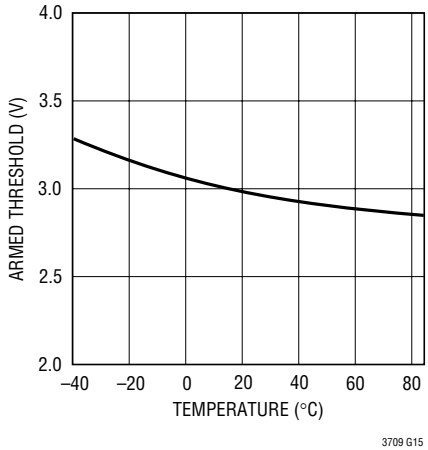
3709 G13

RUN/SS Threshold



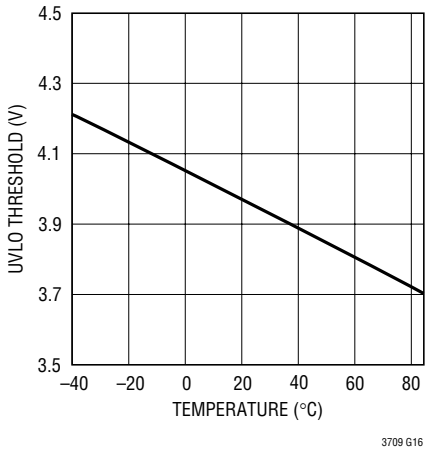
3709 G14

Armed Threshold



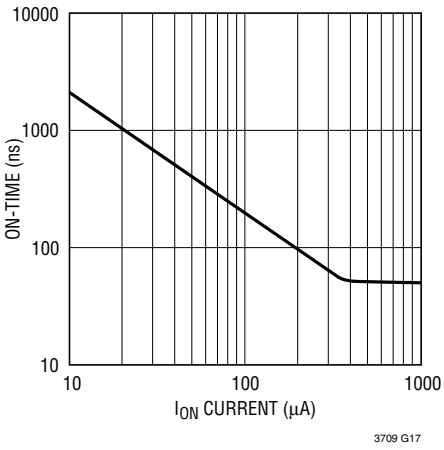
3709 G15

UVLO Threshold



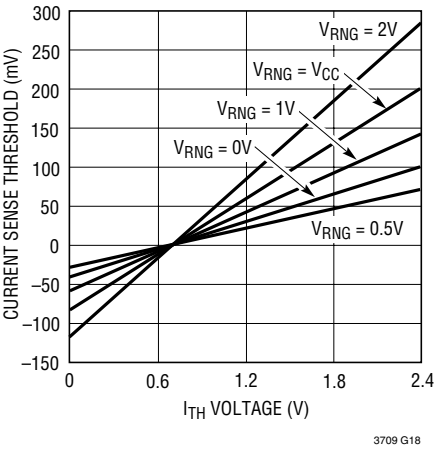
3709 G16

On-Time vs I_{ON} Current



3709 G17

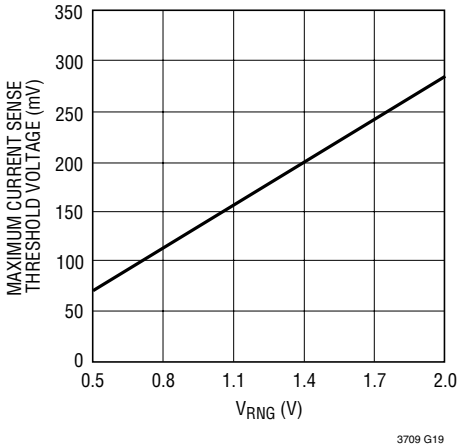
Current Sense Threshold vs I_{TH} Voltage



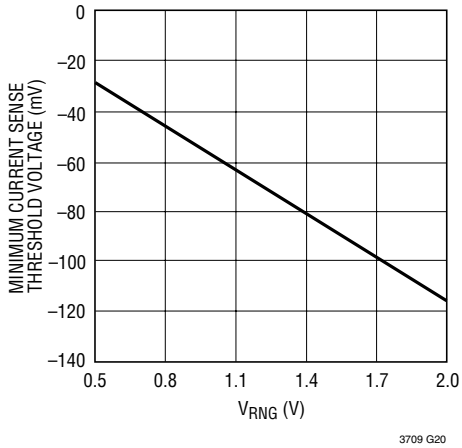
3709 G18

TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Sense Threshold Voltage vs V_{RNG}



Minimum Current Sense Threshold Voltage vs V_{RNG}



PIN FUNCTIONS (QFN/SSOP)

RUN/SS (Pin 1/Pin 6): Run Control and Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage (approximately 0.5s/µF) and the time delay for overcurrent latch-off (see Applications Information). Forcing this pin below 1.4V shuts down the device.

I_{TH} (Pin 2/Pin 7): Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

V_{FB} (Pin 3/Pin 8): Error Amplifier Feedback Input. This pin connects to the error amplifier input. It can be used to attach additional compensation components if desired.

TRACK (Pin 4/Pin 9): Tie the TRACK pin to a resistive divider connected to the output of another LTC3709 for either coincident or ratiometric output tracking (see Applications Information). To disable this feature, tie the pin to V_{CC}. *Do Not Float this pin.*

SGND (Pins 5, 6, 33/Pins 10, 11): Signal Ground. All small-signal components such as C_{SS} and compensation components should connect to this ground and eventually connect to PGND at one point. The Exposed Pad of the QFN package must be soldered to PCB ground.

V_{OS}^- (Pin 7/Pin 12): The (–) Input to the Differential Amplifer.

DIFFOUT (Pin 8/Pin 13): The Output of the Differential Amplifier.

V_{OS}^+ (Pin 9/Pin 14): The (+) Input to the Differential Amplifier.

EXTLPF (Pin 10/Pin 15): Filter Connection for the PLL. This PLL is used to synchronize the LTC3709 with an external clock.

INTLPF (Pin 11/Pin 16): Filter Connection for the PLL. This PLL is use to phase shift the second channel to the first channel by 180°.

PIN FUNCTIONS (QFN/SSOP)

NC (Pin 12/Pins 1, 17, 18, 19, 20): No Connect.

V_{CC} (Pin 17/Pin 25): Main Input Supply. Decouple this pin to SGND with an RC filter (1Ω, 0.1μF).

DRV_{CC} (Pin 21/Pin 29): Driver Supply. Provides supply to the driver for the bottom gate. Also used for charging the bootstrap capacitor.

BG1, BG2 (Pins 22, 20/Pins 30, 28): Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and DRV_{CC}.

PGND1, PGND2 (Pins 23, 19/Pins 31, 27): Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of C_{DRVCC} and the (–) terminal of C_{IN}.

$SENSE1^-$, $SENSE2^-$ (Pins 24, 18/Pins 32, 26): Current Sense Comparator Input. The (–) input to the current comparator is used to accurately Kelvin sense the bottom side of the sense resistor or MOSFET.

$SENSE1^+$, $SENSE2^+$ (Pins 25, 16/Pins 33, 24): Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the SW node unless using a sense resistor (see Applications Information).

SW1, SW2 (Pins 26, 15/Pins 34, 23): Switch Node. The (–) terminal of the bootstrap capacitor C_B connects here. This pin swings from a Schottky diode voltage drop below ground up to V_{IN}.

TG1, TG2 (Pins 27, 14/Pins 35, 22): Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to DRV_{CC} superimposed on the switch node voltage SW.

BOOST1, BOOST2 (Pins 28, 13/Pins 36, 21): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor C_B connects here. This pin swings from a diode voltage drop below DRV_{CC} up to V_{IN} + DRV_{CC}.

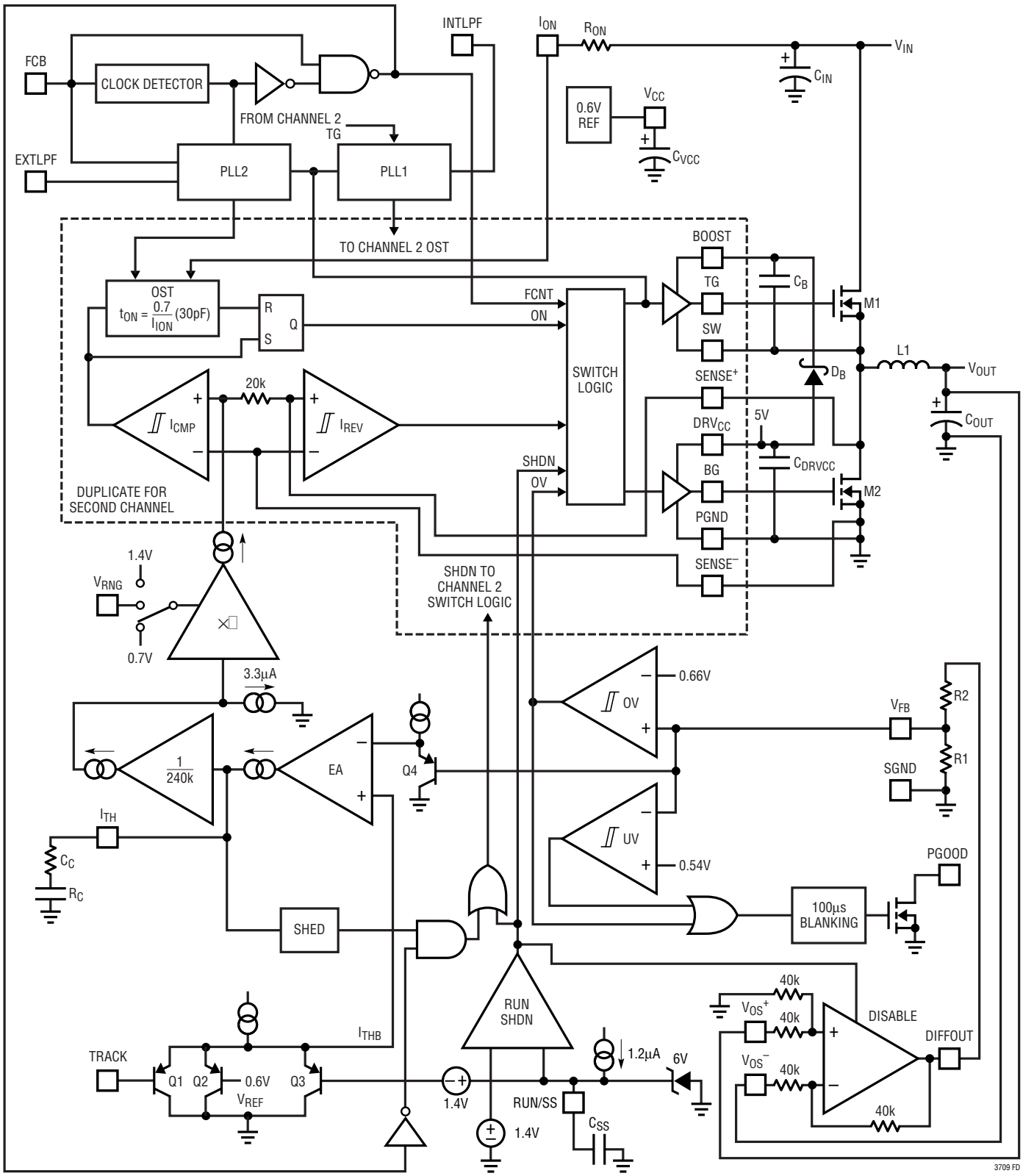
PGOOD (Pin 29/Pin 2): Power Good Output. Open-drain logic output that is pulled to ground when output voltage is not within ±10% of the regulation point. The output voltage must be out of regulation for at least 100μs before the power good output is pulled to ground.

I_{ON} (Pin 30/Pin 3): On-Time Current Input. Tie a resistor from V_{IN} to this pin to set the one-shot timer current and thereby set the switching frequency.

FCB (Pin 31/Pin 4): Forced Continuous and External Clock Input. Tie this pin to ground to force continuous synchronous operation or to V_{CC} to enable discontinuous mode operation at light load. Feeding an external clock signal into this pin will synchronize the LTC3709 to the external clock and enable forced continuous mode.

V_{RNG} (Pin 32/Pin 5): Sense Voltage Range Input. The voltage at this pin is ten times the nominal sense voltage at maximum output current and can be programmed from 0.5V to 2V. The sense voltage defaults to 70mV when this pin is tied to ground, 140mV when tied to V_{CC}.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

MAIN CONTROL LOOP

The LTC3709 is a constant on-time, current mode step-down controller with two channels operating 180 degrees out of phase. In normal operation, each top MOSFET is turned on for a fixed interval determined by its own one-shot timer OST. When the top MOSFET is turned off, the bottom MOSFET is turned on until the current comparator I_{CMP} trips, restarting the one-shot timer and repeating the cycle. The trip level of the current comparator is set by the I_{TH} voltage, which is the output of error amplifier EA. Inductor current is determined by sensing the voltage between the $SENSE^-$ and $SENSE^+$ pins using either the bottom MOSFET on-resistance or a separate sense resistor. At light load, the inductor current can drop to zero and become negative. This is detected by current reversal comparator I_{REV}, which then shuts off the bottom MOSFET, resulting in discontinuous operation. Both switches will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level (0.8V) to initiate another cycle. Discontinuous mode operation is disabled when the FCB pin is tied to ground, forcing continuous synchronous operation.

The main control loop is shut down by pulling the RUN/SS pin low, turning off both top MOSFET and bottom MOSFET. Releasing the pin allows an internal 1.2μA current source to charge an external soft-start capacitor C_{SS}. When this voltage reaches 1.4V, the LTC3709 turns on and begins operating with a clamp on the noninverting input of the error amplifier. This input is also the reference input of the error amplifier. As the voltage on RUN/SS continues to rise, the voltage on the reference input also rises at the same rate, effectively controlling output voltage slew rate.

Operating Frequency

The operating frequency is determined implicitly by the top MOSFET on time and the duty cycle required to maintain regulation. The one-shot timer generates an on-time that is proportional to the ideal duty cycle, thus holding the frequency approximately constant with changes in V_{IN}. The nominal frequency can be adjusted with an external resistor R_{ON}.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In this condition, the top MOSFET is turned off and the bottom MOSFET is turned on and held on until the condition is cleared.

Power Good (PGOOD) Pin

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. In addition, the output feedback voltage must be out of this window for a continuous duration of at least 100μs before the PGOOD is pulled low. This is to prevent any glitch on the feedback voltage from creating a false power bad signal. The PGOOD will indicate a good power immediately when the feedback voltage is in regulation.

Short-Circuit Detection and Protection

After the controller has been started and been given adequate time to charge the output capacitor, the RUN/SS capacitor is used in a short-circuit time-out circuit. If the output voltage falls to less than 67% of its nominal output voltage, the RUN/SS capacitor begins discharging on the assumption that the output is in an overcurrent and/or short-circuit condition. If the condition lasts for a long enough period, as determined by the size of the RUN/SS capacitor, the controller will be shut down until the RUN/SS pin voltage is recycled. This built-in latch off can be overridden by providing a >5μA pull-up at a compliance of 5V to the RUN/SS pin. This current shortens the soft-start period but also prevents net discharge of the RUN/SS capacitor during an overcurrent and/or short-circuit condition.

DRV_{CC}

Power for the top and bottom MOSFET drivers and most of the internal controller circuitry is derived from the DRV_{CC} pin. The top MOSFET driver is powered from a floating bootstrap capacitor C_B. This capacitor is normally recharged from DRV_{CC} through an external Schottky diode D_B when the top MOSFET is turned off.

OPERATION (Refer to Functional Diagram)

Differential Amplifier

This amplifier provides true differential output voltage sensing. Sensing both V_{OUT}^+ and V_{OUT}^- benefits regulation in high current applications and/or applications having electrical interconnection losses. This sensing also isolates the physical power ground from the physical signal ground, preventing the possibility of troublesome "ground loops" on the PC layout and preventing voltage errors caused by board-to-board interconnects.

Dual Phase Operation

An internal phase-lock loop (PLL1) ensures that channel 2 operates exactly at the same frequency as channel 1 and is also phase shifted by 180°, enabling the LTC3709 to operate optimally as a dual phase controller. The loop filter connected to the INTLPF pin provides stability to the PLL. For external clock synchronization, a second PLL (PLL2) is incorporated into the LTC3709. PLL2 will adjust the on-time of channel 1 until its frequency is the same as the external clock. When locked, the PLL2 aligns the turn on of the top MOSFET of channel 1 to the rising edge of the external clock. Compensation for PLL2 is through the EXTLPF pin.

The loop filter components tied to the INTLPF and EXTLPF pins are used to compensate the internal PPL and external PLL respectively. The typical value ranges are:

INTLPF: R_{IPLL} = 2kΩ to 10kΩ, C_{IPLL} = 10nF to 100nF
EXTLP: $R_{EPLL} \leq$ 1kΩ, C_{EPLL}= 10nF to 100nF

For noise suppression, a capacitor with a value of 1nF or less should be placed from INTLPF to ground and EXTLPF to ground.

Second Channel Shutdown During Light Loads

When FCB is tied to V_{CC}, discontinuous mode is selected. In this mode, no reverse current is allowed. The second channel is off when I_{TH} is less than 0.8V for better efficiency. When FCB is tied to ground, forced continuous mode is selected, both channels are on and reversed current is allowed.

APPLICATIONS INFORMATION

The basic LTC3709 application circuit is shown on the first page of this data sheet. External component selection is primarily determined by the maximum load current and begins with the selection of the power MOSFET switches and/or sense resistor. The inductor current is determined by the $R_{DS(ON)}$ of the synchronous MOSFET while the user has the option to use a sense resistor for a more accurate current limiting. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its ability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple specification.

Maximum Sense Voltage and V_{RNG} Pin

Inductor current is determined by measuring the voltage across the $R_{DS(ON)}$ of the synchronous MOSFET or through a sense resistance that appears between the $SENSE^-$ and the $SENSE^+$ pins. The maximum sense voltage is set by the voltage applied to the V_{RNG} pin and is equal to approximately V_{RNG}/7.5. The current mode control loop will not allow the inductor current valleys to exceed V_{RNG}/(7.5 • R_{SENSE}). In practice, one should allow some margin for variations in the LTC3709 and external component values. A good guide for selecting the sense resistance for each channel is:

$$R_{SENSE} = \frac{2 \bullet V_{RNG}}{10 \bullet I_{OUT(MAX)}}$$

The voltage of the V_{RNG} pin can be set using an external resistive divider from V_{CC} between 0.5V and 2V resulting in nominal sense voltages of 50mV to 200mV. Additionally, the V_{RNG} pin can be tied to ground or V_{CC}, in which case the nominal sense voltage defaults to 70mV or 140mV, respectively. The maximum allowed sense voltage is about 1.3 times this nominal value.

APPLICATIONS INFORMATION

Connecting the SENSE+ and SENSE– Pins

The LTC3709 provides the user with an optional method to sense current through a sense resistor instead of using the $R_{DS(ON)}$ of the synchronous MOSFET. When using a sense resistor, it is placed between the source of the synchronous MOSFET and ground. To measure the voltage across this resistor, connect the SENSE+ pin to the source end of the resistor and the SENSE– pin to the other end of the resistor. The SENSE+ and SENSE– pin connections provide the Kelvin connections, ensuring accurate voltage measurement across the resistor. Using a sense resistor provides a well-defined current limit, but adds cost and reduces efficiency. Alternatively, one can use the synchronous MOSFET as the current sense element by simply connecting the SENSE+ pin to the switch node SW and the SENSE– pin to the source of the synchronous MOSFET, eliminating the sense resistor. This improves efficiency, but one must carefully choose the MOSFET on-resistance as discussed in the Power MOSFET Selection section.

Power MOSFET Selection

The LTC3709 requires four external N-channel power MOSFETs, two for the top (main) switches and two for the bottom (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, threshold voltage $V_{(GS)TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The gate drive voltage is set by the 5V DRV_{CC} supply. Consequently, logic-level threshold MOSFETs must be used in LTC3709 applications. If the driver's voltage is expected to drop below 5V, then sub-logic level threshold MOSFETs should be used.

When the bottom MOSFETs are used as the current sense elements, particular attention must be paid to their on-resistance. MOSFET on-resistance is typically specified with a maximum value $R_{DS(ON)(MAX)}$ at 25°C. In this case additional margin is required to accommodate the rise in MOSFET on-resistance with temperature:

$$R_{DS(ON)(MAX)} = \frac{R_{SENSE}}{\rho_T}$$

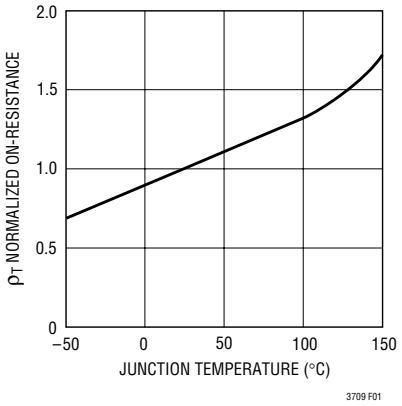


Figure 1. $R_{DS(ON)}$ vs Temperature

The ρ_T term is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C. Junction-to-case temperature is about 20°C in most applications. For a maximum junction temperature of 100°C, using a value $\rho_{100°C} = 1.3$ is reasonable (Figure 1).

The power dissipated by the top and bottom MOSFETs strongly depends upon their respective duty cycles and the load current. When the LTC3709 is operating in continuous mode, the duty cycles for the MOSFETs are:

$$D_{TOP} = \frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The maximum power dissipation in the MOSFETs per channel is:

$$P_{TOP} = D_{TOP} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet \rho_{T(TOP)} \bullet R_{DS(ON)(MAX)} + (0.5) \bullet V_{IN}^2 \bullet \left(\frac{I_{OUT}}{2}\right) \bullet C_{RSS} \bullet f \bullet R_{DS(ON)\_DRV} \left(\frac{1}{\left(DRV_{CC} - V_{GS(TH)}\right)} + \frac{1}{V_{GS(TH)}}\right)$$

$$P_{BOT} = D_{BOT} \bullet \left(\frac{I_{OUT(MAX)}}{2}\right)^2 \bullet \rho_{T(BOT)} \bullet R_{DS(ON)(MAX)}$$

APPLICATIONS INFORMATION

Both top and bottom MOSFETs have I^2R losses and the top MOSFET includes an additional term for transition losses, which are the largest at maximum input voltages. The bottom MOSFET losses are the greatest when the bottom duty cycle is near 100%, during a short circuit or at high input voltage. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than 1/3 of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' "on" resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low "on" resistance with significantly reduced input capacitance for the main switch application in switching regulators.

Operating Frequency

The choice of operating frequency is a tradeoff between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of LTC3709 applications is determined implicitly by the one-shot timer that controls the on time, t_{ON}, of the top MOSFET switch. The on-time is set by the current into the I_{ON} pin according to:

$$t_{ON} = \frac{0.7}{I_{ION}}(30pF)$$

Tying a resistor from V_{IN} to the I_{ON} pin yields an on-time inversely proportional to V_{IN}. For a down converter, this results in approximately constant frequency operation as the input supply varies:

$$f = \frac{V_{OUT}}{0.7 \bullet R_{ON}(30pF)}(\text{Per Phase})$$

PLL and Frequency Synchronization

In the LTC3709, there are two on-chip phase-lock loops (PLLs). One of the PLLs is used to achieve frequency locking and phase separation between the two channels while the second PLL is for locking onto an external clock. Since the LTC3709 is a constant on-time architecture, the error signal generated by the phase detector of the PLL is used to vary the on-time to achieve frequency locking and 180° phase separation.

The synchronization is set up in a "daisy chain" manner whereby channel 2's on-time will be varied with respect to channel 1. If an external clock is present, then channel 1's on-time will be varied and channel 2 will follow suit. Both PLLs are set up with the same capture range and the frequency range that the LTC3709 can be externally synchronized to is between $2 \bullet f_C$ and $0.5 \bullet f_C$, where f_C is the initial frequency setting of the two channels. It is advisable to set initial frequency as close to external frequency as possible.

A limitation of both PLLs is when the on-time is close to the minimum (100ns). In this situation, the PLL will not be able to synchronize up in frequency.

To ensure proper operation of the internal phase-lock loop when no external clock is applied to the FCB pin, the INTLPF pin may need to be pulled down while the output voltage is ramping up. One way to do this is to connect the anode of a silicon diode to the INTLPF pin and its cathode to the PGOOD pin and connect a pull-up resistor between the PGOOD pin and V_{CC}. Refer to Figure 9 for an example.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency.

APPLICATIONS INFORMATION

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}/2$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the inductors must be selected (based on the RMS saturation current ratings). A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Toko and Panasonic.

Schottky Diode Selection

The Schottky diodes conduct during the dead time between the conduction of the power MOSFET switches. It is intended to prevent the body diode of the bottom MOSFET from turning on and storing charge during the dead time, which causes a modest (about 1%) efficiency loss. The diode can be rated for about one-half to one-fifth of the full load current since it is on for only a fraction of the duty cycle. In order for the diode to be effective, the inductance between the diode and the bottom MOSFET must be as small as possible, mandating that these components be placed adjacently. The diode can be omitted if the efficiency loss is tolerable.

C_{IN} and C_{OUT} Selection

In continuous mode, the current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 2 shows the input capacitor ripple current for a 2-phase configuration with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the input voltage is twice the output voltage.

In the Figure 2 graph, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{4} \text{ where } k = 1, 2$$

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

It is important to note that the efficiency loss is proportional to the input RMS current squared and therefore a 2-stage implementation results in 75% less power loss when compared to a single phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also reduced by the reduction of the input ripple current in a 2-phase system. The required amount of input capacitance is further reduced by the factor 2 due to the effective increase in the frequency of the current pulses.

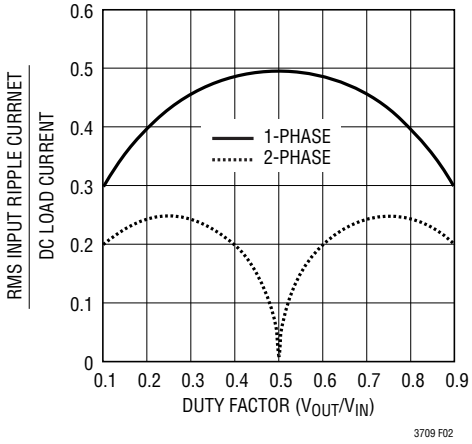


Figure 2. RMS Input Current Comparison

APPLICATIONS INFORMATION

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications providing that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. High performance through-hole capacitors may also be used, but an additional ceramic capacitor in parallel is recommended to reduce the effect of their lead inductance.

Top MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. This capacitor is charged through diode D_B from DRV_{CC} when the switch node is low. Note that the average voltage across C_B is approximately DRV_{CC}. When the top MOSFET turns on, the switch node rises to V_{IN} and the BOOST pin rises to approximately V_{IN} + DRV_{CC}. The boost capacitor needs to store about 100 times the gate charge required by the top MOSFET. In most applications 0.1µF to 0.47µF is adequate.

Discontinuous Mode Operation and FCB Pin

The FCB pin determines whether the bottom MOSFET remains on when current reverses in the inductor. Tying this pin to V_{CC} enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. The load current at which inductor current reverses and discontinuous operation begins depends on the amplitude of the inductor ripple current. The ripple current depends on the choice of inductor value and operating frequency as well as the input and output voltages.

Tying the FCB pin to ground forces continuous synchronous operation, allowing current to reverse at light loads and maintaining high frequency operation.

Besides providing a logic input to force continuous operation, the FCB pin acts as the input for external clock synchronization. Upon detecting a TTL level clock and the frequency is higher than the minimum allowable, channel 1 will lock on to this external clock. This will be followed by channel 2 (see PLL and Frequency Synchronization). The LTC3709 will be forced to operate in forced continuous mode in this situation.

Fault Conditions: Current Limit

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the LTC3709, the maximum sense voltage is controlled by the voltage on the V_{RNG} pin. With valley current control, the maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current. The corresponding output current limit is:

$$I_{LIMIT} = \left(\frac{V_{SNS(MAX)}}{R_{DS(ON)} \bullet \rho_T} + \frac{1}{2} \bullet \Delta I_L \right) \bullet 2$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions which cause the largest power loss in the converter. Note that it is important to check for

APPLICATIONS INFORMATION

self-consistency between the assumed junction temperature and the resulting value of I_{LIMIT}, which heats the junction.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

For a more accurate current limiting, a sense resistor can be used. Sense resistors in the 1W power range are easily available with 5%, 2% or 1% tolerance. The temperature coefficient of these resistors are very low, ranging from ±250ppm/°C to ±75ppm/°C. In this case, the denominator in the above equation can simply be replaced by the R_{SENSE} value.

Minimum Off-Time and Dropout Operation

The minimum off-time $t_{OFF(MIN)}$ is the smallest amount of time that the LTC3709 is capable of turning on the bottom MOSFET, tripping the current comparator and turning the MOSFET back off. This time is generally about 250ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation in order to maintain the duty cycle at its limit. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \frac{1}{1 - t_{OFF(MIN)} \bullet f}$$

A plot of maximum duty cycle vs frequency is shown in Figure 3.

Soft-Start and Latchoff with the RUN/SS Pin

The RUN/SS pin provides a means to shut down the LTC3709 as well as a timer for soft-start and overcurrent latchoff.

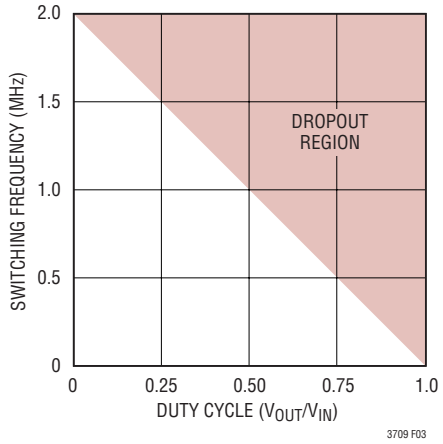


Figure 3. Maximum Switching Frequency vs Duty Cycle

Pulling the RUN/SS pin below 1.4V puts the LTC3709 into a low quiescent current shutdown ($I_Q < 30\mu A$). Releasing the pin allows an internal 1.2µA internal current source to charge the external capacitor C_{SS}. If RUN/SS has been pulled all the way to ground, there is a delay before starting of about:

$$t_{DELAY} = \frac{1.4V}{1.2\mu A} \bullet C_{SS} = \left(1.2s/\mu F\right) C_{SS}$$

When the RUN/SS voltage reaches the ON threshold (typically 1.4V), the LTC3709 begins operating with a clamp on EA's reference voltage. The clamp level is one ON threshold voltage below RUN/SS. As the voltage on RUN/SS continues to rise, EA's reference is raised at the same rate, achieving monotonic output voltage soft-start (Figure 4).

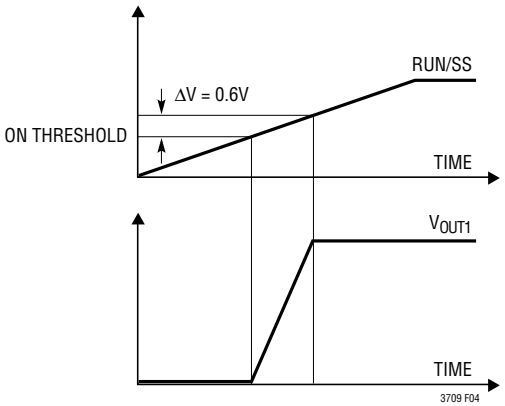


Figure 4. Monotonic Soft-Start Waveforms

APPLICATIONS INFORMATION

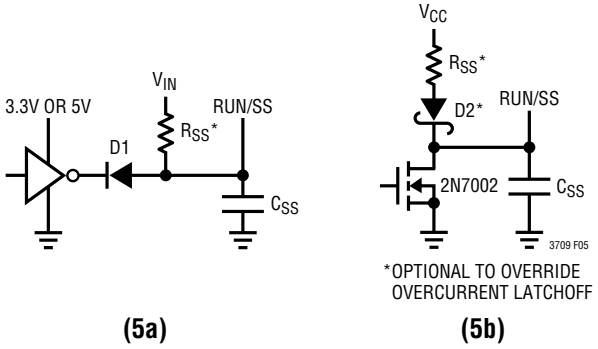


Figure 5. RUN/SS Pin Interfacing with Latchoff Defeated

When RUN/SS rises 0.6V above the ON threshold, the reference clamp is invalidated and the internal precision reference takes over.

After the controller has been started and given adequate time to charge the output capacitor, C_{SS} is used as a short-circuit timer. After the RUN/SS pin charges above 3V, and if the output voltage falls below 67% of its regulated value, then a short-circuit fault is assumed. A 2μA current then begins discharging C_{SS}. If the fault condition persists until the RUN/SS pin drops to 2.5V, then the controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

The overcurrent protection timer requires that the soft-start timing capacitor C_{SS} be made large enough to guarantee that the output is in regulation by the time C_{SS} has reached the 3V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum soft-start capacitor can be estimated from:

$$C_{SS} > C_{OUT}\, V_{OUT}\, R_{SENSE}\, (10^{-4}\ [F/V_S])$$

Overcurrent latchoff operation is not always needed or desired and can prove annoying during troubleshooting. The feature can be overridden by adding a pull-up current of >5μA to the RUN/SS pin. The additional current prevents the discharge of C_{SS} during a fault and also shortens the soft-start period. Using a resistor to V_{IN} as shown in Figure 5 is simple, but slightly increases shutdown current. Any pull-up network must be able to pull RUN/SS above the 3V threshold that arms the latchoff circuit and overcome the 2μA maximum discharge current.

Output Voltage Tracking

The feedback voltage, V_{FB}, will follow the TRACK pin voltage when the TRACK pin voltage is less than the reference voltage, V_{REF} (0.6V). When the TRACK pin voltage is greater than V_{REF}, the feedback voltage will servo to V_{REF}. When selecting components for the TRACK pin, ensure the final steady-state voltage on the TRACK pin is greater than V_{REF} at the end of the tracking interval.

The LTC3709 allows the user to set up start-up sequencing among different supplies in either coincident tracking or ratiometric tracking as shown in Figure 6. To implement the coincident tracking, connect an extra resistor divider

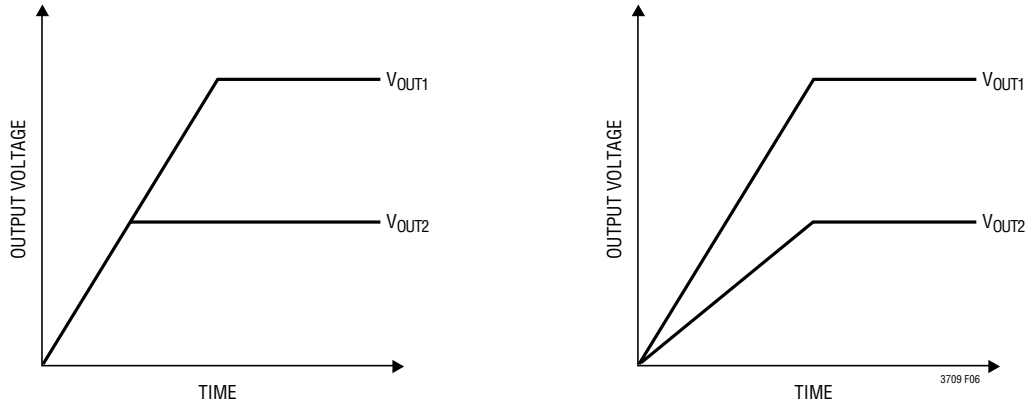


Figure 6. Two Different Forms of Output Voltage Sequencing

APPLICATIONS INFORMATION

to the output of supply 1. This resistor divider is selected to be the same as the divider across supply 2's output. The TRACK pin of supply 2 is connected to this extra resistor divider. For the ratiometric tracking, simply connect the TRACK pin of supply 2 to the V_{FB} pin of supply 1. Figure 7 shows this implementation. Note that in the coincident tracking, **output voltage of supply 1 has to be set higher than output voltage of supply 2**.

Note that since the shutdown trip point varies from part to part, the "slave" part's RUN/SS pin will need to be connected to V_{CC}. This eliminates the possibility that different LTC3709s may shut down at different times.

If output sequencing is not needed, connect the TRACK pins to V_{CC}. *Do Not Float these pins.*

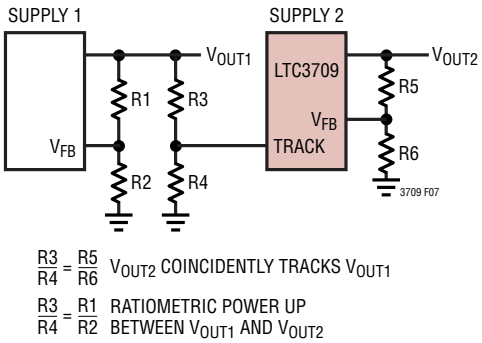


Figure 7. Setup for Coincident and Ratiometric Tracking

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement.

Although all dissipative elements in the circuit produce losses, four main sources account for most of the losses in LTC3709 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, inductor and PC board traces and cause the efficiency to drop at high output currents. In continuous mode the average output current flows through L, but is chopped between the top and bottom MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and the board traces to obtain the DC I^2R loss. For example, if $R_{DS(ON)} = 0.01\Omega$ and $R_L = 0.005\Omega$, the loss will range from 0.1% up to 10% as the output current varies from 1A to 10A for a 1.5V output.

2. Transition loss. This loss arises from the brief amount of time the top MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

$$\text{Transition Loss} \approx (0.5) \bullet V_{IN}^2 \bullet I_{OUT} \bullet C_{RSS} \bullet f \bullet R_{DS(ON)\_DRV}\left(\frac{1}{DRV_{CC} - V_{GS(TH)}} + \frac{1}{V_{GS(TH)}}\right)$$

3. Gate driver supply current. The driver current supplies the gate charge Q_G required to switch the power MOSFETs. This current is typically much larger than the control circuit current. In continuous mode operation:

$$I_{GATECHG} = f\,(Q_{g(TOP)} + Q_{g(BOT)})$$

4. C_{IN} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator. It must have a very low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries. Other losses, including C_{OUT} ESR loss, Schottky conduction loss during dead time and inductor core loss generally account for less than 2% additional loss.

When making any adjustments to improve efficiency, the final arbiter is the total input current for the regulator at your operating point. If you make a change and the input current decreases, then you improved the efficiency. If there is no change in input current, then there is no change in efficiency.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount

APPLICATIONS INFORMATION

equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problems. The I_{TH} pin external components shown in Figure 9 will provide adequate compensation for most applications. For a detailed explanation of switching control loop theory see Application Note 76.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 7V to 28V (15V nominal), V_{OUT} = 2.5V, $I_{OUT(MAX)}$ = 20A, f = 250kHz. First, calculate the timing resistor:

$$R_{ON} = \frac{2.5V}{(0.7V)(250kHz)(30pF)} = 476k$$

and choose the inductor for about 40% ripple current at the maximum V_{IN}. Maximum output current for each channel is 10A:

$$L = \frac{2.5V}{(250kHz)(0.4)(10A)}\left(1-\frac{2.5V}{28V}\right) = 2.3\mu H$$

Selecting a standard value of 1.8µH results in a maximum ripple current of:

$$\Delta I_L = \frac{2.5V}{(250kHz)(1.8\mu H)}\left(1-\frac{2.5V}{28V}\right) = 5.1A$$

Next, choose the synchronous MOSFET switch. Choosing a Si4874 ($R_{DS(ON)}$ = 0.0083Ω (NOM) 0.010Ω (MAX), q_{JA} = 40°C/W) yields a nominal sense voltage of:

$V_{SNS(NOM)}$ = (10A)(1.3)(0.0083Ω) = 108mV

Tying V_{RNG} to 1.1V will set the current sense voltage range for a nominal value of 110mV with current limit occurring at 146mV. To check if the current limit is acceptable, assume a junction temperature of about 80°C above a 70°C ambient with $\rho_{150°C}$ = 1.5:

$$I_{LIMIT} \geq \left(\frac{146mV}{(1.5)(0.010\Omega)} + \frac{1}{2}(5.1A)\right) \bullet 2 = 24A$$

and double check the assumed T_J in the MOSFET:

$$P_{BOT} = \frac{28V-2.5V}{28V}\left(\frac{24A}{2}\right)^2(1.5)(0.010\Omega) = 1.97W$$

T_J = 70°C + (1.97W)(40°C/W) = 149°C

Because the top MOSFET is on for such a short time, an Si4884 $R_{DS(ON)(MAX)}$ = 0.0165Ω, C_{RSS} = 100pF, θ_{JA} = 40°C/W will be sufficient. Checking its power dissipation at current limit with $\rho_{100°C}$ = 1.4:

$$P_{TOP} = \frac{2.5V}{28V}\left(\frac{24A}{2}\right)^2(1.4)(0.0165\Omega) + (1.7)(28V)^2(12A)(100pF)(250kHz)$$
$$= 0.30W + 0.40W = 0.7W$$

T_J = 70°C + (0.7W)(40°C/W) = 98°C

The junction temperatures will be significantly less at nominal current, but this analysis shows that careful attention to heat sinking will be necessary in this circuit.

C_{IN} is chosen for an RMS current rating of about 10A at 85°C. The output capacitors are chosen for a low ESR of 0.013Ω to minimize output voltage changes due to inductor ripple current and load steps. The ripple voltage will be only:

$$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)}\,(ESR)$$
$$= (5.1A)\,(0.013\Omega) = 66mV$$

However, a 0A to 10A load step will cause an output change of up to:

$$\Delta V_{OUT(STEP)} = \Delta I_{LOAD}\,(ESR) = (10A)\,(0.013\Omega) = 130mV$$

An optional 22µF ceramic output capacitor is included to minimize the effect of ESL in the output ripple. The complete circuit is shown in Figure 9.

APPLICATIONS INFORMATION

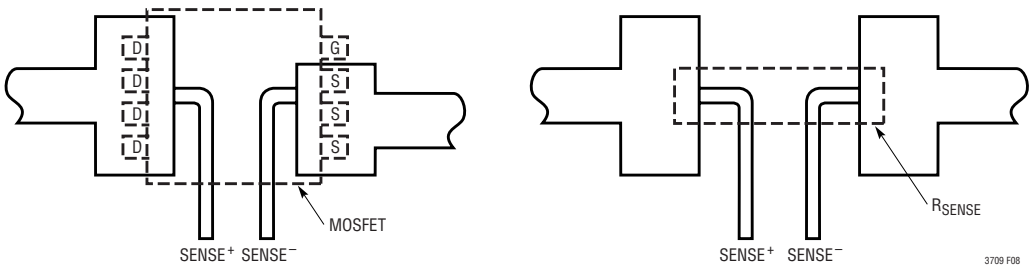
PC Board Layout Checklist

When laying out a PC board follow one of the two suggested approaches. The simple PC board layout requires a dedicated ground plane layer. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, C_{OUT}, MOSFETs, D1, D2 and inductors all in one compact area. It may help to have some components on the bottom side of the board.
- Use an immediate via to connect the components to ground plane including SGND and PGND of LTC3709. Use several larger vias for power components.
- Use a compact plane for switch node (SW) to keep EMI down.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component. You can connect the copper areas to any DC net (V_{IN}, V_{OUT}, GND or to any other DC rail in your system).

When laying out a printed circuit board, without a ground plane, use the following checklist to ensure proper operation of the controller. These items are also illustrated in Figure 9.

- Segregate the signal and power grounds. All small signal components should return to the SGND pin at one point, which is then tied to a "clean" point in the power ground such as the "–" node of C_{IN}.
- Minimize impedance between input ground and output ground.
- Connect PGND1 to the source of M2 or R_{S1} (QFN) directly. This also applies to channel 2.
- Place M2 as close to the controller as possible, keeping the PGND1, BG1 and SW1 traces short. The same for the other channel. SW2 trace should connect to the drain of M2 directly.
- Connect the input capacitor(s) C_{IN} close to the power MOSFETs: (+) node to drain of M1, (–) node to source of M2. This capacitor carries the MOSFET AC current.
- Keep the high dV/dt SW, BOOST and TG nodes away from sensitive small-signal nodes.
- Connect the DRV_{CC} decoupling capacitor C_{VCC} closely to the DRV_{CC} and PGND pins.
- Connect the top driver boost capacitor C_B closely to the BOOST and SW pins.
- Connect the V_{IN} pin decoupling capacitor C_F closely to the V_{CC} and PGND pins.
- Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^-$ and $SENSE^+$ (C_{SENSE}) should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor as shown in Figure 8.

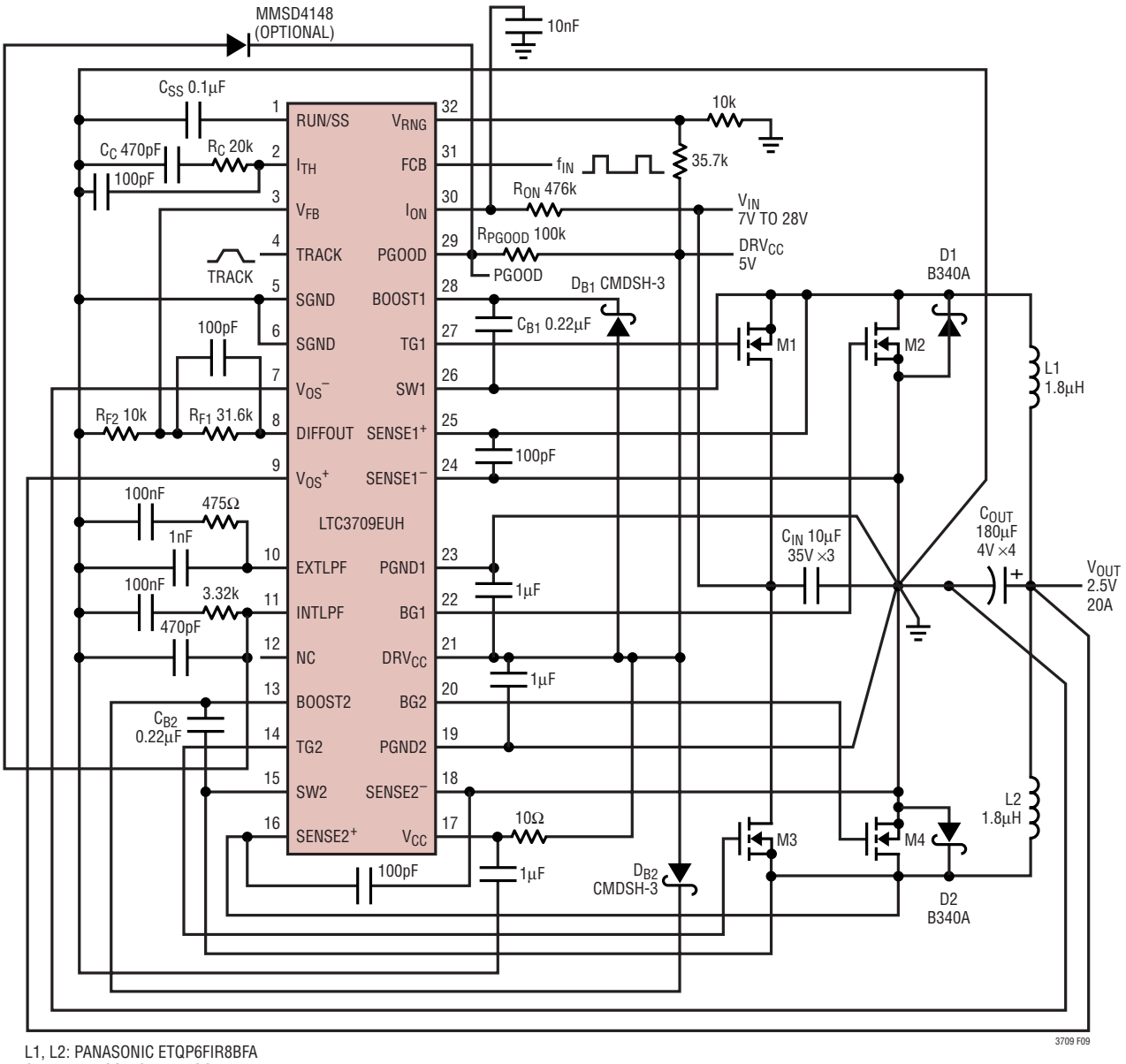


(8a) Sensing the Bottom MOSFET

(8b) Sensing a Resistor

Figure 8. Kelvin Sensing

APPLICATIONS INFORMATION

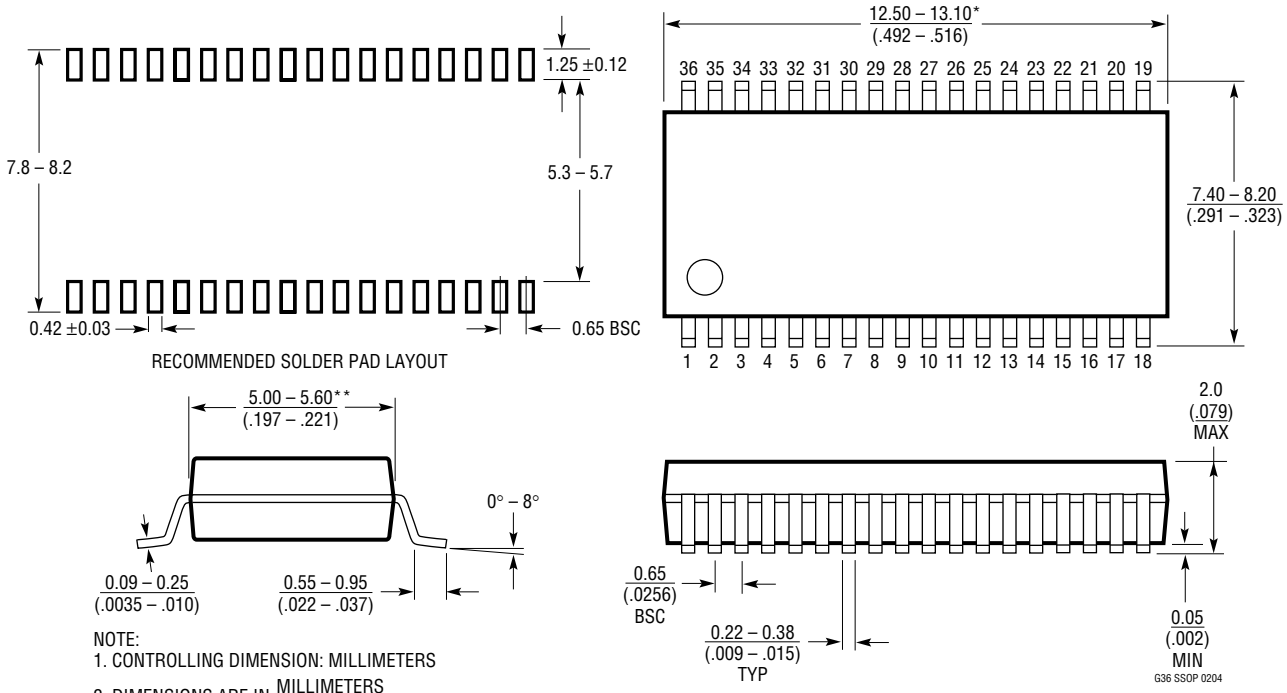


L1, L2: PANASONIC ETQP6FIR8BFA
C_{OUT}: PANASONIC EEFUEOG181R
M1, M3: SILICONIX Si4884DY
M2, M4: SILICONIX Si4874DY

Figure 9. 2-Phase 2.5V/20A Supply at 250kHz with Tracking and External Synch

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



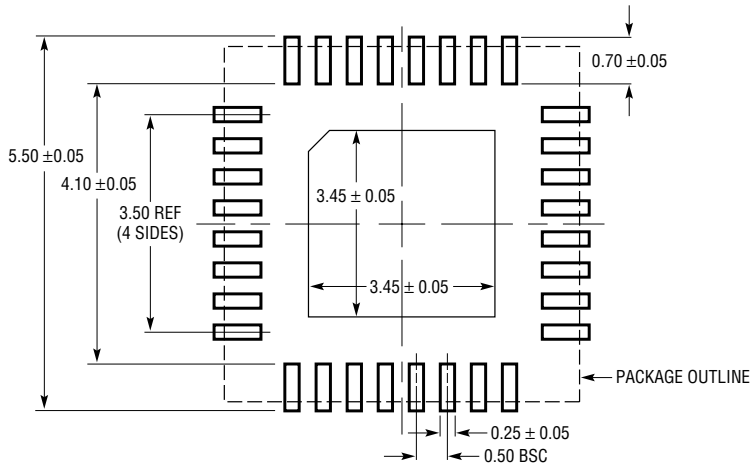
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

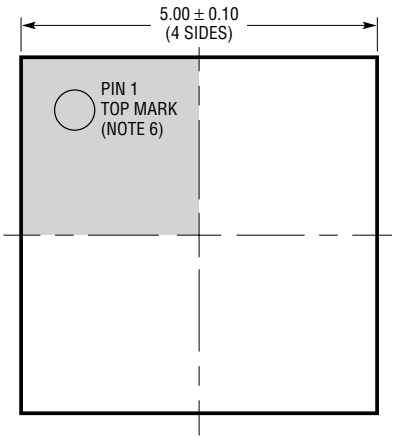
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

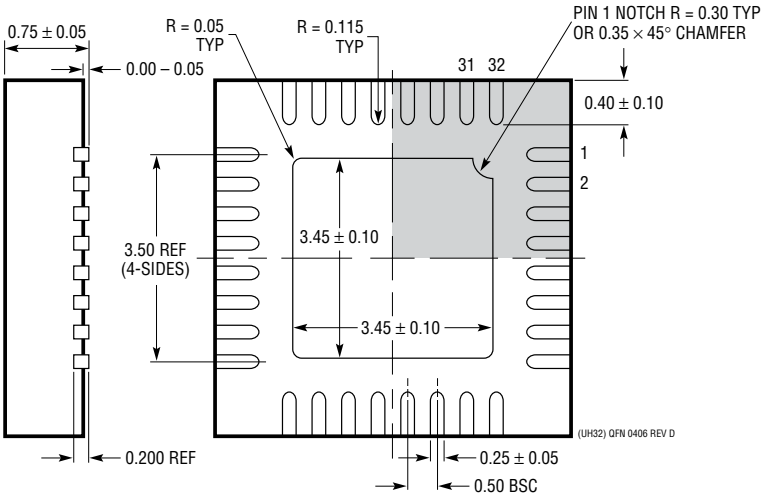
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE