# High Efficiency, Synchronous, 4-Switch Buck-Boost Controller

## FEATURES

- **Single Inductor Architecture Allows $V_{IN}$ Above, Below or Equal to $V_{OUT}$**
- **Wide $V_{IN}$ Range: 4V to 36V Operation**
- **Synchronous Rectification: Up to 98% Efficiency**
- **Current Mode Control**
- **±1% Output Voltage Accuracy: 0.8V < $V_{OUT}$ < 30V**
- Phase-Lockable Fixed Frequency: 200kHz to 400kHz
- Power Good Output Voltage Monitor
- Internal LDO for MOSFET Supply
- Quad N-Channel MOSFET Synchronous Drive
- $V_{OUT}$ Disconnected from $V_{IN}$ During Shutdown
- Adjustable Soft-Start Current Ramping
- Foldback Output Current Limiting
- Selectable Low Current Modes
- Output Overvoltage Protection
- Available in 24-Lead SSOP and Exposed Pad (5mm × 5mm) 32-Lead QFN Packages

## APPLICATIONS

- Automotive Systems
- Telecom Systems
- DC Power Distribution Systems
- High Power Battery-Operated Devices
- Industrial Control

## DESCRIPTION

The LTC®3780 is a high performance buck-boost switching regulator controller that operates from input voltages above, below or equal to the output voltage. The constant frequency current mode architecture allows a phase-lockable frequency of up to 400kHz. With a wide 4V to 30V (36V maximum) input and output range and seamless transfers between operating modes, the LTC3780 is ideal for automotive, telecom and battery-powered systems.

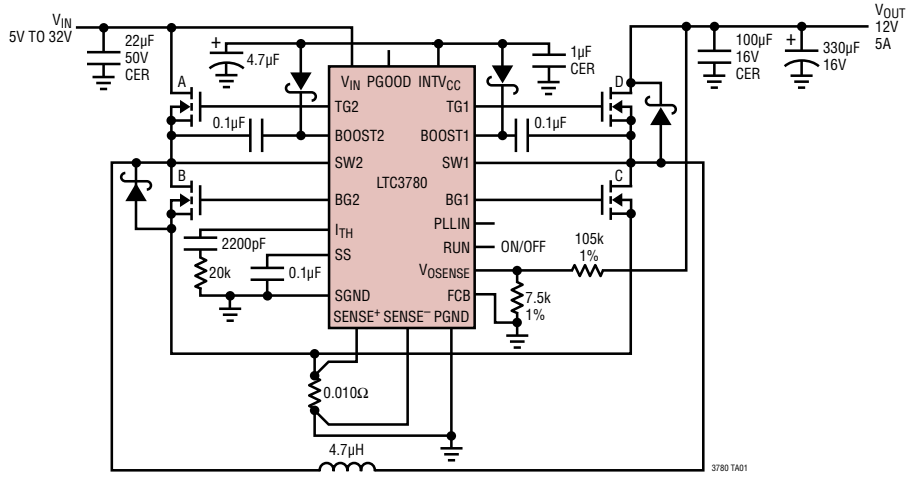
The operating mode of the controller is determined through the FCB pin. For boost operation, the FCB mode pin can select among Burst Mode® operation, discontinuous mode and forced continuous mode. During buck operation, the FCB mode pin can select among skip-cycle mode, discontinuous mode and forced continuous mode. Burst Mode operation and skip-cycle mode provide high efficiency operation at light loads while forced continuous mode and discontinuous mode operate at a constant frequency.

Fault protection is provided by an output overvoltage comparator and internal foldback current limiting. A power good output pin indicates when the output is within 7.5% of its designed set point.

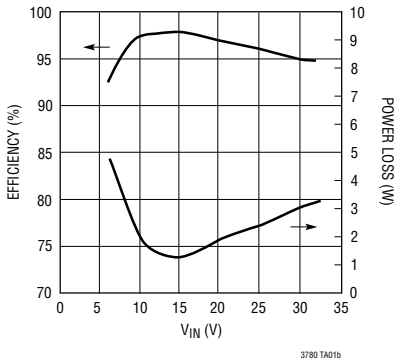


## TYPICAL APPLICATION

**High Efficiency Buck-Boost Converter**




**Efficiency and Power Loss**
**$V_{OUT}$ = 12V, $I_{LOAD}$ = 5A**

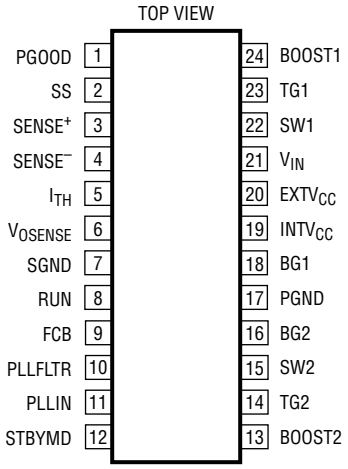



Rev G

## ABSOLUTE MAXIMUM RATINGS (Note 1)

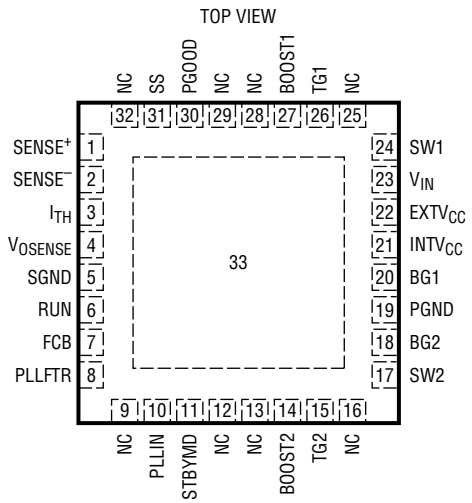
Input Supply Voltage ($V_{IN}$) ..... –0.3V to 36V
Topside Driver Voltages
(BOOST1, BOOST2)..... –0.3V to 42V
Switch Voltage (SW1, SW2)..... –5V to 36V
$INTV_{CC}$, $EXTV_{CC}$, (BOOST – SW1),
(BOOST2 – SW2), PGOOD ..... –0.3V to 7V
RUN, SS..... –0.3V to 6V
PLLIN Voltage..... –0.3V to 5.5V
PLLFLTR Voltage ..... –0.3V to 2.7V
FCB, STBYMD Voltages ..... –0.3V to $INTV_{CC}$
$I_{TH}$, $V_{OSENSE}$ Voltages ..... –0.3V to 2.4V
Peak Output Current <10µs (TG1, TG2, BG1, BG2).....3A
$INTV_{CC}$ Peak Output Current..... 40mA
Operating Junction Temperature Range (Notes 2, 7)
LTC3780E .....–40°C to 85°C
LTC3780I .....–40°C to 125°C
LTC3780MP ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP Only.....300°C

## PIN CONFIGURATION




G PACKAGE
24-LEAD PLASTIC SSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 130°C/W




UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 34°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB

# ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3780EG#PBF | LTC3780EG#TRPBF | LTC3780EG | 24-Lead Plastic SSOP | –40°C to 85°C |
| LTC3780IG#PBF | LTC3780IG#TRPBF | LTC3780IG | 24-Lead Plastic SSOP | –40°C to 125°C |
| LTC3780MPG#PBF | LTC3780MPG#TRPBF | LTC3780MPG | 24-Lead Plastic SSOP | –55°C to 125°C |
| LTC3780EUH#PBF | LTC3780EUH#TRPBF | 3780 | 32-Lead (5mm × 5mm) Plastic QFN | –40°C to 85°C |
| LTC3780IUH#PBF | LTC3780IUH#TRPBF | 3780I | 32-Lead (5mm × 5mm) Plastic QFN | –40°C to 125°C |
| **LEAD BASED FINISH** | **TAPE AND REEL** | **PART MARKING** | **PACKAGE DESCRIPTION** | **TEMPERATURE RANGE** |
| LTC3780EG | LTC3780EG#TR | LTC3780EG | 24-Lead Plastic SSOP | –40°C to 85°C |
| LTC3780IG | LTC3780IG#TR | LTC3780IG | 24-Lead Plastic SSOP | –40°C to 125°C |
| LTC3780MPG | LTC3780MPG#TR | LTC3780MPG | 24-Lead Plastic SSOP | –55°C to 125°C |
| LTC3780EUH | LTC3780EUH#TR | 3780 | 32-Lead (5mm × 5mm) Plastic QFN | –40°C to 85°C |
| LTC3780IUH | LTC3780IUH#TR | 3780I | 32-Lead (5mm × 5mm) Plastic QFN | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

# ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 7) $V_{IN}$ = 15V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Main Control Loop** | | | | | | | |
| $V_{OSENSE}$ | Feedback Reference Voltage | $I_{TH}$ = 1.2V, –40°C ≤ T ≤ 85°C (Note 3)<br>–55°C ≤ T ≤ 125°C | ●<br>● | 0.792<br>0.792 | 0.800<br>0.800 | 0.808<br>0.811 | V<br>V |
| $I_{VOSENSE}$ | Feedback Pin Input Current | (Note 3) | | | –5 | –50 | nA |
| $V_{LOADREG}$ | Output Voltage Load Regulation | (Note 3)<br>$\Delta I_{TH}$ = 1.2V to 0.7V<br>$\Delta I_{TH}$ = 1.2V to 1.8V | <br>●<br>● | | <br>0.1<br>–0.1 | <br>0.5<br>–0.5 | <br>%<br>% |
| $V_{REF(LINEREG)}$ | Reference Voltage Line Regulation | $V_{IN}$ = 4V to 30V, $I_{TH}$ = 1.2V (Note 3) | | | 0.002 | 0.02 | %/V |
| $g_{m(EA)}$ | Error Amplifier Transconductance | $I_{TH}$ = 1.2V, Sink/Source = 3µA (Note 3) | | | 0.32 | | mS |
| $g_{m(GBW)}$ | Error Amplifier GBW | (Note 8) | | | 0.6 | | MHz |
| $I_Q$ | Input DC Supply Current<br>Normal<br>Standby<br>Shutdown Supply Current | (Note 4)<br><br>$V_{RUN}$ = 0V, $V_{STBYMD}$ > 2V<br>$V_{RUN}$ = 0V, $V_{STBYMD}$ = Open | | | <br>2400<br>1500<br>55 | <br><br><br>70 | <br>µA<br>µA<br>µA |
| $V_{FCB}$ | Forced Continuous Threshold | | | 0.76 | 0.800 | 0.84 | V |
| $I_{FCB}$ | Forced Continuous Pin Current | $V_{FCB}$ = 0.85V | | –0.30 | –0.18 | –0.1 | µA |
| $V_{BINHIBIT}$ | Burst Inhibit (Constant Frequency) Threshold | Measured at FCB Pin | | | 5.3 | 5.5 | V |
| UVLO | Undervoltage Reset | $V_{IN}$ Falling | ● | | 3.8 | 4 | V |
| $V_{OVL}$ | Feedback Overvoltage Lockout | Measured at $V_{OSENSE}$ Pin | | 0.84 | 0.86 | 0.88 | V |
| $I_{SENSE}$ | Sense Pins Total Source Current | $V_{SENSE}^-$ = $V_{SENSE}^+$ = 0V | | | –380 | | µA |
| $V_{STBYMD(START)}$ | Start-Up Threshold | $V_{STBYMD}$ Rising | | 0.4 | 0.7 | | V |
| $V_{STBYMD(KA)}$ | Keep-Alive Power-On Threshold | $V_{STBYMD}$ Rising, $V_{RUN}$ = 0V | | | 1.25 | | V |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 7) $V_{IN}$ = 15V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| DF MAX, Boost | Maximum Duty Factor | % Switch C On | | | 99 | | % |
| DF MAX, Buck | Maximum Duty Factor | % Switch A On (in Dropout) | | | 99 | | % |
| $V_{RUN(ON)}$ | RUN Pin On Threshold | $V_{RUN}$ Rising | | 1 | 1.5 | 2 | V |
| $I_{SS}$ | Soft-Start Charge Current | $V_{RUN}$ = 2V | | 0.5 | 1.2 | | µA |
| $V_{SENSE(MAX)}$ | Maximum Current Sense Threshold | Boost: $V_{OSENSE} = V_{REF} – 50mV$<br>Buck: $V_{OSENSE} = V_{REF} – 50mV$ | ●<br>● | 120<br>–95 | 160<br>–110 | 185<br>–150 | mV<br>mV |
| $V_{SENSE(MIN,BUCK)}$ | Minimum Current Sense Threshold | Discontinuous Mode | | | –6 | | mV |
| TG1, TG2 $t_r$ | TG Rise Time | $C_{LOAD}$ = 3300pF (Note 5) | | | 50 | | ns |
| TG1, TG2 $t_f$ | TG Fall Time | $C_{LOAD}$ = 3300pF (Note 5) | | | 45 | | ns |
| BG1, BG2 $t_r$ | BG Rise Time | $C_{LOAD}$ = 3300pF (Note 5) | | | 45 | | ns |
| BG1, BG2 $t_f$ | BG Fall Time | $C_{LOAD}$ = 3300pF (Note 5) | | | 55 | | ns |
| TG1/BG1 $t_{1D}$ | TG1 Off to BG1 On Delay, Switch C On Delay | $C_{LOAD}$ = 3300pF Each Driver | | | 80 | | ns |
| BG1/TG1 $t_{2D}$ | BG1 Off to TG1 On Delay, Synchronous Switch D On Delay | $C_{LOAD}$ = 3300pF Each Driver | | | 80 | | ns |
| TG2/BG2 $t_{3D}$ | TG2 Off to BG2 On Delay, Synchronous Switch B On Delay | $C_{LOAD}$ = 3300pF Each Driver | | | 80 | | ns |
| BG2/TG2 $t_{4D}$ | BG2 Off to TG2 On Delay, Switch A On Delay | $C_{LOAD}$ = 3300pF Each Driver | | | 80 | | ns |
| Mode Transition 1 | BG1 Off to BG2 On Delay, Switch A On Delay | $C_{LOAD}$ = 3300pF Each Driver | | | 250 | | ns |
| Mode Transition 2 | BG2 Off to BG1 On Delay, Synchronous Switch D On Delay | $C_{LOAD}$ = 3300pF Each Driver | | | 250 | | ns |
| $t_{ON(MIN,BOOST)}$ | Minimum On-Time for Main Switch in Boost Operation | Switch C (Note 6) | | | 200 | | ns |
| $t_{ON(MIN,BUCK)}$ | Minimum On-Time for Synchronous Switch in Buck Operation | Switch B (Note 6) | | | 180 | | ns |
| **Internal $V_{CC}$ Regulator** | | | | | | | |
| $V_{INTVCC}$ | Internal $V_{CC}$ Voltage | 7V < $V_{IN}$ < 30V, $V_{EXTVCC}$ = 5V | ● | 5.7 | 6 | 6.3 | V |
| $\Delta V_{LDO(LOADREG)}$ | Internal $V_{CC}$ Load Regulation | $I_{CC}$ = 0mA to 20mA, $V_{EXTVCC}$ = 5V | | | 0.2 | 2 | % |
| $V_{EXTVCC}$ | $EXTV_{CC}$ Switchover Voltage | $I_{CC}$ = 20mA, $V_{EXTVCC}$ Rising | ● | 5.4 | 5.7 | | V |
| $\Delta V_{EXTVCC(HYS)}$ | $EXTV_{CC}$ Switchover Hysteresis | | | | 300 | | mV |
| $\Delta V_{EXTVCC}$ | $EXTV_{CC}$ Switch Drop Voltage | $I_{CC}$ = 20mA, $V_{EXTVCC}$ = 6V | | | 150 | 300 | mV |
| **Oscillator and Phase-Locked Loop** | | | | | | | |
| $f_{NOM}$ | Nominal Frequency | $V_{PLLFLTR}$ = 1.2V | | 260 | 300 | 330 | kHz |
| $f_{LOW}$ | Lowest Frequency | $V_{PLLFLTR}$ = 0V | | 170 | 200 | 220 | kHz |
| $f_{HIGH}$ | Highest Frequency | $V_{PLLFLTR}$ = 2.4V | | 340 | 400 | 440 | kHz |
| $R_{PLLIN}$ | PLLIN Input Resistance | | | | 50 | | kΩ |
| $I_{PLLLPF}$ | Phase Detector Output Current | $f_{PLLIN} < f_{OSC}$<br>$f_{PLLIN} > f_{OSC}$ (Note 9) | | | –15<br>15 | | µA<br>µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 7) $V_{IN}$ = 15V unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **PGOOD Output** | | | | | | | |
| $\Delta V_{FBH}$ | PGOOD Upper Threshold | $V_{OSENSE}$ Rising | | 5.5 | 7.5 | 10 | % |
| $\Delta V_{FBL}$ | PGOOD Lower Threshold | $V_{OSENSE}$ Falling | | –5.5 | –7.5 | –10 | % |
| $\Delta V_{FB(HYST)}$ | PGOOD Hysteresis | $V_{OSENSE}$ Returning | | | 2.5 | | % |
| $V_{PGL}$ | PGOOD Low Voltage | $I_{PGOOD}$ = 2mA | | | 0.1 | 0.3 | V |
| $I_{PGOOD}$ | PGOOD Leakage Current | $V_{PGOOD}$ = 5V | | | | ±1 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** $T_J$ for the QFN package is calculated from the temperature $T_A$ and power dissipation $P_D$ according to the following formula:

$T_J = T_A + (P_D \bullet 34°C/W)$

**Note 3:** The IC is tested in a feedback loop that servos $V_{ITH}$ to a specified voltage and measures the resultant $V_{OSENSE}$.

**Note 4:** Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

**Note 5:** Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

**Note 6:** The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥ 40% of $I_{MAX}$ (see minimum on-time considerations in the Applications Information section).

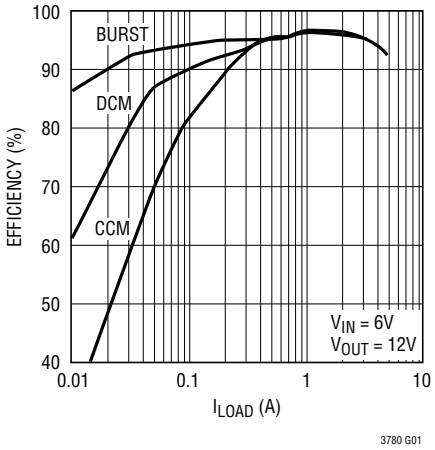
**Note 7:** The LTC3780 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3780E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3780I is guaranteed over the –40°C to 125°C operating junction temperature range, and the LTC3780MP is tested and guaranteed over the full –55°C to 125°C operating junction temperature range.

**Note 8:** This parameter is guaranteed by design.

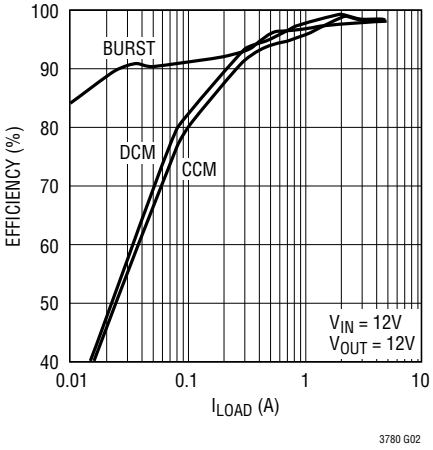
**Note 9:** $f_{OSC}$ is the running frequency for the application.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

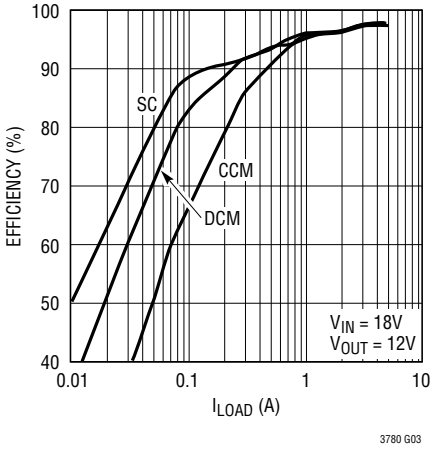
### Efficiency vs Output Current (Boost Operation)



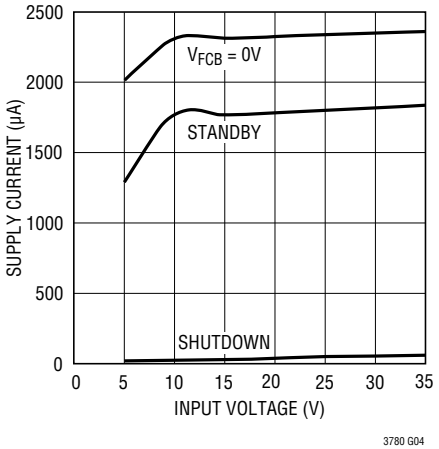

### Efficiency vs Output Current



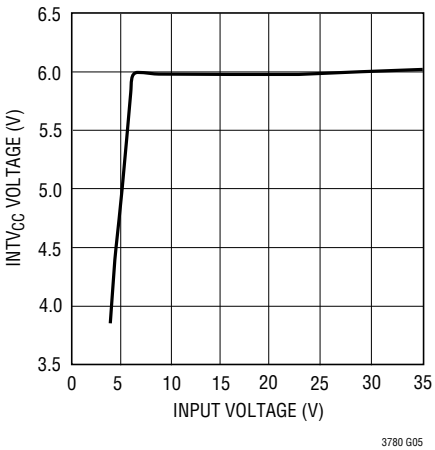

### Efficiency vs Output Current (Buck Operation)



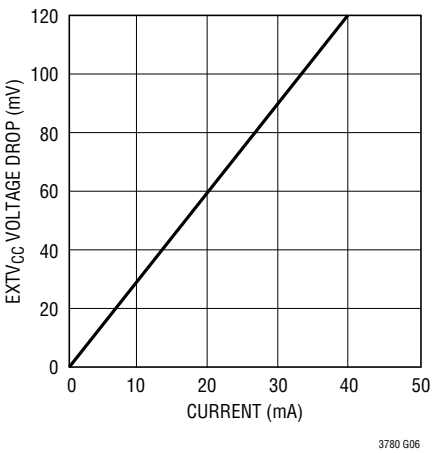

### Supply Current vs Input Voltage



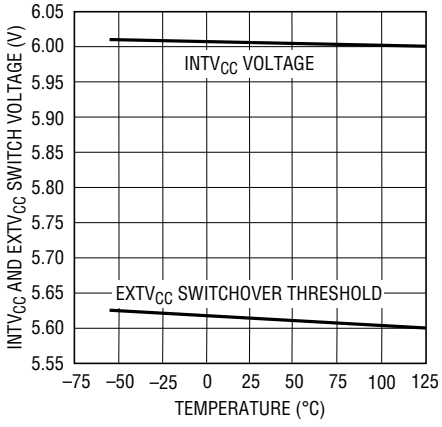

### Internal 6V LDO Line Regulation



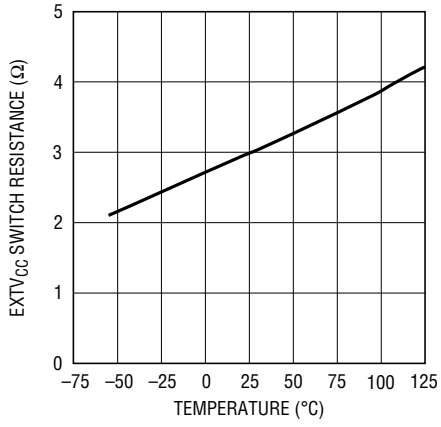

### $EXTV_{CC}$ Voltage Drop



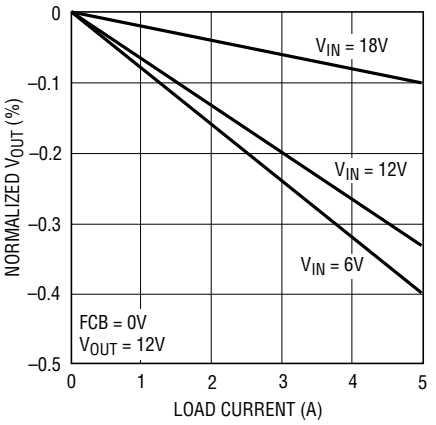

### $INTV_{CC}$ and $EXTV_{CC}$ Switch Voltage vs Temperature




### $EXTV_{CC}$ Switch Resistance vs Temperature

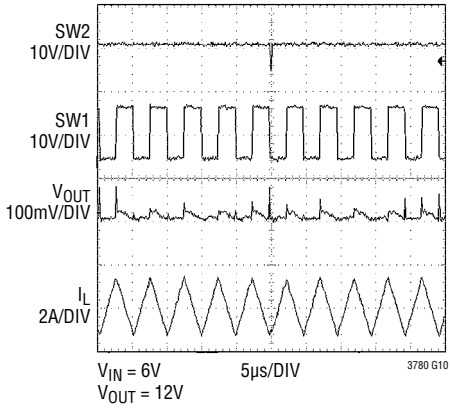



### Load Regulation

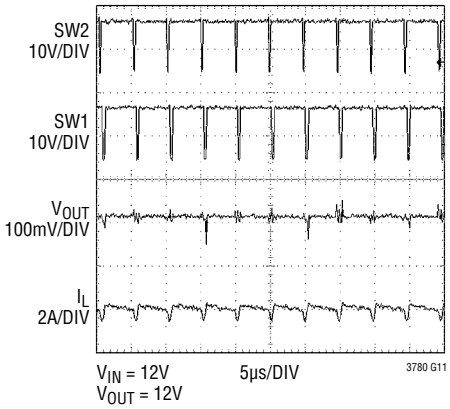


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

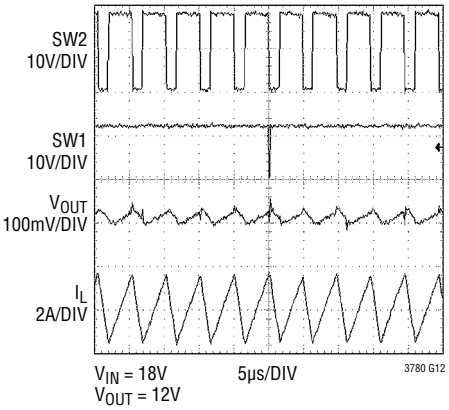
### Continuous Current Mode ($V_{IN}$ = 6V, $V_{OUT}$ = 12V)



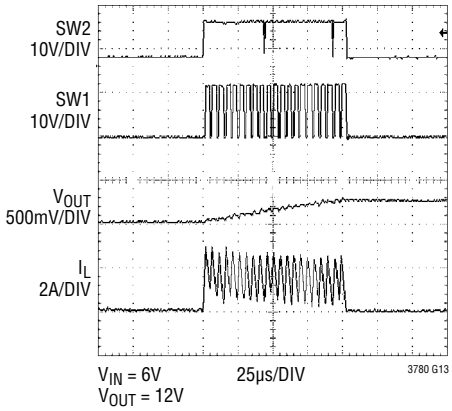

### Continuous Current Mode ($V_{IN}$ = 12V, $V_{OUT}$ = 12V)



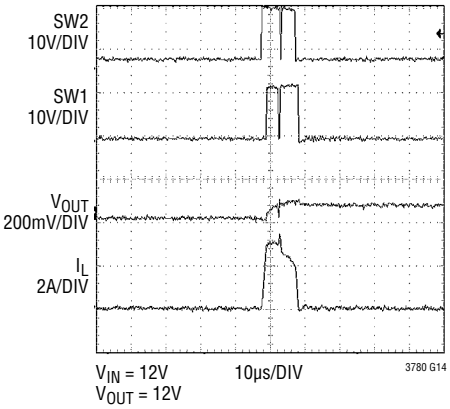

### Continuous Current Mode ($V_{IN}$ = 18V, $V_{OUT}$ = 12V)



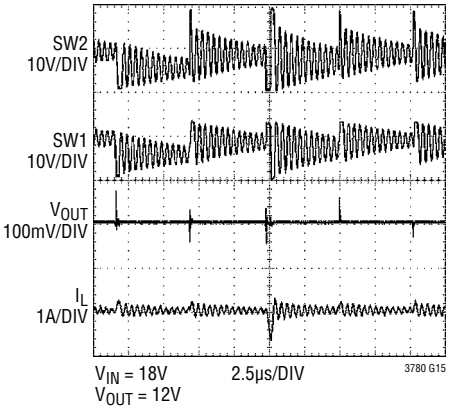

### Burst Mode Operation ($V_{IN}$ = 6V, $V_{OUT}$ = 12V)



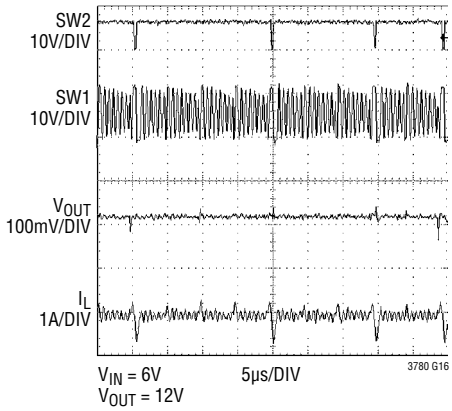

### Burst Mode Operation ($V_{IN}$ = 12V, $V_{OUT}$ = 12V)



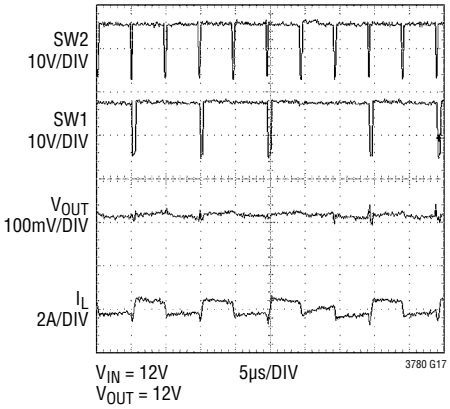

### Skip-Cycle Mode ($V_{IN}$ = 18V, $V_{OUT}$ = 12V)



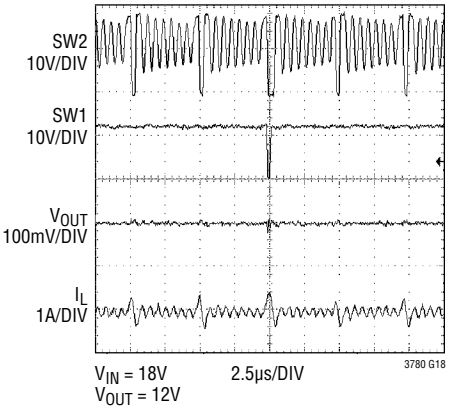

### Discontinuous Current Mode ($V_{IN}$ = 6V, $V_{OUT}$ = 12V)




### Discontinuous Current Mode ($V_{IN}$ = 12V, $V_{OUT}$ = 12V)

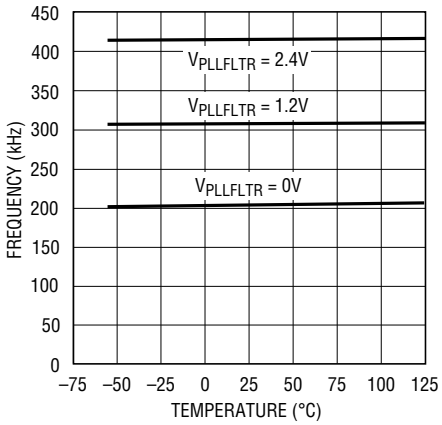



### Discontinuous Current Mode ($V_{IN}$ = 18V, $V_{OUT}$ = 12V)

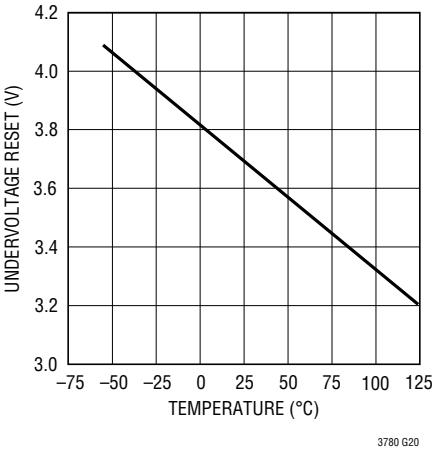


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

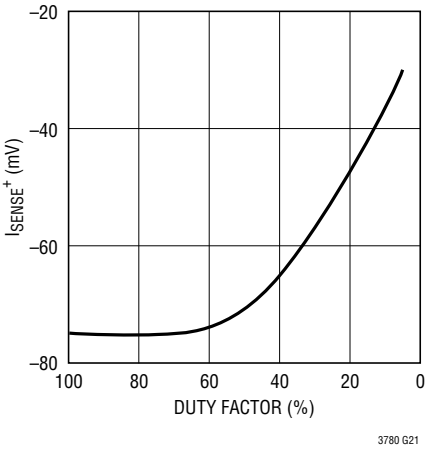
### Oscillator Frequency vs Temperature



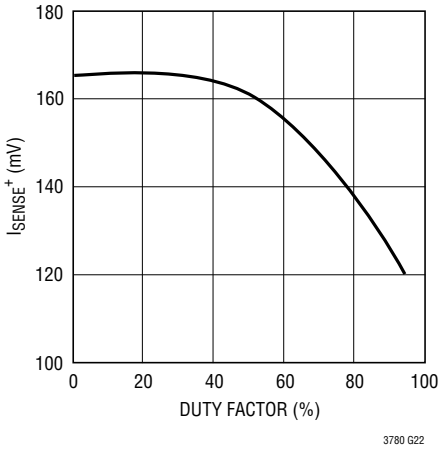

### Undervoltage Reset vs Temperature



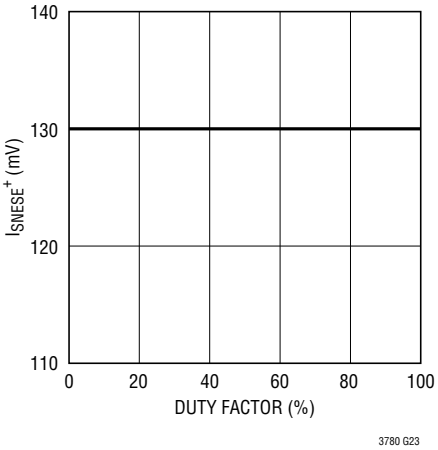

### Minimum Current Sense Threshold vs Duty Factor (Buck)



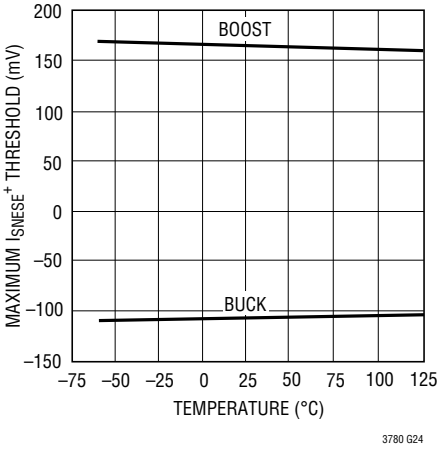

### Maximum Current Sense Threshold vs Duty Factor (Boost)



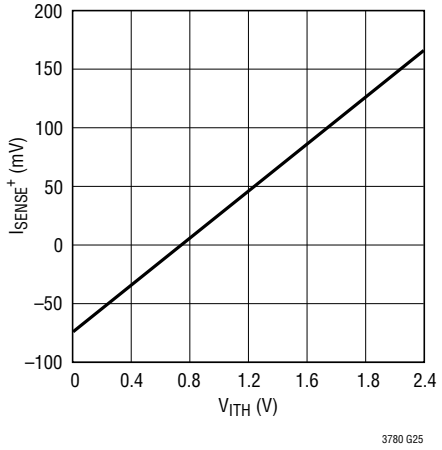

### Maximum Current Sense Threshold vs Duty Factor (Buck)



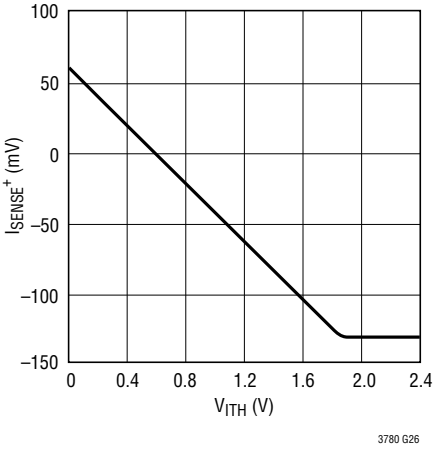

### Minimum Current Sense Threshold vs Temperature



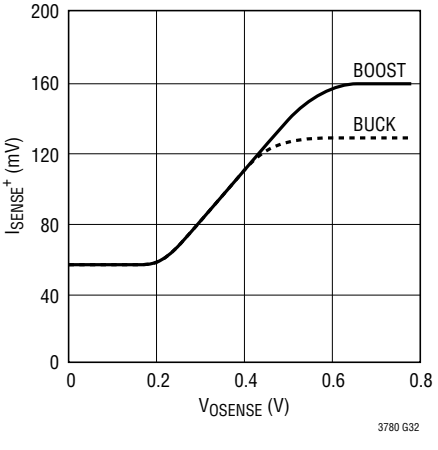

### Peak Current Threshold vs $V_{ITH}$ (Boost)




### Valley Current Threshold vs $V_{ITH}$ (Buck)

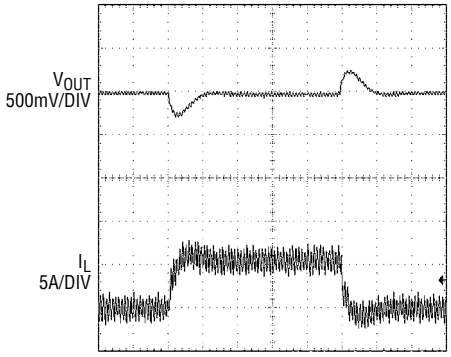



### Current Foldback Limit



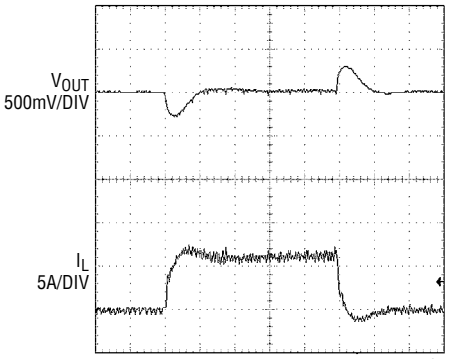
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

### Load Step



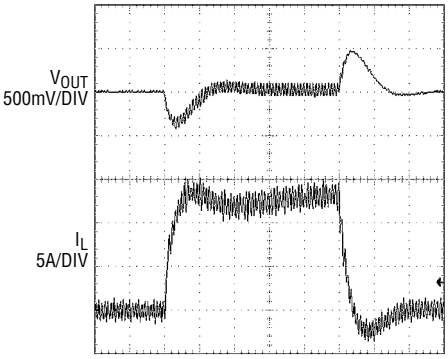

$V_{IN}$ = 18V 200µs/DIV
$V_{OUT}$ = 12V
LOAD STEP: 0A TO 5A
CONTINUOUS MODE

### Load Step



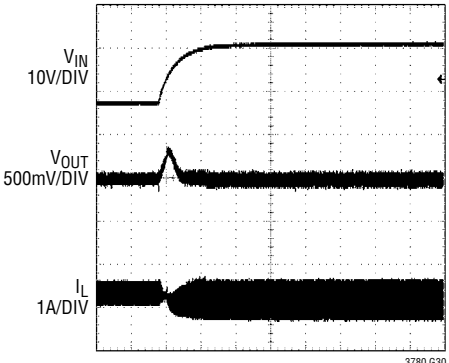

$V_{IN}$ = 12V 200µs/DIV
$V_{OUT}$ = 12V
LOAD STEP: 0A TO 5A
CONTINUOUS MODE

### Load Step



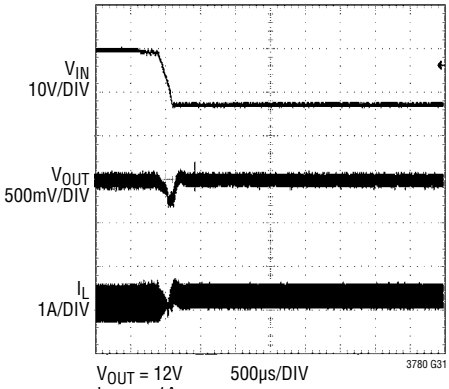

$V_{IN}$ = 6V 200µs/DIV
$V_{OUT}$ = 12V
LOAD STEP: 0A TO 5A
CONTINUOUS MODE

### Line Transient




$V_{OUT}$ = 12V 500µs/DIV
$I_{LOAD}$ = 1A
$V_{IN}$ STEP: 7V TO 20V
CONTINUOUS MODE

### Line Transient




$V_{OUT}$ = 12V 500µs/DIV
$I_{LOAD}$ = 1A
$V_{IN}$ STEP: 20V TO 7V
CONTINUOUS MODE

## PIN FUNCTIONS (SSOP/QFN)

**PGOOD (Pin 1/Pin 30):** Open-Drain Logic Output. PGOOD is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

**SS (Pin 2/Pin 31):** Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit. A minimum value of 6.8nF is recommended on this pin.

**SENSE+ (Pin 3/Pin 1):** The (+) Input to the Current Sense and Reverse Current Detect Comparators. The $I_{TH}$ pin voltage and built-in offsets between SENSE– and SENSE+ pins, in conjunction with $R_{SENSE}$, set the current trip threshold.

**SENSE– (Pin 4/Pin 2):** The (–) Input to the Current Sense and Reverse Current Detect Comparators.

**$I_{TH}$ (Pin 5/Pin 3):** Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V.

**$V_{OSENSE}$ (Pin 6/Pin 4):** Error Amplifier Feedback Input. This pin connects the error amplifier input to an external resistor divider from $V_{OUT}$.

**SGND (Pin 7/Pin 5, Exposed Pad Pin 33):** Signal Ground. All small-signal components and compensation components should connect to this ground, which should be connected to PGND at a single point. The QFN exposed pad must be soldered to PCB ground for electrical connection and rated thermal performance.

**RUN (Pin 8/Pin 6):** Run Control Input. Forcing the RUN pin below 1.5V causes the IC to shut down the switching regulator circuitry. There is a 100k resistor between the RUN pin and SGND in the IC. Do not apply >6V to this pin.

**FCB (Pin 9/Pin 7):** Forced Continuous Control Input. The voltage applied to this pin sets the operating mode of the controller. When the applied voltage is less than 0.8V, the forced continuous current mode is active. When this pin is allowed to float, the Burst Mode operation is active in boost operation and the skip-cycle mode is active in buck operation. When the pin is tied to $INTV_{CC}$, the constant frequency discontinuous current mode is active in buck or boost operation.

**PLLFLTR (Pin 10/Pin 8):** The phase-locked loop's lowpass filter is tied to this pin. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator.

**PLLIN (Pin 11/Pin 10):** External Synchronization Input to Phase Detector. This pin is internally terminated to SGND with 50kΩ. The phase-locked loop will force the rising bottom gate signal of the controller to be synchronized with the rising edge of the PLLIN signal.

**STBYMD (Pin 12/Pin 11):** LDO Control Pin. Determines whether the internal LDO remains active when the controller is shut down. See Operation section for details. If the STBYMD pin is pulled to ground, the SS pin is internally pulled to ground, preventing start-up and thereby providing a single control pin for turning off the controller. To keep the LDO active when RUN is low, for example to power a "wake up" circuit which controls the state of the RUN pin, bypass STBYMD to signal ground with a 0.1µF capacitor, or use a resistor divider from $V_{IN}$ to keep the pin within 2V to 5V.

**BOOST2, BOOST1 (Pins 13, 24/Pins 14, 27):** Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor $C_A$ and $C_B$ (Figure 11) connects here. The BOOST2 pin swings from a diode voltage below $INTV_{CC}$ up to $V_{IN}$ + $INTV_{CC}$. The BOOST1 pin swings from a diode voltage below $INTV_{CC}$ up to $V_{OUT}$ + $INTV_{CC}$.

**TG2, TG1 (Pins 14, 23/Pins 15, 26):** Top Gate Drive. Drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage SW.

**SW2, SW1 (Pins 15, 22/Pins 17, 24):** Switch Node. The (–) terminal of the bootstrap capacitor $C_A$ and $C_B$ (Figure 11) connects here. The SW2 pin swings from a Schottky diode (external) voltage drop below ground up to $V_{IN}$. The SW1 pin swings from a Schottky diode (external) voltage drop below ground up to $V_{OUT}$.

## PIN FUNCTIONS (SSOP/QFN)

**BG2, BG1 (Pins 16, 18/Pins 18, 20):** Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and $INTV_{CC}$.

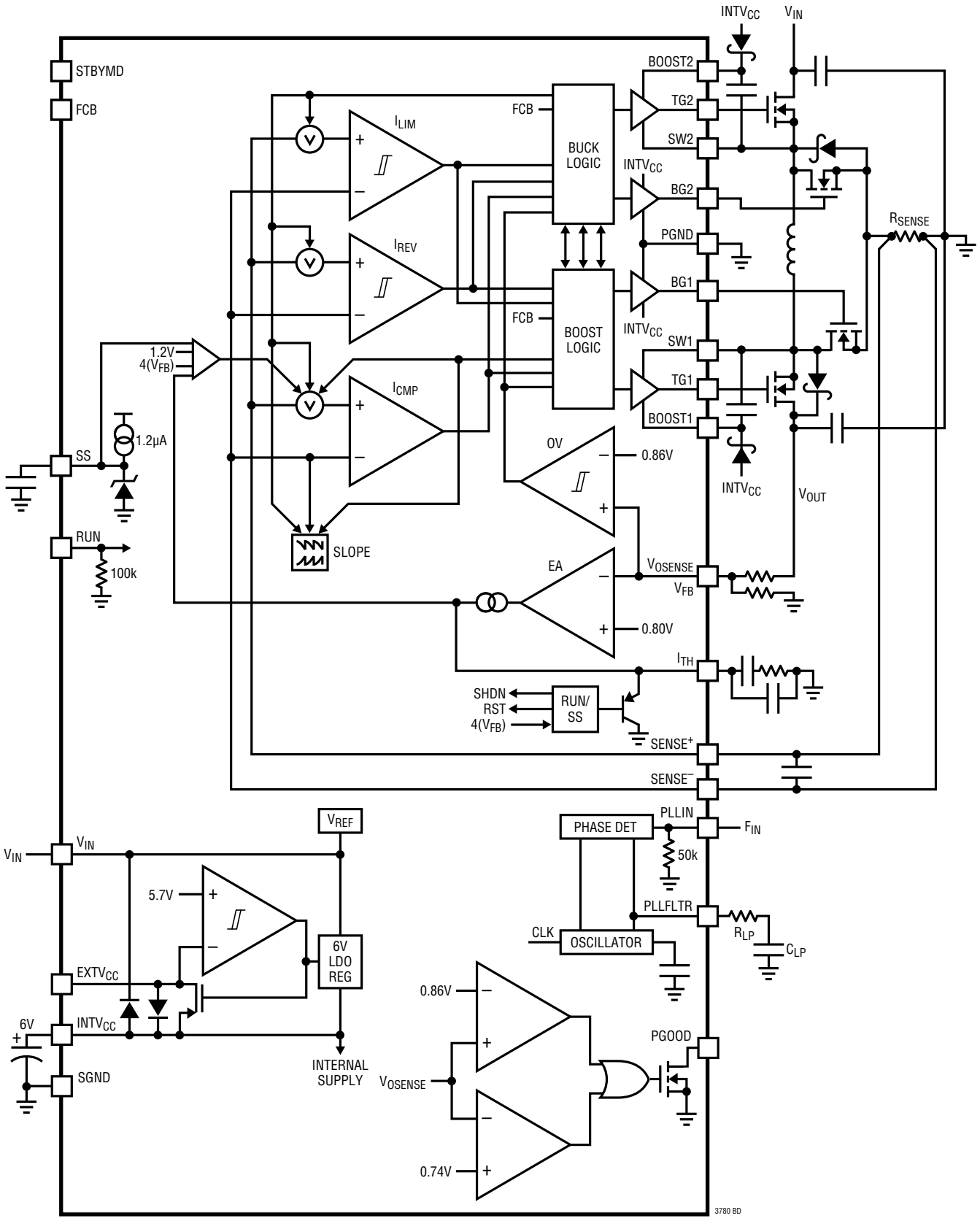
**PGND (Pin 17/Pin 19):** Power Ground. Connect this pin closely to the source of the bottom N-channel MOSFET, the (–) terminal of $C_{VCC}$ and the (–) terminal of $C_{IN}$ (Figure 11).

**$INTV_{CC}$ (Pin 19/Pin 21):** Internal 6V Regulator Output. The driver and control circuits are powered from this voltage. Bypass this pin to ground with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

**$EXTV_{CC}$ (Pin 20/Pin 22):** External $V_{CC}$ Input. When $EXTV_{CC}$ exceeds 5.7V, an internal switch connects this pin to $INTV_{CC}$ and shuts down the internal regulator so that the controller and gate drive power is drawn from $EXTV_{CC}$. Do not exceed 7V at this pin and ensure that $EXTV_{CC} < V_{IN}$.

**$V_{IN}$ (Pin 21/Pin 23):** Main Input Supply. Bypass this pin to SGND with an RC filter (1Ω, 0.1µF).

## BLOCK DIAGRAM



# OPERATION

## MAIN CONTROL LOOP

The LTC3780 is a current mode controller that provides an output voltage above, equal to or below the input voltage. The LTC proprietary topology and control architecture employs a current-sensing resistor in buck or boost modes. The sensed inductor current is controlled by the voltage on the $I_{TH}$ pin, which is the output of the amplifier EA. The $V_{OSENSE}$ pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA.

The top MOSFET drivers are biased from floating boostrap capacitors $C_A$ and $C_B$ (Figure 11), which are normally recharged through an external diode when the top MOSFET is turned off. Schottky diodes across the synchronous switch D and synchronous switch B are not required, but provide a lower drop during the dead time. The addition of the Schottky diodes will typically improve peak efficiency by 1% to 2% at 400kHz.

The main control loop is shut down by pulling the RUN pin low. When the RUN pin voltage is higher than 1.5V, an internal 1.2µA current source charges soft-start capacitor $C_{SS}$ at the SS pin. The $I_{TH}$ voltage is then clamped to the SS voltage while $C_{SS}$ is slowly charged during start-up. This "soft-start" clamping prevents abrupt current from being drawn from the input power supply.

## POWER SWITCH CONTROL

Figure 1 shows a simplified diagram of how the four power switches are connected to the inductor, $V_{IN}$, $V_{OUT}$ and GND. Figure 2 shows the regions of operation for the LTC3780 as a function of duty cycle D. The power switches are properly controlled so the transfer between modes is continuous. When $V_{IN}$ approaches $V_{OUT}$, the buck-boost region is reached; the mode-to-mode transition time is typically 200ns.

### Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. At the start of every cycle, synchronous switch B is turned on first. Inductor current is sensed when synchronous switch B is turned on. After the sensed inductor current falls below the reference voltage, which is proportional to $V_{ITH}$, synchronous switch B is turned off

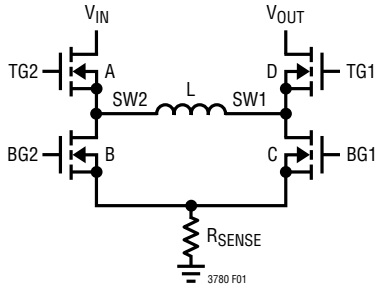



**Figure 1. Simplified Diagram of the Output Switches**

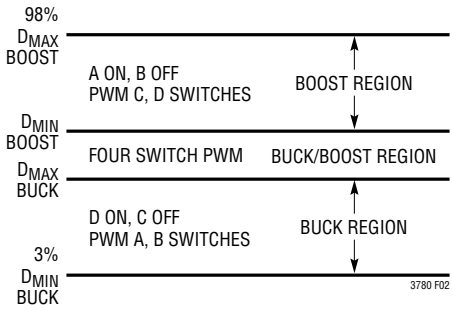



**Figure 2. Operating Mode vs Duty Cycle**

and switch A is turned on for the remainder of the cycle. switches A and B will alternate, behaving like a typical synchronous buck regulator. The duty cycle of switch A increases until the maximum duty cycle of the converter in buck mode reaches $D_{MAX\_BUCK}$, given by:

$$D_{MAX\_BUCK} = 100\% - D_{BUCK\text{-}BOOST}$$

where $D_{BUCK\text{-}BOOST}$ = duty cycle of the buck-boost switch range:

$$D_{BUCK\text{-}BOOST} = (200ns \bullet f) \bullet 100\%$$

and f is the operating frequency in Hz.

Figure 3 shows typical buck mode waveforms. If $V_{IN}$ approaches $V_{OUT}$, the buck-boost region is reached.

### Buck-Boost ($V_{IN} \cong V_{OUT}$)

When $V_{IN}$ is close to $V_{OUT}$, the controller is in buck-boost mode. Figure 4 shows typical waveforms in this mode. Every cycle, if the controller starts with switches B and D turned on, switches A and C are then turned on. Finally, switches A and D are turned on for the remainder of the time. If the controller starts with switches A and C turned

## OPERATION

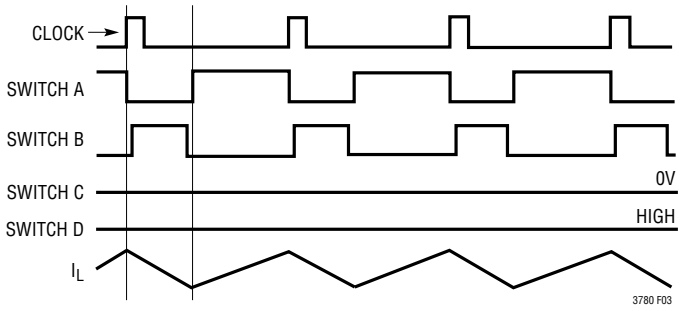



**Figure 3. Buck Mode ($V_{IN}$ > $V_{OUT}$)**

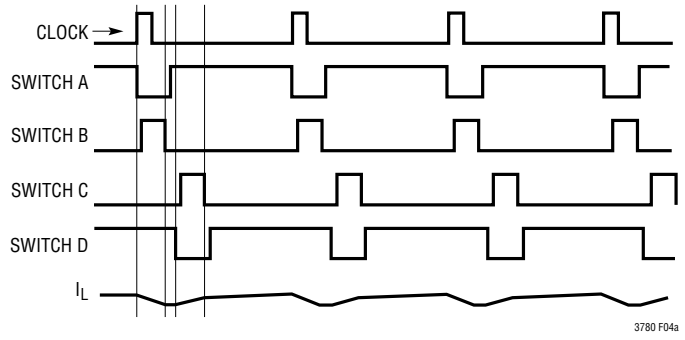



**Figure 4a. Buck-Boost Mode ($V_{IN}$ ≥ $V_{OUT}$)**

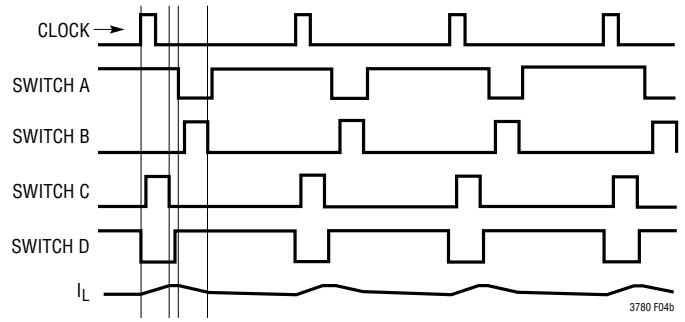



**Figure 4b. Buck-Boost Mode ($V_{IN}$ ≤ $V_{OUT}$)**

**Figure 4. Buck-Boost Mode**

on, switches B and D are then turned on. Finally, switches A and D are turned on for the remainder of the time.

### Boost Region ($V_{IN}$ < $V_{OUT}$)

Switch A is always on and synchronous switch B is always off in boost mode. Every cycle, switch C is turned on first. Inductor current is sensed when switch C is turned on. After the sensed inductor current exceeds the reference voltage which is proportional to $V_{ITH}$, switch C is turned off and synchronous switch D is turned on for the remainder of the cycle. switches C and D will alternate, behaving like a typical synchronous boost regulator.

The duty cycle of switch C decreases until the minimum duty cycle of the converter in boost mode reaches $D_{MIN\_BOOST}$, given by:

$$D_{MIN\_BOOST} = D_{BUCK\text{-}BOOST}$$

where $D_{BUCK\text{-}BOOST}$ is the duty cycle of the buck-boost switch range:

$$D_{BUCK\text{-}BOOST} = (200ns \bullet f) \bullet 100\%$$

and f is the operating frequency in Hz.

Figure 5 shows typical boost mode waveforms. If $V_{IN}$ approaches $V_{OUT}$, the buck-boost region is reached.

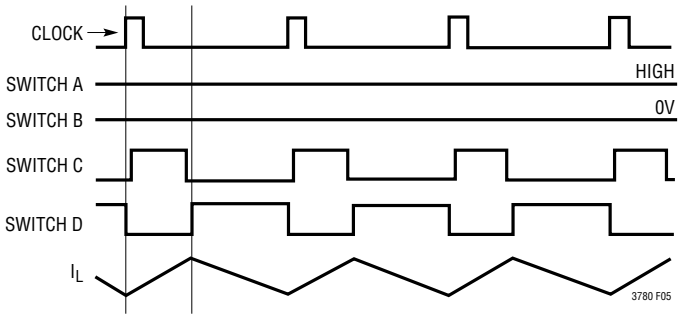



**Figure 5. Boost Mode ($V_{IN}$ < $V_{OUT}$)**

### LOW CURRENT OPERATION

The FCB pin is used to select among three modes for both buck and boost operations by accepting a logic input. Figure 6 shows the different modes.

| FCB PIN | BUCK MODE | BOOST MODE |
|---|---|---|
| 0V to 0.75V | Force Continuous Mode | Force Continuous Mode |
| 0.85V to 5V | Skip-Cycle Mode | Burst Mode Operation |
| >5.3V | DCM with Constant Freq | DCM with Constant Freq |

**Figure 6. Different Operating Modes**

When the FCB pin voltage is lower than 0.8V, the controller behaves as a continuous, PWM current mode synchronous switching regulator. In boost mode, switch A is always on. switch C and synchronous switch D are alternately turned on to maintain the output voltage independent of direction of inductor current. Every ten cycles, switch A is forced off for about 300ns to allow boost capacitor $C_A$ (Figure 13) to

## OPERATION

recharge. In buck mode, synchronous switch D is always on. switch A and synchronous switch B are alternately turned on to maintain the output voltage independent of direction of inductor current. Every ten cycles, synchronous switch D is forced off for about 300ns to allow $C_B$ to recharge. This is the least efficient operating mode at light load, but may be desirable in certain applications. In this mode, the output can source or sink current.

When the FCB pin voltage is below $V_{INTVCC}$ – 1V, but greater than 0.8V, the controller enters Burst Mode operation in boost operation or enters skip-cycle mode in buck operation. During boost operation, Burst Mode operation sets a minimum output current level before inhibiting the switch C and turns off synchronous switch D when the inductor current goes negative. This combination of requirements will, at low currents, force the $I_{TH}$ pin below a voltage threshold that will temporarily inhibit turn-on of power switches C and D until the output voltage drops. There is 100mV of hysteresis in the burst comparator tied to the $I_{TH}$ pin. This hysteresis produces output signals to the MOSFETs C and D that turn them on for several cycles, followed by a variable "sleep" interval depending upon the load current. The maximum output voltage ripple is limited to 3% of the nominal DC output voltage as determined by a resistive feedback divider. During buck operation at no load, switch A is turned on for its minimum on-time. This will not occur every clock cycle when the output load current drops below 1% of the maximum designed load. The body diode of synchronous switch B or the Schottky diode, which is in parallel with switch B, is used to discharge the inductor current; switch B only turns on every ten clock cycles to allow $C_B$ to recharge. As load current is applied, switch A turns on every cycle, and its on-time begins to increase. At higher current, switch B turns on briefly after each turn-off of switch A. switches C and D remain off at light load, except to refresh CA (Figure 11) every 10 clock cycles. In Burst Mode operation/skip-cycle mode, the output is prevented from sinking current.

When the FCB pin voltage is tied to the $INTV_{CC}$ pin, the controller enters constant frequency discontinuous current mode (DCM). For boost operation, synchronous switch D is held off whenever the $I_{TH}$ pin is below a threshold voltage. In every cycle, switch C is used to charge inductor current. After the output voltage is high enough, the controller will enter continuous current buck mode for one cycle to discharge inductor current. In the following cycle, the controller will resume DCM boost operation. For buck operation, constant frequency discontinuous current mode sets a minimum negative inductor current level. synchronous switch B is turned off whenever inductor current is lower than this level. At very light loads, this constant frequency operation is not as efficient as Burst Mode operation or skip-cycle, but does provide lower noise, constant frequency operation.

### FREQUENCY SYNCHRONIZATION AND FREQUENCY SETUP

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the PLLIN pin. The phase detector output at the PLLFLTR pin is also the DC frequency control input of the oscillator. The frequency ranges from 200kHz to 400kHz, corresponding to a DC voltage input from 0V to 2.4V at PLLFLTR. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to its minimum frequency.

### $INTV_{CC}/EXTV_{CC}$ Power

Power for all power MOSFET drivers and most internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open, an internal 6V low dropout linear regulator supplies $INTV_{CC}$ power. If $EXTV_{CC}$ is taken above 5.7V, the 6V regulator is turned off and an internal switch is turned on, connecting $EXTV_{CC}$ to $INTV_{CC}$. This allows the $INTV_{CC}$ power to be derived from a high efficiency external source.

### POWER GOOD (PGOOD) PIN

The PGOOD pin is connected to an open drain of an internal MOSFET. The MOSFET turns on and pulls the pin low when the output is not within ±7.5% of the nominal output level as determined by the resistive feedback divider. When the output meets the ±7.5% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 7V.

## OPERATION

### FOLDBACK CURRENT

Foldback current limiting is activated when the output voltage falls below 70% of its nominal level, reducing power waste. During start-up, foldback current limiting is disabled.

### INPUT UNDERVOLTAGE RESET

The SS capacitor will be reset if the input voltage is allowed to fall below approximately 4V. The SS capacitor will attempt to charge through a normal soft-start ramp after the input voltage rises above 4V.

### OUTPUT OVERVOLTAGE PROTECTION

An overvoltage comparator guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In this case, synchronous switch B and synchronous switch D are turned on until the overvoltage condition is cleared or the maximum negative current limit is reached. When inductor current is lower than the maximum negative current limit, synchronous switch B and synchronous switch D are turned off, and switch A and switch C are turned on until the inductor current reaches another negative current limit. If the comparator still detects an overvoltage condition, switch A and switch C are turned off, and synchronous switch B and synchronous switch D are turned on again.

### SHORT-CIRCUIT PROTECTION AND CURRENT LIMIT

Switch A on-time is limited by output voltage. When output voltage is reduced and is lower than its nominal level, switch A on-time will be reduced.

In every boost mode cycle, current is limited by a voltage reference, which is proportional to the $I_{TH}$ pin voltage. The maximum sensed current is limited to 160mV. In every buck mode cycle, the maximum sensed current is limited to 130mV.

### STANDBY MODE PIN

The STBYMD pin is a three-state input that controls circuitry within the IC as follows: When the STBYMD pin is held at ground, the SS pin is pulled to ground. When the pin is left open, the internal SS current source charges the SS capacitor, allowing turn-on of the controller and activating necessary internal biasing. When the STBYMD pin is taken above 2V, the internal linear regulator is turned on independent of the state on the RUN and SS pins, providing an output power source for “wake-up” circuitry. Bypass the pin with a small capacitor (0.1µF) to ground if the pin is not connected to a DC potential.

# APPLICATIONS INFORMATION

Figure 11 is a basic LTC3780 application circuit. External component selection is driven by the load requirement, and begins with the selection of $R_{SENSE}$ and the inductor value. Next, the power MOSFETs are selected. Finally, $C_{IN}$ and $C_{OUT}$ are selected. This circuit can be configured for operation up to an input voltage of 36V.

### Selection of Operation Frequency

The LTC3780 uses a constant frequency architecture and has an internal voltage controlled oscillator. The switching frequency is determined by the internal oscillator capacitor. This internal capacitor is charged by a fixed current plus an additional current that is proportional to the voltage applied to the PLLFLTR pin. The frequency of this oscillator can be varied over a 2-to-1 range. The PLLFLTR pin can be grounded to lower the frequency to 200kHz or tied to 2.4V to yield approximately 400kHz. When PLLIN is left open, the PLLFLTR pin goes low, forcing the oscillator to minimum frequency.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 7. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency. The maximum switching frequency is approximately 400kHz.

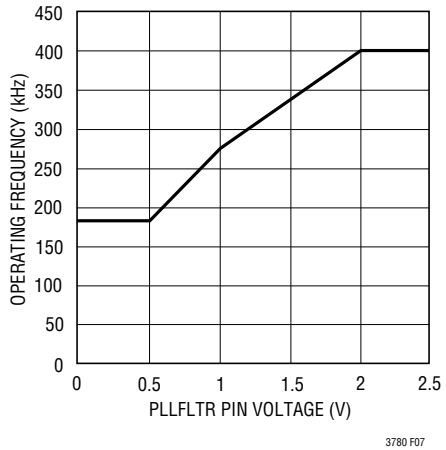



**Figure 7. Frequency vs PLLFLTR Pin Voltage**

### Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple $\Delta I_L$ is typically set to 20% to 40% of the maximum inductor current at boost mode $V_{IN(MIN)}$. For a given ripple the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 \bullet \left(V_{OUT} - V_{IN(MIN)}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%\,Ripple \bullet V_{OUT}^2} H,$$

$$L_{BUCK} > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%\,Ripple \bullet V_{IN(MAX)}} H$$

where:

f is operating frequency, Hz

% Ripple is allowable inductor current ripple, %

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

$V_{OUT}$ is output voltage, V

$I_{OUT(MAX)}$ is maximum output load current

For high efficiency, choose an inductor with low core loss, such as ferrite and molypermalloy (from Magnetics, Inc.). Also, the inductor should have low DC resistance to reduce the $I^2R$ losses, and must be able to handle the peak inductor current without saturation. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

### $R_{SENSE}$ Selection and Maximum Output Current

$R_{SENSE}$ is chosen based on the required output current. The current comparator threshold sets the peak of the inductor current in boost mode and the maximum inductor valley current in buck mode. In boost mode, the maximum average load current at $V_{IN(MIN)}$ is:

$$I_{OUT(MAX,BOOST)} = \left(\frac{160mV}{R_{SENSE}} - \frac{\Delta I_L}{2}\right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

## APPLICATIONS INFORMATION

where $\Delta I_L$ is peak-to-peak inductor ripple current. In buck mode, the maximum average load current is:

$$I_{OUT(MAX,BUCK)} = \frac{130mV}{R_{SENSE}} + \frac{\Delta I_L}{2}$$

Figure 8 shows how the load current ($I_{MAXLOAD} \bullet R_{SENSE}$) varies with input and output voltage

The maximum current sensing $R_{SENSE}$ value for the boost mode is:

$$R_{SENSE(MAX)} = \frac{2 \bullet 160mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT} + \Delta I_{L,BOOST} \bullet V_{IN(MIN)}}$$

The maximum current sensing $R_{SENSE}$ value for the buck mode is:

$$R_{SENSE(MAX)} = \frac{2 \bullet 130mV}{2 \bullet I_{OUT(MAX,BUCK)} - \Delta I_{L,BUCK}}$$

The final $R_{SENSE}$ value should be lower than the calculated $R_{SENSE(MAX)}$ in both the boost and buck modes. A 20% to 30% margin is usually recommended.

### $C_{IN}$ and $C_{OUT}$ Selection

In boost mode, input current is continuous. In buck mode, input current is discontinuous. In buck mode, the selection of input capacitor $C_{IN}$ is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

In boost mode, the discontinuous current shifts from the input to the output, so $C_{OUT}$ must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$Ripple\ (Boost,Cap) = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

$$Ripple\ (Buck,Cap) = \frac{I_{OUT(MAX)} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{C_{OUT} \bullet V_{IN(MAX)} \bullet f} V$$

where $C_{OUT}$ is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{BOOST,ESR} = I_{L(MAX,BOOST)} \bullet ESR$$

$$\Delta V_{BUCK,ESR} = I_{L(MAX,BUCK)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings, such as OS-CON and POSCAP.

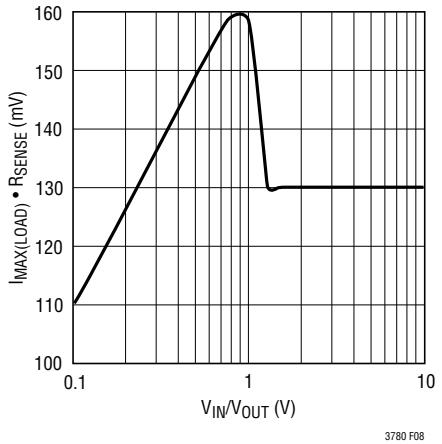



**Figure 8. Load Current vs $V_{IN}/V_{OUT}$**

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### Power MOSFET Selection and Efficiency Considerations

The LTC3780 requires four external N-channel power MOSFETs, two for the top switches (switch A and D, shown in Figure 1) and two for the bottom switches (switch B and C shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR,DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance $C_{RSS}$ and maximum current $I_{DS(MAX)}$.

The drive voltage is set by the 6V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3780 applications. If the input voltage is expected to drop below 5V, then the sub-logic threshold MOSFETs should be considered.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in boost mode, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A,BOOST} = \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}\right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

where $\rho_T$ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C as shown in Figure 9. For a maximum junction temperature of 125°C, using a value $\rho_T$ = 1.5 is reasonable.

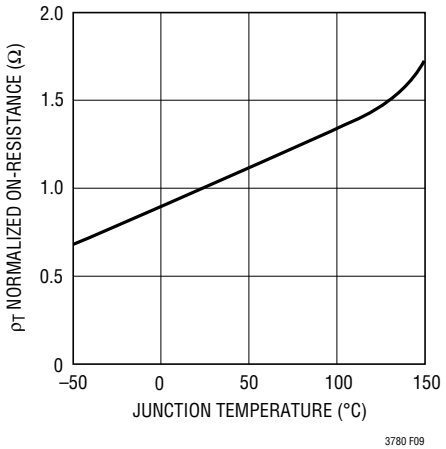


**Figure 9. Normalized $R_{DS(ON)}$ vs Temperature**

Switch B operates in buck mode as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)}$$

Switch C operates in boost mode as the control switch. Its power dissipation at maximum current is given by:

$$P_{C,BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho_T \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where $C_{RSS}$ is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in boost mode, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}\right)^2 \bullet \rho_T \bullet R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of $T_J$ can then be compared to the original, assumed value used in the iterative calculation process.

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### Schottky Diode (D1, D2) Selection and Light Load Operation

The Schottky diodes D1 and D2 shown in Figure 13 conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D2 significantly reduces reverse recovery current between switch D turn-off and switch C turn-on, which improves converter efficiency and reduces switch C voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

In buck mode, when the FCB pin voltage is $0.85 < V_{FCB} < 5V$, the converter operates in skip-cycle mode. In this mode, synchronous switch B remains off until the inductor peak current exceeds one-fifth of its maximum peak current. As a result, D1 should be rated for about one-half to one-third of the full load current.

In boost mode, when the FCB pin voltage is higher than 5.3V, the converter operates in discontinuous current mode. In this mode, synchronous switch D remains off until the inductor peak current exceeds one-fifth of its maximum peak current. As a result, D2 should be rated for about one-third to one-fourth of the full load current.

In buck mode, when the FCB pin voltage is higher than 5.3V, the converter operates in constant frequency discontinuous current mode. In this mode, synchronous switch B remains on until the inductor valley current is lower than the sense voltage representing the minimum negative inductor current level ($V_{SENSE}$ = –5mV). Both switch A and B are off until next clock signal.

In boost mode, when the FCB pin voltage is $0.85 < V_{FCB} < 5.3V$, the converter operates in Burst Mode operation. In this mode, the controller clamps the peak inductor current to approximately 20% of the maximum inductor current. The output voltage ripple can increase during Burst Mode operation.

### $INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 6V at the $INTV_{CC}$ pin from the $V_{IN}$ supply pin. $INTV_{CC}$ powers the drivers and internal circuitry within the LTC3780. The $INTV_{CC}$ pin regulator can supply a peak current of 40mA and must be bypassed to ground with a minimum of 4.7µF tantalum, 10µF special polymer or low ESR type electrolytic capacitor. A 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND IC pins is highly recommended. Good bypassing is necessary to supply the high transient current required by MOSFET gate drivers.

Higher input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3780 to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculations. The total $INTV_{CC}$ current can be supplied by either the 6V internal linear regulator or by the $EXTV_{CC}$ input pin. When the voltage applied to the $EXTV_{CC}$ pin is less than 5.7V, all of the $INTV_{CC}$ current is supplied by the internal 6V linear regulator. Power dissipation for the IC in this case is $V_{IN} \bullet I_{INTVCC}$, and overall efficiency is lowered. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, a typical application operating in continuous current mode might draw 24mA from a 24V supply when not using the $EXTV_{CC}$ pin:

$T_J = 70°C + 24mA \bullet 24V \bullet 34°C/W = 90°C$

Use of the $EXTV_{CC}$ input pin reduces the junction temperature to:

$T_J = 70°C + 24mA \bullet 6V \bullet 34°C/W = 75°C$

To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum $V_{IN}$.

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### $EXTV_{CC}$ Connection

The LTC3780 contains an internal P-channel MOSFET switch connected between the $EXTV_{CC}$ and $INTV_{CC}$ pins. When the voltage applied to $EXTV_{CC}$ rises above 5.7V, the internal regulator is turned off and a switch connects the $EXTV_{CC}$ pin to the $INTV_{CC}$ pin thereby supplying internal power. The switch remains closed as long as the voltage applied to $EXTV_{CC}$ remains above 5.5V. This allows the MOSFET driver and control power to be derived from the output when ($5.7V < V_{OUT} < 7V$) and from the internal regulator when the output is out of regulation (start-up, short-circuit). If more current is required through the $EXTV_{CC}$ switch than is specified, an external Schottky diode can be interposed between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Ensure that $EXTV_{CC} \leq V_{IN}$.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 6V regulator at the cost of a small efficiency penalty.
2. $EXTV_{CC}$ connected directly to $V_{OUT}$ ($5.7V < V_{OUT} < 7V$). This is the normal connection for a 6V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 5.5V to 7V range, it may be used to power $EXTV_{CC}$ provided it is compatible with the MOSFET gate drive requirements.

### Output Voltage

The LTC3780 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 0.800V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

### Topside MOSFET Driver Supply ($C_A$, $D_A$, $C_B$, $D_B$)

Referring to Figure 11, the external bootstrap capacitors $C_A$ and $C_B$ connected to the BOOST1 and BOOST2 pins supply the gate drive voltage for the topside MOSFET switches A and D. When the top MOSFET switch A turns on, the switch node SW2 rises to $V_{IN}$ and the BOOST2 pin rises to approximately $V_{IN} + INTV_{CC}$. When the bottom MOSFET switch B turns on, the switch node SW2 drops to low and the boost capacitor $C_B$ is charged through $D_B$ from $INTV_{CC}$. When the top MOSFET switch D turns on, the switch node SW1 rises to $V_{OUT}$ and the BOOST1 pin rises to approximately $V_{OUT} + INTV_{CC}$. When the bottom MOSFET switch C turns on, the switch node SW1 drops to low and the boost capacitor $C_A$ is charged through $D_A$ from $INTV_{CC}$. The boost capacitors $C_A$ and $C_B$ need to store about 100 times the gate charge required by the top MOSFET switch A and D. In most applications a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

### Run Function

The RUN pin provides simple ON/OFF control for the LTC3780. Driving the RUN pin above 1.5V permits the controller to start operating. Pulling RUN below 1.5V puts the LTC3780 into low current shutdown. Do not apply more than 6V to the RUN pin.

### Soft-Start Function

Soft-start reduces the input power sources' surge currents by gradually increasing the controller's current limit (proportional to an internally buffered and clamped equivalent of $V_{ITH}$).

An internal 1.2µA current source charges up the $C_{SS}$ capacitor. As the voltage on SS increases from 0V to 2.4V, the internal current limit rises from $0V/R_{SENSE}$ to $150mV/R_{SENSE}$. The output current limit ramps up slowly, taking 1.5s/µF to reach full current. The output current thus ramps up slowly, eliminating the starting surge current required from the input power supply.

$$T_{IRMP} = \frac{2.4V}{1.2\mu A} \bullet C_{SS} = (1.5s/\mu F) \bullet C_{SS}$$

Do not apply more than 6V to the SS pin.

Current foldback is disabled during soft-start until the voltage on $C_{SS}$ reaches 2V. Make sure $C_{SS}$ is large enough when there is loading during start-up.

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### The Standby Mode (STBYMD) Pin Function

The standby mode (STBYMD) pin provides several choices for start-up and standby operational modes. If the pin is pulled to ground, the SS pin is internally pulled to ground, preventing start-up and thereby providing a single control pin for turning off the controller. If the pin is left open or bypassed to ground with a capacitor, the SS pin is internally provided with a starting current, permitting external control for turning on the controller. If the pin is connected to a voltage greater than 1.25V, the internal regulator ($INTV_{CC}$) will be on even when the controller is shut down (RUN pin voltage < 1.5V). In this mode, the onboard 6V linear regulator can provide power to keep-alive functions such as a keyboard controller.

### Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In boost mode, maximum sense voltage and the sense resistance determines the maximum allowed inductor peak current, which is:

$$I_{L(MAX,BOOST)} = \frac{160mV}{R_{SENSE}}$$

In buck mode, maximum sense voltage and the sense resistance determines the maximum allowed inductor valley current, which is:

$$I_{L(MAX,BUCK)} = \frac{130mV}{R_{SENSE}}$$

To further limit current in the event of a short circuit to ground, the LTC3780 includes foldback current limiting. If the output falls by more than 30%, then the maximum sense voltage is progressively lowered to about one third of its full value.

### Fault Conditions: Overvoltage Protection

A comparator monitors the output for overvoltage conditions. The comparator (OV) detects overvoltage faults greater than 7.5% above the nominal output voltage. When the condition is sensed, switches A and C are turned off, and switches B and D are turned on until the overvoltage condition is cleared. During an overvoltage condition, a negative current limit ($V_{SENSE}$ = –60mV) is set to limit negative inductor current. When the sensed current inductor current is lower than –60mV, switch A and C are turned on, and switch B and D are turned off until the sensed current is higher than –20mV. If the output is still in overvoltage condition, switch A and C are turned off, and switch B and D are turned on again.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuit produce losses, four main sources account for most of the losses in LTC3780 circuits:

1. DC $I^2R$ losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

   $$\text{Transition Loss} \approx 1.7A^{-1} \bullet V_{IN2} \bullet I_{OUT} \bullet C_{RSS} \bullet f$$

   where $C_{RSS}$ is the reverse transfer capacitance.

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3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as an output derived boost network or alternate supply if available.
4. $C_{IN}$ and $C_{OUT}$ loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both $C_{IN}$ and $C_{OUT}$ are required to have low ESR to minimize the AC $I^2R$ loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other losses. Schottky diode D1 and D2 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch C causes reverse recovery current loss in boost mode.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If you make a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

### Design Example

As a design example, assume $V_{IN}$ = 5V to 18V (12V nominal), $V_{OUT}$ = 12V (5%), $I_{OUT(MAX)}$ = 5A and f = 400kHz.

Set the PLLFLTR pin at 2.4V for 400kHz operation. The inductance value is chosen first based on a 30% ripple current assumption. In buck mode, the ripple current is:

$$\Delta I_{L,BUCK} = \frac{V_{OUT}}{f \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{RIPPLE,BUCK} = \frac{\Delta I_{L,BUCK} \bullet 100}{I_{OUT}}\%$$

The highest value of ripple current occurs at the maximum input voltage. In boost mode, the ripple current is:

$$\Delta I_{L,BOOST} = \frac{V_{IN}}{f \bullet L} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

$$I_{RIPPLE,BOOST} = \frac{\Delta I_{L,BOOST} \bullet 100}{I_{IN}}\%$$

The highest value of ripple current occurs at $V_{IN} = V_{OUT}/2$.

A 6.8µH inductor will produce 11% ripple in boost mode ($V_{IN}$ = 6V) and 29% ripple in buck mode ($V_{IN}$ = 18V).

The $R_{SENSE}$ resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances.

$$R_{SENSE} = \frac{2 \bullet 160mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT} + \Delta I_{L,BOOST} \bullet V_{IN(MIN)}}$$

Select an $R_{SENSE}$ of 10mΩ.

Output voltage is 12V. Select R1 as 20k. R2 is:

$$R2 = \frac{V_{OUT} \bullet R1}{0.8} - R1$$

Select R2 as 280k. Both R1 and R2 should have a tolerance of no more than 1%.

Next, choose the MOSFET switches. A suitable choice is the Siliconix Si4840 ($R_{DS(ON)}$ = 0.009Ω (at $V_{GS}$ = 6V), $C_{RSS}$ = 150pF, $\theta_{JA}$ = 40°C/W).

The maximum power dissipation of switch A occurs in boost mode when switch A stays on all the time. Assuming a junction temperature of $T_J$ = 150°C with $\rho_{150°C}$ = 1.5, the power dissipation at $V_{IN}$ = 5V is:

$$P_{A,BOOST} = \left(\frac{12}{5} \bullet 5\right)^2 \bullet 1.5 \bullet 0.009 = 1.94W$$

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Double-check the $T_J$ in the MOSFET with 70°C ambient temperature:

$T_J = 70°C + 1.94W \bullet 40°C/W = 147.6°C$

The maximum power dissipation of switch B occurs in buck mode. Assuming a junction temperature of $T_J = 80°C$ with $\rho_{80°C} = 1.2$, the power dissipation at $V_{IN} = 18V$ is:

$$P_{B,BUCK} = \frac{18-12}{18} \bullet 5^2 \bullet 1.2 \bullet 0.009 = 90mW$$

Double-check the $T_J$ in the MOSFET at 70°C ambient temperature:

$T_J = 70°C + 0.09W \bullet 40°C/W = 73.6°C$

The maximum power dissipation of switch C occurs in boost mode. Assuming a junction temperature of $T_J = 110°C$ with $\rho_{110°C} = 1.4$, the power dissipation at $V_{IN} = 5V$ is:

$$P_{C,BOOST} = \frac{(12-5)\bullet 12}{5^2} \bullet 5^2 \bullet 1.4 \bullet 0.009 + 2 \bullet 12^3 \bullet \frac{5}{5} \bullet 150p \bullet 400k = 1.27W$$

Double-check the $T_J$ in the MOSFET at 70°C ambient temperature:

$T_J = 70°C + 1.08W \bullet 40°C/W = 113°C$

The maximum power dissipation of switch D occurs in boost mode when its duty cycle is higher than 50%. Assuming a junction temperature of $T_J$ = 100°C with $\rho_{100°C} = 1.35$, the power dissipation at $V_{IN} = 5V$ is:

$$P_{D,BOOST} = \frac{5}{12} \bullet \left(\frac{12}{5} \bullet 5\right)^2 \bullet 1.35 \bullet 0.009 = 0.73W$$

Double-check the $T_J$ in the MOSFET at 70°C ambient temperature:

$T_J = 70°C + 0.73W \bullet 40°C/W = 99°C$

$C_{IN}$ is chosen to filter the square current in buck mode. In this mode, the maximum input current peak is:

$$I_{IN,PEAK(MAX,BUCK)} = 5 \bullet \left(1 + \frac{29\%}{2}\right) = 5.7A$$

A low ESR (10mΩ) capacitor is selected. Input voltage ripple is 57mV (assuming ESR dominate ripple).

$C_{OUT}$ is chosen to filter the square current in boost mode. In this mode, the maximum output current peak is:

$$I_{OUT,PEAK(MAX,BOOST)} = \frac{12}{5} \bullet 5 \bullet \left(1 + \frac{11\%}{2}\right) = 10.6A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 53mV (assuming ESR dominate ripple).

### PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
- Place $C_{IN}$, switch A, switch B and D1 in one compact area. Place $C_{OUT}$, switch C, switch D and D2 in one compact area. One layout example is shown in Figure 10.

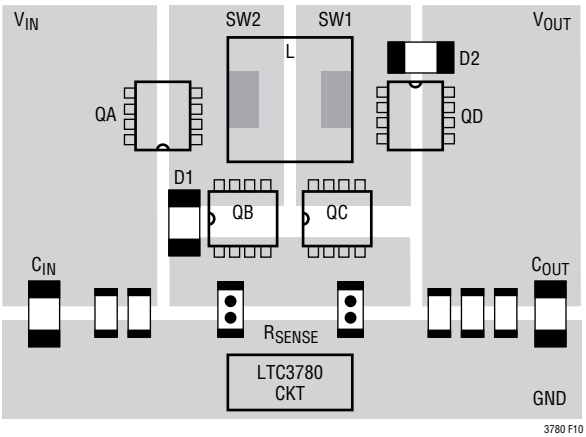


**Figure 10. Switches Layout**

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- Use immediate vias to connect the components (including the LTC3780's SGND and PGND pins) to the ground plane. Use several large vias for each power component.
- Use planes for $V_{IN}$ and $V_{OUT}$ to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net ($V_{IN}$ or GND).
- Segregate the signal and power grounds. All small-signal components should return to the SGND pin at one point, which is then tied to the PGND pin close to the sources of switch B and switch C.
- Place switch B and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Keep the high dV/dT SW1, SW2, BOOST1, BOOST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D1 and the $C_{IN}$ capacitor should have short leads and PC trace lengths. The path formed by switch C, switch D, D2 and the $C_{OUT}$ capacitor also should have short leads and PC trace lengths.
- The output capacitor (–) terminals should be connected as close as possible the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor $C_A$ closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor $C_B$ closely to the BOOST2 and SW2 pins.
- Connect the input capacitors $C_{IN}$ and output capacitors $C_{OUT}$ closely to the power MOSFETs. These capacitors carry the MOSFET AC current in boost and buck mode.
- Connect $V_{OSENSE}$ pin resistive dividers to the (+) terminals of $C_{OUT}$ and signal ground. A small $V_{OSENSE}$ bypass capacitor may be connected closely to the LTC3780 SGND pin. The R2 connection should not be along the high current or noise paths, such as the input capacitors.
- Route $SENSE^-$ and $SENSE^+$ leads together with minimum PC trace spacing. Avoid sense lines pass through noisy area, such as switch nodes. The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor. One layout example is shown in Figure 12.
- Connect the $I_{TH}$ pin compensation network close to the IC, between $I_{TH}$ and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, $C_{VCC}$, close to the IC, between the $INTV_{CC}$ and the power ground pins. This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.

## APPLICATIONS INFORMATION

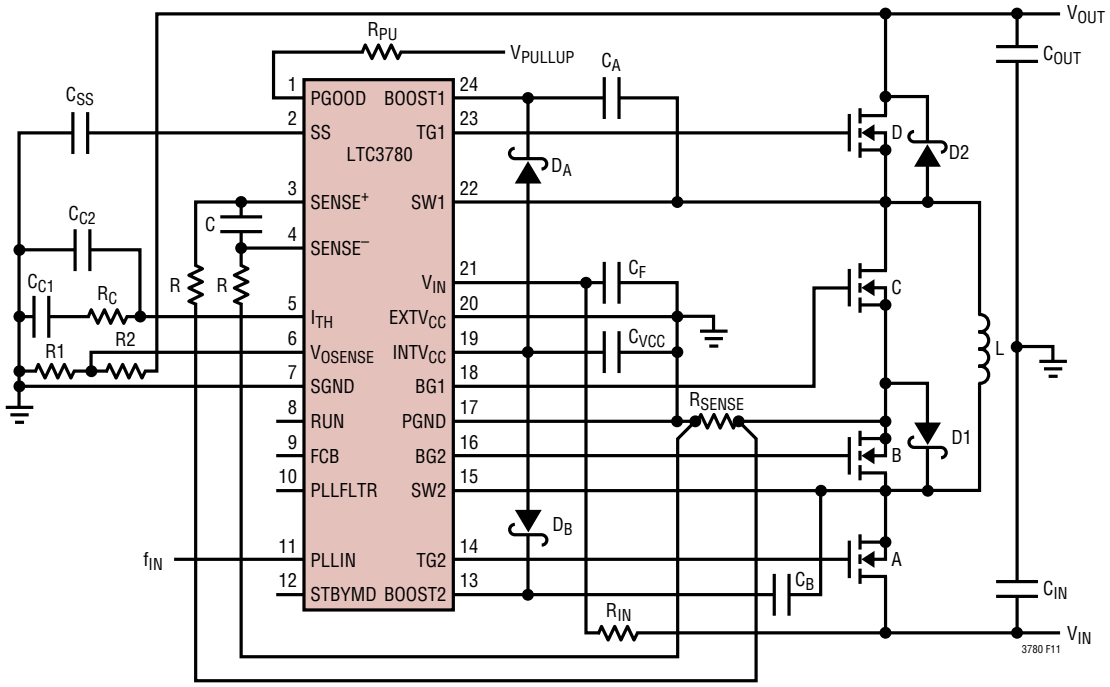



**Figure 11. LTC3780 Layout Diagram**

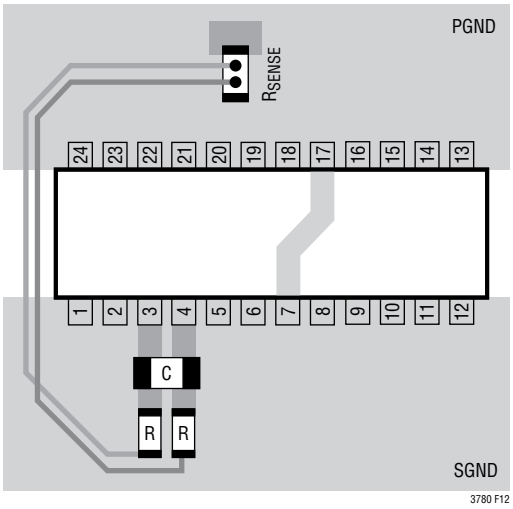
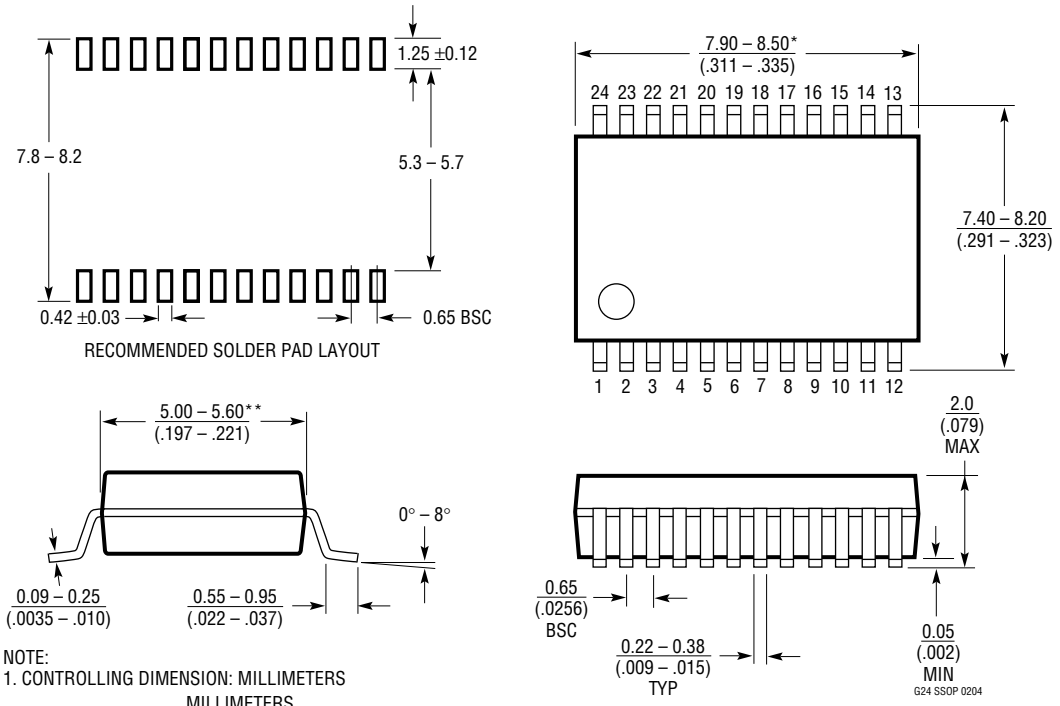



**Figure 12. Sense Lines Layout**

# PACKAGE DESCRIPTION

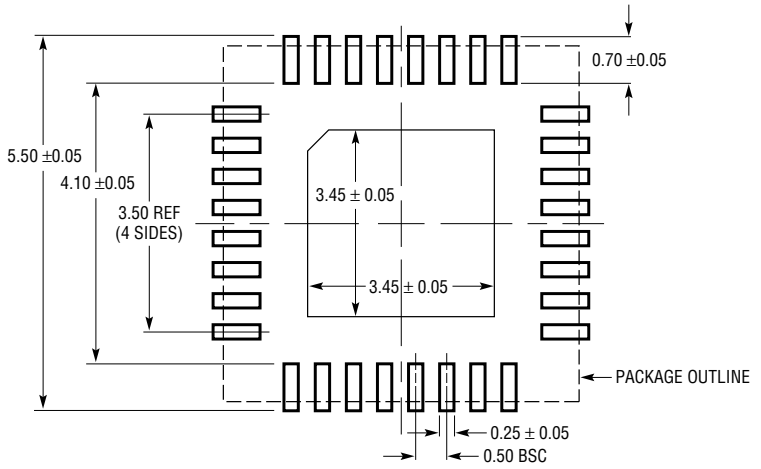
**G Package**
**24-Lead Plastic SSOP (5.3mm)**
(Reference LTC DWG # 05-08-1640)




NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

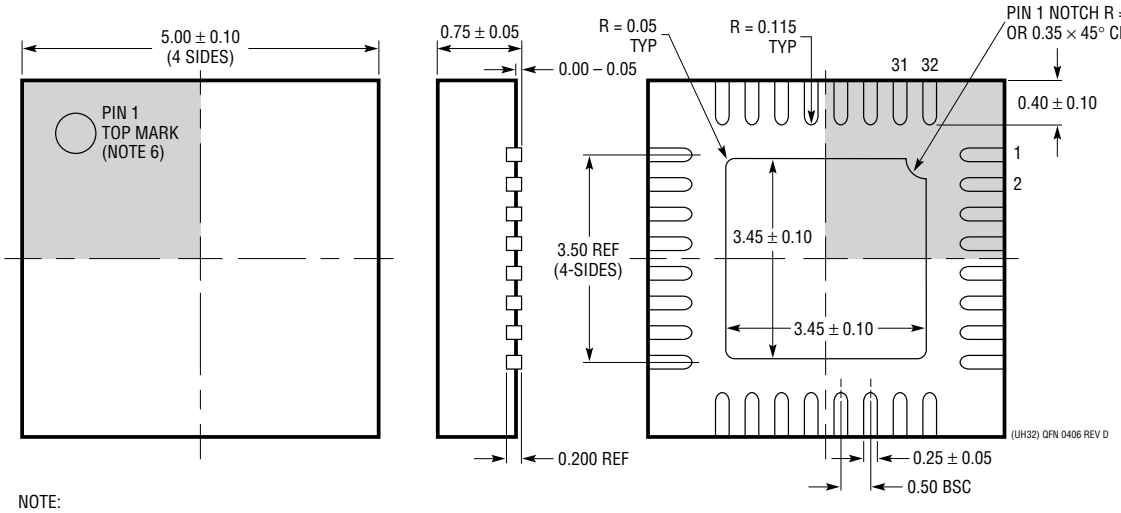
# PACKAGE DESCRIPTION

**UH Package**
**32-Lead Plastic QFN (5mm × 5mm)**
(Reference LTC DWG # 05-08-1693 Rev D)




RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD




NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY (Revision history begins at Rev F)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| F | 4/13 | Updated Note 7, fixed typos | 2, 3, 4, 5 |
| G | 2/19 | Added MP-Grade/Lead Free part number | 3 |