No R_{SENSE} Current Mode Boost DC/DC Controller

FEATURES

- **No Current Sense Resistor Required**
- **V_{OUT} up to 60V**
- **Constant Frequency 550kHz Operation**
- **Internal Soft-Start and Optional External Soft-Start**
- Adjustable Current Limit
- Pulse Skipping at Light Load
- V_{IN} Range: 2.75V to 9.8V
- ±1.5% Voltage Reference Accuracy
- Current Mode Operation for Excellent Line and Load Transient Response
- Low Profile (1mm) SOT-23 and 2mm × 3mm DFN Packages

APPLICATIONS

- Telecom Power Supplies
- 42V Automotive Systems
- 24V Industrial Controls
- IP Phone Power Supplies

DESCRIPTION

The LTC®3872-1 is a constant frequency current mode boost DC/DC controller that drives an N-channel power MOSFET and requires very few external components. The No R_{SENSE}™ architecture eliminates the need for a sense resistor, improves efficiency and saves board space.

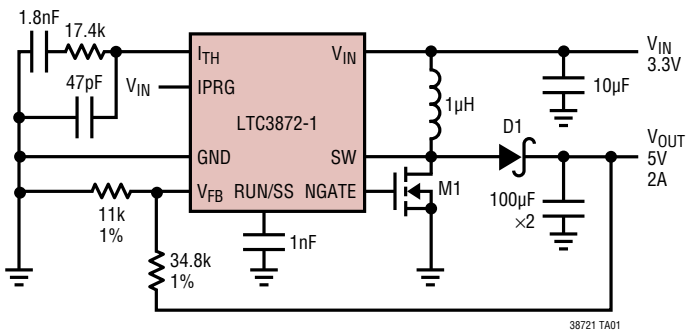
The LTC3872-1 provides excellent AC and DC load and line regulation with ±1.5% output voltage accuracy. It incorporates an undervoltage lockout feature that shuts down the device when the input voltage falls below 2.3V.

LTC3872-1 has the same functionality as the standard LTC3872 except that it has no frequency foldback in current limit.

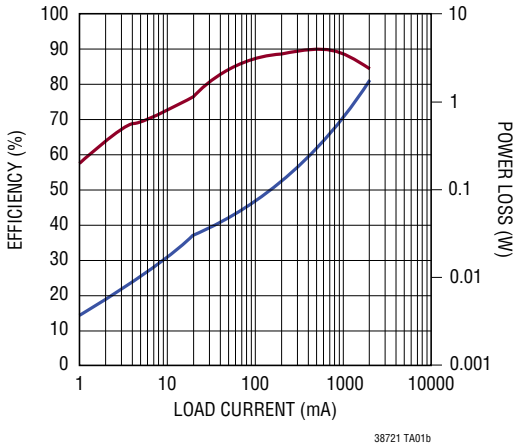
High switching frequency of 550kHz allows the use of a small inductor. The LTC3872-1 is available in an 8-lead low profile (1mm) ThinSOT™ package and 8-pin 2mm × 3mm DFN package.

TYPICAL APPLICATION

High Efficiency 3.3V Input, 5V Output Boost Converter



Efficiency and Power Loss vs Load Current

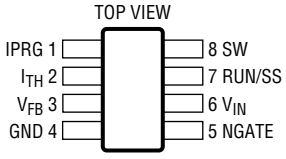


ABSOLUTE MAXIMUM RATINGS (Note 1)

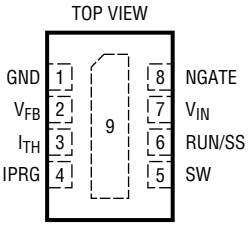
Input Supply Voltage (V_{IN}), RUN/SS ..... –0.3V to 10V
IPRG Voltage ..... –0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH} Voltages ..... –0.3V to 2.4V
SW Voltage ..... –0.3V to 60V

Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
TS8 Package ..... 300°C

PIN CONFIGURATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 150°C, θ_{JA} = 195°C/W



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3872ETS8-1#PBF	LTC3872ETS8-1#TRPBF	LTCFN	8-Lead Plastic TSOT-23	–40°C to 85°C
LTC3872ITS8-1#PBF	LTC3872ITS8-1#TRPBF	LTCFN	8-Lead Plastic TSOT-23	–40°C to 125°C
LTC3872HTS8-1#PBF	LTC3872HTS8-1#TRPBF	LTCFN	8-Lead Plastic TSOT-23	–40°C to 150°C
LTC3872EDDB-1#PBF	LTC3872EDDB-1#TRPBF	LCFK	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3872IDDB-1#PBF	LTC3872IDDB-1#TRPBF	LCFK	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC3872HDDB-1#PBF	LTC3872HDDB-1#TRPBF	LCFK	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 4.2V unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Voltage Range			●	2.75		9.8	V
Input DC Supply Current Normal Operation Shutdown UVLO	Typicals at V_{IN} = 4.2V (Note 4) 2.75V ≤ V_{IN} ≤ 9.8V $V_{RUN/SS}$ = 0V V_{IN} < UVLO Threshold				 250 8 20	 400 20 35	 µA µA µA
Undervoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		● ●	2.3 2.05	2.45 2.3	2.75 2.55	V V
Shutdown Threshold (at RUN/SS)	$V_{RUN/SS}$ Falling $V_{RUN/SS}$ Rising		● ●	0.6 0.65	0.85 0.95	1.05 1.15	V V
Regulated Feedback Voltage	(Note 5) LTC3872-1E LTC3872-1I and LTC3872-1H		● ●	1.182 1.178	1.2 1.2	1.218 1.218	V V
Feedback Voltage Line Regulation	2.75V < V_{IN} < 9V (Note 5)				0.14		mV/V
Feedback Voltage Load Regulation	V_{ITH} = 1.6V (Note 5) V_{ITH} = 1V (Note 5)				0.05 –0.05		% %
V_{FB} Input Current	(Note 5)				25	50	nA
RUN/SS Pull Up Current	$V_{RUN/SS}$ = 0			0.35	0.7	1.25	µA
Oscillator Frequency Normal Operation	 V_{FB} = 1V			 500	 550	 650	 kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF				40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF				40		ns
Peak Current Sense Voltage	IPRG = GND (Note 6)	LTC3872-1E LTC3872-1I LTC3872-1H	● ● ●	90 85 80	105 105 105	120 120 120	mV mV mV
	IPRG = Float	LTC3872-1E LTC3872-1I LTC3872-1H	● ● ●	160 150 145	180 180 180	200 200 200	mV mV mV
	IPRG = V_{IN}	LTC3872-1E LTC3872-1I LTC3872-1H	● ● ●	260 250 240	285 285 285	310 310 310	mV mV mV
Default Internal Soft-Start Time					1		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3872-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3872-1E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3872-1I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3872-1H is guaranteed over the full –40°C to 150°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3872-1TS8: $T_J = T_A + (P_D \bullet 195°C/W)$

LTC3872-1DDB: $T_J = T_A + (P_D \bullet 76°C/W)$

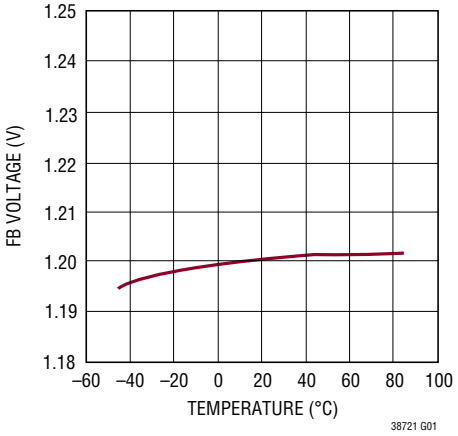
Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information.

Note 5: The LTC3872-1 is tested in a feedback loop which servos V_{FB} to the reference voltage with the I_{TH} pin forced to the midpoint of its voltage range (0.7V ≤ V_{ITH} ≤ 1.9V, midpoint = 1.3V).

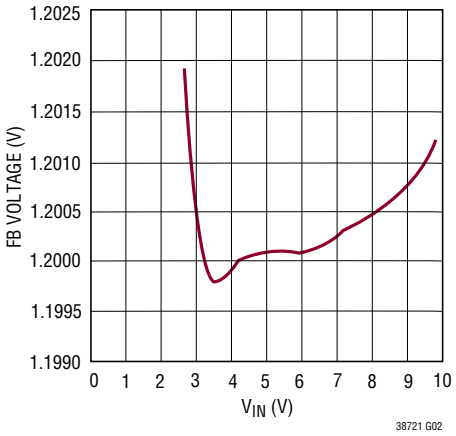
Note 6: Rise and fall times are measured at 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

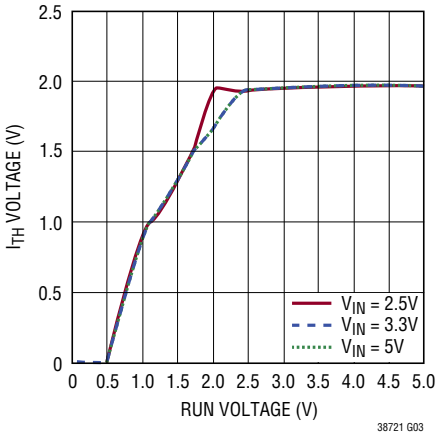
FB Voltage vs Temperature



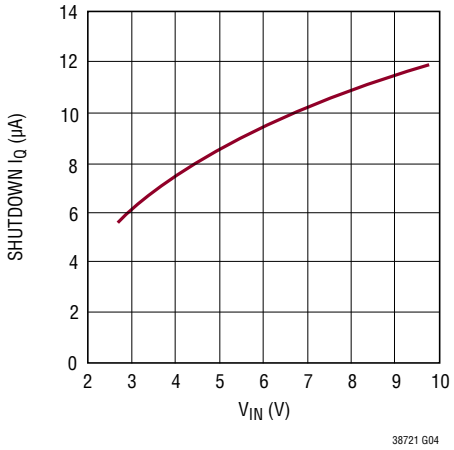
FB Voltage Line Regulation



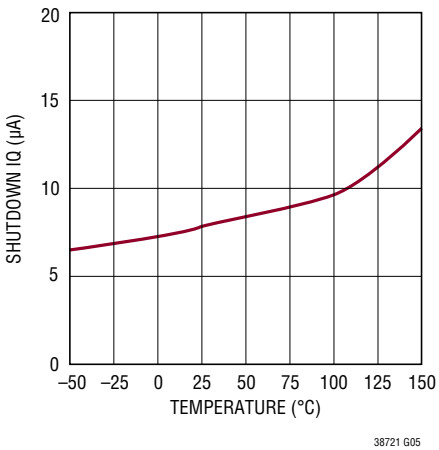
I_{TH} Voltage vs RUN/SS Voltage



Shutdown I_Q vs V_{IN}

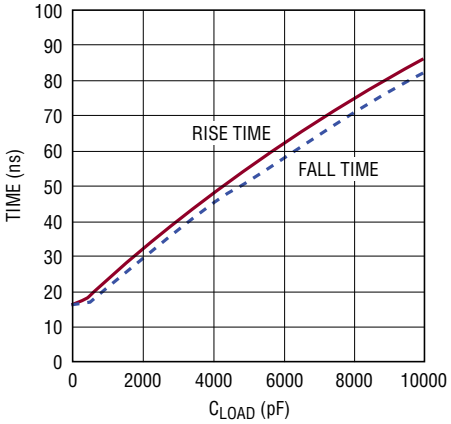


Shutdown I_Q vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Gate Drive Rise and Fall Time vs C_{LOAD}



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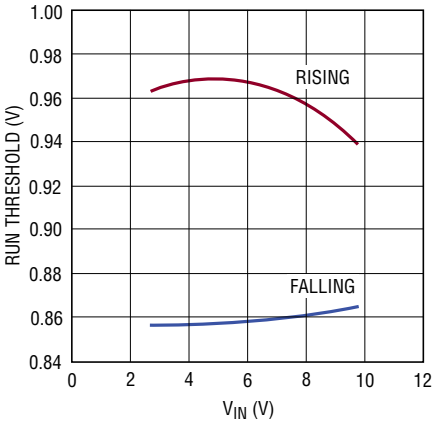
RUN/SS Threshold vs V_{IN}



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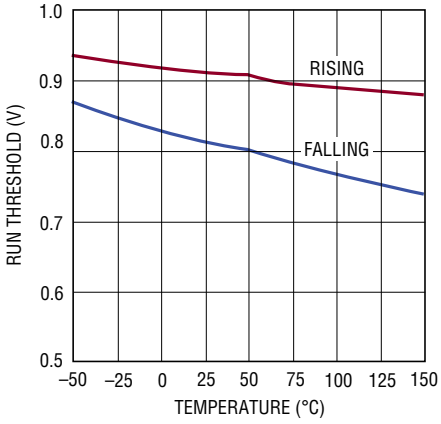
RUN/SS Threshold vs Temperature



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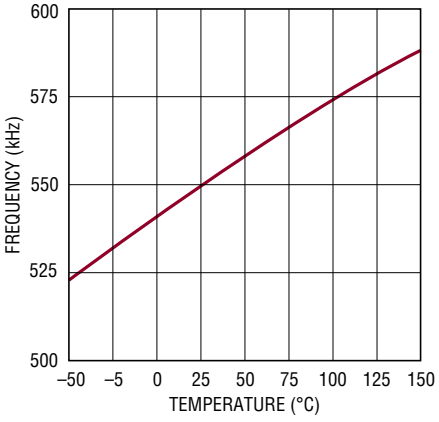
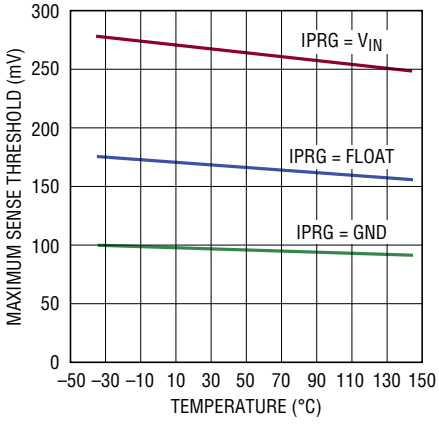
Frequency vs Temperature



38721 G09

Maximum Sense Threshold vs Temperature



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PIN FUNCTIONS (TS8/DD8)

IPRG (Pin 1/Pin 4): Current Sense Limit Select Pin.

I_{TH} (Pin 2/Pin 3): Error Amplifier Compensation Point. Nominal voltage range for this pin is 0.7V to 1.9V.

V_{FB} (Pin 3/Pin 2): Receives the feedback voltage from an external resistor divider across the output.

GND (Pin 4/Pin 1, Exposed Pad Pin 9): Ground. The exposed pad must be soldered to PCB ground for electrical contact and rated thermal performance.

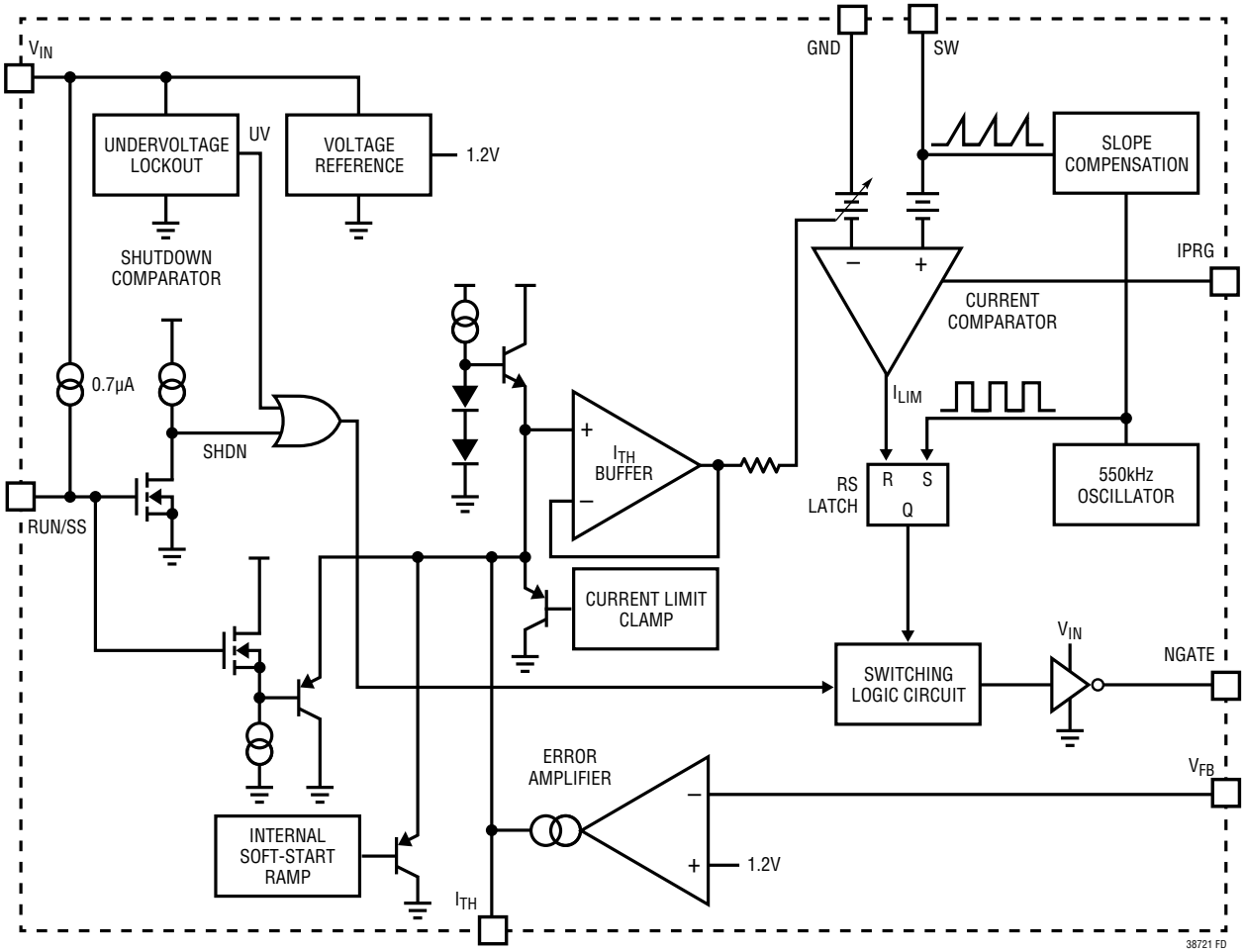
NGATE (Pin 5/Pin 8): Gate Drive for the External N-Channel MOSFET. This pin swings from 0V to V_{IN}.

V_{IN} (Pin 6/Pin 7): Supply Pin. This pin must be closely decoupled to GND.

RUN/SS (Pin 7/Pin 6): Shutdown and external soft-start pin. In shutdown, all functions are disabled and the NGATE pin is held low.

SW (Pin 8/Pin 5): Switch node connection to inductor and current sense input pin through external slope compensation resistor. Normally, the external N-channel MOSFET's drain is connected to this pin.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3872-1 is a No R_{SENSE} constant frequency, current mode controller for DC/DC boost, SEPIC and flyback converter applications. The LTC3872-1 is distinguished from conventional current mode controllers because the current control loop can be closed by sensing the voltage drop across the power MOSFET switch or across a discrete sense resistor, as shown in Figures 1 and 2. This No R_{SENSE} sensing technique improves efficiency, increases power density and reduces the cost of the overall solution.

For circuit operation, please refer to the Block Diagram of the IC and the Typical Application on the front page. In normal operation, the power MOSFET is turned on when the oscillator sets the RS latch and is turned off when the current comparator resets the latch. The divided-down output voltage is compared to an internal 1.2V reference by the error amplifier, which outputs an error signal at the I_{TH} pin. The voltage on the I_{TH} pin sets the current comparator input threshold. When the load current increases, a fall in the FB voltage relative to the reference voltage causes the I_{TH} pin to rise, which causes the current comparator to trip at a higher peak inductor current value. The average inductor current will therefore rise until it equals the load current, thereby maintaining output regulation.

The LTC3872-1 can be used either by sensing the voltage drop across the power MOSFET or by connecting the SW pin to a conventional sensing resistor in the source of the power MOSFET. Sensing the voltage across the power MOSFET maximizes converter efficiency and minimizes the component count; the maximum rating for this pin, 60V, allows MOSFET sensing in a wide output voltage range.

The RUN/SS pin controls whether the IC is enabled or is in a low current shutdown state. With the RUN/SS pin below 0.85V, the chip is off and the input supply current is typically only 8µA. With an external capacitor connected to the RUN/SS pin an optional external soft-start is enabled. A 0.7µA trickle current will charge the capacitor, pulling the RUN/SS pin above shutdown threshold and slowly ramping RUN/SS to limit the V_{ITH} during start-up. Because the noise on the SW pin could couple into the RUN/SS pin, disrupting the trickle charge current that charges the RUN/SS pin, a 1M resistor is recommended to pull-up the RUN/SS pin when external soft-start is used. When RUN/SS is driven by an external logic, a minimum of 2.75V logic is recommended to allow the maximum I_{TH} range.

Light Load Operation

Under very light load current conditions, the I_{TH} pin voltage will be very close to the zero current level of 0.85V. As the load current decreases further, an internal offset at the current comparator input will assure that the current comparator remains tripped (even at zero load current) and the regulator will start to skip cycles, as it must, in order to maintain regulation. This behavior allows the regulator to maintain constant frequency down to very light loads, resulting in low output ripple as well as low audible noise and reduced RF interference, while providing high light load efficiency.

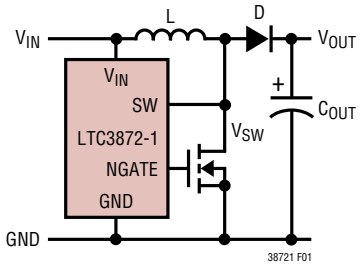


Figure 1. SW Pin (Internal Sense Pin) Connection for Maximum Efficiency

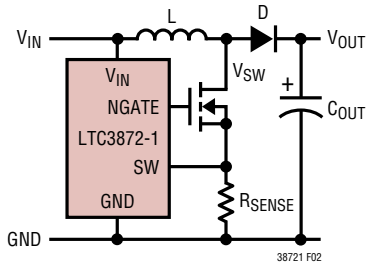


Figure 2. SW Pin (Internal Sense Pin) Connection for Sensing Resistor

APPLICATIONS INFORMATION

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

$$V_O = 1.2V \bullet \left(1 + \frac{R2}{R1}\right)$$

The external resistor divider is connected to the output as shown in the Typical Application on the front page, allowing remote voltage sensing.

Application Circuits

A basic LTC3872-1 application circuit is shown on the front page of this data sheet. External component selection is driven by the characteristics of the load and the input supply.

Duty Cycle Considerations

For a boost converter operating in a continuous conduction mode (CCM), the duty cycle of the main switch is:

$$D = \left(\frac{V_O + V_D - V_{IN}}{V_O + V_D}\right)$$

where V_D is the forward voltage of the boost diode. For converters where the input voltage is close to the output voltage, the duty cycle is low and for converters that develop a high output voltage from a low; voltage input supply, the duty cycle is high. The minimum on-time of the LTC3872-1 is typically around 250ns. This time limits the minimum duty cycle of the LTC3872-1. The maximum duty cycle of the LTC3872-1 is around 90%. Although frequency foldback feature of the regular LTC3872 enables the user to obtain higher output voltage, it also increases inductor ripple current.

The Peak and Average Input Currents

The control circuit in the LTC3872-1 is measuring the input current (either by using the $R_{DS(ON)}$ of the power MOSFET or by using a sense resistor in the MOSFET source), so the output current needs to be reflected back to the input in order to dimension the power MOSFET properly. Based on the fact that, ideally, the output power is equal to the input power, the maximum average input current is:

$$I_{IN(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The peak input current is:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

Ripple Current I_L and the χ Factor

The constant χ in the equation above represents the percentage peak-to-peak ripple current in the inductor, relative to its maximum value. For example, if 30% ripple current is chosen, then χ = 0.30, and the peak current is 15% greater than the average.

For a current mode boost regulator operating in CCM, slope compensation must be added for duty cycles above 50% in order to avoid subharmonic oscillation. For the LTC3872-1, this ramp compensation is internal. Having an internally fixed ramp compensation waveform, however, does place some constraints on the value of the inductor and the operating frequency. If too large an inductor is used, the resulting current ramp (I_L) will be small relative to the internal ramp compensation (at duty cycles above 50%), and the converter operation will approach voltage mode (ramp compensation reduces the gain of the current loop). If too small an inductor is used, but the converter is still operating in CCM (continuous conduction mode), the internal ramp compensation may be inadequate to prevent subharmonic oscillation. To ensure good current mode gain and avoid subharmonic oscillation, it is recommended that the ripple current in the inductor fall in the range of 20% to 40% of the maximum average current. For example, if the maximum average input current is 1A, choose an I_L between 0.2A and 0.4A, and a value χ between 0.2 and 0.4.

Inductor Selection

Given an operating input voltage range, and having chosen the operating frequency and ripple current in the inductor,

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the inductor value can be determined using the following equation:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

where:

$$\Delta I_L = \chi \bullet \frac{I_{O(MAX)}}{1-D_{MAX}}$$

Remember that boost converters are **not** short-circuit protected. Under a shorted output condition, the inductor current is limited only by the input supply capability.

The minimum required saturation current of the inductor can be expressed as a function of the duty cycle and the load current, as follows:

$$I_{L(SAT)} \geq \left(1+\frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1-D_{MAX}}$$

The saturation current rating for the inductor should be checked at the minimum input voltage (which results in the highest inductor current) and maximum output current.

Operating in Discontinuous Mode

Discontinuous mode operation occurs when the load current is low enough to allow the inductor current to run out during the off-time of the switch. Once the inductor current is near zero, the switch and diode capacitances resonate with the inductance to form damped ringing at 1MHz to 10MHz. If the off-time is long enough, the drain voltage will settle to the input voltage.

Depending on the input voltage and the residual energy in the inductor, this ringing can cause the drain of the power MOSFET to go below ground where it is clamped by the body diode. This ringing is not harmful to the IC and it has been shown not to contribute significantly to EMI. Any attempt to damp it with a snubber will degrade the efficiency.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore, copper losses will increase. Generally, there is a tradeoff between core losses and copper losses that needs to be balanced.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper losses and preventing saturation. Ferrite core material saturates "hard," meaning that the inductance collapses rapidly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently, output voltage ripple. **Do not allow the core to saturate!**

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko and Sumida.

Power MOSFET Selection

The power MOSFET serves two purposes in the LTC3872-1: it represents the main switching element in the power path and its $R_{DS(ON)}$ represents the current sensing element for the control loop. Important parameters for the power MOSFET include the drain-to-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$) versus gate-to-source voltage, the gate-to-source and gate-to-drain charges (Q_{GS} and Q_{GD}, respectively), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{TH(JC)}$ and $R_{TH(JA)}$). Logic-level (4.5V $V_{GS-RATED}$) threshold MOSFETs should be used when input voltage is high, otherwise if low input voltage operation is expected (e.g., supplying power from a lithium-ion battery or a 3.3V logic supply), then sublogic-level (2.5V $V_{GS-RATED}$) threshold MOSFETs should be used.

Pay close attention to the BV_{DSS} specifications for the MOSFETs relative to the maximum actual switch voltage in the application. Many logic-level devices are limited

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to 30V or less, and the switch node can ring during the turn-off of the MOSFET due to layout parasitics. Check the switching waveforms of the MOSFET directly across the drain and source terminals using the actual PC board layout (not just on a lab breadboard!) for excessive ringing.

During the switch on-time, the control circuit limits the maximum voltage drop across the power MOSFET to about 285mV, 105mV and 185mV at low duty cycle with IPRG tied to V_{IN}, GND, or left floating respectively. The peak inductor current is therefore limited to (285mV, 105mV and 185mV)/$R_{DS(ON)}$ depending on the status of the IPRG pin.

The relationship between the maximum load current, duty cycle and the $R_{DS(ON)}$ of the power MOSFET is:

$$R_{DS(ON)} \le V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \rho_T}$$

$V_{SENSE(MAX)}$ is the maximum voltage drop across the power MOSFET. $V_{SENSE(MAX)}$ is typically 285mV, 185mV and 105mV. It is reduced with increasing duty cycle as shown in Figure 3. The ρ_T term accounts for the temperature coefficient of the $R_{DS(ON)}$ of the MOSFET, which is typically 0.4%/°C. Figure 4 illustrates the variation of normalized $R_{DS(ON)}$ over temperature for a typical power MOSFET.

Another method of choosing which power MOSFET to use is to check what the maximum output current is for a given $R_{DS(ON)}$, since MOSFET on-resistances are available in discrete values.

$$I_{O(MAX)} = V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right)\bullet R_{DS(ON)} \bullet \rho_T}$$

It is worth noting that the $1 - D_{MAX}$ relationship between $I_{O(MAX)}$ and $R_{DS(ON)}$ can cause boost converters with a wide input range to experience a dramatic range of maximum input and output current. This should be taken into consideration in applications where it is important to limit the maximum current drawn from the input supply.

Voltage on the NGATE pin should be within –0.3V to (V_{IN} + 0.3V) limits. Voltage stress below –0.3V and above V_{IN} + 0.3V can damage internal MOSFET driver, see Functional Diagram. This is especially important in case of driving MOSFETs with relatively high package inductance (DPAK and bigger) or inadequate layout. A small Schottky diode between NGATE pin and ground can prevent negative voltage spikes. Two small Schottky diodes can inhibit positive and negative voltage spikes (Figure 5).

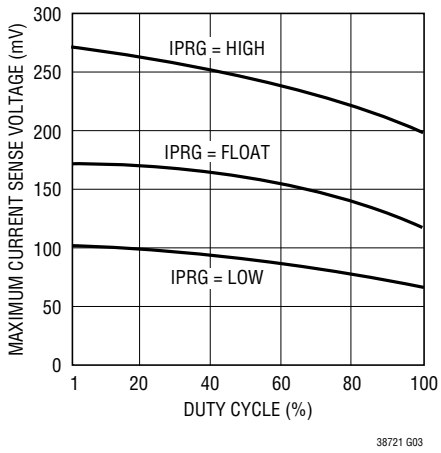

Figure 3. Maximum SENSE Threshold Voltage vs Duty Cycle

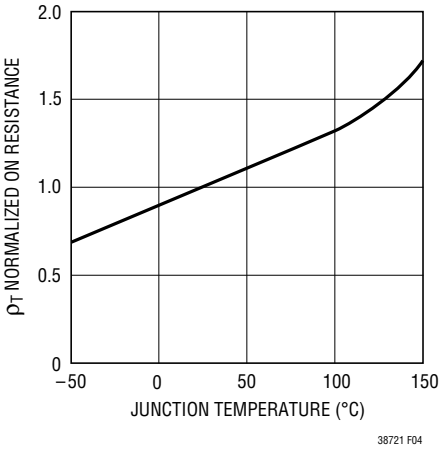

Figure 4. Normalized $R_{DS(ON)}$ vs Temperature

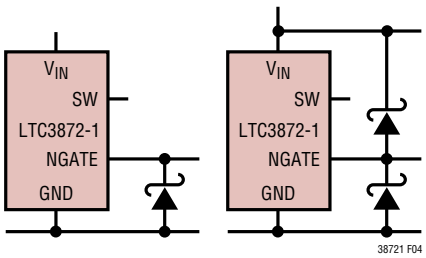

Figure 5

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Calculating Power MOSFET Switching and Conduction Losses and Junction Temperatures

In order to calculate the junction temperature of the power MOSFET, the power dissipated by the device must be known. This power dissipation is a function of the duty cycle, the load current and the junction temperature itself (due to the positive temperature coefficient of its $R_{DS(ON)}$). As a result, some iterative calculation is normally required to determine a reasonably accurate value. Since the controller is using the MOSFET as both a switching and a sensing element, care should be taken to ensure that the converter is capable of delivering the required load current over all operating conditions (line voltage and temperature), and for the worst-case specifications for $V_{SENSE(MAX)}$ and the $R_{DS(ON)}$ of the MOSFET listed in the manufacturer's data sheet.

The power dissipated by the MOSFET in a boost converter is:

$$P_{FET} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T$$

$$+k \bullet V_O{}^{1.85} \bullet \frac{I_{O(MAX)}}{(1-D_{MAX})} \bullet C_{RSS} \bullet f$$

The first term in the equation above represents the I^2R losses in the device, and the second term, the switching losses. The constant, k = 1.7, is an empirical factor inversely related to the gate drive current and has the dimension of 1/current.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P_{FET} \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(CA)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Output Diode Selection

To maximize efficiency, a fast switching diode with low forward drop and low reverse leakage is desired. The output diode in a boost converter conducts current during the switch off-time. The peak reverse voltage that the diode must withstand is equal to the regulator output voltage. The average forward current in normal operation is equal to the output current, and the peak current is equal to the peak inductor current.

$$I_{D(PEAK)} = I_{L(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1-D_{MAX}}$$

The power dissipated by the diode is:

$$P_D = I_{O(MAX)} \bullet V_D$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in this equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the board to the ambient temperature in the enclosure.

Remember to keep the diode lead lengths short and to observe proper switch-node layout (see Board Layout Checklist) to avoid excessive ringing and increased dissipation.

Output Capacitor Selection

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct component for a given output ripple voltage. The effects of these three parameters (ESR, ESL and bulk C) on the output voltage ripple waveform are illustrated in Figure 6e for a typical boost converter.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} \le \frac{0.01 \bullet V_O}{I_{IN(PEAK)}}$$

APPLICATIONS INFORMATION

where:

$$I_{IN(PEAK)} = \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

For the bulk C component, which also contributes 1% to the total ripple:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet V_O \bullet f}$$

For many designs it is possible to choose a single capacitor type that satisfies both the ESR and bulk C requirements for the design. In certain demanding applications, however, the ripple voltage can be improved significantly by connecting two or more types of capacitors in parallel. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

Once the output capacitor ESR and bulk capacitance have been determined, the overall ripple voltage waveform should be verified on a dedicated PC board (see Board Layout section for more information on component placement). Lab breadboards generally suffer from excessive series inductance (due to inter-component wiring), and these parasitics can make the switching waveforms look significantly worse than they would be on a properly designed PC board.

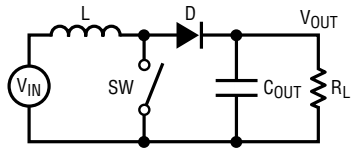
The output capacitor in a boost regulator experiences high RMS ripple currents, as shown in Figure 7. The RMS output capacitor ripple current is:

$$I_{RMS(COUT)} \approx I_{O(MAX)} \bullet \sqrt{\frac{V_O - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

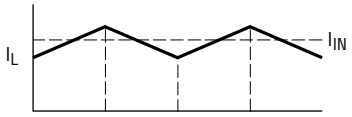
Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Manufacturers such as Nichicon, United Chemicon and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic, at a somewhat higher price.

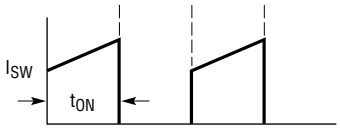
In surface mount applications, multiple capacitors may have to be placed in parallel in order to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount packages. In the case of tantalum, it is critical that the capacitors have been surge tested for use in switching power supplies. An excellent choice is AVX TPS series of surface mount tantalum. Also, ceramic capacitors are now available with extremely low ESR, ESL and high ripple current ratings.



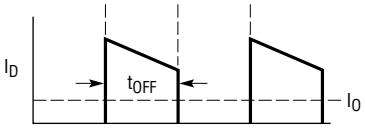
6a. Circuit Diagram



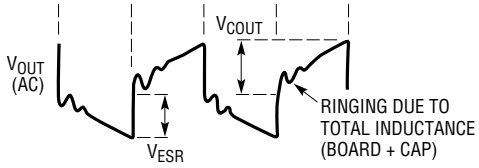
6b. Inductor and Input Currents



6c. Switch Current



6d. Diode and Output Currents



6e. Output Voltage Ripple Waveform

Figure 6. Switching Waveforms for a Boost Converter

APPLICATIONS INFORMATION

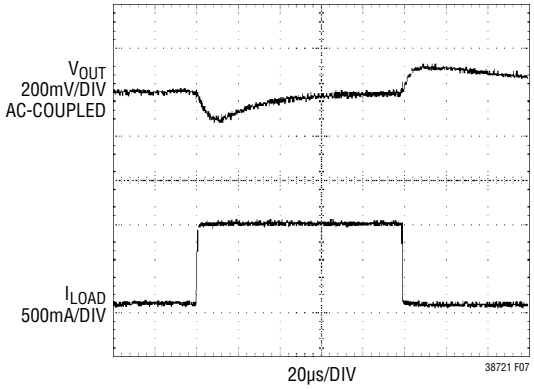


Figure 7. Load Transient Response for a 3.3V Input, 5V Output Boost Converter Application, 0.1A to 1A Step

Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input and the input current waveform is continuous (see Figure 6b). The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended, although it is not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3 \bullet \frac{V_{IN(MIN)}}{L \bullet f} \bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. **Be sure to specify surge-tested capacitors!**

Efficiency Considerations: How Much Does VDS Sensing Help?

The efficiency of a switching regulator is equal to the output power divided by the input power (×100%).

Percent efficiency can be expressed as:

% Efficiency = 100% – (L1 + L2 + L3 + …),

where L1, L2, etc. are the individual loss components as a percentage of the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for the majority of the losses in LTC3872-1 application circuits:

1. The supply current into V_{IN}. The V_{IN} current is the sum of the DC supply current I_Q (given in the Electrical Characteristics) and the MOSFET driver and control currents. The DC supply current into the V_{IN} pin is typically about 250µA and represents a small power loss (much less than 1%) that increases with V_{IN}. The driver current results from switching the gate capacitance of the power MOSFET; this current is typically much larger than the DC current. Each time the MOSFET is switched on and then off, a packet of gate charge Q_G is transferred from V_{IN} to ground. The resulting dQ/dt is a current that must be supplied to the Input capacitor by an external supply. If the IC is operating in CCM:

$$I_{Q(TOT)} \approx I_Q = f \bullet Q_G$$

$$P_{IC} = V_{IN} \bullet (I_Q + f \bullet Q_G)$$

2. Power MOSFET switching and conduction losses. The technique of using the voltage drop across the power MOSFET to close the current feedback loop was chosen because of the increased efficiency that results from not having a sense resistor. The losses in the power MOSFET are equal to:

$$P_{FET} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{DS(ON)} \bullet D_{MAX} \bullet \rho_T + k \bullet V_O{}^{1.85} \bullet \frac{I_{O(MAX)}}{1-D_{MAX}} \bullet C_{RSS} \bullet f$$

The I^2R power savings that result from not having a discrete sense resistor can be calculated almost by inspection.

$$P_{R(SENSE)} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_{SENSE} \bullet D_{MAX}$$

To understand the magnitude of the improvement with this V_{DS} sensing technique, consider the 3.3V input, 5V output power supply shown in the Typical Application on the front page. The maximum load current is 7A (10A peak) and the duty cycle is 39%. Assuming a ripple current of 40%, the peak inductor current is 13.8A and the average

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is 11.5A. With a maximum sense voltage of about 140mV, the sense resistor value would be 10mΩ, and the power dissipated in this resistor would be 514mW at maximum output current. Assuming an efficiency of 90%, this sense resistor power dissipation represents 1.3% of the overall input power. In other words, for this application, the use of V_{DS} sensing would increase the efficiency by approximately 1.3%.

For more details regarding the various terms in these equations, please refer to the section Boost Converter: Power MOSFET Selection.

3. The losses in the inductor are simply the DC input current squared times the winding resistance. Expressing this loss as a function of the output current yields:

$$P_{R(WINDING)} = \left(\frac{I_{O(MAX)}}{1-D_{MAX}}\right)^2 \bullet R_W$$

4. Losses in the boost diode. The power dissipation in the boost diode is:

$$P_{DIODE} = I_{O(MAX)} \bullet V_D$$

The boost diode can be a major source of power loss in a boost converter. For the 3.3V input, 5V output at 7A example given above, a Schottky diode with a 0.4V forward voltage would dissipate 2.8W, which represents 7% of the input power. Diode losses can become significant at low output voltages where the forward voltage is a significant percentage of the output voltage.

5. Other losses, including C_{IN} and C_O ESR dissipation and inductor core losses, generally account for less than 2% of the total additional loss.

Checking Transient Response

The regulator loop response can be verified by looking at the load transient response. Switching regulators generally take several cycles to respond to an instantaneous step in resistive load current. When the load step occurs, V_O immediately shifts by an amount equal to $(\Delta I_{LOAD})(ESR)$, and then C_O begins to charge or discharge (depending on the direction of the load step) as shown in Figure 7. The regulator feedback loop acts on the resulting error amp output signal to return V_O to its steady-state value. During this recovery time, V_O can be monitored for overshoot or ringing that would indicate a stability problem.

A second, more severe transient can occur when connecting loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_O, causing a nearly instantaneous drop in V_O. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive in order to limit the inrush current di/dt to the load.

Boost Converter Design Example

The design example given here will be for the circuit shown on the front page. The input voltage is 3.3V, and the output is 5V at a maximum load current of 2A.

1. The duty cycle is:

$$D = \left(\frac{V_O + V_D - V_{IN}}{V_O + V_D}\right) = \frac{5+0.4-3.3}{5+0.4} = 38.9\%$$

2. An inductor ripple current of 40% of the maximum load current is chosen, so the peak input current (which is also the minimum saturation current) is:

$$I_{IN(PEAK)} = \left(1+\frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1-D_{MAX}} = 1.2 \bullet \frac{2}{1-0.39} = 3.9A$$

The inductor ripple current is:

$$\Delta I_L = \chi \bullet \frac{I_{O(MAX)}}{1-D_{MAX}} = 0.4 \bullet \frac{2}{1-0.39} = 1.3A$$

And so the inductor value is:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX} = \frac{3.3V}{1.3A \bullet 550kHz} \bullet 0.39 = 1.8\mu H$$

The component chosen is a 2.2µH inductor made by Sumida (part number CEP125-H 1ROMH).

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3. Assuming a MOSFET junction temperature of 125°C, the room temperature MOSFET $R_{DS(ON)}$ should be less than:

$$R_{DS(ON)} \le V_{SENSE(MAX)} \bullet \frac{1-D_{MAX}}{\left(1+\frac{\chi}{2}\right)\bullet I_{O(MAX)} \bullet \rho_T}$$

$$= 0.175V \bullet \frac{1-0.39}{\left(1+\frac{0.4}{2}\right)\bullet 2A \bullet 1.5} \approx 30m\Omega$$

The MOSFET used was the Si3460 DDV, which has a maximum $R_{DS(ON)}$ of 27mΩ at 4.5V V_{GS}, a BV_{DSS} of greater than 30V, and a gate charge of 13.5nC at 4.5V V_{GS}.

4. The diode for this design must handle a maximum DC output current of 2A and be rated for a minimum reverse voltage of V_{OUT}, or 5V. A 25A, 15V diode from On Semiconductor (MBRB2515L) was chosen for its high power dissipation capability.

5. The output capacitor usually consists of a lower valued, low ESR ceramic.

6. The choice of an input capacitor for a boost converter depends on the impedance of the source supply and the amount of input ripple the converter will safely tolerate. For this particular design two 22µF Taiyo Yuden ceramic capacitors (JMK325BJ226MM) are required (the input and return lead lengths are kept to a few inches). As with the output node, check the input ripple with a single oscilloscope probe connected across the input capacitor terminals.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3872-1. These items are illustrated graphically in the layout diagram in Figure 8. Check the following in your layout:

1. The Schottky diode should be closely connected between the output capacitor and the drain of the external MOSFET.

2. The input decoupling capacitor (0.1µF) should be connected closely between V_{IN} and GND.

3. The trace from SW to the switch point should be kept short.

4. Keep the switching node NGATE away from sensitive small signal nodes.

5. The V_{FB} pin should connect directly to the feedback resistors. The resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.

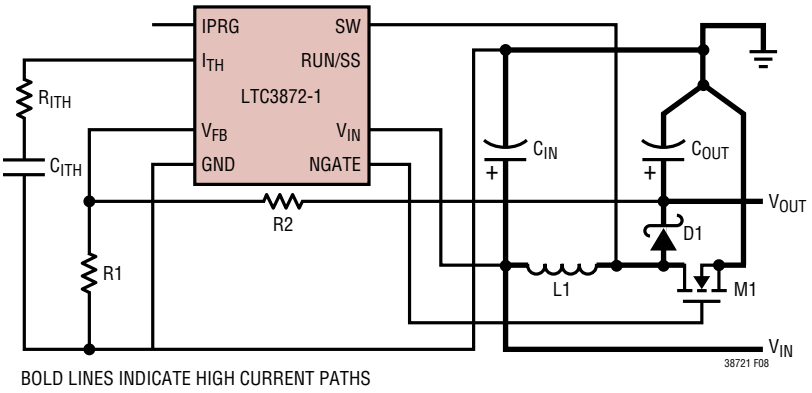
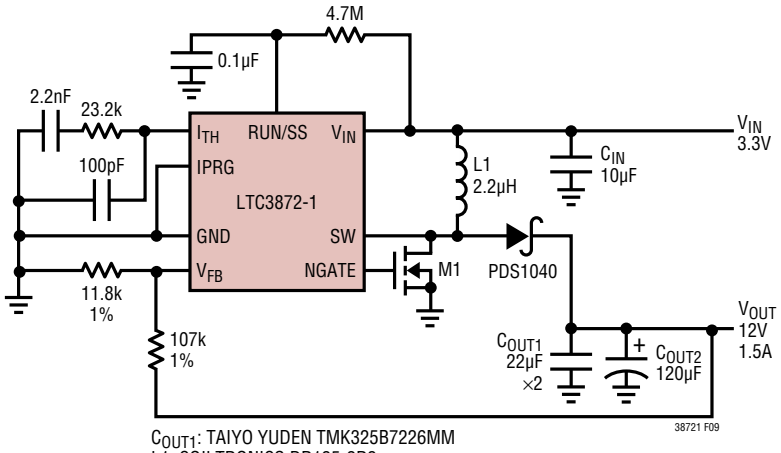


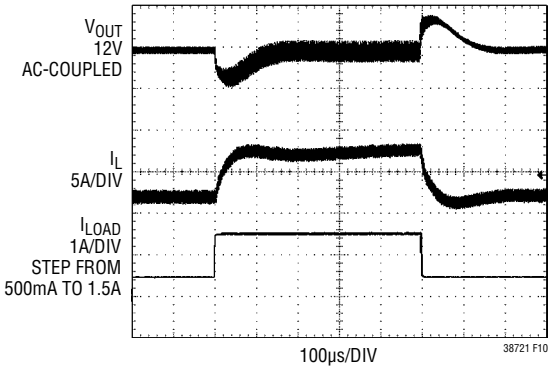
Figure 8. LTC3872-1 Layout Diagram (See PC Board Layout Checklist)

TYPICAL APPLICATIONS

High Efficiency 3.3V Input, 12V Output Boost Converter

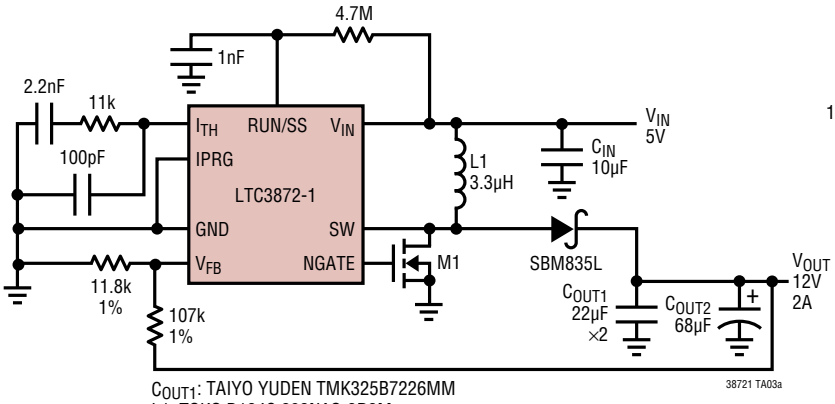


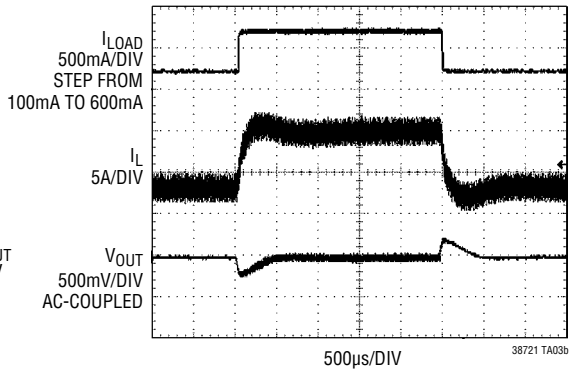
C_{OUT1}: TAIYO YUDEN TMK325B7226MM
L1: COILTRONICS DR125-2R2
M1: VISHAY Si4114DY



TYPICAL APPLICATIONS

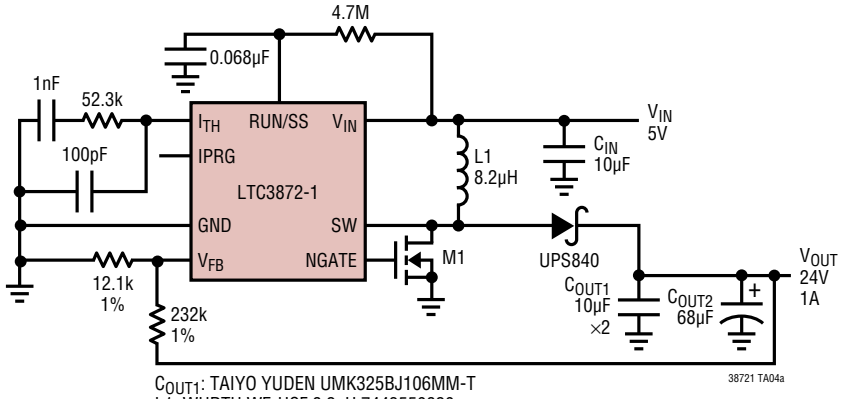
High Efficiency 5V Input, 12V Output Boost Converter





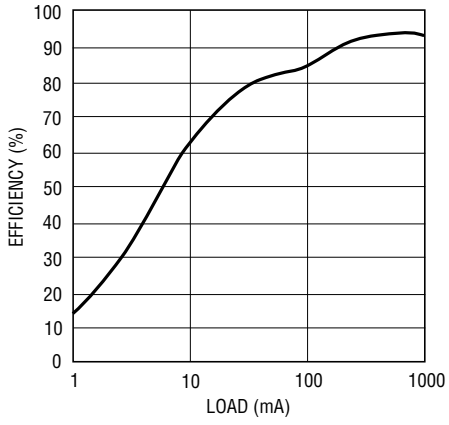
C_{OUT1}: TAIYO YUDEN TMK325B7226MM
L1: TOKO D124C 892NAS-3R3M
M1: IRF3717

High Efficiency 5V Input, 24V Output Boost Converter

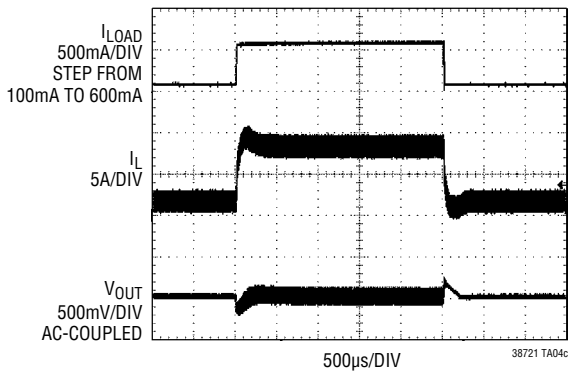


C_{OUT1}: TAIYO YUDEN UMK325BJ106MM-T
L1: WURTH WE-HCF 8.2µH 7443550820
M1: VISHAY Si4174DY

Efficiency

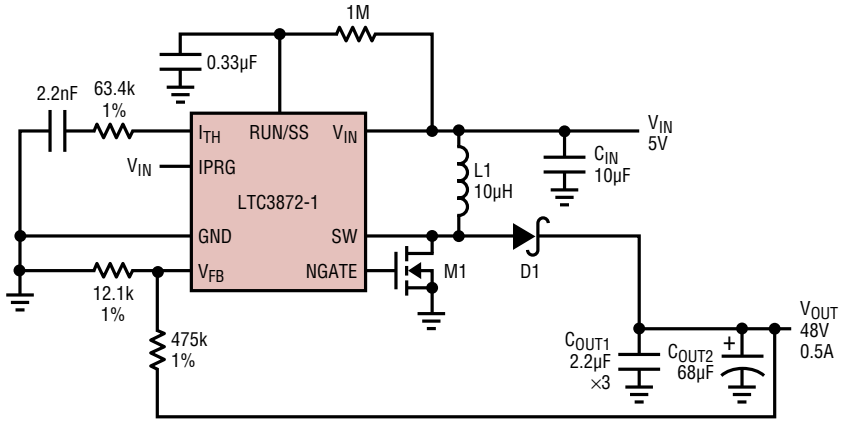


Load Step



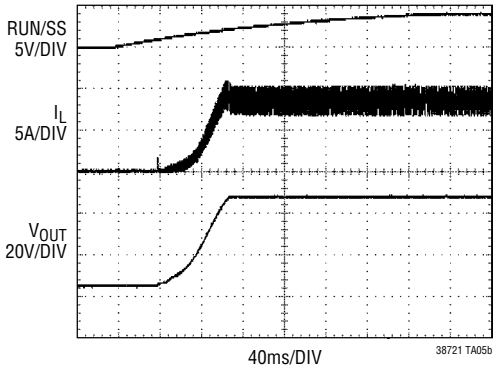
TYPICAL APPLICATIONS

High Efficiency 5V Input, 48V Output Boost Converter

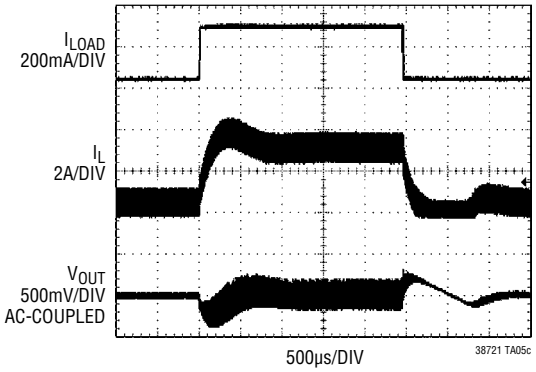


C_{OUT1}: NIPPON CHEMI-CON KTS101B225M43N
D1: DIODES INC. PDS760
L1: SUMIDA CDEP147NP-100
M1: VISHAY Si7850DP

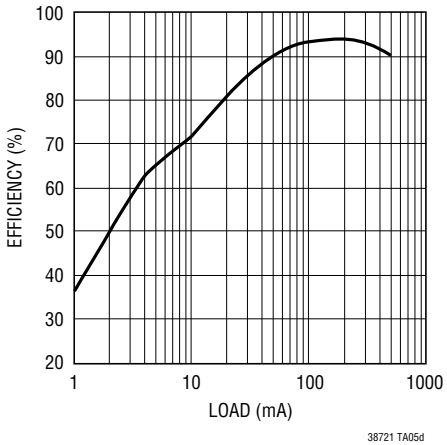
Soft-Start



Load Step



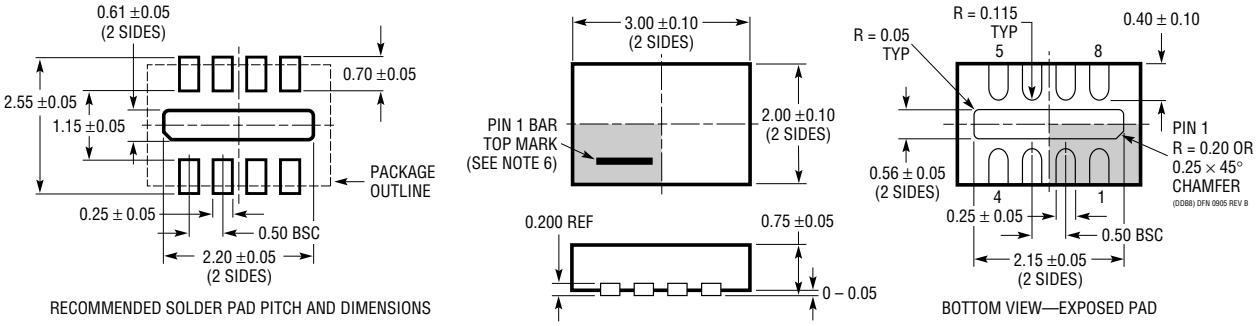
Efficiency



PACKAGE DESCRIPTION

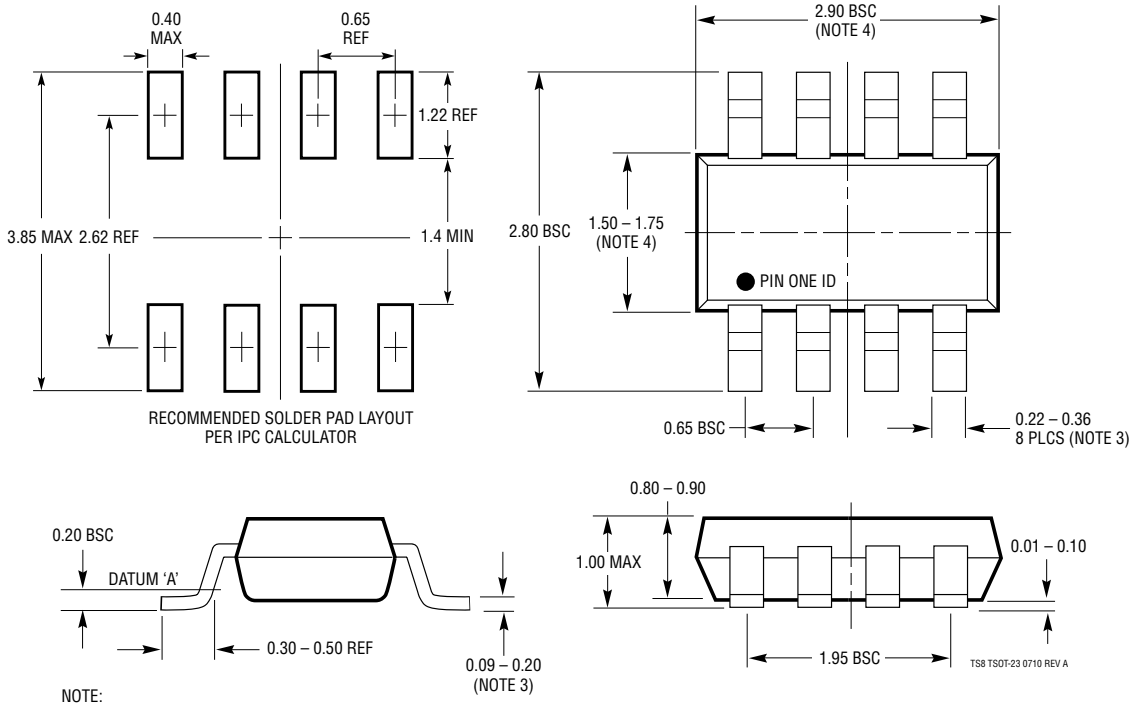
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193