Synchronous Rectifier Driver for Forward Converters

FEATURES

- **N-Channel Synchronous Rectifier MOSFET Driver**
- **Programmable Timeout Protection**
- **Reverse Inductor Current Protection**
- Pulse Transformer Synchronization
- Wide V_{CC} Supply Range: 4.5V to 11V
- 15ns Rise/Fall Times at V_{CC} = 5V, C_L = 4700pF
- Undervoltage Lockout
- Small SO-8 Package

APPLICATIONS

- 48V Input Isolated DC/DC Converters
- Isolated Telecom Power Supplies
- High Voltage Distributed Power Step-Down Converters
- Industrial Control System Power Supplies
- Automotive and Heavy Equipment

DESCRIPTION

The LTC®3900 is a secondary-side synchronous rectifier driver designed to be used in isolated forward converter power supplies. The chip drives N-channel rectifier MOSFETs and accepts pulse sychronization from the primary-side controller via a pulse transformer.

The LTC3900 incorporates a full range of protection for the external MOSFETs. A programmable timeout function is included that disables both drivers when the synchronization signal is missing or incorrect. Additionally, the chip senses the output inductor current through the drain-source resistance of the catch MOSFET, shutting off the MOSFET if the inductor current reverses. The LTC3900 also shuts off the drivers if the supply voltage is too low.

TYPICAL APPLICATION

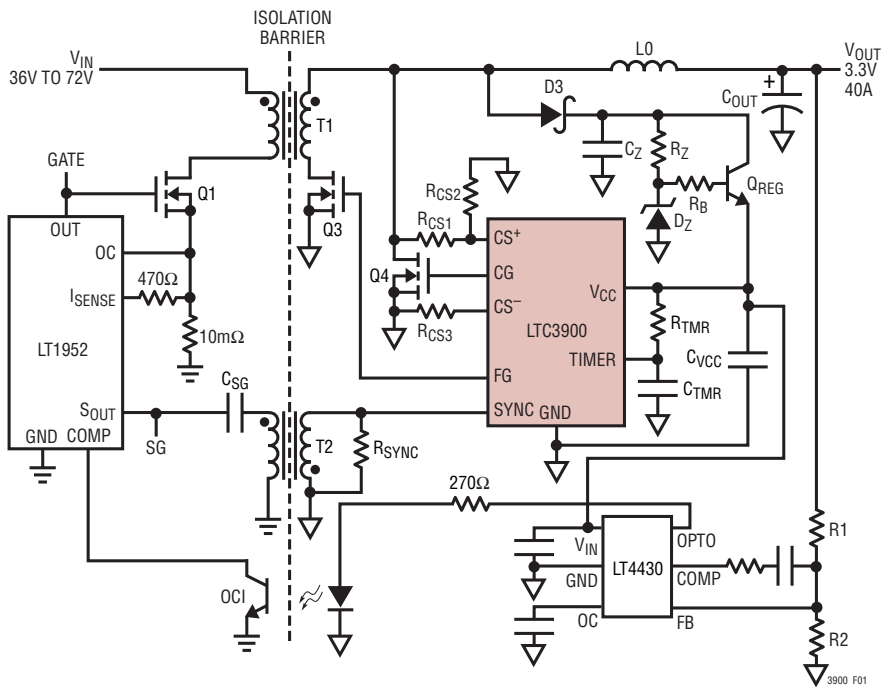
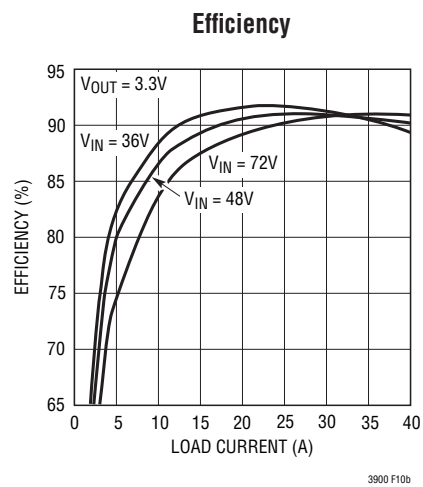


Figure 1. Simplified Isolated Synchronous Forward Converter



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} 12V

Input Voltage
- CS^-, TIMER ..... –0.3V to (V_{CC} +0.3V)
- SYNC ..... –12V to 12V

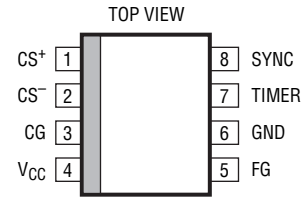
Input Current
- CS^+ 15mA

Operating Junction Temperature Range (Note 2)
- LTC3900E ..... –40°C to 125°C
- LTC3900I ..... –40°C to 125°C
- LTC3900H ..... –40°C to 150°C
- LTC3900MP ..... –55°C to 150°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3900ES8#PBF	LTC3900ES8#TRPBF	3900	8-Lead Plastic Small Outline	–40°C to 125°C
LTC3900IS8#PBF	LTC3900IS8#TRPBF	3900	8-Lead Plastic Small Outline	–40°C to 125°C
LTC3900HS8#PBF	LTC3900HS8#TRPBF	3900	8-Lead Plastic Small Outline	–40°C to 150°C
LTC3900MPS8#PBF	LTC3900MPS8#TRPBF	3900	8-Lead Plastic Small Outline	–55°C to 150°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3900ES8	LTC3900ES8#TR	3900	8-Lead Plastic Small Outline	–40°C to 125°C
LTC3900IS8	LTC3900IS8#TR	3900	8-Lead Plastic Small Outline	–40°C to 125°C
LTC3900HS8	LTC3900HS8#TR	3900	8-Lead Plastic Small Outline	–40°C to 150°C
LTC3900MPS8	LTC3900MPS8#TR	3900	8-Lead Plastic Small Outline	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage Range		●	4.5	5	11	V
V_{UVLO}	V_{CC} Undervoltage Lockout Threshold V_{CC} Undervoltage Lockout Hysteresis	Rising Edge Rising Edge to Falling Edge	●		4.1 0.5	4.5	V V
I_{VCC}	V_{CC} Supply Current	V_{SYNC} = 0V f_{SYNC} = 100kHz, C_{FG} = C_{CG} = 4700pF (Note 4)	● ●		0.5 7	1 15	mA mA
Timer							
V_{TMR}	Timer Threshold Voltage		●	–10%	V_{CC}/5	10%	V
I_{TMR}	Timer Input Current	V_{TMR} = 0V	●		–6	–10	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{TMRDIS}	Timer Discharge Time	C_{TMR} = 1000pF, R_{TMR} = 4.7k	●		40	120	ns
V_{TMRMAX}	Timer Pin Clamp Voltage	C_{TMR} = 1000pF, R_{TMR} = 4.7k			2.5		V
Current Sense							
$I_{CS}+$	CS^+ Input Current	$V_{CS}+$ = 0V	●			±1	µA
$I_{CS}–$	$CS^–$ Input Current	$V_{CS}–$ = 0V	●			±1	µA
V_{CSMAX}	CS^+ Pin Clamp Voltage	I_{IN} = 5mA, V_{SYNC} = –5V			11		V
V_{CS}	Current Sense Threshold Voltage	$V_{CS}–$ = 0V LTC3900E/LTC3900I (Note 5) LTC3900H/LTC3900MP (Note 5)	 ● ●	7.5 3 1	10.5	13.5 18 20	mV mV mV
SYNC Input							
I_{SYNC}	SYNC Input Current	V_{SYNC} = ±10V	●		±1	±10	µA
V_{SYNCP}	SYNC Input Positive Threshold SYNC Positive Input Hysteresis	 (Note 6)	●	1.0	1.4 0.2	1.8	V V
V_{SYNCN}	SYNC Input Negative Threshold SYNC Negative Input Hysteresis	 (Note 6)	●	–1.8	–1.4 0.2	–1.0	V V
Driver Output							
R_{ONH}	Driver Pull-Up Resistance	I_{OUT} = –100mA LTC3900E/LTC3900I LTC3900H/LTC3900MP	 ● ●		0.9	1.2 1.6 2.0	Ω Ω Ω
R_{ONL}	Driver Pull-Down Resistance	I_{OUT} = 100mA LTC3900E/LTC3900I LTC3900H/LTC3900MP	 ● ●		0.9	1.2 1.6 2.0	Ω Ω Ω
I_{PK}	Driver Peak Output Current	(Note 6)			2		A
Switching Characteristics (Note 7)							
t_d	SYNC Input to Driver Output Delay	C_{FG} = C_{CG} = 4700pF, V_{SYNC} = ±5V LTC3900E/LTC3900I LTC3900H/LTC3900MP	 ● ●		60	 120 150	 ns ns
t_{SYNC}	Minimum SYNC Pulse Width	V_{SYNC} = ±5V	●	75			ns
t_r, t_f	Driver Rise/Fall Time	C_{FG} = C_{CG} = 4700pF, V_{SYNC} = ±5V			15		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3900 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3900E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3900I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3900H is guaranteed over the full –40°C to 150°C operating junction temperature range. The LTC3900MP is guaranteed and tested over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Supply current in normal operation is dominated by the current needed to charge and discharge the external MOSFET gates. This current will vary with supply voltage, switching frequency and the external MOSFETs used.

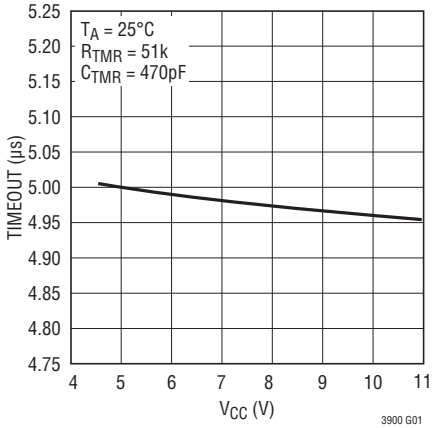
Note 5: The current sense comparator threshold has a 0.33%/°C temperature coefficient (TC) to match the TC of the external MOSFET $R_{DS(ON)}$.

Note 6: Guaranteed by design, not subject to test.

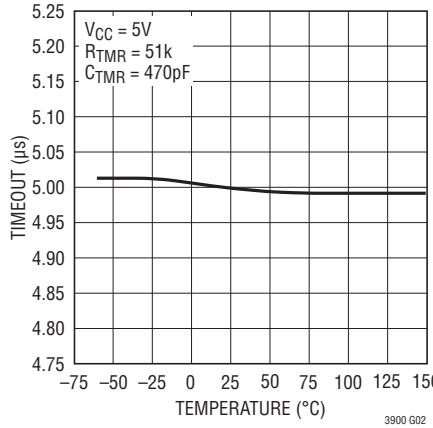
Note 7: Rise and fall times are measured using 10% and 90% levels. Delay times are measured from ±1.4V at SYNC input to 20%/80% levels at the driver output.

TYPICAL PERFORMANCE CHARACTERISTICS

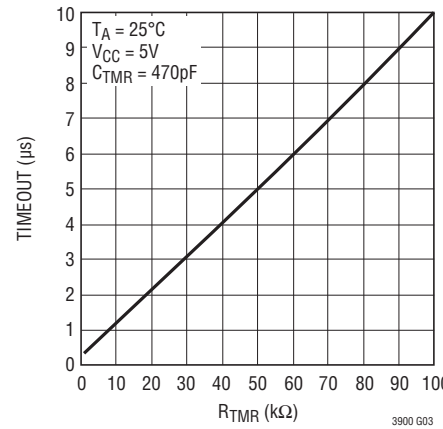
Timeout vs V_{CC}



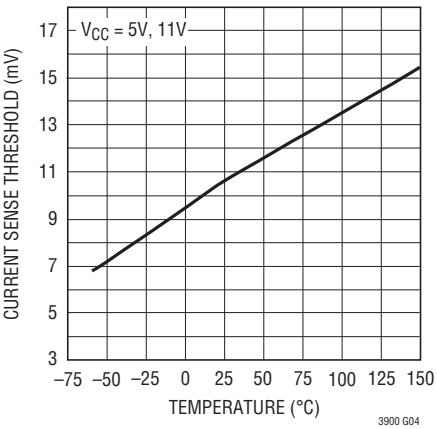
Timeout vs Temperature



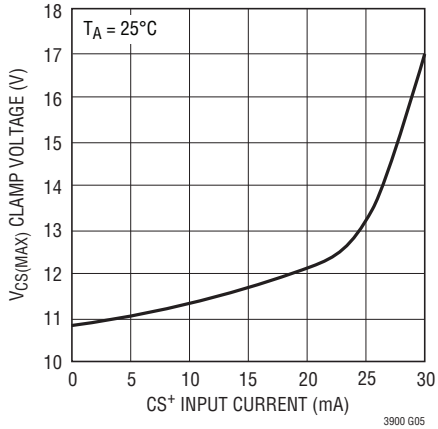
Timeout vs R_{TMR}



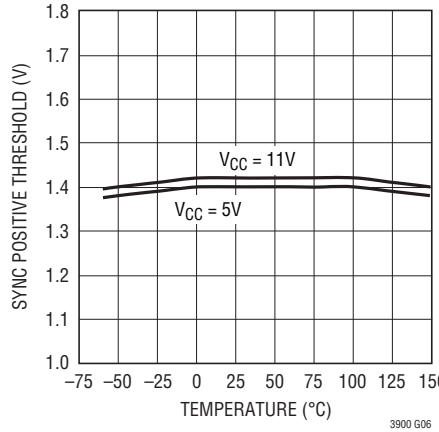
Current Sense Threshold vs Temperature



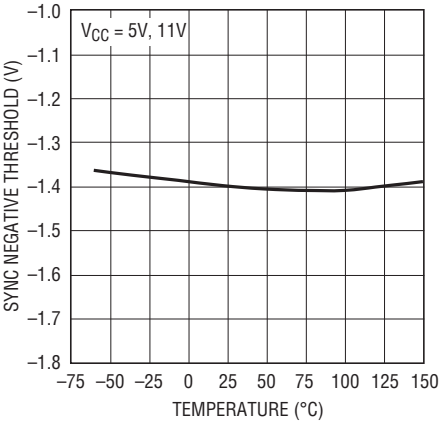
$V_{CS(MAX)}$ Clamp Voltage vs CS^+ Input Current



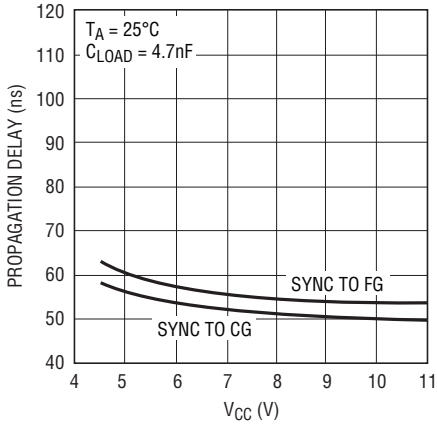
SYNC Positive Threshold vs Temperature



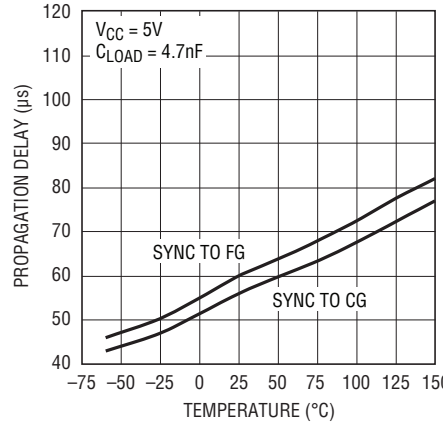
SYNC Negative Threshold vs Temperature



Propagation Delay vs V_{CC}

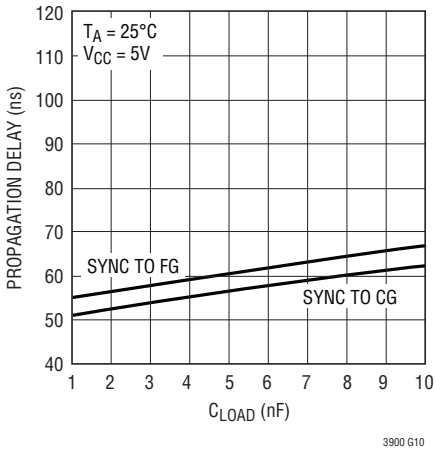


Propagation Delay vs Temperature

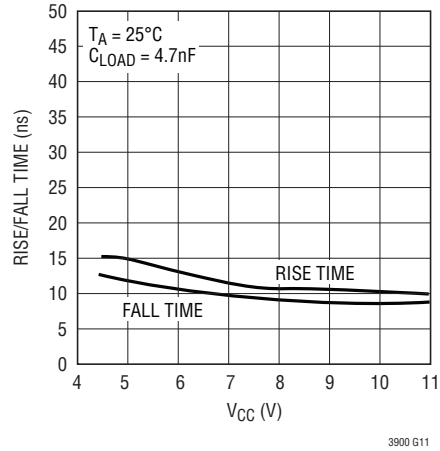


TYPICAL PERFORMANCE CHARACTERISTICS

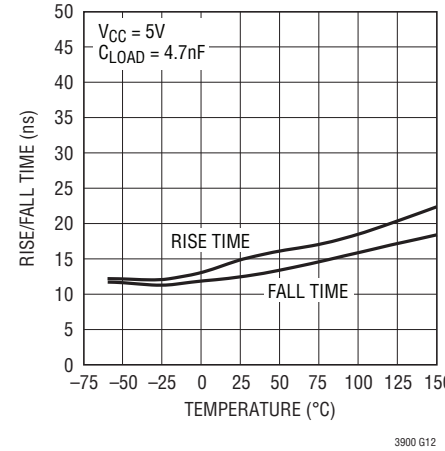
Propagation Delay vs C_{LOAD}



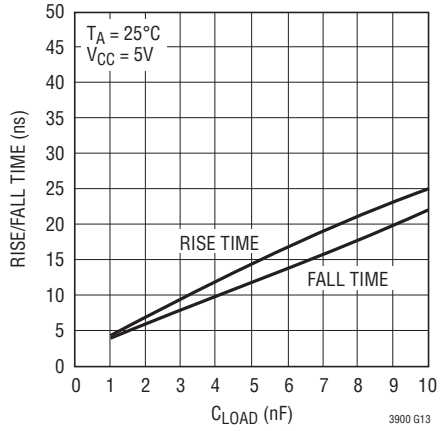
Rise/Fall Time vs V_{CC}



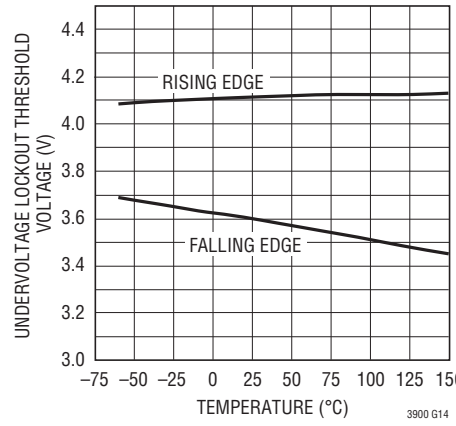
Rise/Fall Time vs Temperature



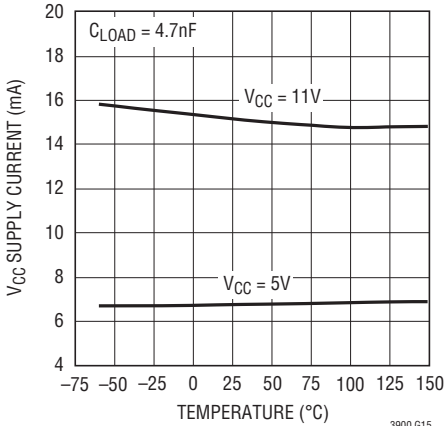
Rise/Fall Time vs Load Capacitance



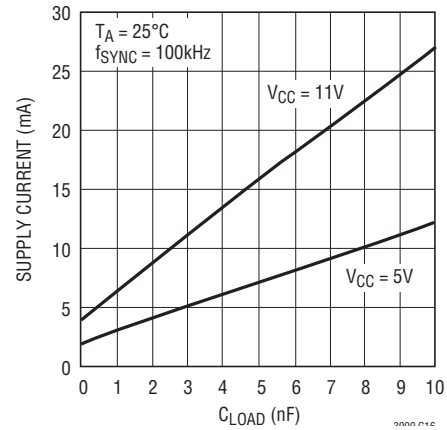
Undervoltage Lockout Threshold Voltage vs Temperature



V_{CC} Supply Current vs Temperature



V_{CC} Supply Current vs Load Capacitance



PIN FUNCTIONS

CS+, CS– (Pin 1, 2): Current Sense Differential Input. Connect CS+ through a series resistor to the drain of the external catch MOSFET, Q4. Connect CS– to the source. The LTC3900 monitors the CS inputs 250ns after CG goes high. If the inductor current reverses and flows into the MOSFET causing CS+ to rise above CS– by more than 10.5mV, the LTC3900 pulls CG low. See the Current Sense section for more details on choosing the resistance value for R_{CS1} to R_{CS3}.

CG (Pin 3): Catch MOSFET Gate Driver. This pin drives the gate of the external N-channel catch MOSFET, Q4.

V_{CC} (Pin 4): Main Supply Input. This pin powers the drivers and the rest of the internal circuitry. Bypass this pin to GND using a 4.7µF ceramic capacitor in close proximity to the LTC3900.

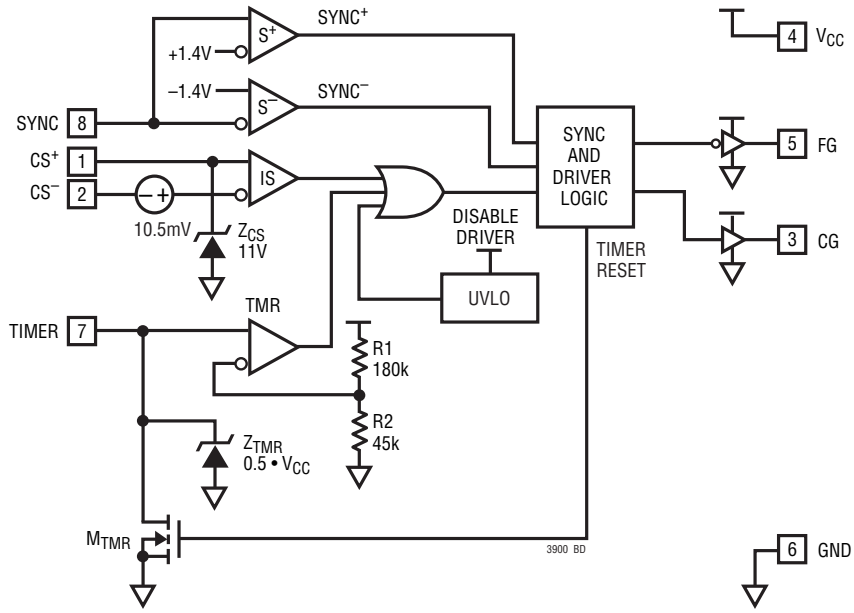
FG (Pin 5): Forward MOSFET Gate Driver. This pin drives the gate of the external N-channel forward MOSFET, Q3.

GND (Pin 6): The V_{CC} bypass capacitor should be connected directly to this GND pin.

TIMER (Pin 7): Timer Input. Connect this pin to an external R-C network to program the timeout period. The LTC3900 resets the timer at every negative transition of the SYNC input. If the SYNC signal is missing or incorrect, the LTC3900 pulls both CG and FG low once the TIMER pin goes above the timeout threshold. See the Timer section for more details on programming the timeout period.

SYNC (Pin 8): Driver Synchronization Input. This input is signal edge sensitive. A negative voltage slew at SYNC forces FG to pull high and CG to pull low. A positive voltage slew at SYNC forces FG to pull low and CG to pull high. The SYNC input can accept both pulse or square wave signals.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Overview

In a typical forward converter topology, a power transformer is used to provide the functions of input/output isolation and voltage step-down to achieve the required low output voltage. Schottky diodes are often used on the secondary-side to provide rectification. Schottky diodes, though easy to use, result in a loss of efficiency due to relatively high voltage drops. To improve efficiency, synchronous output rectifiers utilizing N-channel MOSFETs can be used instead of Schottky diodes. The LTC3900 provides all of the necessary functions required to drive the synchronous rectifier MOSFETs.

Figure 1 shows a simplified forward converter application. T1 is the power transformer; Q1 is the primary-side power transistor driven by the primary controller, LT1952 output (OUT). The pulse transformer T2 provides synchronization and is driven by LT1952 synchronization signal, S_{OUT} or SG from the primary controller. Q3 and Q4 are secondary-side synchronous switches driven by the LTC3900's FG and CG output. Inductor L_O and capacitor C_{OUT} form the output filter to provide a steady DC output voltage for the load. Also shown in Figure 1 is the feedback path from V_{OUT} through the optocoupler driver LT4430 and an optocoupler, back to the primary controller to regulate V_{OUT}.

Each full cycle of the forward converter operation consists of two periods. In the first period, Q1 turns on and the primary-side delivers power to the load through T1. SG goes high and T2 generates a negative pulse at the LTC3900 SYNC input. The LTC3900 forces FG to turn on and CG to turn off, Q3 conducts. Current flows to the load through Q3, T1 and L_O. In the next period, Q1 turns off, SG goes low and T2 generates a positive pulse at the LTC3900 SYNC input. The LTC3900 forces FG to turn off and CG to turn on, Q4 conducts. Current continues to flow to the load through Q4 and L_O. Figure 2 shows the LTC3900 synchronization waveforms.

External MOSFET Protection

A programmable timer and a differential input current sense comparator are included in the LTC3900 for protection of the external MOSFET during power down and Burst Mode® operation. The chip also shuts off the MOSFETs if $V_{CC} < 4.1V$.

When the primary controller is powering down, the primary controller shuts down first and the LTC3900 continues to operate for a while by drawing power from the V_{CC} bypass cap, C_{VCC}. The SG signal stops switching and there is no SYNC pulse to the LTC3900. The LTC3900 keeps one of the drivers turned on depending on the polarity of the last SYNC pulse. If the last SYNC pulse is positive, CG will remain high and the catch MOSFET, Q4 will stay on. The inductor current will start falling down to zero and continue going in the negative direction due to the voltage that is still present across the output capacitor (the current now flows from C_{OUT} back to L_O). If Q4 is turned off while the inductor current is negative, the inductor current will produce high voltage across Q4, resulting in a MOSFET avalanche. Depending on the amount of energy stored in the inductor, this avalanche energy may damage Q4.

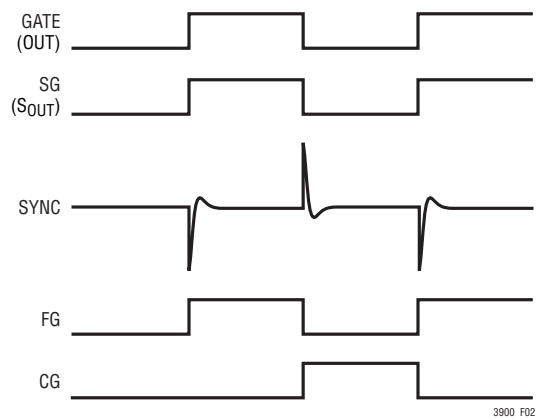


Figure 2. Synchronization Waveforms

APPLICATIONS INFORMATION

The timer circuit and current sense comparator in LTC3900 are used to prevent reverse current buildup in the output inductor.

Timer

Figure 3 shows the LTC3900 timer internal and external circuits. The timer operates by using an external R-C charging network to program the time-out period. On every negative transition at the SYNC input, the chip generates a 200ns pulse to reset the timer cap. If the SYNC signal is missing or incorrect, allowing the timer cap voltage to go high, it shuts off both drivers once the voltage reaches the time-out threshold. Figure 4 shows the timer waveforms.

A typical forward converter cycle always turns on Q3 and Q4 alternately and the SYNC input should alternate between positive and negative pulses. The LTC3900 timer also includes sequential logic to monitor the SYNC input sequence. If after one negative pulse, the SYNC comparator receives another negative pulse, the LTC3900 will not reset the timer cap. If no positive SYNC pulse appears, both drivers are shut off once the timer times out. Once positive pulses reappear the timer resets and the drivers start switching again. This is to protect the external components in situations where only negative SYNC pulse is present and FG output remains high. Figure 5 shows the timer waveforms with incorrect SYNC pulses.

The LTC3900 has two separate SYNC comparators (S^+ and S^- in the Block Diagram) to detect the positive and negative pulses. The threshold voltages of both comparators are designed to be of the same magnitude (1.4V typical) but opposite in polarity. In some situations, for example during power up or power down, the SYNC pulse magnitude may be low, slightly higher or lower than the threshold of the comparators. This can cause only one of the SYNC comparators to trip. This also appears as incorrect SYNC pulse and the timer will not reset.

The timeout period is determined by the external R_{TMR} and C_{TMR} values and is independent of the V_{CC} voltage. This is achieved by making the timeout threshold a ratio of V_{CC}. The ratio is 0.2x, set internally by R1 and R2 (see Figure 3). The timeout period should be programmed to be around one period of the primary switching frequency using the following formula:

$$TIMEOUT = 0.2 \bullet R_{TMR} \bullet C_{TMR} + 0.27E\text{-}6$$

To reduce error in the timeout setting due to the discharge time, select C_{TMR} between 100pF and 1000pF. Start with a C_{TMR} around 470pF and then calculate the required R_{TMR}. C_{TMR} should be placed as close as possible to the LTC3900 with minimum PCB trace between C_{TMR}, the TIMER pin and GND. This is to reduce any ringing caused by the PCB trace inductance when C_{TMR} discharges. This ringing may introduce error to the timeout setting.

The timer input also includes a current sinking clamp circuit (Z_{TMR} in Figure 3) that clamps this pin to about $0.5 \bullet V_{CC}$ if there is missing SYNC/timer reset pulse. This clamp circuit prevents the timer cap from getting fully charged up to the rail, which results in a longer discharge

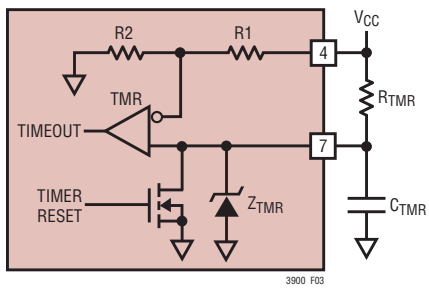


Figure 3. Timer Circuit

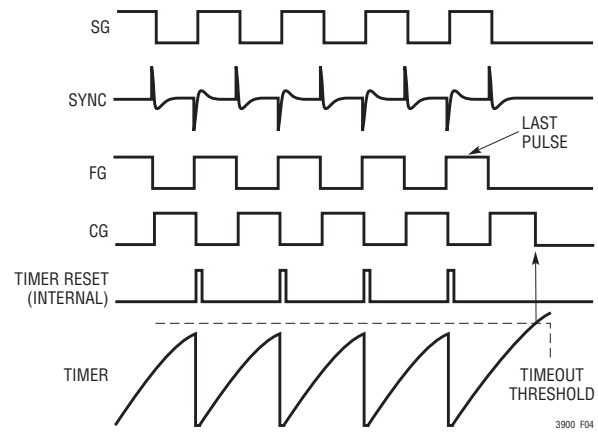


Figure 4. Timer Waveforms

APPLICATIONS INFORMATION

time. The current sinking capability of the circuit is around 1mA. The timeout function can be disabled by connecting the timer pin to GND.

Current Sense

The differential input current sense comparator is used for sensing the voltage across the drain-to-source terminals of Q4 through the CS^+ and CS^- pins. If the inductor current reverses into the Q4 causing CS^+ to rise above CS^- by more than 10.5mV, the LTC3900 pulls CG low. This comparator is used to prevent inductor reverse current buildup during power down or Burst Mode operation, which may cause damage to the MOSFET. The 10.5mV input threshold has a positive temperature coefficient, which closely matches the TC of the external MOSFET $R_{DS(ON)}$. The current sense comparator is only active 250ns after CG goes high; this is to avoid any ringing immediately after Q4 is switched on.

Under light load conditions, if the inductor average current is less than half of its peak-to-peak ripple current, the inductor current will reverse into Q4 during a portion of the switching cycle, forcing CS^+ to rise above CS^-. The current sense comparator input threshold is set at 10.5mV to prevent tripping under light load conditions. If the product of the inductor negative peak current and MOSFET $R_{DS(ON)}$ is higher than 10.5mV, the LTC3900 will operate in discontinuous current mode. Figure 6 shows the LTC3900 operating in discontinuous current mode; the CG output goes low before the next negative SYNC pulse, as soon as the inductor current becomes negative. Discontinuous current mode is sometimes undesirable. To disable discontinuous current mode operation, add a resistor divider, R_{CS1} and R_{CS2} at the CS^+ pin to increase the 10.5mV threshold so that the LTC3900 operates in continuous mode at no load.

The LTC3900 CS^+ pin has an internal current sinking clamp circuit (Z_{CS} in the Block Diagram) that clamps the pin to 11V. The clamp circuit is to be used together with the external series resistor, R_{CS1} to protect the CS^+ pin from high Q4 drain voltage in the power transfer cycle. During the power transfer cycle, Q4 is off, the drain voltage of Q4 is determined by the primary input voltage and the transformer turns ratio. This voltage can be high and may damage the LTC3900 if CS^+ is connected directly to the drain of Q4. The current sinking capability of the clamp circuit is 5mA minimum.

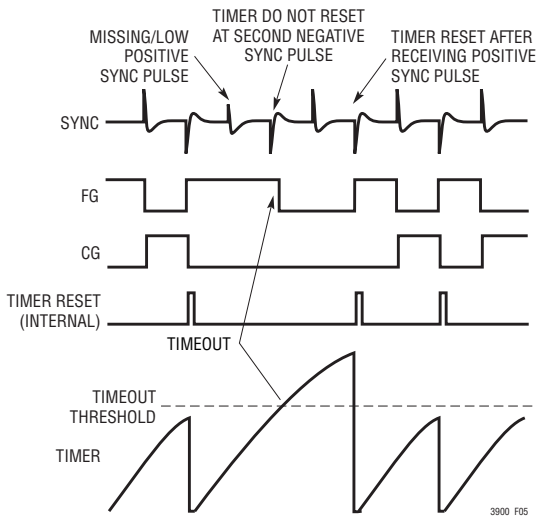


Figure 5. Timer Waveforms with Incorrect SYNC Pulses

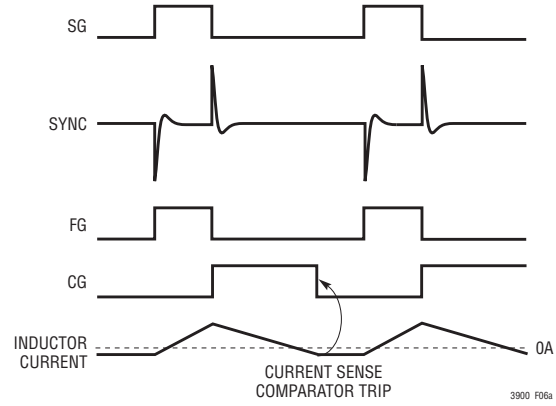


Figure 6a. Discontinuous Current Mode Operation at No Load

APPLICATIONS INFORMATION

The value of the resistors, R_{CS1}, R_{CS2} and R_{CS3}, should be calculated using the following formulas to meet both the threshold and clamp voltage requirements:

$k = 48 \bullet I_{RIPPLE} \bullet R_{DS(ON)} - 1$

$R_{CS2} = \{200 \bullet V_{IN(MAX)} \bullet (N_S/N_P) - 2200 \bullet (1 + k)\} / k$

$R_{CS1} = k \bullet R_{CS2}$

$R_{CS3} = \{R_{CS1} \bullet R_{CS2}\} / \{R_{CS1} + R_{CS2}\}$

If k = 0 or less than zero, R_{CS2} is not needed and $R_{CS1} = R_{CS3} = \{V_{IN(MAX)} \bullet (N_S/N_P) - 11V\} / 5mA$

where:

I_{RIPPLE} = Inductor peak-to-peak ripple current

$R_{DS(ON)}$ = On-resistance of Q4 at $I_{RIPPLE}/2$

$V_{IN(MAX)}$ = Primary side main supply maximum input voltage

N_S/N_P = Power transformer T1, turn ratio

If the LTC3900 still operates in discontinuous mode with the calculated resistance value, increase the value of R_{CS1} to raise the threshold. The resistors R_{CS1} and R_{CS2} and the CS^+ pins input capacitance plus the PCB trace capacitance form an R-C delay; this slows down the response time of the comparator. The resistors and CS^+ input leakage currents also create an input offset error.

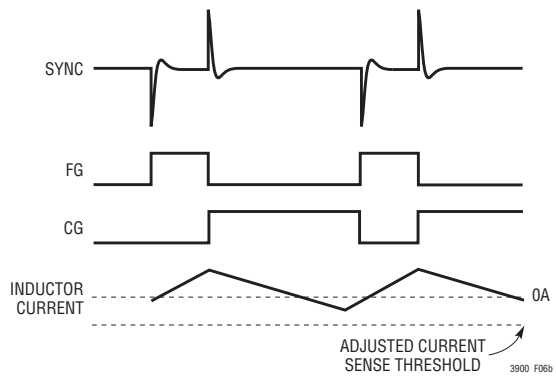


Figure 6b. Continuous Current Mode Operation with Adjusted Current Sense Threshold

To minimize this delay and error, do not use resistance value higher than required and make the PCB trace from the resistors to the LTC3900 CS^+/CS^- pins as short as possible. Add a series resistor, R_{CS3} with value equal to parallel sum of R_{CS1} and R_{CS2} to the CS^- pin and connect the other end of R_{CS3} directly to the source of Q4.

SYNC Input

Figure 7 shows the external circuit for the LTC3900 SYNC input. With a selected type of pulse transformers, the values of the C_{SG} and R_{SYNC} should be adjusted to obtain an optimum SYNC pulse amplitude and width. A bigger capacitor, C_{SG}, generates a higher and wider SYNC pulse. The peak of this pulse should be much higher than the typical LTC3900 SYNC threshold of ±1.4V. Amplitudes greater than ±5V will help to speed up the SYNC comparator and reduce the SYNC to drivers propagation delay. The pulse width should be wider than 75ns. Overshoot during the pulse transformer reset interval must be minimized and kept below the minimum SYNC threshold of ±1V. The amount of overshoot can be reduced by having a smaller R_{SYNC}.

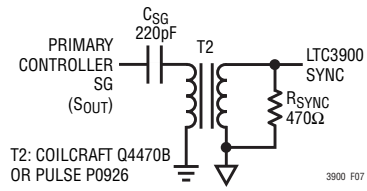


Figure 7. SYNC Input Circuit

APPLICATIONS INFORMATION

An alternative method of generating the SYNC pulse is shown in Figure 8. This circuit produces square SYNC pulses with amplitude dependent on the logic supply voltage. The SYNC pulse width can be adjusted with R1 and C1 without affecting the pulse amplitude.

For nonisolated applications, the SYNC input can be driven directly by a bipolar square pulse. To reduce the propagation delay, make the positive and negative magnitude of the square wave much greater than the ±1.4V SYNC threshold.

V_{CC} Regulator

The V_{CC} supply for the LTC3900 can be generated by peak rectifying the transformer secondary winding as shown in Figure 9. The Zener diode D_Z sets the output voltage to (V_Z – 0.7V). A resistor, R_B (on the order of a few hundred ohms), in series with the base of Q_{REG} may be required to surpress high frequency oscillations depending on Q_{REG}'s selection.

The LTC3900 has an UVLO detector that pulls the drivers output low if V_{CC} < 4.1V. The UVLO detector has 0.5V of hysteresis to prevent chattering.

In a typical forward converter, the secondary-side circuits have no power until the primary-side controller starts operating. Since the power for biasing the LTC3900 is derived from the power transformer T1, the LTC3900 will initially remain off. During that period (V_{CC} < 4.1V), the output rectifier MOSFETs Q3 and Q4 will remain off and the MOSFETs body diodes will conduct. The MOSFETs may experience very high power dissipation due to a high voltage drop in the body diodes. To prevent MOSFET damage, V_{CC} voltage greater than 4.1V should be provided quickly. The V_{CC} supply circuit shown in Figure 9 will provide power for the LTC3900 within the first few switching pulses of the primary controller, preventing overheating of the MOSFETs.

MOSFET Selection

The required MOSFET $R_{DS(ON)}$ should be determined based on allowable power dissipation and maximum required output current.

The body diodes conduct during the power-up phase, when the LTC3900 V_{CC} supply is ramping up. The CG and FG signals stay low and the inductor current flows through the body diodes. The body diodes must be able to handle the load current during start-up until V_{CC} reaches 4.1V.

The LTC3900 drivers dissipate power when switching MOSFETs. The power dissipation increases with switching frequency, V_{CC} and size of the MOSFETs. To calculate

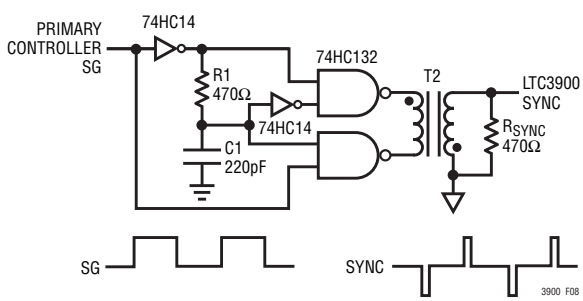


Figure 8. Symmetrical SYNC Drive

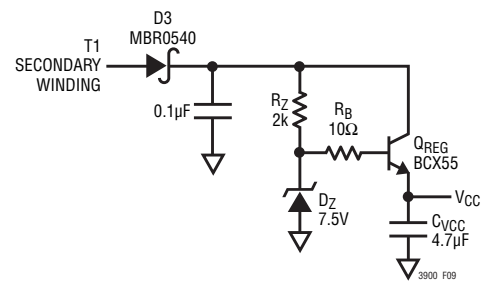


Figure 9. V_{CC} Regulator

APPLICATIONS INFORMATION

the driver dissipation, the total gate charge Q_G is used. This parameter is found on the MOSFET manufacturers data sheet.

The power dissipated in each LTC3900 MOSFET driver is:

$$P_{DRIVER} = Q_G \bullet V_{CC} \bullet f_{SW}$$

where f_{SW} is the switching frequency of the converter.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3900 for your layout:

1. Connect the 4.7µF bypass capacitor as close as possible to the V_{CC} and GND pins.

2. Connect the two MOSFET drain terminals directly to the transformer. The two MOSFET sources should be as close together as possible.

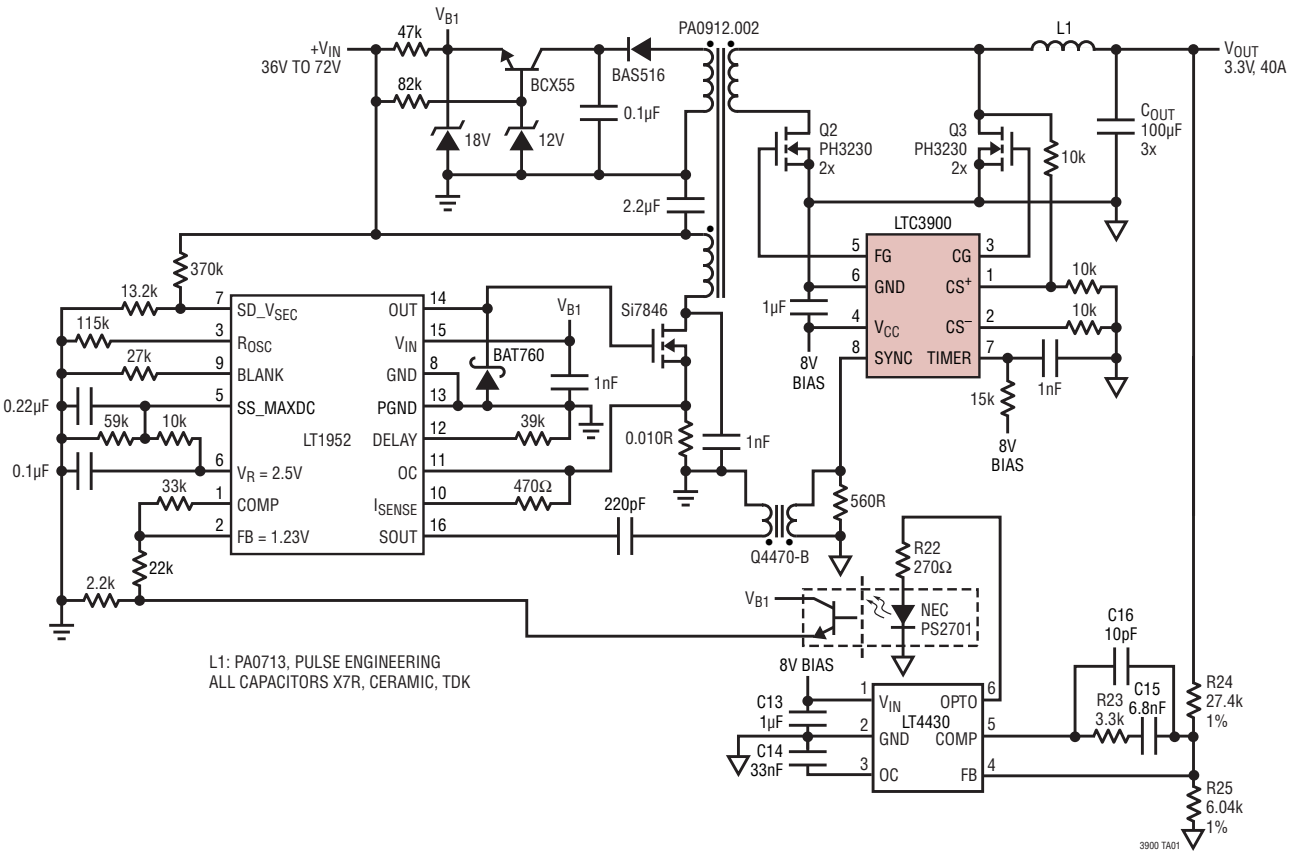
3. Keep the timer, SYNC and V_{CC} regulator circuit away from the high current path of Q3, Q4 and T1.

4. Place the timer capacitor, C_{TMR}, as close as possible to the LTC3900.

5. Keep the PCB trace from the resistors R_{CS1}, R_{CS2} and R_{CS3} to the LTC3900 CS^+/CS^- pins as short as possible. Connect the other ends of the resistors directly to the drain and source of the MOSFET, Q4.

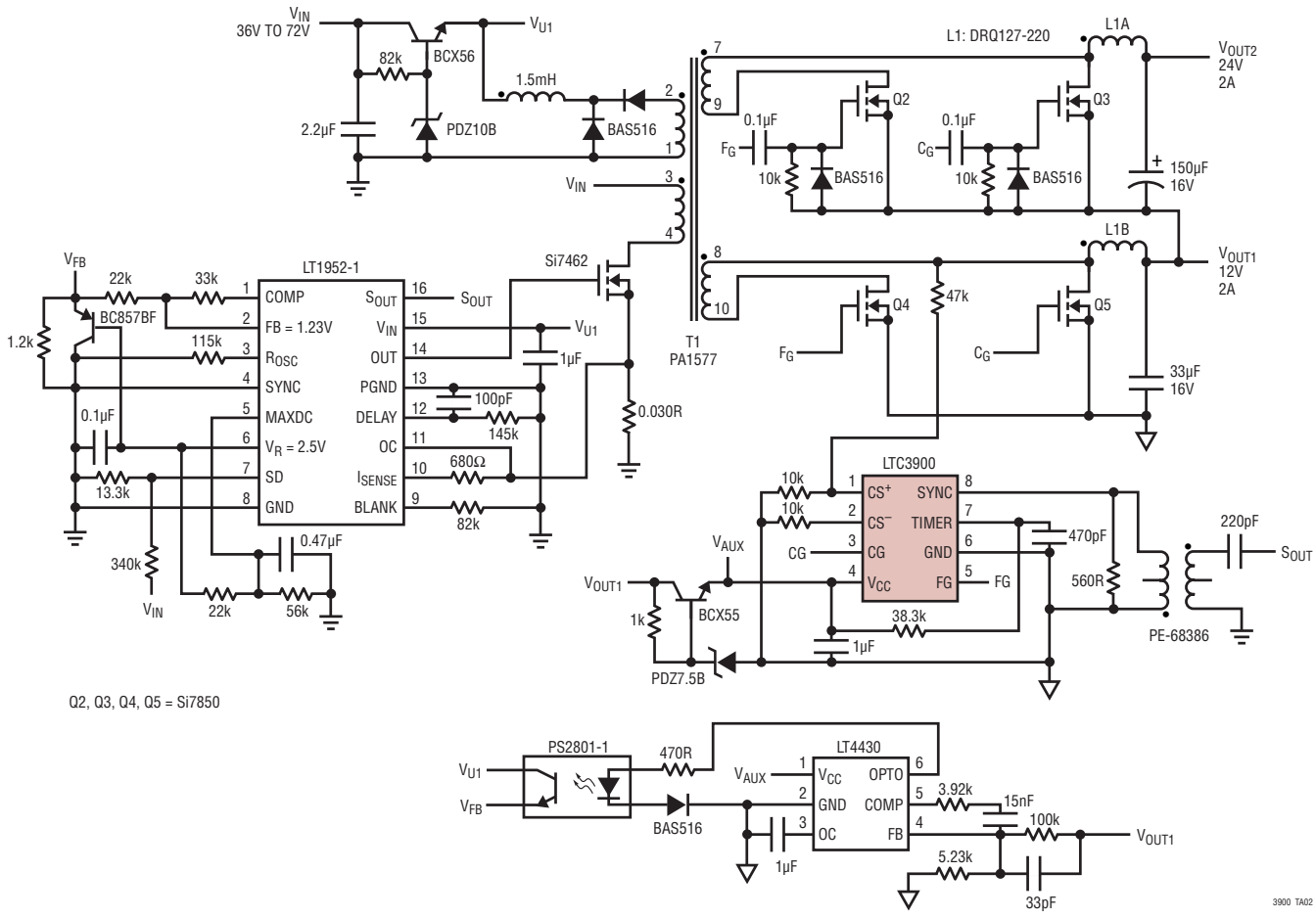
TYPICAL APPLICATIONS

36V to 72V, 3.3V at 40A Synchronous Forward Converter



TYPICAL APPLICATIONS

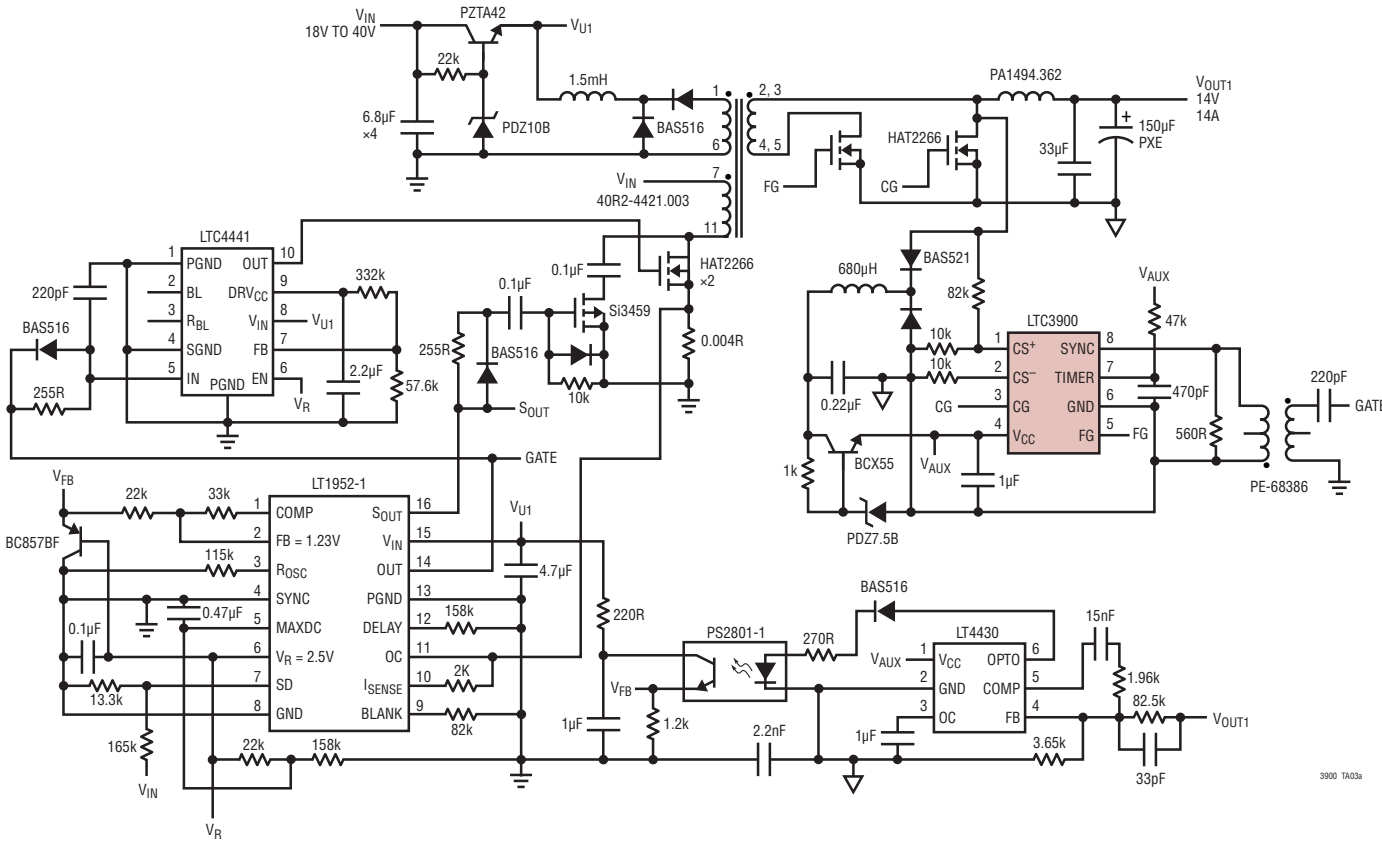
36V to 72V Input to 12V and 24V (or ± 12V), 2A Output Converter in 1/8th Brick Footprint



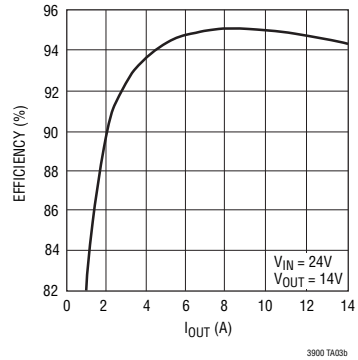
The LTC3900 can drive multiple synchronous output rectifiers. The 12V and 24V or ±12V output converter has good cross regulation due to low voltage drops in the output MOSFETs. Other combinations like 3.3V and –5V or 1.5V and 5V can be easily achieved by changing the transformer turns ratio.

TYPICAL APPLICATIONS

18V to 40V Input to 14V at 14A Output Converter in 1/4 Brick Footprint

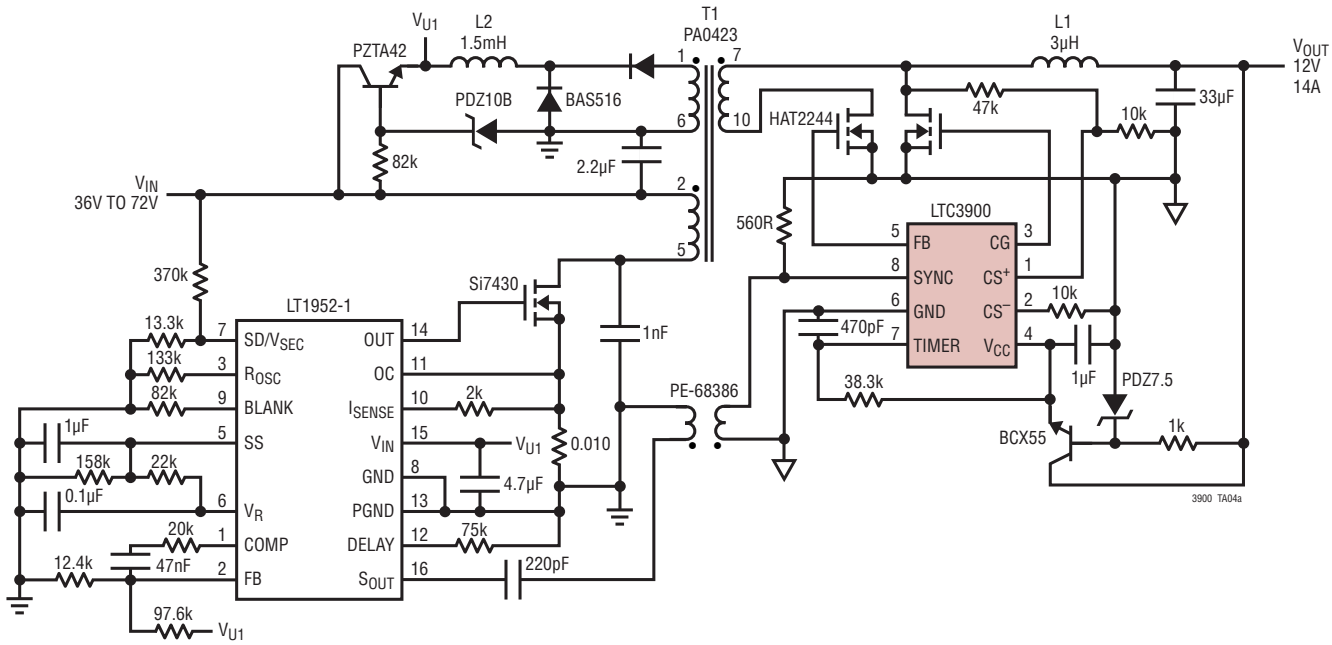


By Using Active Reset and 60V MOSFETs Converter is Achieving 94% to 95% Efficiency with Only Four MOSFETs.



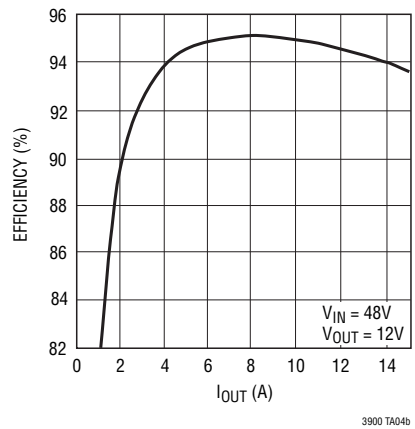
TYPICAL APPLICATIONS

36V to 72V Input to 12V, 14A Output Converter in 1/8th Brick Footprint



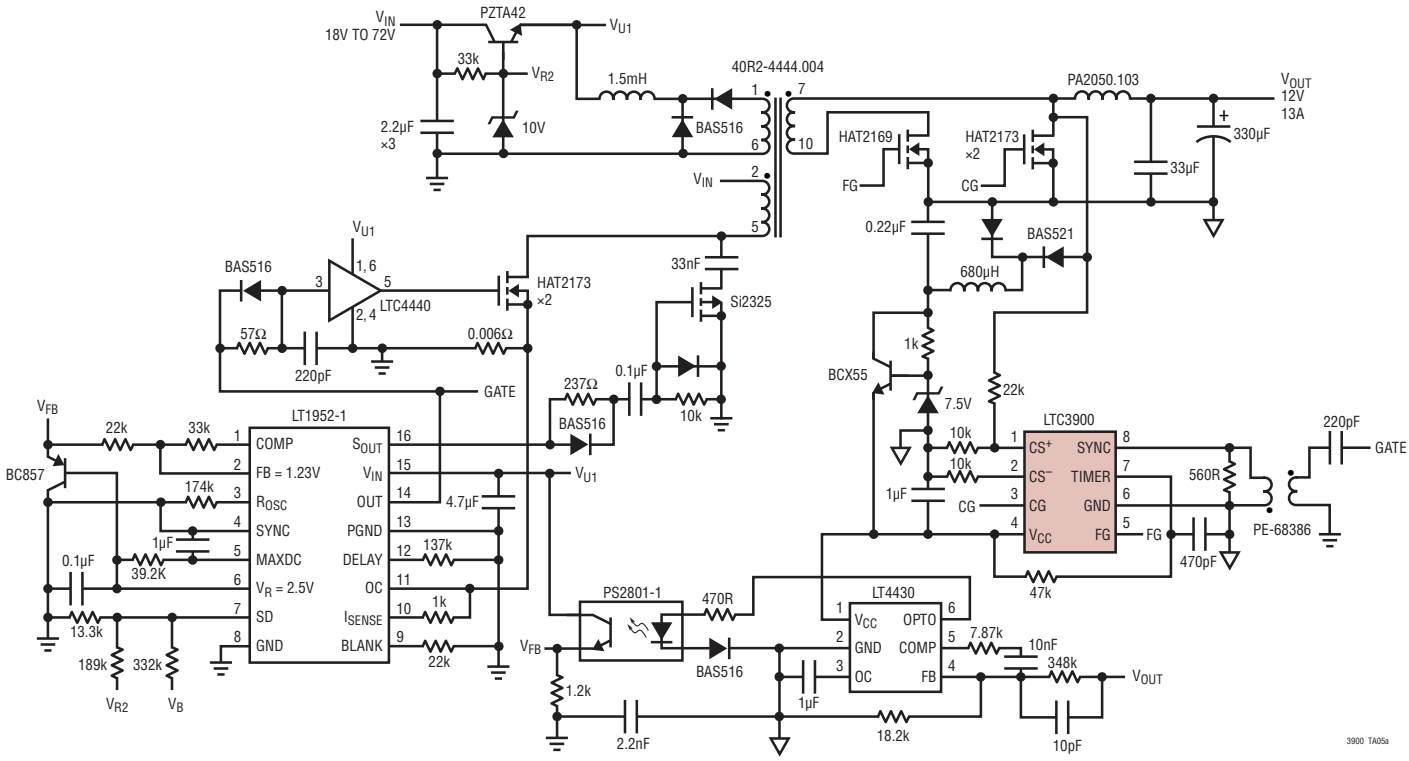
L1: PULSE PA1393.302
L2: COILCRAFT DO1607B-155
ALL CERAMIC CAPS ARE X5R OR X7R

The Efficiency of 12V Output Converter is Over 95% at 8A Output.

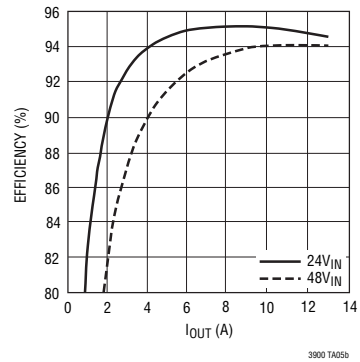


TYPICAL APPLICATIONS

18V to 72V Input to 12V at 13A Active Reset Converter Fits in 1/8th Brick Size

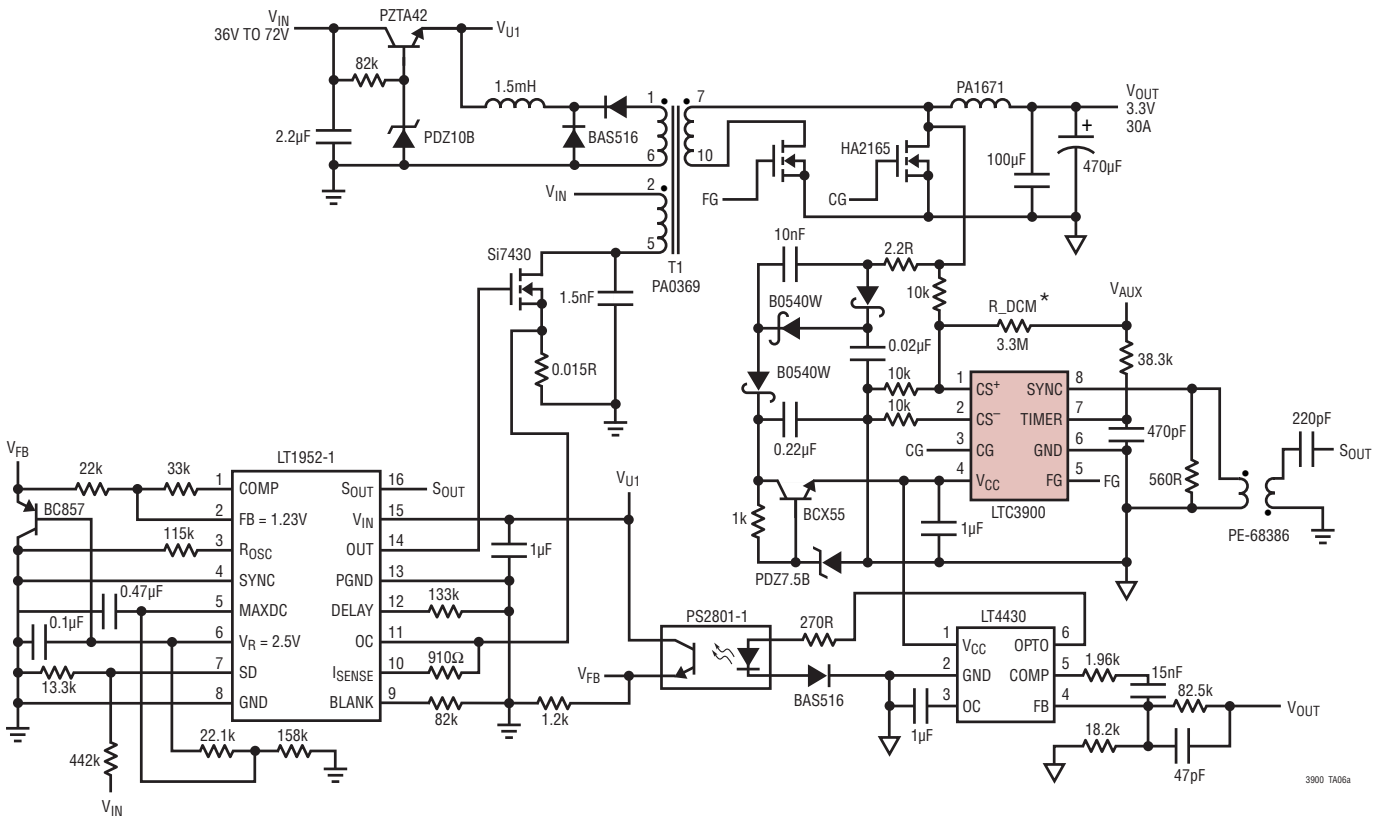


The High Efficiency of Converter is Achieved by Precise MOSFET Timing Provided by LT1952 and LTC3900 Controllers.



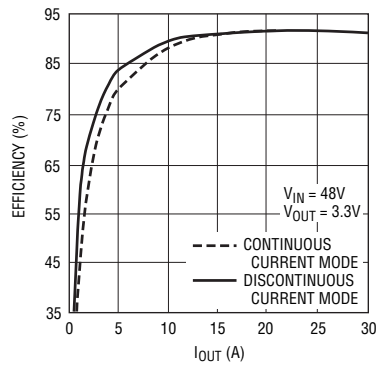
TYPICAL APPLICATIONS

Synchronous Forward Converter With Pulse Skip Mode



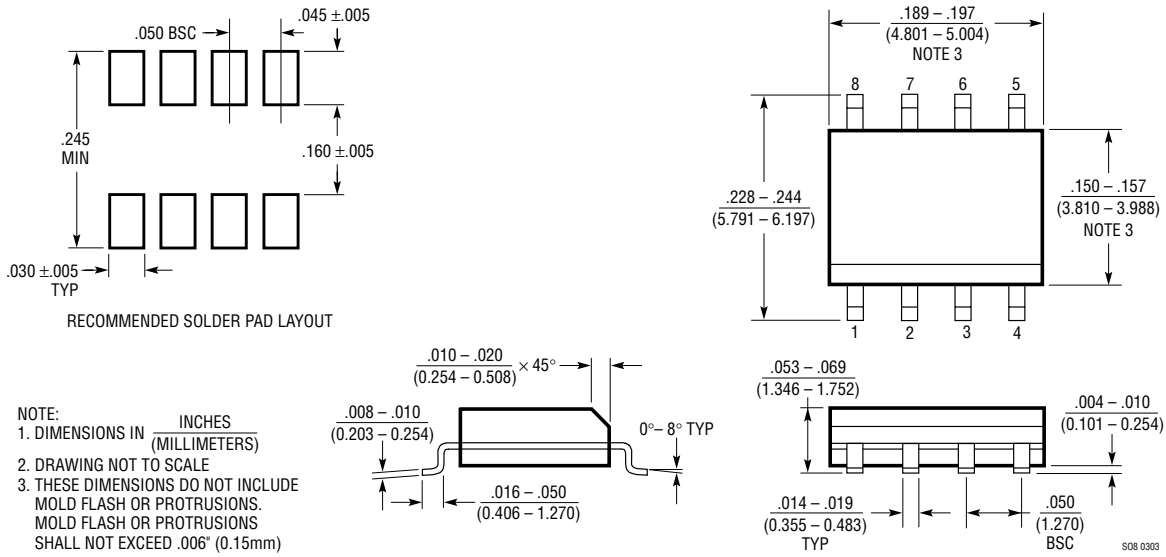
*CONVERTERS THAT USE THE LTC3900 CAN BE FORCED TO OPERATE IN DISCONTINUOUS CURRENT MODE AT LIGHT LOADS BY OFFSETTING THE CURRENT SENSE INPUT WITH R_DCM RESISTOR.

The Discontinuous Current Mode (DCM) Operation of Circuit is About 10% More Efficient with 1A-2A Loads. The No Load Input Current is 15mA in DCM Versus 90mA in CCM.



PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	5/11	Added H- and MP-grade parts. Reflected throughout the data sheet.	1 to 20