LTC4001-1



2A Synchronous Buck Li-Ion Charger

FEATURES

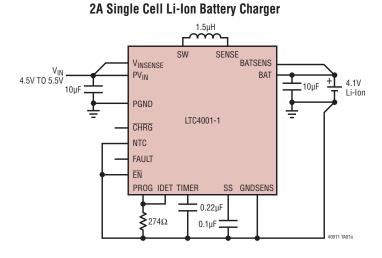
- Low Power Dissipation
- 2A Maximum Charge Current
- No External MOSFETs, Sense Resistor or Blocking Diode Required
- Remote Sensing at Battery Terminals
- Programmable Charge Termination Timer
- Preset 4.1V Float Voltage with ±0.5% Accuracy
- 4.1V Float Voltage Improves Battery Life and High Temperature Safety Margin
- Programmable Charge Current Detection/ Termination
- Automatic Recharge
- Thermistor Input for Temperature Qualified Charging
- Compatible with Current Limited Wall Adapters
- Low Profile 16-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- Handheld Battery-Powered Devices
- Handheld Computers
- Charging Docks and Cradles
- Digital Cameras
- Smart Phones

σ, LT, LTC and LTM are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

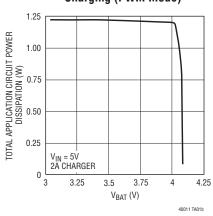


DESCRIPTION

The LTC[®]4001-1 is a 2A Li-Ion battery charger intended for 5V wall adapters. It utilizes a 1.5MHz synchronous buck converter topology to reduce power dissipation during charging. Low power dissipation, an internal MOSFET and sense resistor allow a physically small charger that can be embedded in a wide range of handheld applications. The LTC4001-1 includes complete charge termination circuitry, automatic recharge and a $\pm 1\%$ 4.1V float voltage. Input short-circuit protection is included so no blocking diode is required.

This 4.1V version of the standard LTC4001 is intended for applications which will be operated or stored above approximately 60°C. Under these conditions, the reduced float voltage will trade-off initial cell capacity for the benefit of increased capacity retention over the life of the battery. A reduced float voltage also minimizes swelling in prismatic and polymer cells, and avoids open CID (pressure fuse) in cylindrical cells.

Battery charge current, charge timeout and end-of-charge indication parameters are set with external components. Additional features include shorted cell detection, temperature qualified charging and overvoltage protection. The LTC4001-1 is available in a low profile (0.75mm) 16-lead (4mm \times 4mm) QFN package.



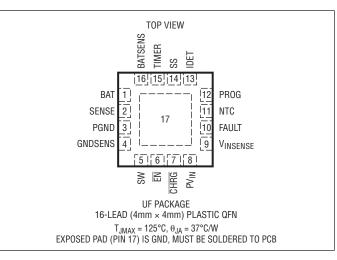
Power Loss vs V_{BAT} Charging (PWM Mode)

ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV _{IN} , V _{INSENSE}
t < 1ms, DC < 1% –0.3V to 7V
Steady State0.3V to 6V
SW, SENSE, BAT, BATSENS, SS, FAULT, CHRG, EN, NTC,
PROG, IDET, TIMER Voltage0.3V to 6V
Operating Temperature Range (Note 3) –40°C to 85°C
Operating Junction Temperature
(Note 5)40°C to 125°C
Storage Temperature Range –65°C to 125°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4001EUF-1#PBF	LTC4001EUF-1#TRPBF	40011	16-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}$ C. $V_{IN} = 5$ V, $V_{\overline{EN}} = 0$ V, $R_{PROG} = 549\Omega$, $R_{IDET} = 549\Omega$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
V _{IN}	Supply Voltage	(Note 2)		4		5.5	V
I _{IN}		PV _{IN} Connected to V _{INSENSE} , PROG and IDET Pins Open, Charger On				2	mA
		Shutdown, $\overline{EN} = V_{IN}$				50	μA
V _{FLOAT}	V _{BAT} Regulated Float Voltage	Measured from BATSENS to GNDSENS	•	4.059 4.079	4.1 4.1	4.141 4.121	V V
I _{BAT}	Current Mode Charge Current	$\begin{array}{l} R_{PROG} = 549\Omega, V_{BAT} = 3.5V \\ R_{PROG} = 1.10k, V_{BAT} = 3.5V \\ Shutdown, \overline{EN} = V_{IN} \end{array}$		1.8 0.9	2 1	2.2 1.1 ±5	Α Α μΑ
I _{TRIKL}	Trickle Charge Current	V _{BAT} = 2V		35	50	65	mA
V _{TRIKL}	Trickle Charge Threshold	V _{BAT} Rising V _{BAT} Falling		3.05 2.85	3.1 3.0	3.20 3.05	V V
V _{UVL}	V _{IN} Undervoltage Lockout Voltage	V _{IN} Rising, Measured from V _{INSENSE} to GNDSENS		2.7		2.82	V
ΔV_{UVL}	V _{IN} Undervoltage Lockout Hysteresis	Measured from V _{INSENSE} to GNDSENS			100		mV
V _{ASD}	Automatic Shutdown Threshold Voltage	VINSENSE – VBATSENS Rising (Turn-On), VBATSENSE = 4V VINSENSE – VBATSENS Falling (Turn-Off), VBATSENSE = 4V		200 15	250 30	300 60	mV mV



ELECTRICAL CHARACTERISTICS The \bullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{EN} = 0V, R_{PROG} = 549 Ω , R_{IDET} = 549 Ω , unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS
f _{OSC}	Oscillator Frequency		1.3	1.5	1.7	MHz
D	Maximum Duty Factor				100	%
R _{PFET}	R _{DS(ON)} of P-Channel MOSFET	Measured from PV _{IN} to SW		127		mΩ
R _{NFET}	R _{DS(ON)} of N-Channel MOSFET	Measured from SW to PGND		121		mΩ
t _{TIMER}	Timer Accuracy	C _{TIMER} = 0.22µF		±10		%
V _{EN}	Enable Input Threshold Voltage	V _{EN} Rising	0.6	0.8	1	V
$\Delta V_{\overline{EN}}$	Enable Input Hysteresis			100		mV
V _{PROG}	PROG Pin Voltage	$R_{PROG} = 549\Omega$		1.213		V
V _{IDET}	IDET Pin Voltage	$R_{IDET} = 549\Omega$		1.213		V
I _{IDET}	IDET Threshold	$R_{IDET} = 549\Omega$	150	200	250	mA
ICHRG	CHRG Pin Weak Pull-Down Current	V _{CHRG} = 1V	15	30	50	μA
V _{CHRG}	CHRG Pin Output Low Voltage	I _{CHRG} = 5mA		0.2	0.4	V
V _{OL}	FAULT Pin Output Low Voltage	1mA Load			0.4	V
V _{OH}	FAULT Pin Output High Voltage	1mA Load	4.6			V
V _{RECHRG}	Recharge Battery Threshold Voltage	V _{FLOAT} – V _{RECHRG} V _{BAT} Falling	50	100	135	mV
t _{RB}	Recharge Filter Time Constant		4			ms
t _{RECHRG}	Recharge Time	Percent of Total Charge Time		50		%
t _{TRIKL}	Low-Battery Trickle Charge Time	Percent of Total Charge Time, V_{BAT} < 2.8V, Measured Using BATSENS and GNDSENS Pins		25		%
I _{SS}	Soft-Start Ramp Current	$V_{BAT} < V_{FLOAT} - 100 mV$, V_{BAT} Across BATSENS and GNDSENS Pins	6	12.8	16	μA
V _{COLD}	NTC Pin Cold Temperature Fault Threshold	From NTC to GNDSENS Pin Rising Threshold Falling Threshold		0.74 V _{INSENSE} 0.72 V _{INSENSE}		V V
V _{HOT}	NTC Pin Hot Temperature Fault Threshold	From NTC to GNDSENS Pin Falling Threshold Rising Threshold		0.29 V _{INSENSE} 0.30 V _{INSENSE}		V V
V _{DIS}	NTC Disable Threshold (Falling)	From NTC to GNDSENS Pin	0.015 • V _{INSENSE}	0.02 • V _{INSENSE}	0.025 • V _{INSENSE}	V
ΔV_{DIS}	NTC Disable Hysteresis	From NTC to GNDSENS Pin		0.01 • V _{INSENSE}		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Operation with current limited wall adapters is allowed down to the undervoltage lockout threshold.

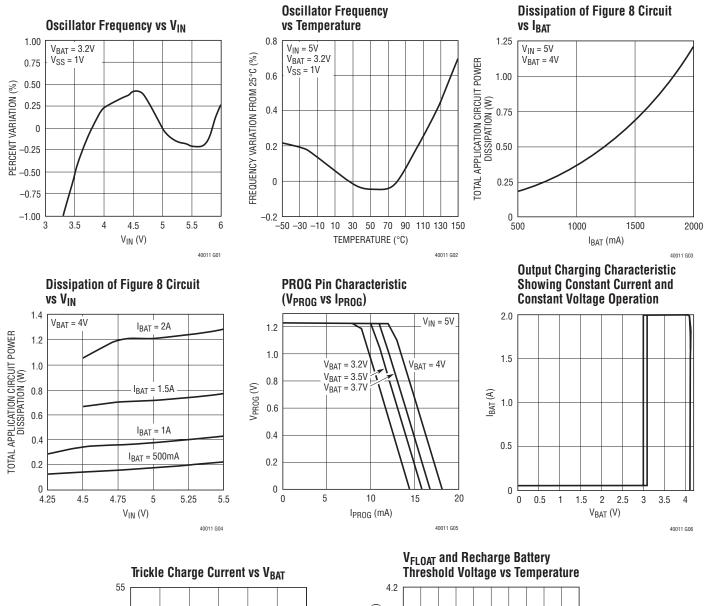
Note 3: The LTC4001E-1 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

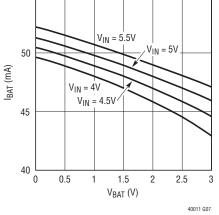
Note 4: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

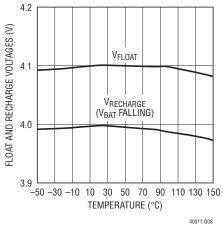
$$T_J = T_A + (P_D \bullet 37^{\circ}C/W)$$

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature my impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

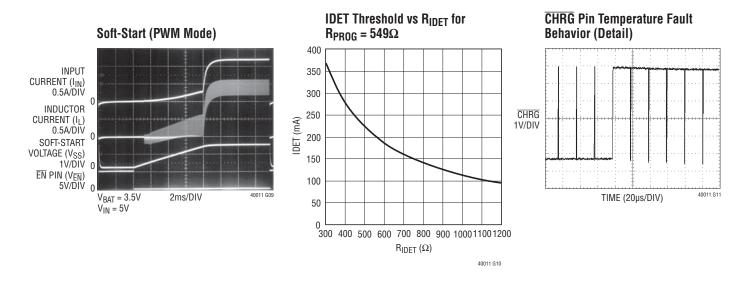








TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

BAT (Pin 1): Battery Charger Output Terminal. Connect a 10μ F ceramic chip capacitor between BAT and PGND to keep the ripple voltage small.

SENSE (Pin 2): Internal Sense Resistor. Connect to external inductor.

PGND (Pin 3): Power Ground.

GNDSENS (Pin 4): Ground Sense. Connect this pin to the negative battery terminal. GNDSENS provides a Kelvin connection for PGND and must be connected to PGND schematically.

SW (Pin 5): Switch Node Connection. This pin connects to the drains of the internal main and synchronous power MOSFET switches. Connect to external inductor.

EN (Pin 6): Enable Input Pin. Pulling the \overline{EN} pin high places the LTC4001-1 into a low power state where the BAT drain current drops to less than $3\mu A$ and the supply current is reduced to less than $50\mu A$. For normal operation, pull the pin low.

CHRG (Pin 7): Open-Drain Charge Status Output. When the battery is being charged, CHRG is pulled low by an internal N-channel MOSFET. When the charge current drops below the IDET threshold (set by the R_{IDET} programming resistor) for more than 5milliseconds, the N-channel MOSFET turns

off and a 30μ A current source is connected from \overline{CHRG} to ground. (This signal is latched and is reset by initiating a new charge cycle.) When the timer runs out or the input supply is removed, the current source will be disconnected and the \overline{CHRG} pin is forced to a high impedance state. A temperature fault causes this pin to blink.

 PV_{IN} (Pin 8): Positive Supply Voltage Input. This pin connects to the power devices inside the chip. V_{IN} ranges from 4V to 5.5V for normal operation. Operation down to the undervoltage lockout threshold is allowed with current limited wall adapters. Decouple with a 10µF or larger surface mounted ceramic capacitor.

 $V_{INSENSE}$ (Pin 9): Positive Supply Sense Input. This pin connects to the inputs of all input comparators (UVL, V_{IN} to V_{BAT}). It also supplies power to the controller portion of this chip. When the BATSENS pin rises to within 30mV of $V_{INSENSE}$, the LTC4001-1 enters sleep mode, dropping I_{IN} to 50µA. Tie this pin directly to the terminal of the PV_{IN} decoupling capacitor.

FAULT (Pin 10): Battery Fault. This pin is a logic high if a shorted battery is detected or if a temperature fault is detected. A temperature fault occurs with the temperature monitor circuit enabled and the thermistor temperature is either below 0°C or above 50°C (typical).



PIN FUNCTIONS

NTC (Pin 11): Input to the NTC (Negative Temperature Coefficient) Thermistor Temperature Monitoring Circuit. Under normal operation, tie a thermistor from the NTC pin to the GNDSENS pin and a resistor of equal value from NTC to V_{IN}. When the voltage on this pin is above $0.74V_{IN}$ (Cold, 0°C) or below $0.29V_{IN}$ (Hot, 50°C), charging is disabled and the CHRG pin blinks. When the voltage on NTC comes back between $0.74V_{IN}$ and $0.29V_{IN}$, the timer continues where it left off and charging resumes. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. If the NTC function is not used connect the NTC pin to GNDSENS. This will disable all of the NTC functions. NTC should never be pulled above V_{IN}.

PROG (Pin 12): Charge Current Program. The R_{PROG} resistor connects from this pin to GNDSENS, setting the current:

$$R_{PROG} = \frac{1.110k}{I_{BAT(AMPS)}}$$

where $\mathsf{I}_{\mathsf{BAT}}$ is the high rate battery charging current.

IDET (Pin 13): Charge Rate Detection Threshold. Connecting a resistor, R_{IDET} to GNDSENS programs the charge rate detection threshold. If $R_{IDET} = R_{PROG}$, \overline{CHRG} provides an $I_{BAT}/10$ indication. For other thresholds see the Applications Information section.

SS (Pin 14): Soft-Start/Compensation. Provides soft-start function and compensation for the float voltage control loop and compensation for the charge current control loop. Tie a soft-start/compensation capacitor between this pin and GNDSENS.

TIMER (Pin 15): Timer Capacitor. The timer period is set by placing a capacitor, C_{TIMER} , to GNDSENS. Set C_{TIMER} to:

C_{TIMER} = Time (Hrs) • 0.0733 (μF)

where time is the desired charging time.

Connect this pin to IDET to disable the timer. Connect this pin to GNDSENS to end battery charging when I_{BAT} drops below the IDET charge rate threshold.

BATSENS (Pin 16): Battery Sense Input. An internal resistor divider sets the final float voltage at this pin. The resistor divider is disconnected in sleep mode or when

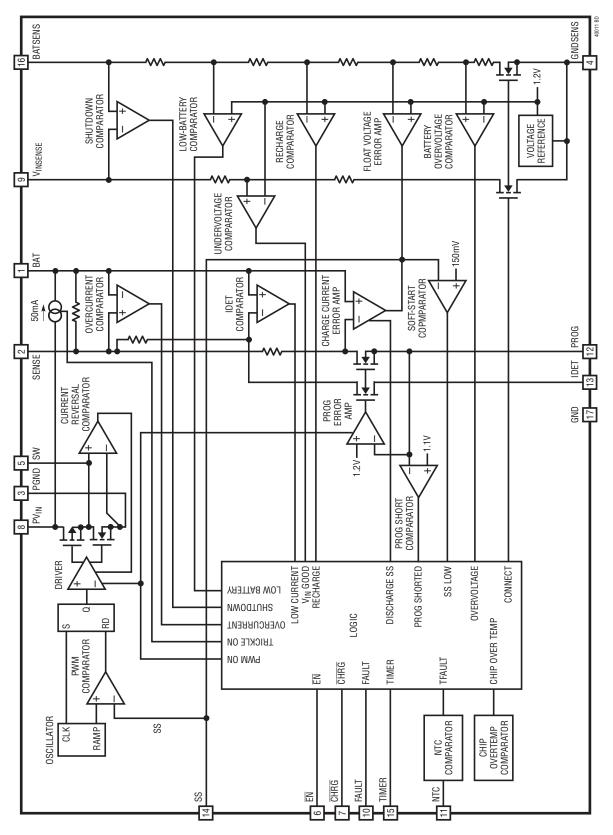
 $\overline{\text{EN}}$ = H to reduce the battery drain current. Connect this pin to the positive battery terminal.

Exposed Pad (Pin 17): Ground. This pin must be soldered to the PCB ground (PGND) for electrical contact and rated thermal performance.





BLOCK DIAGRAM



LINEAR TECHNOLOGY

LTC4001-1

OPERATION

The LTC4001-1 is a constant current, constant voltage Li-lon battery charger based on a synchronous buck architecture. Low power dissipation makes continuous high rate (2A) battery charging practical. The battery DC charge current is programmed by a resistor R_{PROG} (or a DAC output current) at the PROG pin. The final battery float voltage is internally set to 4.1V.

Charging begins when the V_{IN} voltage rises above the UVLO level (approximately 2.75V), V_{IN} is 250mV greater than the battery voltage and \overline{EN} is low. At the beginning of the charge cycle, if the battery voltage is less than the trickle charge threshold, 3V, the charger goes into trickle charge mode and delivers approximately 50mA to the battery using a linear charger. If the battery voltage stays low for more than one quarter of the charge time, the battery is considered faulty, the charge cycle is terminated and the FAULT pin produces a logic high output.

When the battery voltage exceeds the trickle charge threshold, the low rate linear charger is turned off and the high rate PWM charger ramps up (based on the SS pin capacitance) reaching its full-scale constant current (set via the PROG pin). When the battery approaches the float voltage, the charge current will start to decrease. When the charge current drops below the charge rate detection threshold (set via the IDET pin) for more than 5ms, an internal comparator turns off the internal pull-down N-channel MOSFET at the CHRG pin, and connects a weak current source (30µA typical) to ground to indicate a near end-of-charge condition.

Total charge time is set by an external capacitor connected to the timer pin. After timeout occurs, the charge cycle is terminated and the \overline{CHRG} pin is forced to a high impedance state. To restart the charge cycle, remove and reapply the input voltage, or momentarily shut the charger down via the \overline{EN} pin. Also, a new charge cycle will begin if the battery voltage drops below the recharge threshold voltage (100mV below the float voltage). A recharge cycle lasts only one-half of the normal charge time. A negative temperature coefficient (NTC) thermistor located close to the battery pack can be used to monitor battery temperature and suspend charging when battery temperature is outside the 0°C to 50°C window. A temperature fault drives the FAULT pin high and makes the CHRG pin blink. When the input voltage (V_{IN}) is present, the charger can be shut down by pulling the EN pin up.

IDET Blanking

The IDET comparator provides an end-of-charge indication by sensing when battery charge current is less than the IDET threshold. To prevent a false end-of-charge indication from occurring during soft-start, this comparator is blanked until the battery voltage approaches the float voltage.

Automatic Battery Recharge

After the charge cycle is completed and if both the battery and the input power supply (wall adapter) are still connected, a new charge cycle will begin if the battery voltage drops below 4V due to self-discharge or external loading. This will keep the battery near maximum capacity at all times without manually restarting the charge cycle.

In some applications such as battery charging in GPRS cellphones, large load current transients may cause battery voltage to momentarily drop below the recharge threshold. To prevent these transients from initiating a recharge cycle when it is not needed, the output of the recharge comparator is digitally qualified. Only if the battery voltage stays below the recharge threshold for at least 4ms will battery recharging occur. (GPRS qualification is available even if timeout is disabled.)

Undervoltage Lockout and Automatic Shutdown

Internal undervoltage lockout circuits monitor V_{IN} and keep the charger circuits shut down until V_{IN} rises above the undervoltage lockout threshold (3V). The UVLO has a built-in hysteresis of 100mV. Furthermore, to protect against reverse current, the charger also shuts down if V_{IN} is less than V_{BAT}. If automatic shutdown is tripped, V_{IN} must increase to more than 250mV above V_{BAT} to allow charging.





OPERATION

Overvoltage, Chip Overtemperature and Short-Circuit Current Protection

The LTC4001-1 includes overvoltage, chip overtemperature and several varieties of short-circuit protection.

A comparator turns off both chargers (high rate and trickle) if battery voltage exceeds the float voltage by approximately 5%. This may occur in situations where the battery is accidentally disconnected while battery charging is underway.

A comparator continuously monitors on-chip temperature and will shut off the battery charger when chip temperature

exceeds approximately 160°C. Battery charging will be enabled again when temperature drops to approximately 150°C.

Short-circuit protection is provided in several different ways. First, a hard short on the battery terminals will cause the charge to enter trickle charge mode, limiting charge current to the trickle charge current (typically 50mA). Second, PWM charging is prevented if the high rate charge current is programmed far above the 2A maximum recommended charge current (via the PROG pin). Third, an overcurrent comparator monitors the peak inductor current.



Soft-Start and Compensation Capacitor Selection

The LTC4001-1 has a low current trickle charger and a PWM-based high current charger. Soft-start is used whenever the high rate charger is initially turned on, preventing high start-up current. Soft-start ramp rate is set by the internal 12.8 μ A pull-up current and an external capacitor. The control range on the SS pin is approximately 0.3V to 1.6V. With a 0.1 μ F capacitor, the time to ramp up to maximum duty cycle is approximately 10ms.

The external capacitor on the SS pin also sets the compensation for the current control loop and the float voltage control loop. A minimum capacitance of 10nF is required.

Charge Current and IDET Programming

The LTC4001-1 has two different charge modes. If the battery is severely depleted (battery voltage less than 2.9V) a 50mA trickle current is initially used. If the battery voltage is greater than the trickle charge threshold, high rate charging is used.

This higher charge current is programmable and is approximately 915 times the current delivered by the PROG pin. This current is usually set with an external resistor from PROG to GNDSENS, but it may also be set with a current output DAC connected to the PROG pin. The voltage on the PROG pin is nominally 1.213V.

For 2A charge current:

$$R_{PROG} = \frac{915 \bullet 1.213V}{2A} \cong 554.9\Omega$$

The IDET threshold (a charge current threshold used to determine when the battery is nearly fully charged) is programmed in much the same way as the PROG pin, except that the IDET threshold is 91.5 times the current delivered by the IDET pin. This current is usually set with an external resistor from IDET to ground, but it may also be set with a current output DAC. The voltage on the PROG pin is nominally 1.213V.

For 200mA IDET current (corresponding to C/10 for a 2AHr battery):

$$R_{\text{IDET}} = \frac{91.5 \cdot 1.213V}{0.2A} \cong 554.9\Omega$$

 $1.10 k\Omega$ programs approximately 100mA and 274 Ω approximately 400mA.

For applications where IDET is set to one tenth of the high rate charge current, and slightly poorer charger current and IDET threshold accuracy is acceptable, the PROG and IDET pins may be tied together and a single resistor, R1, can program both (Figure 1).

$$R1 = \frac{457.5 \bullet 1.213}{I_{CHABGE}}$$

and

$$IDET = \frac{I_{CHARGE}}{10}$$

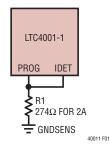


Figure 1. Programming Charge Current and IDET Threshold with a Single Resistor



The equations for calculating R1 (used in single resistor programming) differ from the equations for calculating R_{PROG} and R_{IDET} (2-resistor programming) and reflect the fact that the current from both the IDET and PROG pins must flow through a single resistor R1 when a single programming resistor is used.

CHRG Status Output Pin

When a charge cycle starts, the \overline{CHRG} pin is pulled to ground by an internal N-channel MOSFET which is capable of driving an LED. When the charge current drops below the end-of-charge (IDET) threshold for at least 4ms, and the battery voltage is close to the float voltage, the N-channel MOSFET turns off and a weak 30µA current source to ground is connected to the \overline{CHRG} pin. This weak pull-down remains until the charge cycle ends. After charging ends, the pin will become high impedance. By using two different value resistors, a microprocessor can detect three states from this pin (charging, end-of-charge and charging stopped). See Figure 2.

To detect the charge mode, force the digital output pin, OUT, high and measure the voltage on the \overline{CHRG} pin. The N-channel MOSFET will pull the pin low even with a 2k pull-up resistor. Once the charge current drops below the end-of-charge threshold, the N-channel MOSFET is turned off and a 30µA current source is connected to the \overline{CHRG} pin. The IN pin will then be pulled high by the 2k resistor connected to OUT. Now force the OUT pin into a high impedance state, the current source will pull the

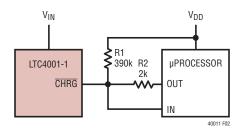


Figure 2. Microprocessor Interface

pin low through the 390k resistor. When charging stops, the CHRG pin changes to a high impedance state and the 390k resistor will then pull the pin high to indicate charging has stopped.

Charge Termination

Battery charging may be terminated several different ways, depending on the connections made to the TIMER pin. For time-based termination, connect a capacitor between the TIMER pin and GNDSENS (C_{TIMER} = Time(Hrs) 0.0733µF). Charging may be terminated when charge current drops below the IDET threshold by tying TIMER to GNDSENS. Finally, charge termination may be defeated by tying TIMER to IDET. In this case, an external device can terminate charging by pulling the EN pin high.

Battery Temperature Detection

When battery temperature is out of range (either too hot or too cold) charging is temporarily halted and the FAULT pin is driven high. In addition, if the battery is still charging at a high rate (greater than the IDET current) when a temperature fault occurs, the CHRG pin NMOS turns on and off at approximately 50kHz, alternating between a high and low duty factor at an approximate rate of 1.5Hz (Figure 3). This provides a low rate visual indication (1.5Hz) when driving an LED from the CHRG pin while providing a fast temperature fault indication (20µs typical) to a microprocessor by tying the CHRG pin to an interrupt line. Serrations within this pulse are typically 500ns wide.

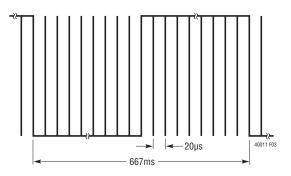


Figure 3. CHRG Temperature Fault Waveform

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and GNDSENS and the resistor, R_{NOM}, from the NTC pin to V_{INSENSE}. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C. The LTC4001-1 goes into hold mode when the resistance, R_{HOT}, of the NTC thermistor drops to 0.41 times the value of R_{NOM} . For instance for $R_{NTC} = 10k$. (The value for a Vishay NTHS0603N02N1002J thermistor at 25°C) hold occurs at approximately 4.1k, which occurs at 50°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4001-1 is designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of R_{NOM}. This resistance is R_{COLD}. For the Vishay 10k thermistor, this value is 28.2k, which corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables the NTC function.

Thermistors

The LTC4001-1 NTC trip points were designed to work with thermistors whose resistance temperature characteristics follow Vishay Dale's "R-T Curve 2." However, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 7 will also work (Vishay Dale R-T Curve 2 shows a ratio of R_{COLD} to R_{HOT} of 2.815/0.4086 = 6.89).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 1." Using these as indicated in the NTC Thermistor section will give temperature trip points of approximately 3°C and 47°C, a delta of 44°C. This delta in temperature can be moved in either direction by changing the value of R_{NOM} with respect to R_{NTC} . Increasing

 R_{NOM} will move the trip points to higher temperatures. To calculate R_{NOM} for a shift to lower temperature for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25^{\circ}\text{C}$$

where R_{COLD} is the resistance ratio of R_{NTC} at the desired cold temperature trip point. If you want to shift the trip points to higher temperatures use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.4086} \bullet R_{NTC}$$
 at 25°C

where R_{HOT} is the resistance ratio of R_{NTC} at the desired hot temperature trip point.

Here is an example using a 100k R-T Curve 1 thermistor from Vishay Dale. The difference between trip points is 44°C, from before, and we want the cold trip point to be 0°C, which would put the hot trip point at 44°C. The R_{NOM} needed is calculated as follows:

$$R_{\text{NOM}} = \frac{R_{\text{COLD}}}{2.815} \bullet R_{\text{NTC}} \text{ at } 25^{\circ}\text{C}$$
$$= \frac{3.266}{2.815} \bullet 100\text{k} = 116\text{k}$$

The nearest 1% value for R_{NOM} is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 44°C respectively. To extend the delta between the cold and hot trip points a resistor, R1, can be added in series with R_{NTC} (see Figure 4). The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086}$$
$$R1 = \frac{0.4086}{2.815 - 0.4086} \bullet (R_{COLD} - R_{HOT}) - R_{HOT}$$



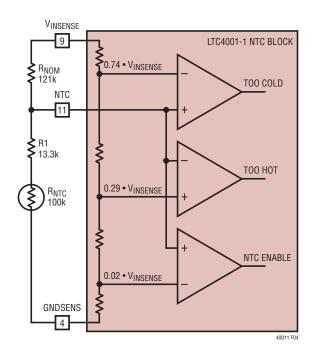


Figure 4. Extending the Delta Temperature

where R_{NOM} is the value of the bias resistor, R_{HOT} and R_{COLD} are the values of R_{NTC} at the desired temperature trip points. Continuing the example from before with a desired hot trip point of 50°C:

$$R_{\text{NOM}} = \frac{R_{\text{COLD}} - R_{\text{HOT}}}{2.815 - 0.4086} = \frac{100 \text{k} \cdot (3.2636 - 0.3602)}{2.815 - 0.4086}$$

= 120.8k, 121k is nearest 1%
R1=100k \cdot (\frac{0.4086}{2.815 - 0.4086} \cdot (3.266 - 0.3602) - 0.3602)
= 13.3k, 13.3k is nearest 1%

The final solution is as shown if Figure 4 where $R_{NOM} = 121k$, R1 = 13.3k and $R_{NTC} = 100k$ at 25°C.

Input and Output Capacitors

The LTC4001-1 uses a synchronous buck regulator to provide high battery charging current. A 10μ F chip ceramic

capacitor is recommended for both the input and output capacitors because it provides low ESR and ESL and can handle the high RMS ripple currents. However, some high Q capacitors may produce high transients due to self-resonance under some start-up conditions, such as connecting the charger input to a hot power source. For more information, refer to Application Note 88.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 1.5MHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of the output capacitor is 0.1Ω and the battery impedance is raised to 2Ω with a bead or inductor, only 5% of the ripple current will flow in the battery. Similar techniques may also be applied to minimize EMI from the input leads.



Inductor Selection

A high (1.5MHz) operating frequency was chosen for the buck switcher in order to minimize the size of the inductor. However, take care to use inductors with low core losses at this frequency. A good choice is the IHLP-2525AH-01 from Vishay Dale.

To calculate the inductor ripple current:

$$\Delta I_{L} = \frac{V_{BAT} - \frac{V_{BAT}^{2}}{V_{IN}}}{L \bullet f}$$

where V_{BAT} is the battery voltage, V_{IN} is the input voltage, L is the inductance and f is the PWM oscillator frequency (typically 1.5MHz). Maximum inductor ripple current occurs at maximum V_{IN} and V_{BAT} = V_{IN}/2.

Peak inductor current will be:

 $\mathsf{I}_{\mathsf{PK}} = \mathsf{I}_{\mathsf{BAT}} + 0.5 \bullet \Delta \mathsf{I}_{\mathsf{L}}$

where IBAT is the maximum battery charging current.

When sizing the inductor make sure that the peak current will not exceed the saturation current of the inductors. Also, ΔI_L should never exceed 0.4(I_{BAT}) as this may interfere with proper operation of the output short-circuit protection comparator. 1.5µH provides reasonable inductor ripple current in a typical application. With 1.5µH and 2A charge current:

$$\Delta I_{L} = \frac{2.85V - \frac{2.85V^{2}}{5.5V}}{1.5\mu H \bullet 1.5MHz} = 0.61A_{P-P}$$

and

I_{PK} = 2.31A

Remote Sensing

For highest float voltage accuracy, tie GNDSENS and BATSENS directly to the battery terminals. In a similar fashion, tie BAT and PGND directly to the battery terminals. This eliminates IR drops in the GNDSENS and BATSENS lines by preventing charge current from flowing in them.

Operation with a Current Limited Wall Adapter

Wall adapters with or without current limiting may be used with the LTC4001-1, however, lowest power dissipation battery charging occurs with a current limited wall adapter. To use this feature, the wall adapter must limit at a current smaller than the high rate charge current programmed into the LTC4001-1. For example, if the LTC4001-1 is programmed to charge at 2A, the wall adapter current limit must be less than 2A.

To understand operation with a current limited wall adapter, assume battery voltage, V_{BAT}, is initially below V_{TRIKL}, the trickle charge threshold (Figure 5). Battery charging begins at approximately 50mA, well below the wall adapter current limit so the voltage into the LTC4001-1 (V_{IN}) is the wall adapter's rated output voltage (VADAPTER). Battery voltage rises eventually reaching V_{TRIKL}. The linear charger shuts off, the PWM (high rate) charger turns on and a softstart cycle begins. Battery charging current rises during the soft-start cycle causing a corresponding increase in wall adapter load current. When the wall adapter reaches current limit, the wall adapter output voltage collapses and the LTC4001-1 PWM charger duty cycle ramps up to 100% (the topside PMOS switch in the LTC4001-1 buck regulator stays on continuously). As the battery voltage approaches V_{FLOAT}, the float voltage error amplifier commands the PWM charger to deliver less than ILIMIT. The wall adapter exits current limit and the V_{IN} jumps back up



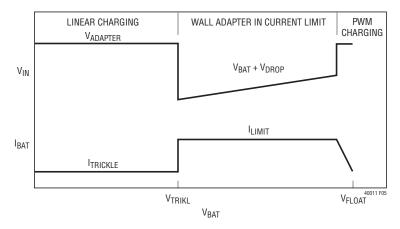


Figure 5. Charging Characteristic

to $V_{ADAPTER}$. Battery charging current continues to drop as the V_{BAT} rises, dropping to zero at V_{FLOAT} . Because the voltage drop in the LTC4001-1 is very low when charge current is highest, power dissipation is also very low.

Thermal Calculations (PWM and Trickle Charging)

The LTC4001-1 operates as a linear charger when conditioning (trickle) charging a battery and operates as a high rate buck battery charger at all other times. Power dissipation should be determined for both operating modes.

For linear charger mode:

 $P_{D} = (V_{IN} - V_{BAT}) \bullet I_{TRIKL} + V_{IN} \bullet I_{IN}$

where I_{IN} is V_{IN} current consumed by the IC.

Worst-case dissipation occurs for $V_{BAT} = 0$, maximum V_{IN} , and maximum quiescent and trickle charge current. For example with 5.5V maximum input voltage and 65mA worst case trickle charge current, and 2mA worst case chip quiescent current:

 $P_D = (5.5 - 0) \cdot 65mA + 5.5 \cdot 2mA = 368.5mW$

LTC4001-1 power dissipation is very low if a current limited wall adapter is used and allowed to enter current limit. When the wall adapter is in current limit, the voltage drop across the LTC4001-1 charger is:

 $V_{DROP} = I_{LIMIT} \bullet R_{PFET}$

where I_{LIMIT} is the wall adapter current limit and R_{PFET} is the on resistance of the topside PMOS switch.

The total LTC4001-1 power dissipation during current limited charging is:

 $P_{D} = (V_{BAT} + V_{DROP}) \bullet (I_{IN} + I_{P}) + V_{DROP} \bullet I_{LIMIT}$

where I_{IN} is the chip quiescent current and I_P is total current flowing through the IDET and PROG programming pins. Maximum dissipation in this mode occurs with the highest V_{BAT} that keeps the wall adapter in current limit (which is very close to V_{FLOAT}), highest quiescent current I_{IN} , highest PMOS on resistance R_{PFET} , highest I_{LIMIT} and highest programming current I_P .

Assume the LTC4001-1 is programmed for 2A charging and 200mA IDET and that a 1.5A wall adapter is being used:

 I_{LIMIT} = 1500mA, R_{PFET} = 127m $\Omega,~I_{IN}$ = 2mA, I_P = 4mA and $V_{BAT}\approx V_{FLOAT}$ = 4.141V

then:

 $V_{DROP} = 1500$ mA • 127m $\Omega = 190.5$ mV

and:

 $P_D = (4.141V + 0.1905V) \bullet (2mA + 4mA) + 0.1905V$ • 1500mA = 312mW

Power dissipation in buck battery charger mode may be estimated from the dissipation curves given in the Typical Performance Characteristics section of the data sheet. This will slightly overestimate chip power dissipation because it assumes all loss, including loss from external components, occurs within the chip.

Insert the highest power dissipation figure into the following equation to determine maximum junction temperature:

$$T_J = T_A + (P_D \bullet 37^{\circ}C/W)$$

The LTC4001-1 includes chip overtemperature protection. If junction temperature exceeds 160°C (typical), the chip will stop battery charging until chip temperature drops below 150°C.

Using the LTC4001-1 in Applications Without a Battery

The LTC4001-1 is normally used in end products that only operate with the battery attached (Figure 6). Under these conditions the battery is available to supply load transient currents. For indefinite operation with a powered wall adapter there are only two requirements—that the average current drawn by the load is less than the high rate charge current, and that V_{BAT} stays above the trickle charge threshold when the load is initially turned on and during other load transients. When making this determination take into account battery impedance. If battery voltage is less than the trickle charge threshold, the system load may be turned off until V_{BAT} is high enough to meet these conditions.

The situation changes dramatically with the battery removed (Figure 7). Since the battery is absent, V_{BAT} begins at zero when a powered wall adapter is first connected to the battery charger. *With a maximum load less than the LTC4001-1 trickle charge current*, battery voltage will ramp up until V_{BAT} crosses the trickle charge threshold. When this occurs, the LTC4001-1 switches over from trickle charge to high rate (PWM) charge mode but initially delivers zero current (because the soft-start pin is at zero). Battery voltage drops as a result of the system load, crossing below the trickle charge threshold. The charger re-enters trickle charge mode and the battery voltage ramps up again until the battery charger re-enters high rate mode.

The soft-start voltage is slightly higher this time around (than in the previous PWM cycle). Every successive time that the charger enters high rate (PWM) charge mode, the soft-start pin is at a slightly higher voltage. Eventually high rate charge mode begins with a soft-start voltage that causes the PWM charger to provide more current than the system load demands, and V_{BAT} rapidly rises until the float voltage is reached.

For battery-less operation, system load current should be restricted to less than the worst case trickle charge current (preferably less than 30mA) when V_{BAT} is less than 3.15V (through an undervoltage lockout or other means). Above $V_{BAT} = 3.15V$, system load current less than or equal to the high rate charge current is allowed. If operation without a battery is required, additional low-ESR output filtering improves start-up and other load transients. Battery-less start-up is also improved if a 10k resistor is placed in series with the soft-start capacitor.

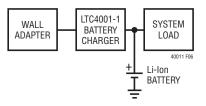


Figure 6. Typical Application



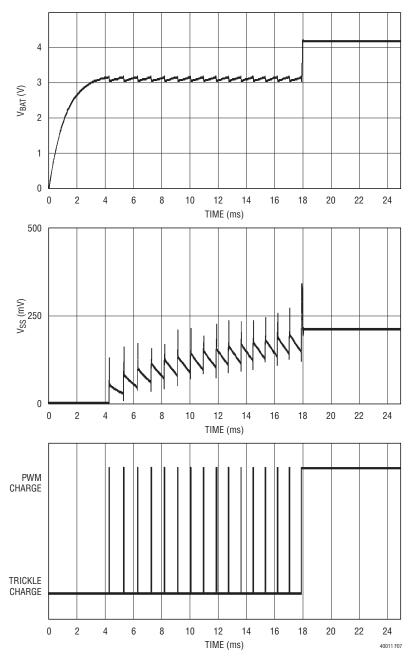


Figure 7. Battery-Less Start-Up



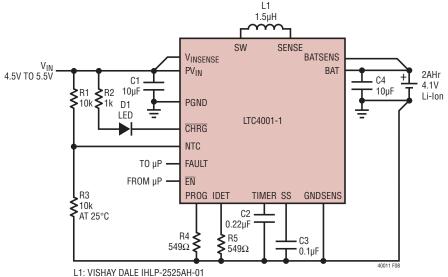
Layout Considerations

Switch rise and fall times are kept under 5ns for maximum efficiency. To minimize radiation, the SW pin and input bypass capacitor leads (between PV_{IN} and PGND) should be kept as short as possible. A ground plane should be used under the switching circuitry to prevent interplane coupling. The Exposed Pad must be connected to the ground plane for proper power dissipation. The other paths contain only DC and/or 1.5MHz tri-wave ripple current and are less critical.

With the exception of the input and output filter capacitors (which should be connected to PGND) all other components that return to ground should be connected to GNDSENS.

Recommended Components Manufacturers

For a list of recommend component manufacturers, contact the Linear Technology application department.



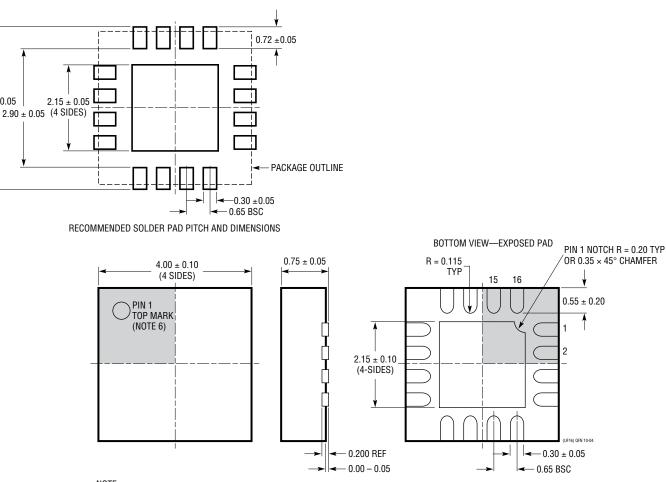
R3: NTC VISHAY DALE NTHS0603N02N1002J





PACKAGE DESCRIPTION

 4.35 ± 0.05



UF Package 16-Lead Plastic QFN (4mm × 4mm) (Reference LTC DWG # 05-08-1692)

NOTE:

1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)

2. DRAWING NOT TO SCALE

3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE

MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE

5. EXPOSED PAD SHALL BE SOLDER PLATED

6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION

ON THE TOP AND BOTTOM OF PACKAGE

