4A, High Efficiency, Standalone Li-Ion Battery Charger

FEATURES

- **Complete Charger Controller for 2-, 3- or 4-Cell Lithium-Ion Batteries**
- **High Conversion Efficiency: Up to 96%**
- **Output Currents Exceeding 4A**
- **±0.8% Accurate Preset Voltages: 8.4V, 12.6V, 16.8V**
- **Built-In Charge Termination with Automatic Restart**
- **AC Adapter Current Limiting Maximizes Charge Rate***
- Automatic Conditioning of Deeply Discharged Batteries
- Thermistor Input for Temperature Qualified Charging
- Wide Input Voltage Range: 6V to 28V
- 0.5V Dropout Voltage; Maximum Duty Cycle: 98%
- Programmable Charge Current: ±4% Accuracy
- Indicator Outputs for Charging, C/10 Current Detection and AC Adapter Present
- Charging Current Monitor Output
- 16-Pin Narrow SSOP Package

APPLICATIONS

- Notebook Computers
- Portable Instruments
- Battery-Backup Systems
- Standalone Li-Ion Chargers

DESCRIPTION

The LTC®4006 is a complete constant-current/constant-voltage charger controller for 2-, 3- or 4-cell lithium batteries in a small package using few external components. The PWM controller is a synchronous, quasi-constant frequency, constant off-time architecture that will not generate audible noise even when using ceramic capacitors.

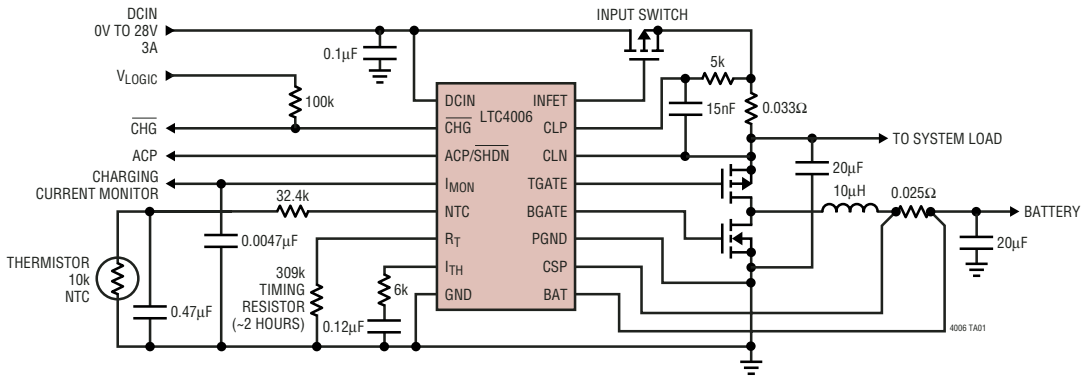
The LTC4006 is available in 8.4V, 12.6V and 16.8V versions with ±0.8% voltage accuracy. Charging current is programmable with a single sense resistor to ±4% typical accuracy. Charging current can be monitored as a representative voltage at the I_{MON} pin. A timer, programmed by an external resistor, sets the total charge time or is reset to 25% of total charge time after C/10 charging current is reached. Charging automatically resumes when the cell voltage falls below 3.9V/cell.

Fully discharged cells are automatically trickle charged at 10% of the programmed current until the cell voltage exceeds 2.5V/cell. Charging terminates if the low-battery condition persists for more than 25% of the total charge time.

The LTC4006 includes a thermistor sensor input that suspends charging if an unsafe temperature condition is detected and automatically resumes charging when the battery temperature returns to within safe limits.

TYPICAL APPLICATION

4A Li-Ion Battery Charger

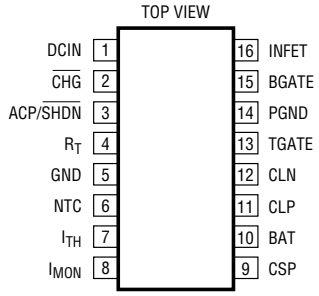


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltage from DCIN, CLP, CLN, TGATE, INFET, ACP/$\overline{SHDN}$, $\overline{CHG}$ to GND ..... +32V to –0.3V
Voltage from CLP to CLN ..... ±0.3V
CSP, BAT to GND ..... +28V to –0.3V
R_T to GND ..... +7V to –0.3V
NTC ..... +10V to –0.3V
Operating Ambient Temperature Range (Note 4) ..... –40°C to 85°C
Operating Junction Temperature ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC4006EGN-2 LTC4006EGN-4 LTC4006EGN-6
GN PART MARKING
40062 40064 40066

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	DCIN Operating Range			6		28	V
I_{DCIN}	DCIN Operating Current	Sum of Current from CLP, CLN, DCIN			3	5	mA
V_{TOL}	Voltage Accuracy	(Note 2) LTC4006-6 LTC4006-6 LTC4006-2 LTC4006-2 LTC4006-4 LTC4006-4	 ● ● ●	 8.333 8.316 12.499 12.474 16.665 16.632	 8.4 8.4 12.6 12.6 16.8 16.8	 8.467 8.484 12.700 12.726 16.935 16.968	 V V V V V V
I_{TOL}	Current Accuracy (Note 3)	$V_{CSP} – V_{BAT}$ Target = 100mV V_{BAT} = 11.5V (LTC4006-2) V_{BAT} = 7.6V (LTC4006-6) V_{BAT} = 12V (LTC4006-4)	 ●	–4 –5		4 5	% %
		V_{BAT} < 6V, $V_{CSP} – V_{BAT}$ Target = 10mV		–60		60	%
		6V ≤ V_{BAT} ≤ V_{LOBAT}, $V_{CSP} – V_{BAT}$ Target = 10mV		–40		40	%
T_{TOL}	Termination Timer Accuracy	R_{RT} = 270k	●	–15		15	%
Shutdown							
	Battery Leakage Current	DCIN = 0V DCIN = 0V DCIN = 20V, $V_{\overline{SHDN}}$ = 0V, V_{BAT} = 12V	 ● ●	 –10	20 25 0	35 45 10	µA µA µA
UVLO	Undervoltage Lockout Threshold	DCIN Rising, V_{BAT} = 0V	●	4.2	4.7	5.5	V
	Shutdown Threshold at ACP/$\overline{SHDN}$		●	1		2.5	V
	DCIN Current in Shutdown	$V_{\overline{SHDN}}$ = 0V, Sum of Current from CLP, CLN, DCIN			2	3	mA
Current Sense Amplifier, CA1							
	Input Bias Current Into BAT Pin				11.67		µA
CMSL	CA1/I_1 Input Common Mode Low		●	0			V
CMSH	CA1/I_1 Input Common Mode High		●			V_{CLN} – 0.2	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Comparators I_{CMP} and I_{REV}							
I_{TMAX}	Maximum Current Sense Threshold ($V_{CSP} - V_{BAT}$)	V_{ITH} = 2.5V	●	140	165	200	mV
I_{TREV}	Reverse Current Threshold ($V_{CSP} - V_{BAT}$)				–30		mV
Current Sense Amplifier, CA2							
	Transconductance				1		mmho
	Source Current	Measured at I_{TH}, V_{ITH} = 1.4V			–40		µA
	Sink Current	Measured at I_{TH}, V_{ITH} = 1.4V			40		µA
Current Limit Amplifier							
	Transconductance				1.5		mmho
V_{CLP}	Current Limit Threshold		●	93	100	107	mV
I_{CLP}	CLP Input Bias Current				100		nA
Voltage Error Amplifier, EA							
	Transconductance				1		mmho
	Sink Current	Measured at I_{TH}, V_{ITH} = 1.4V			36		µA
OVSD	Overvoltage Shutdown Threshold as a Percent of Programmed Charger Voltage		●	102	107	110	%
Input P-Channel FET Driver (INFET)							
	DCIN Detection Threshold ($V_{DCIN} - V_{CLN}$)	DCIN Voltage Ramping Up from V_{CLN} – 0.1V	●	0	0.17	0.25	V
	Forward Regulation Voltage ($V_{DCIN} - V_{CLN}$)		●		25	50	mV
	Reverse Voltage Turn-Off Voltage ($V_{DCIN} - V_{CLN}$)	DCIN Voltage Ramping Down	●	–60	–25		mV
	INFET "On" Clamping Voltage ($V_{DCIN} - V_{INFET}$)	I_{INFET} = 1µA	●	5	5.8	6.5	V
	INFET "Off" Clamping Voltage ($V_{DCIN} - V_{INFET}$)	I_{INFET} = –25µA				0.25	V
Thermistor							
NTCVR	Reference Voltage During Sample Time				4.5		V
	High Threshold	V_{NTC} Rising	●	NTCVR • 0.48	NTCVR • 0.5	NTCVR • 0.52	V
	Low Threshold	V_{NTC} Falling	●	NTCVR • 0.115	NTCVR • 0.125	NTCVR • 0.135	V
	Thermistor Disable Current	$V_{NTC} \leq$ 10V				10	µA
Indicator Outputs (ACP/$\overline{SHDN}$, $\overline{CHG}$)							
C10TOL	C/10 Indicator Accuracy	Voltage Falling at PROG	●	0.375	0.400	0.425	V
LBTOL	LOBAT Threshold Accuracy	LTC4006-6 LTC4006-2 LTC4006-4	● ● ●	4.70 7.27 9.70	4.93 7.5 10	5.14 7.71 10.28	V V V
	RESTART Threshold Accuracy	LTC4006-6 LTC4006-2 LTC4006-4	● ● ●	7.5 11.35 15.15	7.8 11.7 15.6	7.96 11.94 15.92	V V V
V_{OL}	Low Logic Level of ACP/$\overline{SHDN}$, $\overline{CHG}$	I_{OL} = 100µA	●			0.5	V
V_{OH}	High Logic Level of ACP/$\overline{SHDN}$	I_{OH} = –1µA	●	2.7			V
I_{PO}	Pull-Up Current on ACP/$\overline{SHDN}$	V = 0V			–10		µA
IC10	C/10 Indicator Sink Current from $\overline{CHG}$	V_{OH} = 3V	●	15	25	38	µA
I_{OFF}	Off State Leakage Current of $\overline{CHG}$	V_{OH} = 3V		–1		1	µA
	Timer Defeat Threshold at $\overline{CHG}$			1			V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator							
f_{OSC}	Regulator Switching Frequency			255	300	345	kHz
f_{MIN}	Regulator Switching Frequency in Drop Out	Duty Cycle ≥ 98%		20	25		kHz
DC_{MAX}	Regulator Maximum Duty Cycle	$V_{CSP} = V_{BAT}$		98	99		%
Gate Drivers (TGATE, BGATE)							
	V_{TGATE} High ($V_{CLN} - V_{TGATE}$)	I_{TGATE} = –1mA				50	mV
	V_{BGATE} High	C_{LOAD} = 3000pF		4.5	5.6	10	V
	V_{TGATE} Low ($V_{CLN} - V_{TGATE}$)	C_{LOAD} = 3000pF		4.5	5.6	10	V
	V_{BGATE} Low	I_{BGATE} = 1mA				50	mV
	TGATE Transition Time						
TGTR	TGATE Rise Time	C_{LOAD} = 3000pF, 10% to 90%			50	110	ns
TGTF	TGATE Fall Time	C_{LOAD} = 3000pF, 10% to 90%			50	100	ns
	BGATE Transition Time						
BGTR	BGATE Rise Time	C_{LOAD} = 3000pF, 10% to 90%			40	90	ns
BGTF	BGATE Fall Time	C_{LOAD} = 3000pF, 10% to 90%			40	80	ns
	V_{TGATE} at Shutdown ($V_{CLN} - V_{TGATE}$)	I_{TGATE} = –1µA, DCIN = 0V, CLN = 12V				100	mV
	V_{BGATE} at Shutdown	I_{BGATE} = 1µA, DCIN = 0V, CLN = 12V				100	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

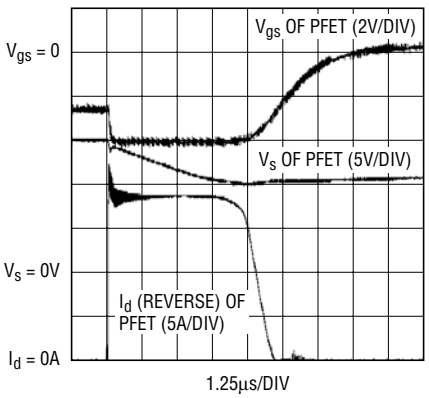
Note 2: See Test Circuit

Note 3: Does not include tolerance of current sense resistor.

Note 4: The LTC4006E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

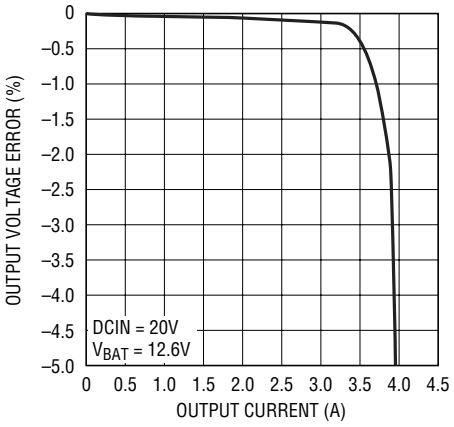
INFET Response Time to Reverse Current



TEST PERFORMED ON DEMOBOARD
V_{IN} = 15VDC LTC4006-2
CHARGER = ON INFET = 1/2 Si4925DY
I_{CHARGE} = <10mA

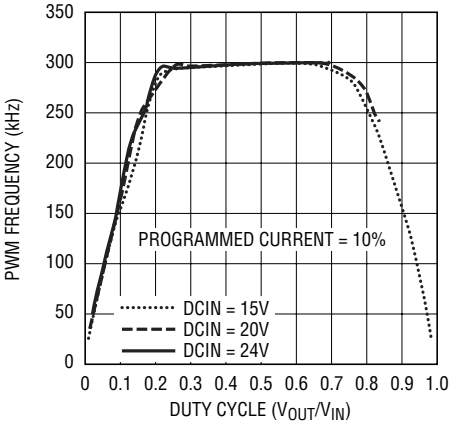
4006 G01

V_{OUT} vs I_{OUT}



4006 G02

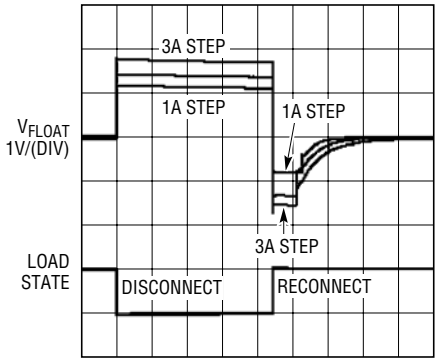
PWM Frequency vs Duty Cycle



4006 G03

TYPICAL PERFORMANCE CHARACTERISTICS

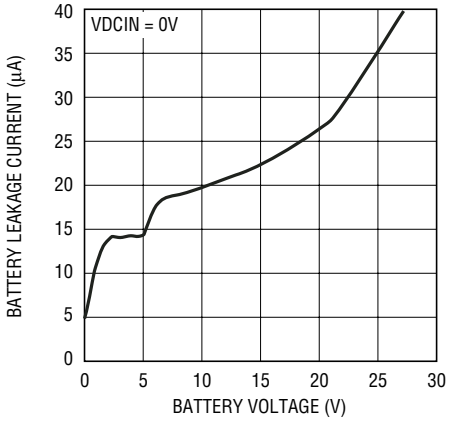
Disconnect/Reconnect Battery (Load Dump)



LOAD CURRENT = 1A, 2A, 3A
DCIN = 20V
LTC4006-2

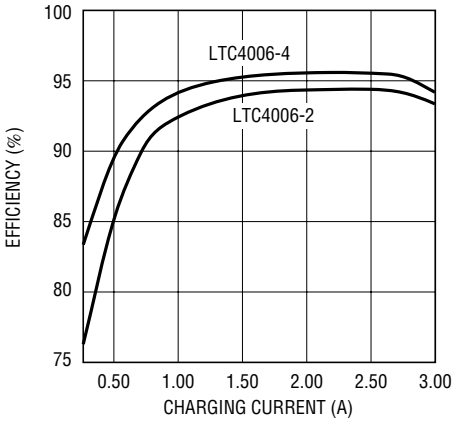
4006 G04

Battery Leakage Current vs Battery Voltage



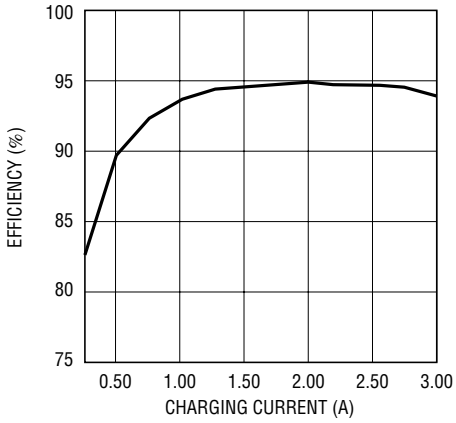
4006 G05

Efficiency at 19VDC V_{IN}



4006 G07

LTC4006-2 Efficiency with 15VDC V_{IN}



4006 G08

PIN FUNCTIONS

DCIN (Pin 1): External DC Power Source Input. Bypass this pin with at least 0.01µF. See Applications Information section.

$\overline{\text{CHG}}$ (Pin 2): Open-Drain Charge Status Output. When the battery is being charged, the $\overline{\text{CHG}}$ pin is pulled low by an internal N-channel MOSFET. When the charge current drops below 10% of programmed current, the N-channel MOSFET turns off and a 25µA current source is connected from the $\overline{\text{CHG}}$ pin to GND. When the timer runs out or the input supply is removed, the current source will be disconnected and the $\overline{\text{CHG}}$ pin is forced into a high impedance state. A pull-up resistor is required. The timer function is defeated by forcing this pin below 1V (or connecting it to GND).

ACP/$\overline{\text{SHDN}}$ (Pin 3): Open-Drain Output used to indicate if the AC adapter voltage is adequate for charging. Active high digital output. Internal 10µA pull-up to 3.5V. The charger can also be inhibited by pulling this pin below 1V. Reset the charger by pulsing the pin low for a minimum of 0.1µs.

PIN FUNCTIONS

R_T (Pin 4): Timer Resistor. The timer period is set by placing a resistor, R_{RT}, to GND.

The timer period is t_{TIMER} = (1hour • R_{RT}/154k)

If this resistor is not present, the charger will not start.

GND (Pin 5): Ground for low power circuitry.

NTC (Pin 6): A thermistor network is connected from NTC to GND. This pin determines if the battery temperature is safe for charging. The charger and timer are suspended if the thermistor indicates a temperature that is unsafe for charging. The thermistor function may be disabled with a 300k to 500k resistor from DCIN to NTC.

I_{TH} (Pin 7): Control Signal of the Inner Loop of the Current Mode PWM. Higher I_{TH} voltage corresponds to higher charging currrent in normal operation. A 6.04k resistor, in series with a capacitor of at least 0.1µF to GND, provides loop compensation. Typical full-scale output current is 40µA. Nominal voltage range for this pin is 0V to 3V.

I_{MON} (Pin 8): Current Monitoring Output. The voltage at this pin provides a linear indication of charging current. Peak current is equivalent to 1.19V. Zero current is approximately 0.309V. A capacitor from I_{MON} to ground is required to filter higher frequency components. If V_{BAT} < 2.5V/cell, then $V(I_{MON})$ = 1.19V when conditioning a depleted battery. Any current sourced or sinked from this pin directly affects the charging current accuracy. If this pin is to be monitored, a high impedance input buffer should be used.

CSP (Pin 9): Current Amplifier CA1 Input. This pin and the BAT pin measure the voltage across the sense resistor, R_{SENSE}, to provide the instantaneous current signals required for both peak and average current mode operation.

BAT (Pin 10): Battery Sense Input and the Negative Reference for the Current Sense Resistor. A precision internal resistor divider sets the final float potential on this pin. The resistor divider is disconnected during shutdown.

CLP (Pin 11): Positive Input to the Supply Current Limiting Amplifier, CL1. The threshold is set at 100mV above the voltage at the CLN pin. When used to limit supply current, a filter is needed to filter out the switching noise. If no current limit function is desired, connect this pin to CLN.

CLN (Pin 12): Negative Reference for the Input Current Limit Amplifier, CL1. This pin also serves as the power supply for the IC. A 10µF to 22µF bypass capacitor should be connected as close as possible to this pin.

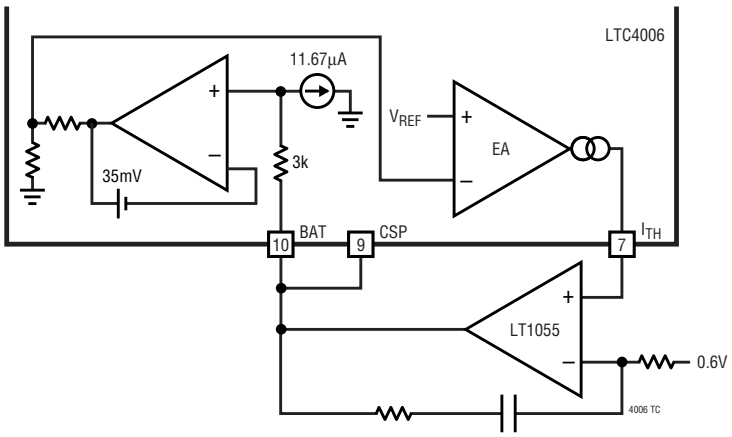
TGATE (Pin 13): Drives the top external P-channel MOSFET of the battery charger buck converter.

PGND (Pin 14): High Current Ground Return for the BGATE Driver.

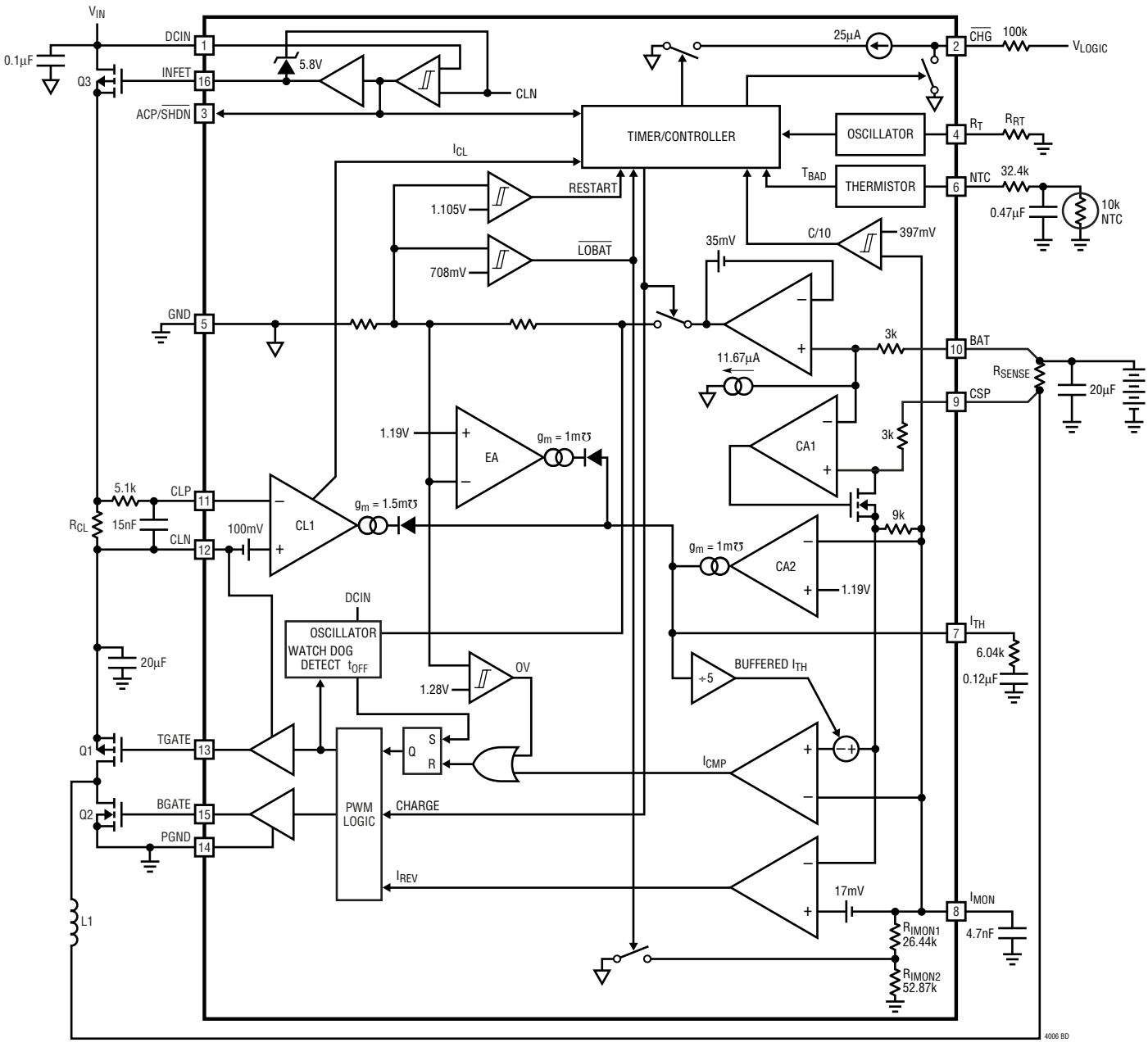
BGATE (Pin 15): Drives the bottom external N-channel MOSFET of the battery charger buck converter.

INFET (Pin 16): Drives the Gate of the External Input PFET.

TEST CIRCUIT



BLOCK DIAGRAM



OPERATION

Overview

The LTC4006 is a synchronous current mode PWM step-down (buck) switcher battery charger controller. The charge current is programmed by the sense resistor (R_{SENSE}) between the CSP and BAT pins. The final float voltage is internally programmed to 8.4V (LTC4006-6), 12.6V (LTC4006-2) or 16.8V (LTC4006-4) with better than ±0.8% accuracy. Charging begins when the potential at the DCIN pin rises above the voltage at CLN (and the UVLO voltage) and the ACP/$\overline{SHDN}$ pin is allowed to go high; the $\overline{CHG}$ pin is set low. At the beginning of the charge cycle, if the cell voltage is below 2.5V, the charger will trickle charge the battery with 10% of the maximum programmed current. If the cell voltage stays below 2.5V for 25% of the total charge time, the charge sequence will be terminated immediately and the $\overline{CHG}$ pin will be set to a high impedance.

An external thermistor network is sampled at regular intervals. If the thermistor value exceeds design limits, charging is suspended. If the thermistor value returns to an acceptable value, charging resumes. An external resistor on the R_T pin sets the total charge time. The timer can be defeated by forcing the $\overline{CHG}$ pin to a low voltage.

As the battery approaches the final float voltage, the charge current will begin to decrease. When the current drops to 10% of the programmed charge current, an internal C/10 comparator will indicate this condition by sinking 25µA at the $\overline{CHG}$ pin. The charge timer is also reset to 25% of the total charge time. If this condition is caused by an input current limit condition, described below, then the C/10 comparator will be inhibited. When a time-out occurs, charging is terminated immediately and the $\overline{CHG}$ pin changes to a high impedance. The charger will automatically restart if the cell voltage is less than 3.9V. To restart the charge cycle manually, simply remove the input voltage and reapply it, or force the ACP/$\overline{SHDN}$ pin low momentarily. When the input voltage is not present, the charger goes into a sleep mode, dropping battery current drain to 15µA. This greatly reduces the current drain on the battery and increases the standby time. The charger can be inhibited at any time by forcing the ACP/$\overline{SHDN}$ pin to a low voltage.

Input FET

The input FET circuit performs two functions. It enables the charger if the input voltage is higher than the CLN pin and provides the logic indicator of AC present on the ACP/$\overline{SHDN}$ pin. It controls the gate of the input FET to keep a low forward voltage drop when charging and also prevents reverse current flow through the input FET.

If the input voltage is less than V_{CLN}, it must go at least 170mV higher than V_{CLN} to activate the charger. When this occurs the ACP/$\overline{SHDN}$ pin is released and pulled up with an internal load to indicate that the adapter is present. The gate of the input FET is driven to a voltage sufficient to keep a low forward voltage drop from drain to source. If the voltage between DCIN and CLN drops to less than 25mV, the input FET is turned off slowly. If the voltage between DCIN and CLN is ever less than –25mV, then the input FET is turned off in less than 10µs to prevent significant reverse current from flowing in the input FET. In this condition, the ACP/$\overline{SHDN}$ pin is driven low and the charger is disabled.

Battery Charger Controller

The LTC4006 charger controller uses a constant off-time, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the SR latch and turned off when the main current comparator I_{CMP} resets the SR latch. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current trips the current comparator I_{REV} or the beginning of the next cycle. The oscillator uses the equation:

$$t_{OFF} = \frac{V_{DCIN} - V_{BAT}}{V_{DCIN} \bullet f_{OSC}}$$

to set the bottom MOSFET on time. This activity is diagrammed in Figure 1.

The peak inductor current, at which I_{CMP} resets the SR latch, is controlled by the voltage on I_{TH}. I_{TH} is in turn controlled by several loops, depending upon the situation at hand. The average current control loop converts the voltage between CSP and BAT to a representative current. Error amp CA2

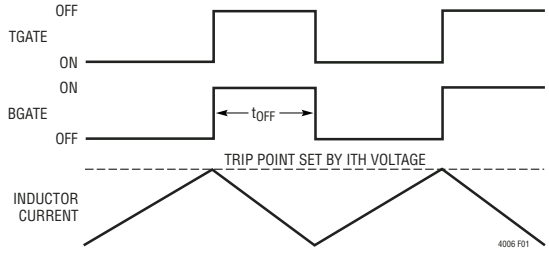


Figure 1

OPERATION

Table 1. Truth Table for LTC4006 Operation

MODE	DCIN	BAT VOLTAGE	BAT CURRENT	ACP/$\overline{SHDN}$	TIMER STATE	$\overline{CHG}$*
Shut Down by Low Adapter Voltage	<BAT	>UVLO	Leakage	LOW	Reset	HIGH
Conditioning a Depleted Battery	>BAT	<2.5V/Cell	10% Programmed Current	HIGH	Running	LOW
Normal Charging	>BAT	>2.5V/Cell	Programmed Current	HIGH	Running	LOW
Input Current Limited Charging	>BAT	>2.5V/Cell	Programmed Current	HIGH	Running	LOW
Charger Paused Due to Thermistor Out of Range	>BAT	X	OFF	HIGH	Paused	LOW or 25µA (Faulted)
Shut Down by ACP/$\overline{SHDN}$ Pin	>BAT	X	OFF	Forced LOW	Reset	HIGH
Terminated by Low-Battery Fault (Note 1)	>BAT	<2.5V/Cell	OFF	HIGH	>T/4 Stopped	HIGH (Faulted)
Top-Off Charging. C/10 is Latched	>BAT	V_{FLOAT}	OFF	HIGH	<T/4 After C/10 Comparator Trip. Running	25µA
Timer is Reset by C/10 Comparator (Latched), then Terminates After 1/4 T	>BAT	V_{FLOAT}	OFF	HIGH	>T/4 After C/10 Comparator Trip. Stopped	HIGH (Waiting for Restart)
Terminated by Expired Timer	>BAT	V_{FLOAT}**	OFF	HIGH	>T Stopped	HIGH (Waiting for Restart)
Timer Defeated. (Low-Battery Conditioning Still Functional)	X	X	X	X	X	Forced LOW
Shut Down by Undervoltage Lockout	>BAT and <UVL	<UVL	OFF	HIGH	Reset	HIGH**
Timer Defeated Until V_{BAT} > 3.9V/Cell	>BAT	2.5V ≤ V_{BAT} ≤3.9V (V/Cell)	Programmed Current	HIGH	Running	LOW

*Open Drain. High when used with pull-up resistor.
**Most probable condition, X = Don't care

Note 1: If a depleted battery is inserted while the charger is in this state, the charger must be reset to initiate charging.

compares this current against the desired current programmed by R_{IMON} at the I_{MON} pin and adjusts I_{TH} until:

$$\frac{V_{REF}}{R_{IMON}} = \frac{V_{CSP} - V_{BAT} + 11.67\mu A \bullet 3k\Omega}{3k\Omega}$$

therefore,

$$I_{CHARGE} = \left(\frac{V_{REF}}{R_{IMON}} - 11.67\mu A\right) \bullet \frac{3k\Omega}{R_{SENSE}}$$

The voltage at BAT is divided down by an internal resistor divider and is used by error amp EA to decrease I_{TH} if the divider voltage is above the 1.19V reference. When the charging current begins to decrease, the voltage at I_{MON} will decrease in direct proportion. The voltage at I_{MON} is then given by:

$$V_{IMON} = \left(I_{CHARGE} \bullet R_{SENSE} + 11.67\mu A \bullet 3k\Omega\right) \bullet \frac{R_{IMON}}{3k\Omega}$$

The accuracy of V_{IMON} will range from 0% to I_{TOL}.

V_{IMON} is plotted in Figure 2.

The amplifier CL1 monitors and limits the input current to a preset level (100mV/R_{CL}). At input current limit, CL1 will decrease the I_{TH} voltage, thereby reducing charging current. When this condition is detected, the C/10 indicator will

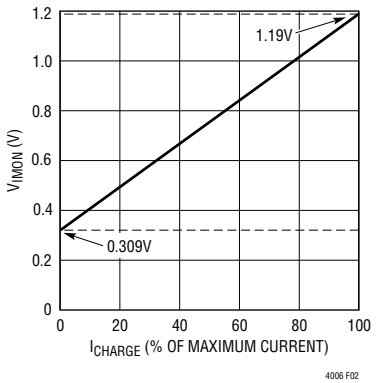


Figure 2. V_{IMON} vs I_{CHARGE}

OPERATION

Table 2. Truth Table for LTC4006 Operation (Supplemental)

NUMBER	FROM STATE	TO STATE	MODE	DCIN	BAT VOLTAGE	PRESENT C/10 LATCH	NEXT C/10 LATCH	MAX BAT CURRENT	ACP/$\overline{SHDN}$	TIMER STATE	$\overline{CHG}$*
1	Any	MSD	Shut Down by Low Adapter Voltage	<BAT			0	OFF	LOW	Reset	HIGH
2	MSD	SD	Charge Shutdown	>BAT			0	OFF	HIGH	Reset	HIGH
3	SD, CONDITION, CHARGE	SD	Shut Down by Undervoltage Lockout	>BAT and <UVL				OFF	HIGH	Reset	HIGH**
4	SD	CONDITION	Start Conditioning a Depleted Battery	>BAT	<2.5V/Cell			10% Programmed Current	HIGH		LOW
5	CONDITION	CONDITION	Input Current Limited Condition Charging	>BAT	<2.5V/Cell			<10% Programmed Current (Note 2)	HIGH	Running	LOW
6	CONDITION	CONDITION	Conditioning a Depleted Battery	>BAT	<2.5V/Cell			10% Programmed Current	HIGH	Running	LOW
7	CONDITION	CONDITION	Timer Defeated. (Low-Battery Conditioning Still Functional)	>BAT	<2.5V/Cell			10% Programmed Current	HIGH	Ignored	Forced LOW
8	CONDITION	SD	Charger Paused Due to Thermistor Out of Range	>BAT	<2.5V/Cell			OFF	HIGH	Paused	LOW (Faulted)
9	CONDITION	SD	Timeout in CONDITION Mode	>BAT	<2.5V/Cell			OFF	HIGH	>T/4	HIGH (Faulted)
10	CONDITION	SD	Shut Down by ACP/$\overline{SHDN}$ Pin	>BAT	<2.5V/Cell		0	OFF	Forced LOW	Reset	HIGH
11	CONDITION	CHARGE	Start Normal Charging	>BAT	>2.5V/Cell			Programmed Current	HIGH	Running	
12	CHARGE	CHARGE	Timer Defeated. (Low-Battery Conditioning Still Functional)	>BAT	>2.5V/Cell			Programmed Current	HIGH	Ignored	Forced LOW
13	SD	CHARGE	Restart	>BAT	$2.5V \le V_{BAT} \le 3.9V$ (V/Cell)		0	Programmed Current	HIGH	Reset	
14	CHARGE	CHARGE	Top-Off Charging	>BAT	>3.9V/Cell	0		Programmed Current	HIGH	Running	LOW
15	CHARGE	CHARGE	C/10 Latch is SET when Battery Current is Less Than 10% of Programmed Current	>BAT	>2.5V/Cell		1	Programmed Current	HIGH	Reset	25µA
16	CHARGE	CHARGE	Top-Off Charging	>BAT	>3.9V/Cell	1		Programmed Current	HIGH	Running	25µA
17	CHARGE	CHARGE	Input Current Limited Charging	>BAT	>2.5V/Cell			<Programmed Current (Note 2)	HIGH		
18	CHARGE	SD	Charger Paused Due to Thermistor Out of Range	>BAT	>2.5V/Cell			OFF	HIGH	Paused	LOW or 25µA (Faulted)
19	CHARGE	SD	Shut Down by ACP/$\overline{SHDN}$ Pin	>BAT	>2.5V/Cell		0	OFF	Forced LOW	Reset	HIGH
20	CHARGE	SD	Terminated by Low-Battery Fault (Note 1)	>BAT	<2.5V/Cell		0	OFF	HIGH	>T/4 then Reset	HIGH (Faulted)
21	CHARGE	SD	Terminates After 1/4 T	>BAT	V_{FLOAT}	1		OFF	HIGH	>T/4 then Reset	HIGH
22	CHARGE	SD	Terminates After T	>BAT	V_{FLOAT}**	0		OFF	HIGH	>T/4 then Reset	HIGH

Note 1: If a depleted battery is inserted while the charger is in this state, the charger must be reset to initiate charging.

Note 2: See section on "Adapter Limiting".

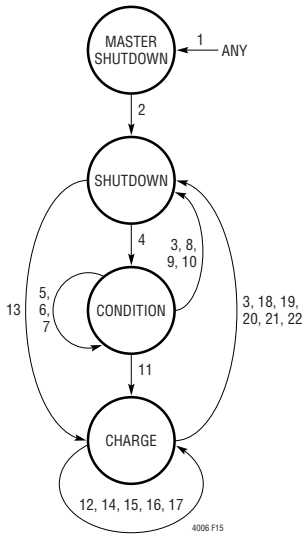
Note 3: The information contained in this table is supplemental to the LTC4006 data sheet and has not been production qualified.

Note 4: Blank fields indicate no change, not considered, or other states impact value.

*Open Drain. High when used with pull-up resistor.

** Most probable condition.

LTC4006: State Diagram (Supplemental)



OPERATION

be inhibited if it is not already active. If the charging current decreases below 10% to 15% of programmed current, while engaged in input current limiting, BGATE will be forced low to prevent the charger from discharging the battery. Audible noise can occur in this mode of operation.

An overvoltage comparator guards against voltage transient overshoots (>7% of programmed value). In this case, both MOSFETs are turned off until the overvoltage condition is cleared. This feature is useful for batteries which "load dump" themselves by opening their protection switch to perform functions such as calibration or pulse mode charging.

As the voltage at BAT increases to near the input voltage at DCIN, the converter will attempt to turn on the top MOSFET continuously ("dropout"). A watchdog timer detects this condition and forces the top MOSFET to turn off for about 300ns at 40µs intervals. This is done to prevent audible noise when using ceramic capacitors at the input and output.

Charger Startup

When the charger is enabled, it will not begin switching until the I_{TH} voltage exceeds a threshold that assures initial current will be positive. This threshold is 5% to 15% of the maximum programmed current. After the charger begins switching, the various loops will control the current at a level that is higher or lower than the initial current. The duration of this transient condition depends upon the loop compensation but is typically less than 100µs.

Thermistor Detection

The thermistor detection circuit is shown in Figure 3. It requires an external resistor and capacitor in order to function properly.

The thermistor detector performs a sample-and-hold function. An internal clock, whose frequency is determined by the timing resistor connected to R_T, keeps switch S1 closed to sample the thermistor:

$t_{SAMPLE} = 127.5 \bullet 20 \bullet R_{RT} \bullet 17.5pF = 13.8ms,$

for $R_{RT} = 309k$

The external RC network is driven to approximately 4.5V and settles to a final value across the thermistor of:

$$V_{RTH(FINAL)} = \frac{4.5V \bullet R_{TH}}{R_{TH} + R9}$$

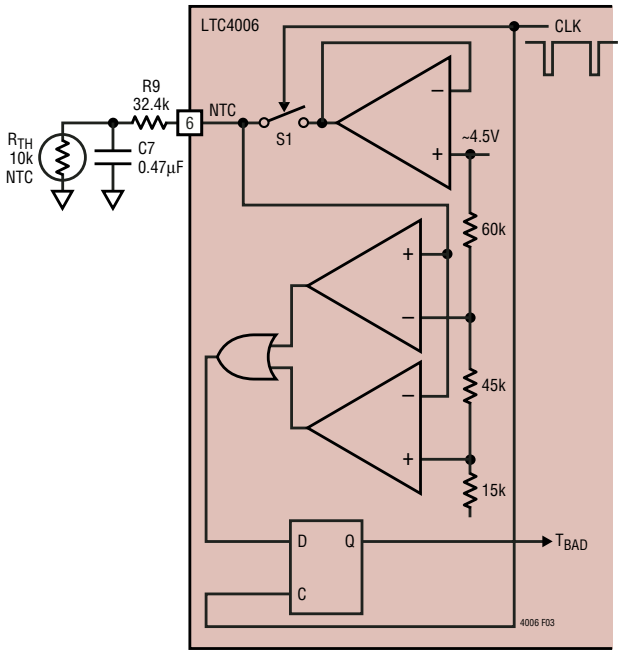


Figure 3

This voltage is stored by C7. Then the switch is opened for a short period of time to read the voltage across the thermistor.

$t_{HOLD} = 10 \bullet R_{RT} \bullet 17.5pF = 54µs,$

for $R_{RT} = 309k$

When the t_{HOLD} interval ends the result of the thermistor testing is stored in the D flip-flop (DFF). If the voltage at NTC is within the limits provided by the resistor divider feeding the comparators, then the NOR gate output will be low and the DFF will set T_{BAD} to zero and charging will continue. If the voltage at NTC is outside of the resistor divider limits, then the DFF will set T_{BAD} to one, the charger will be shut down, and the timer will be suspended until T_{BAD} returns to zero (see Figure 4).

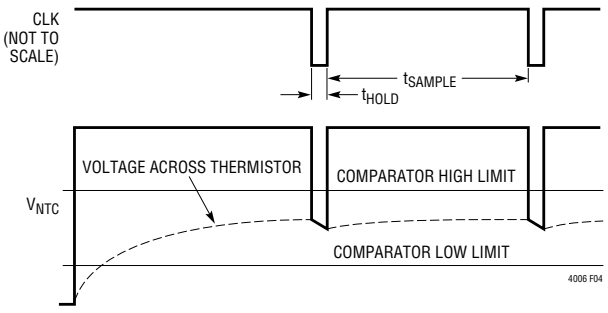


Figure 4

APPLICATIONS INFORMATION

Charger Current Programming

The basic formula for charging current is:

$$I_{CHARGE(MAX)} = \frac{100mV}{R_{SENSE}}$$

Table 3. Recommended R_{SENSE} Resistor Values

I_{MAX} (A)	R_{SENSE} (Ω) 1%	R_{SENSE} (W)
1.0	0.100	0.25
2.0	0.050	0.25
3.0	0.033	0.5
4.0	0.025	0.5

Setting the Timer Resistor

The charger termination timer is designed for a range of 1 hour to 3 hours with a ±15% uncertainty. The timer is programmed by the resistor R_{RT} using the following equation:

$t_{TIMER} = 10 \bullet 2^{27} \bullet R_{RT} \bullet 17.5pF$ (Refer to Figure 5) (seconds)

It is important to keep the parasitic capacitance on the R_T pin to a minimum. The trace connecting R_T to R_{RT} should be as short as possible.

$\overline{CHG}$ Status Output Pin

When the charge cycle starts, the $\overline{CHG}$ pin is pulled down to ground by an internal N-channel MOSFET that can drive more than 100µA. When the charge current drops to 10% of the full-scale current (C/10), the N-channel MOSFET is turned off and a weak 25µA current source to ground is connected to the $\overline{CHG}$ pin. After a time out occurs, the pin will go into a high impedance state. By using two different value pull-up resistors, a microprocessor can detect three states from this pin (charging, C/10 and stop charging). See Figure 6.

Battery Detection

It is generally not good practice to connect a battery while the charger is running. The timer is in an unknown state and the charger could provide a large surge current into the battery for a brief time. The circuit shown in Figure 7 keeps the charger shut down and the timer reset while a battery is not connected.

Alternatively, a normally closed switch can be used to detect when the battery is present (see Figure 8).

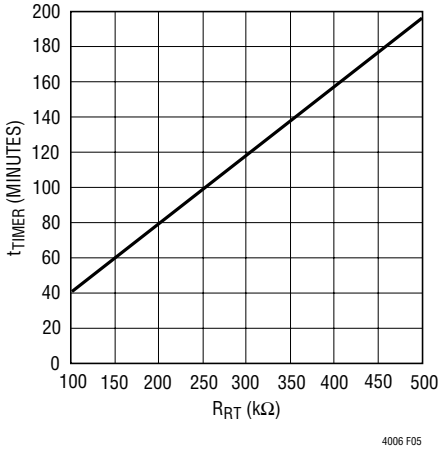


Figure 5. t_{TIMER} vs R_{RT}

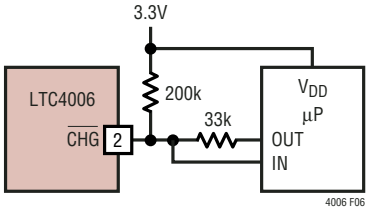


Figure 6. Microprocessor Interface

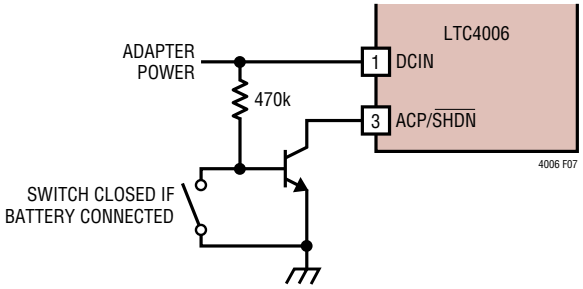


Figure 7

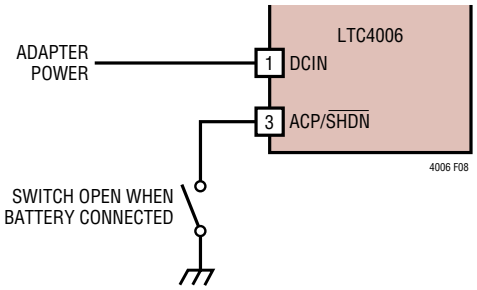


Figure 8

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Soft-Start

The LTC4006 is soft started by the 0.12µF capacitor on the I_{TH} pin. On start-up, I_{TH} pin voltage will rise quickly to 0.5V, then ramp up at a rate set by the internal 40µA pull-up current and the external capacitor. Battery charging current starts ramping up when I_{TH} voltage reaches 0.8V and full current is achieved with I_{TH} at 2V. With a 0.12µF capacitor, time to reach full charge current is about 2ms and it is assumed that input voltage to the charger will reach full value in less than 2ms. The capacitor can be increased up to 1µF if longer input start-up times are needed.

Input and Output Capacitors

The input capacitor (C2) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one half of output charging current. Actual capacitance value is not critical. Solid tantalum low ESR capacitors have high ripple current rating in a relatively small surface mount package, *but caution must be used when tantalum capacitors are used for input or output bypass*. High input surge currents can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Only Kemet T495 series of "Surge Robust" low ESR tantalums are rated for high surge conditions such as battery to ground.

The relatively high ESR of an aluminum electrolytic for C1, located at the AC adapter input terminal, is helpful in reducing ringing during the hot-plug event. Refer to Application Note 88 for more information.

Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (at least 20µF) from Tokin, United Chemi-Con/Marcon, et al. Other alternative capacitors include OS-CON capacitors from Sanyo.

The output capacitor (C3) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29(V_{BAT})\left(1-\frac{V_{BAT}}{V_{DCIN}}\right)}{(L1)(f)}$$

For example:

V_{DCIN} = 19V, V_{BAT} = 12.6V, L1 = 10µH, and f = 300kHz, I_{RMS} = 0.41A.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C3 is 0.2Ω and the battery impedance is raised to 4Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

Inductor Selection

Higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition, the effect of inductor value on ripple current and low current operation must also be considered. The inductor ripple current ΔI_L decreases with higher frequency and increases with higher V_{IN}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. In no case should ΔI_L exceed $0.6(I_{MAX})$ due to limits imposed by I_{REV} and CA1. Remember the maximum ΔI_L occurs at the maximum input voltage. In practice 10µH is the lowest value recommended for use.

Lower charger currents generally call for larger inductor values. Use Table 4 as a guide for selecting the correct inductor value for your application.

APPLICATIONS INFORMATION

Table 4

MAXIMUM AVERAGE CURRENT (A)	INPUT VOLTAGE (V)	MINIMUM INDUCTOR VALUE (μH)
1	≤20	40 ±20%
1	>20	56 ±20%
2	≤20	20 ±20%
2	>20	30 ±20%
3	≤20	15 ±20%
3	>20	20 ±20%
4	≤20	10 ±20%
4	>20	15 ±20%

Charger Switching Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with the charger: a P-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set internally. This voltage is typically 6V. Consequently, logic-level threshold MOSFETs must be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, total gate capacitance Q_G, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. The charger is operating in continuous mode at moderate to high currents so the duty cycles for the top and bottom MOSFETs are given by:

Main Switch Duty Cycle = V_{OUT}/V_{IN}

Synchronous Switch Duty Cycle = $(V_{IN} – V_{OUT})/V_{IN}$.

The MOSFET power dissipations at maximum output current are given by:

$$PMAIN = V_{OUT}/V_{IN}(I^2_{MAX})(1 + \delta\Delta T)R_{DS(ON)} + k(V^2_{IN})(I_{MAX})(C_{RSS})(f_{OSC})$$

$$PSYNC = (V_{IN} – V_{OUT})/V_{IN}(I^2_{MAX})(1 + \delta\Delta T)R_{DS(ON)}$$

Where δ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current. Both MOSFETs have I^2R losses while the PMAIN equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch is nearly 100%. The term $(1 + \delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET characteristics; if not, then C_{RSS} can be calculated using $C_{RSS} = Q_{GD}/\Delta V_{DS}$. The constant k = 2 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

If the charger is to operate in low dropout mode or with a high duty cycle greater than 85%, then the topside P-channel efficiency generally improves with a larger MOSFET. Using asymmetrical MOSFETs may achieve cost savings or efficiency gains.

The Schottky diode D1, shown in the Typical Application on the back page, conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 4A regulators due to the relatively small average current. Larger diodes can result in additional transition losses due to their larger junction capacitance.

The diode may be omitted if the efficiency loss can be tolerated.

Calculating IC Power Dissipation

The power dissipation of the LTC4006 is dependent upon the gate charge of the top and bottom MOSFETs (Q_{G1} and Q_{G2} respectively). The gate charge is determined from the manufacturer's data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the MOSFET. Use 6V for the gate voltage swing and V_{DCIN} for the drain voltage swing.

$$P_D = V_{DCIN} \bullet (f_{OSC}\ (Q_{G1} + Q_{G2}) + I_{DCIN})$$

APPLICATIONS INFORMATION

Example:

V_{DCIN} = 19V, f_{OSC} = 345kHz, Q_{G1} = Q_{G2} = 15nC.

PD = 292mW

I_{DCIN} = 5mA

Adapter Limiting

An important feature of the LTC4006 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog control is used, with closed-loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 9 senses the voltage across R_{CL}, connected between the CLP and DCIN pins. When this voltage exceeds 100mV, the amplifier will override programmed charging current to limit adapter current to 100mV/R_{CL}. A lowpass filter formed by 5kΩ and 15nF is required to eliminate switching noise. If the current limit is not used, CLP should be connected to CLN.

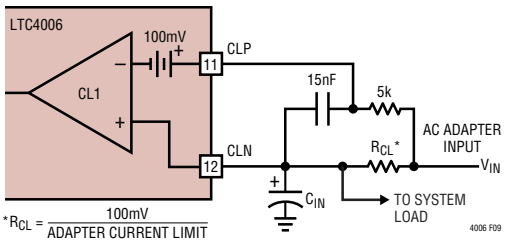

Figure 9. Adapter Current Limiting

Setting Input Current Limit

To set the input current limit, you need to know the minimum wall adapter current rating. Subtract 7% for the input current limit tolerance and use that current to determine the resistor value.

R_{CL} = 100mV/I_{LIM}

I_{LIM} = Adapter Min Current –
(Adapter Min Current • 7%)

As is often the case, the wall adapter will usually have at least a +10% current limit margin and many times one can simply set the adapter current limit value to the actual adapter rating (see Figure 9).

Designing the Thermistor Network

There are several networks that will yield the desired function of voltage vs temperature needed for proper operation of the thermistor. The simplest of these is the voltage divider shown in Figure 10. Unfortunately, since the HIGH/LOW comparator thresholds are fixed internally, there is only one thermistor type that can be used in this network; the thermistor must have a HIGH/LOW resistance ratio of 1:7. If this happy circumstance is true for

Table 5. Common R_{CL} Resistor Values

ADAPTER RATING (A)	–7% ADAPTER RATING (A)	R_{CL} VALUE* (Ω) 1%	R_{CL} LIMIT (A)	R_{CL} POWER DISSIPATION (W)	R_{CL} POWER RATING (W)
1.5	1.40	0.068	1.47	0.15	0.25
1.8	1.67	0.062	1.61	0.16	0.25
2.0	1.86	0.051	1.96	0.20	0.25
2.3	2.14	0.047	2.13	0.21	0.25
2.5	2.33	0.043	2.33	0.23	0.50
2.7	2.51	0.039	2.56	0.26	0.50
3.0	2.79	0.036	2.79	0.28	0.50
3.3	3.07	0.033	3.07	0.31	0.50
3.6	3.35	0.030	3.35	0.33	0.50
4.0	3.72	0.027	3.72	0.37	0.50

* Rounded to nearest 5% standard step value. Many non-standard values are popular.

APPLICATIONS INFORMATION

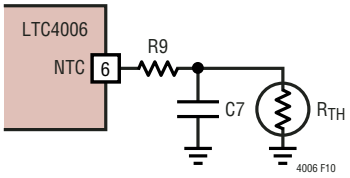

Figure 10. Voltage Divider Thermistor Network

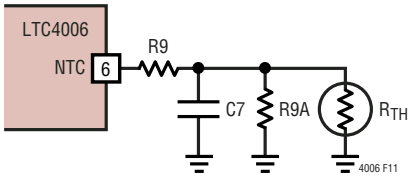

Figure 11. General Thermistor Network

you, then simply set R9 = $R_{TH(LOW)}$

If you are using a thermistor that doesn't have a 1:7 HIGH/LOW ratio, or you wish to set the HIGH/LOW limits to different temperatures, then the more generic network in Figure 11 should work.

Once the thermistor, R_{TH}, has been selected and the thermistor value is known at the temperature limits, then resistors R9 and R9A are given by:

For NTC thermistors:

$$R9 = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(LOW)} - R_{TH(HIGH)})$$

$$R9A = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(LOW)} - 7 \bullet R_{TH(HIGH)})$$

where $R_{TH(LOW)} > 7 \bullet R_{TH(HIGH)}$

For PTC thermistors:

$$R9 = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(HIGH)} - R_{TH(LOW)})$$

$$R9A = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(HIGH)} - 7 \bullet R_{TH(LOW)})$$

where $R_{TH(HIGH)} > 7R_{TH(LOW)}$

Example #1: 10kΩ NTC with custom limits

TLOW = 0°C, THIGH = 50°C
R_{TH} = 10k at 25°C,
$R_{TH(LOW)}$ = 32.582k at 0°C
$R_{TH(HIGH)}$ = 3.635k at 50°C
R9 = 24.55k → 24.3k (nearest 1% value)
R9A = 99.6k → 100k (nearest 1% value)

Example #2: 100kΩ NTC

TLOW = 5°C, THIGH = 50°C
R_{TH} = 100k at 25°C,
$R_{TH(LOW)}$ = 272.05k at 5°C
$R_{TH(HIGH)}$ = 33.195k at 50°C
R9 = 226.9k → 226k (nearest 1% value)
R9A = 1.365M → 1.37M (nearest 1% value)

Example #3: 22kΩ PTC

TLOW = 0°C, THIGH = 50°C
R_{TH} = 22k at 25°C,
$R_{TH(LOW)}$ = 6.53k at 0°C
$R_{TH(HIGH)}$ = 61.4k at 50°C
R9 = 43.9k → 44.2k (nearest 1% value)
R9A = 154k

Sizing the Thermistor Hold Capacitor

During the hold interval, C7 must hold the voltage across the thermistor relatively constant to avoid false readings. A reasonable amount of ripple on NTC during the hold interval is about 10mV to 15mV. Therefore, the value of C7 is given by:

$$C7 = t_{HOLD}/(R9/7 \bullet -\ln(1 - 8 \bullet 15mV/4.5V))$$
$$= 10 \bullet R_{RT} \bullet 17.5pF/(R9/7 \bullet -\ln(1 - 8 \bullet 15mV/4.5V))$$

Example:

R9 = 24.3k
R_{RT} = 309k (~2 hour timer)
C7 = 0.57µF → 0.56µF (nearest value)

Disabling the Thermistor Function

If the thermistor is not needed, connecting a resistor between DCIN and NTC will disable it. The resistor should be sized to provide at least 10µA with the minimum voltage applied to DCIN and 10V at NTC. Do not exceed 30µA into NTC. Generally, a 301k resistor will work for DCIN less than 15V. A 499k resistor is recommended for DCIN between 15V and 24V.

Optional Simple Battery Discharge Path Circuit

It is NOT recommended that one permit battery current to flow backwards through R_{SENSE}, inductor and out the TGATE MOSFET internal diode to reach V_{OUT}. The TGATE MOSFET is off when $V_{IN} < V_{BAT}$. Figure 12 shows an optional high efficiency discharge path for the battery such that V_{OUT} power comes from lossless "diode or" of V_{IN} and V_{BAT}. Normally when $V_{IN} > V_{BAT}$, P-channel MOSFET Q1B V_{GS} =

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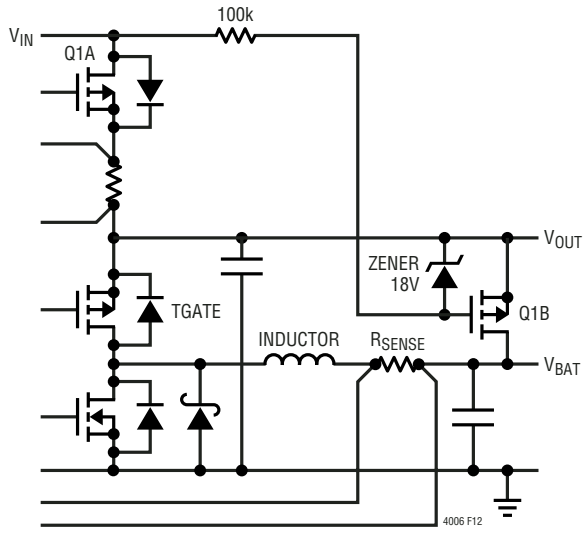

Figure 12. Optional Simple High Efficiency Battery Discharge Path

0V keeping Q1B in the off state while P-channel MOSFET Q1A is on. If V_{IN} were to suddenly go away, Q1B internal diode will provide a passive but instant discharge path for battery current to reach V_{OUT} and hold up the load. Q1B internal diode has the same current rating as the FET itself, but has a very high V_f of about a volt such that heat will quickly build up in Q1B if left alone. However as V_{IN}'s voltage falls below V_{BAT} by Q1B's V_{GS} threshold, Q1B will then turn on shorting out its internal diode removing both the heat and voltage losses created by the diode. When V_{IN} falls to zero volts, Q1B gate will be driven to the same voltage as V_{BAT} providing the lowest possible RDS_{ON} value. A zener diode along with a 100k resistor in series with the Q1B gate protects the gate from any hazardous voltage spikes that can exceed Q1B maximum permissible V_{GS} voltage. The zener voltage rating must be less than Q1B $V_{GS(MAX)}$ voltage but greater than V_{BAT}.

Since Q1A and Q1B are always at opposite states and share the same load, it is often advantagous to combine both FETs into a single package and save PCB space. The P_D rate of the FET that is on is enhanced when the other FET is off. The choice of a combined Q1 should take into account the highest load current conditions of both paths and choose whichever is greater as the driving force behind the MOSFET selection. If the V_{IN} supply is going to collapse very slowly such that Q1B is not turned on quickly enough for the given load and stay within its P_D limits, you should install a suitable Schottky diode in parallel with Q1B.

PCB Layout Considerations

For maximum efficiency, the switch node rise and fall times should be minimized. To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential. (See Figure 13.) Here is a PCB layout priority list for proper layout. Layout the PCB using this specific order.

1. Input capacitors need to be placed as close as possible to switching FET's supply and ground connections. Shortest copper trace connections possible. These parts must be on the same layer of copper. Vias must not be used to make this connection.
2. The control IC needs to be close to the switching FET's gate terminals. Keep the gate drive signals short for a clean FET drive. This includes IC supply pins that connect to the switching FET source pins. The IC can be placed on the opposite side of the PCB relative to above.
3. Place inductor input as close as possible to switching FET's output connection. Minimize the surface area of this trace. Make the trace width the minimum amount needed to support current—no copper fills or pours. Avoid running the connection using multiple layers in parallel. Minimize capacitance from this node to any other trace or plane.

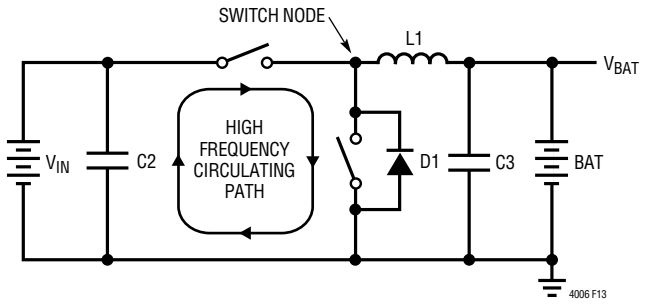

Figure 13. High Speed Switching Path

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4. Place the output current sense resistor right next to the inductor output but oriented such that the IC's current sense feedback traces going to resistor are not long. The feedback traces need to be routed together as a single pair on the same layer at any given time with smallest trace spacing possible. Locate any filter component on these traces next to the IC and not at the sense resistor location.
5. Place output capacitors next to the sense resistor output and ground.
6. Output capacitor ground connections need to feed into same copper that connects to the input capacitor ground before tying back into system ground.

General Rules

7. Connection of switching ground to system ground or internal ground plane should be single point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection.
8. Route analog ground as a trace tied back to IC ground (analog ground pin if present) before connecting to any other ground. Avoid using the system ground plane. CAD trick: make analog ground a separate ground net and use a 0Ω resistor to tie analog ground to system ground.
9. A good rule of thumb for via count for a given high current path is to use 0.5A per via. Be consistent.
10. If possible, place all the parts listed above on the same PCB layer.
11. Copper fills or pours are good for all power connections except as noted above in Rule 3. You can also use copper planes on multiple layers in parallel too—this helps with thermal management and lower trace inductance improving EMI performance further.
12. For best current programming accuracy provide a Kelvin connection from R_{SENSE} to CSP and BAT. See Figure 13 as an example.

It is important to keep the parasitic capacitance on the R_T, CSP and BAT pins to a minimum. The traces connecting these pins to their respective resistors should be as short as possible.

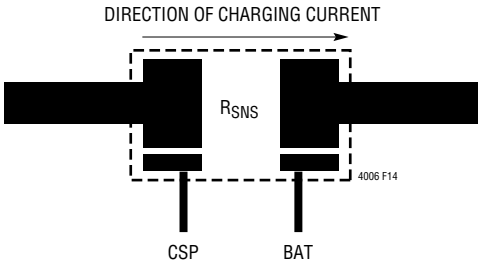
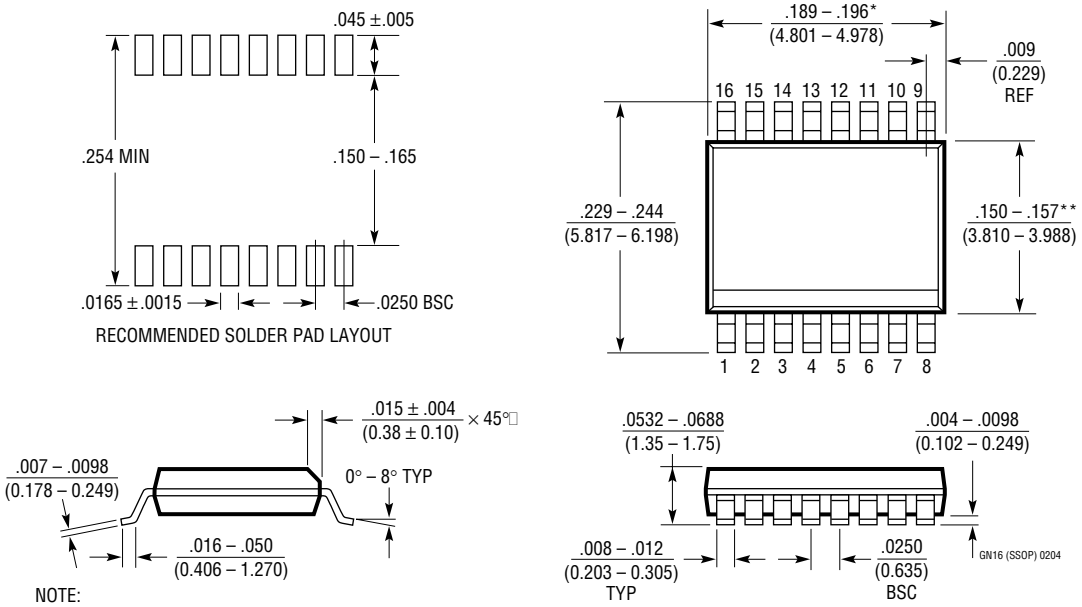


Figure 14. Kelvin Sensing of Charging Current

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE