LTC4009
LTC4009-1/LTC4009-2

High Efficiency, Multi-Chemistry Battery Charger

FEATURES

- **General Purpose Battery Charger Controller**
- **Efficient 550kHz Synchronous Buck PWM Topology**
- **±0.5% Output Float Voltage Accuracy**
- **Programmable Charge Current: 4% Accuracy**
- **Programmable AC Adapter Current Limit: 3% Accuracy**
- **No Audible Noise with Ceramic Capacitors**
- Wide Input Voltage Range: 6V to 28V
- Wide Output Voltage Range: 2V to 28V
- Indicator Outputs for AC Adapter Present, Charging, C/10 Current Detection and Input Current Limiting
- Analog Charge Current Monitor
- Micropower Shutdown
- Thermally Enhanced 20-Pin 4mm × 4mm × 0.75mm QFN Package

APPLICATIONS

- Notebook Computers
- Portable Instruments
- Battery Backup Systems

DESCRIPTION

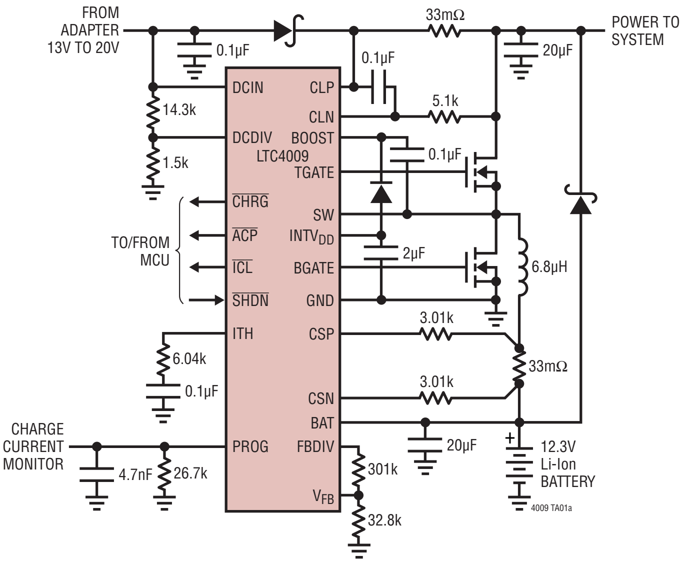
The LTC®4009 is a constant-current/constant-voltage battery charger controller. It uses a synchronous quasi-constant frequency PWM control architecture that will not generate audible noise with ceramic bulk capacitors. Charge current is set by the combination of external sense, input and programming resistors. With no built-in termination, the LTC4009 family charges a wide range of batteries under external control.

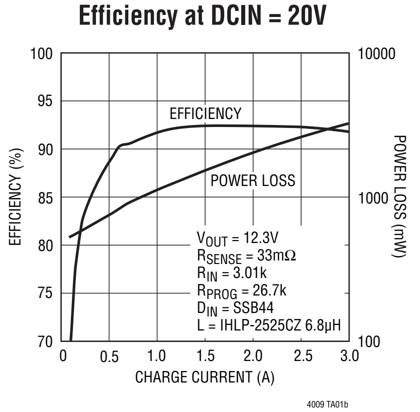
The LTC4009 features a fully adjustable output voltage, while the LTC4009-1 and LTC4009-2 can be pin-programmed for lithium-ion/polymer battery packs of 1-, 2-, 3- or 4-series cells. The LTC4009-1 provides output voltage of 4.1V/cell, and the LTC4009-2 is a 4.2V/cell version.

The device includes AC adapter input current limiting which maximizes the charge rate for a fixed input power level. An external sense resistor programs the input current limit, and the $\overline{\text{ICL}}$ status pin indicates when the battery charge current is being reduced as a result of AC adapter current limiting.

The $\overline{\text{CHRG}}$ status pin is active during all charging modes, including special indication for low charge current.

TYPICAL APPLICATION



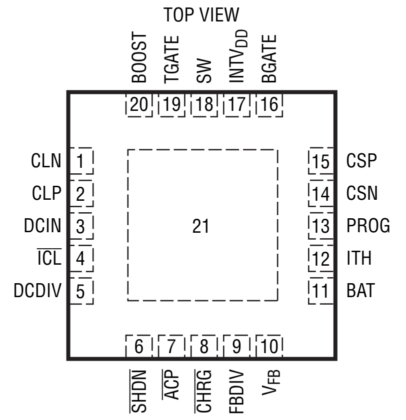


ABSOLUTE MAXIMUM RATINGS (Note 1)

DCIN, CLP, CLN or SW to GND	–0.3V to 30V
CLP to CLN	±0.3V
CSP, CSN or BAT to GND	–0.3V to 28V
CSP to CSN	±0.3V
BOOST to GND	–0.3V to 36V
BOOST to SW	–0.3V to 7V
DCDIV, $\overline{SHDN}$, FVS0, FVS1 or V_{FB} to GND	–0.3V to 7V
$\overline{ACP}$, $\overline{CHRG}$ or $\overline{ICL}$ to GND	–0.3V to 30V
Operating Temperature Range (Note 2)	–40°C to 125°C
Junction Temperature (Note 3)	125°C
Storage Temperature Range	–65°C to 150°C

PIN CONFIGURATION

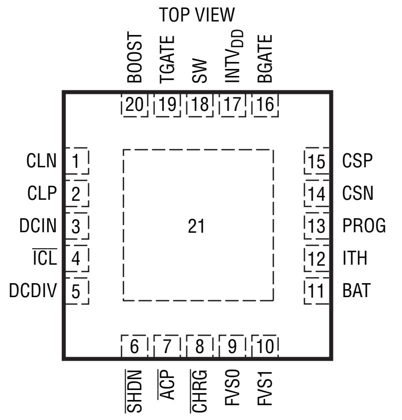
LTC4009



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

LTC4009-1
LTC4009-2



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4009CUF#PBF	LTC4009CUF#TRPBF	4009	20-Lead (4mm × 4mm) Plastic QFN	0°C to 85°C
LTC4009CUF-1#PBF	LTC4009CUF-1#TRPBF	40091	20-Lead (4mm × 4mm) Plastic QFN	0°C to 85°C
LTC4009CUF-2#PBF	LTC4009CUF-2#TRPBF	40092	20-Lead (4mm × 4mm) Plastic QFN	0°C to 85°C
LTC4009IUF#PBF	LTC4009IUF#TRPBF	4009	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC4009IUF-1#PBF	LTC4009IUF-1#TRPBF	40091	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC4009IUF-2#PBF	LTC4009IUF-2#TRPBF	40092	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DCIN = 20V, BAT = 12V, GND = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Voltage Regulation							
V_{TOL}	V_{BAT} Accuracy (See Test Circuits)	LTC4009		–0.5		0.5	%
		C-Grade	●	–0.8		0.8	%
		I-Grade	●	–1.0		1.0	%
		LTC4009-1/LTC4009-2		–0.6		0.6	%
		C-Grade	●	–0.8		0.8	%
		FVS1 = 0V, FVS0 = 0V, I-Grade	●	–1.1		1.1	%
		FVS1 = 0V, FVS1 = 5V, I-Grade	●	–1.15		1.15	%
		FVS1 = 5V, FVS0 = 0V, I-Grade	●	–1.25		1.25	%
		FVS1 = 5V, FVS1 = 5V, I-Grade	●	–1.35		1.35	%
I_{VFB}	V_{FB} Input Bias Current	V_{FB} = 1.2V			±20		nA
R_{ON}	FBDIV On-Resistance	I_{LOAD} = 100μA	●		85	190	Ω
$I_{LEAK-FBDIV}$	FBDIV Output Leakage Current	$\overline{SHDN}$ = 0V, FBDIV = 0V	●	–1	0	1	μA
V_{BOV}	V_{FB} Overvoltage Threshold	LTC4009	●	1.235	1.281	1.32	V
	BAT Overvoltage Threshold	LTC4009-1/LTC4009-2, Relative to Selected Output Voltage	●	103	106	109	%
Charge Current Regulation							
I_{TOL}	Charge Current Accuracy with R_{IN} = 3.01k, 6V < BAT < 18V (LTC4009), 6V < BAT < 15V (LTC4009-1, LTC4009-2)	R_{PROG} = 26.7k		–4		4	%
		C-Grade	●	–5		5	%
		I-Grade	●	–9.5		9.5	%
		V_{SENSE} = 0mV, PROG = 1.2V		–12.75	–11.67	–10.95	μA
A_I	Current Sense Amplifier Gain (PROG ΔI) with R_{IN} = 3.01k, 6V < BAT < 18V (LTC4009), 6V < BAT < 15V (LTC4009-1, LTC4009-2)	V_{SENSE} Step from 0mV to 5mV, PROG = 1.2V		–1.78	–1.66	–1.54	μA
V_{CS-MAX}	Maximum Peak Current Sense Threshold Voltage per Cycle (R_{IN} = 3.01k)	ITH = 2V, C-Grade	●	140	195	250	mV
		ITH = 2V, I-Grade	●	125		265	mV
		ITH = 5V	●		325	430	mV
V_{C10}	C/10 Indicator Threshold Voltage	PROG Falling		340	400	460	mV
V_{REV}	Reverse Current Threshold Voltage	PROG Falling		180	253	295	mV
Input Current Regulation							
V_{CL}	Current Limit Threshold	CLP – CLN		97	100	103	mV
		C-Grade	●	96	100	104	mV
		I-Grade	●	92		108	mV
I_{CLN}	CLN Input Bias Current	CLN = CLP			±100		nA
V_{ICL}	$\overline{ICL}$ Indicator Threshold	(CLP – CLN) – V_{CL}		–8	–5	–2	mV
DCIN, CLP Supplies							
OVR	Operating Voltage Range	DCIN and CLP		6		28	V
I_{DCO}	DCIN Operating Current	No Gate Loads			1.5	2	mA
I_{CLPO}	CLP Operating Current	CLP = 20V, No Gate Loads			0.5	0.8	mA
V_{CBT}	CLP Boost Threshold Voltage	CLP – DCIN, CLP Rising	●	10	25	60	mV
V_{CNT}	CLP Normal Threshold Voltage (Note 5)	DCIN – CLP, CLP Falling	●	10	25	60	mV
V_{OVP}	DCDIV Overvoltage Protection Threshold	DCDIV Rising		1.75	1.825	1.9	V
$V_{OVP(HYST)}$	DCDIV OVP Threshold Hysteresis				110		mV
Shutdown							
V_{ACP}	DCDIV AC Present Threshold Voltage	DCDIV Rising	●	1.13	1.2	1.27	V
$V_{ACP(HYST)}$	DCDIV ACP Threshold Hysteresis Voltage				50		mV
I_{DCDIV}	DCDIV Input Current	DCDIV = 1.2V		–1	0	1	μA
V_{IL}	$\overline{SHDN}$ Input Voltage Low		●			300	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. DCIN = 20V, BAT = 12V, GND = 0V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	$\overline{\text{SHDN}}$ Input Voltage High		●	1.4			V
R_{IN}	$\overline{\text{SHDN}}$ Pull-Down Resistance				50		kΩ
I_{DCS}	DCIN Shutdown Current	$\overline{\text{SHDN}}$ = 0V			215		µA
I_{CLPS}	CLP Shutdown Current	CLP = 12V, $\overline{\text{SHDN}}$ = 0V or DCDIV = 0V	●		9	18	µA
$I_{LEAK\text{-}BAT}$	BAT Leakage Current	$\overline{\text{SHDN}}$ = 0V or DCDIV = 0V, 0V ≤ CSP = CSN = BAT ≤ 20V	●	–1.5	0	1.5	µA
$I_{LEAK\text{-}CSN}$	CSN Leakage Current	$\overline{\text{SHDN}}$ = 0V or DCDIV = 0V, 0V ≤ CSP = CSN = BAT ≤ 20V	●	–1.5	0	1.5	µA
$I_{LEAK\text{-}CSP}$	CSP Leakage Current	$\overline{\text{SHDN}}$ = 0V or DCDIV = 0V, 0V ≤ CSP = CSN = BAT ≤ 20V	●	–1.5	0	1.5	µA
$I_{LEAK\text{-}SW}$	SW Leakage Current	$\overline{\text{SHDN}}$ = 0V or DCDIV = 0V, 0V ≤ SW ≤ 20V	●	–1	0	2	µA
$INTV_{DD}$ Regulator							
$INTV_{DD}$	Output Voltage	No Load	●	4.85	5	5.15	V
ΔV_{DD}	Load Regulation	I_{DD} = 20mA			–0.4	–1	%
I_{DD}	Short-Circuit Current (Note 6)	$INTV_{DD}$ = 0V		50	85	130	mA
Switching Regulator							
V_{CE}	Charge Enable Threshold Voltage	CLP – BAT, CLP Rising C-Grade I-Grade	 ● ●	 65 60	 100	 135 140	 mV mV
I_{ITH}	ITH Current	ITH = 1.4V			–40/+90		µA
f_{TYP}	Typical Switching Frequency			467	550	633	kHz
f_{MIN}	Minimum Switching Frequency	C_{LOAD} = 3.3nF		20	25		kHz
DC_{MAX}	Maximum Duty Cycle	C_{LOAD} = 3.3nF		98	99		%
$t_{R\text{-}TG}$	TGATE Rise Time	C_{LOAD} = 3.3nF, 10% – 90%			60	110	ns
$t_{F\text{-}TG}$	TGATE Fall Time	C_{LOAD} = 3.3nF, 90% – 10%			50	110	ns
$t_{R\text{-}BG}$	BGATE Rise Time	C_{LOAD} = 3.3nF, 10% – 90%			60	110	ns
$t_{F\text{-}BG}$	BGATE Fall Time	C_{LOAD} = 3.3nF, 90% – 10%			60	110	ns
t_{NO}	TGATE, BGATE Non-Overlap Time	C_{LOAD} = 3.3nF, 10% – 10%			110		ns
Float Voltage Select Inputs (LTC4009-1/LTC4009-2 Only)							
V_{IL}	Input Voltage Low					0.5	V
V_{IH}	Input Voltage High			3.5			V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ 5V		–10		10	µA
Indicator Outputs							
V_{OL}	Output Voltage Low	I_{LOAD} = 100µA, PROG = 1.2V				500	mV
I_{LEAK}	Output Leakage	$\overline{\text{SHDN}}$ = 0V, DCDIV = 0V, V_{OUT} = 20V	●	–10		10	µA
I_{C10}	$\overline{\text{CHRG}}$ C/10 Current Sink	$\overline{\text{CHRG}}$ = 2.5V	●	15	25	38	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4009C is guaranteed to meet performance specifications over the 0°C to 85°C operating temperature range. The LTC4009I is guaranteed to meet performance specifications over the –40°C to 125°C operating temperature range.

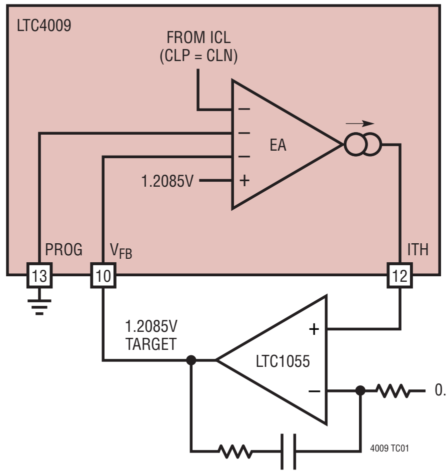
Note 3: Operating junction temperature T_J (in °C) is calculated from the ambient temperature T_A and the total continuous package power dissipation P_D (in watts) by the formula $T_J = T_A + (\theta_{JA} \bullet PD)$. Refer to the Applications Information section for details.

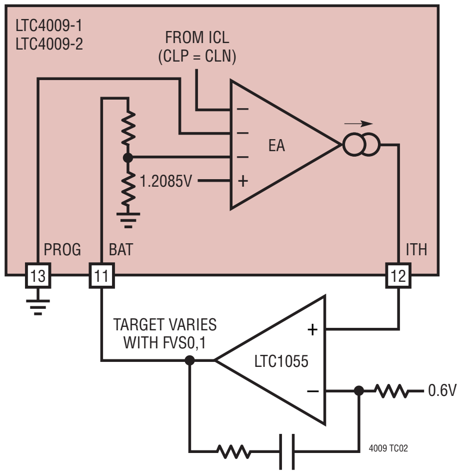
Note 4: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND, unless otherwise specified.

Note 5: This threshold is guaranteed to be satisfied if CLP = DCIN when the LTC4009 exits shutdown.

Note 6: Output current may be limited by internal power dissipation. Refer to the Applications Information section for details.

TEST CIRCUITS

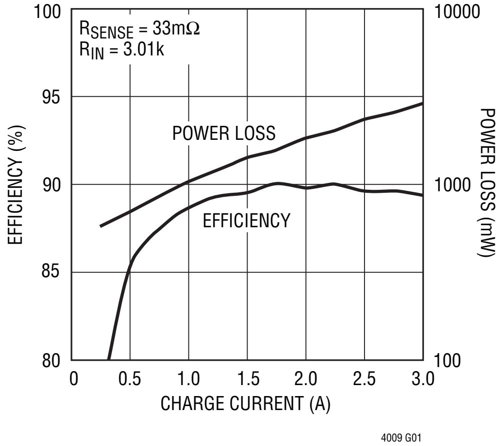




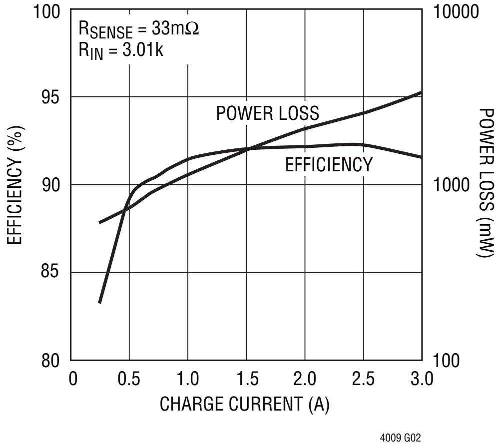
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. D_{IN} = SSB44, L = IHLP-2525 6.8µH)

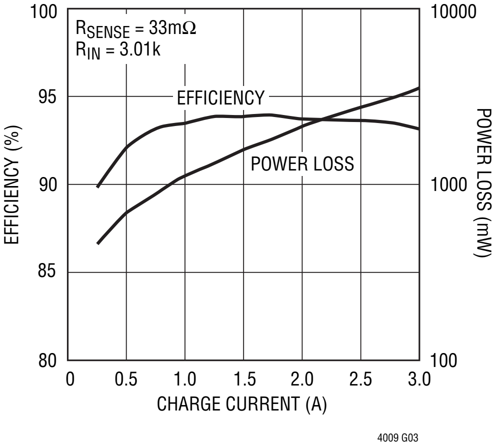
Efficiency at DCIN = 20V, BAT = 8V



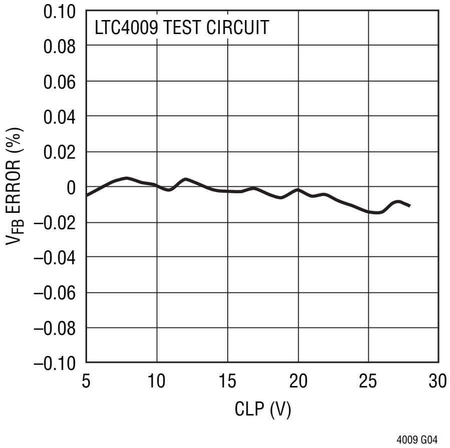
Efficiency at DCIN = 20V, BAT = 12V



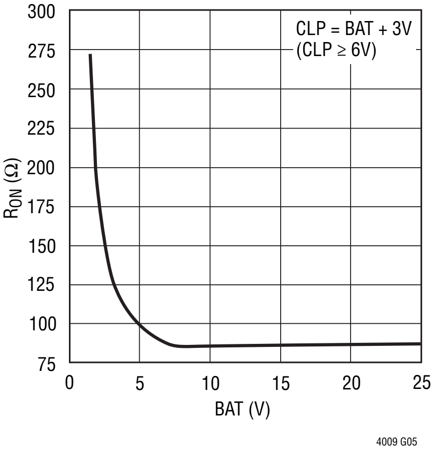
Efficiency at DCIN = 20V, BAT = 16V



V_{FB} Line Regulation



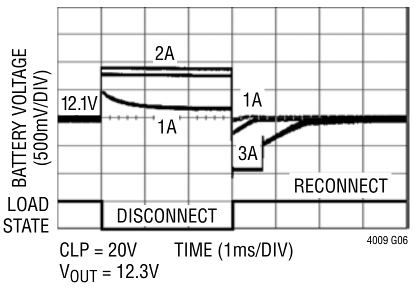
FBDIV R_{ON} vs BAT



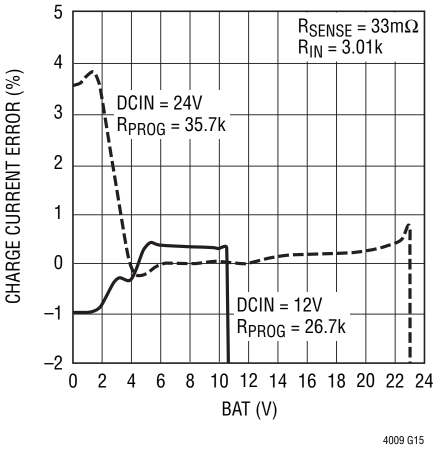
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. D_{IN} = SSB44, L = IHLP-2525 6.8µH)

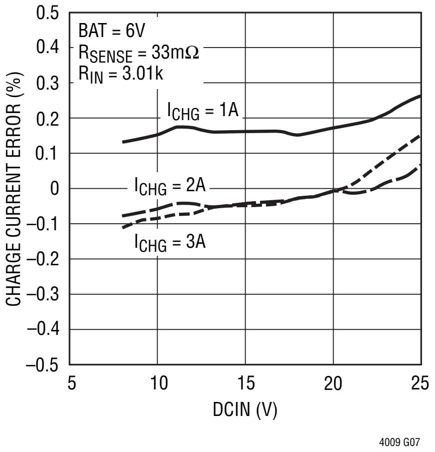
Battery Load Dump



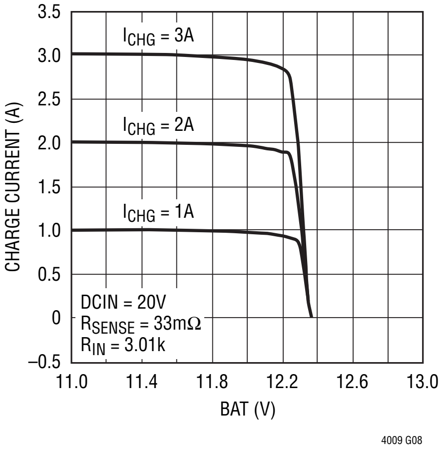
Charge Current Accuracy



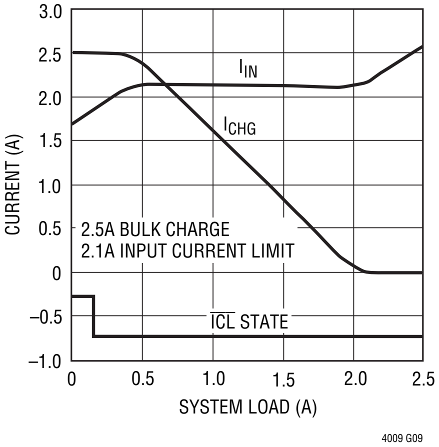
Charge Current Line Regulation



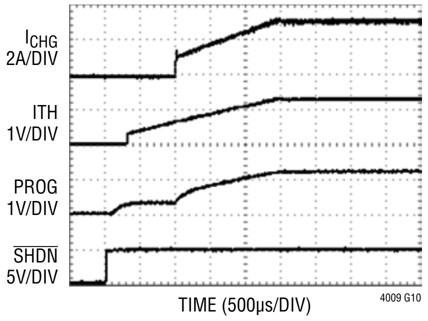
Charge Current Load Regulation



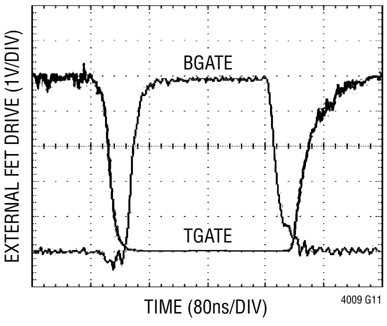
Input Current Limit



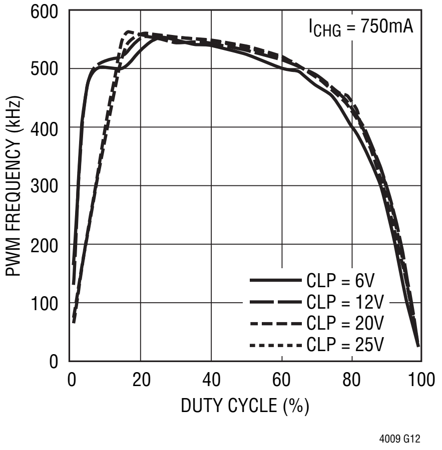
PWM Soft-Start



Gate Drive Non-Overlap

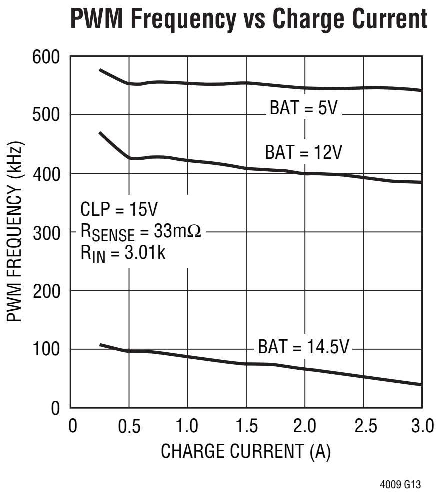


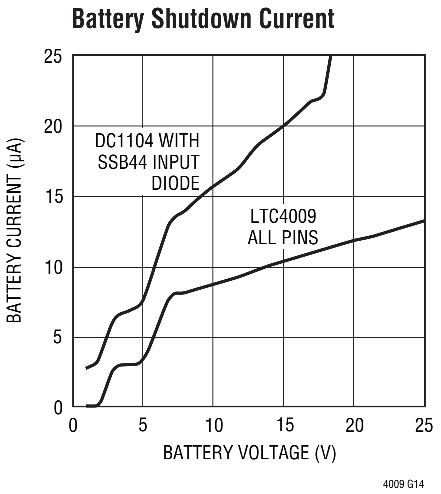
PWM Frequency vs Duty Cycle



TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise noted. D_{IN} = SSB44, L = IHLP-2525 6.8µH)


PWM Frequency vs Charge Current


Battery Shutdown Current

PIN FUNCTIONS

CLN (Pin 1): Adapter Input Current Limit Negative Input. The LTC4009 senses voltage on this pin to determine if the charge current should be reduced to limit total input current. The threshold is set 100mV below the CLP pin. An external filter should be used to remove switching noise. This input should be tied to CLP if not used. Operating voltage range is (CLP – 110mV) to CLP.

CLP (Pin 2): Adapter Input Current Limit Positive Input. The LTC4009 also draws power from this pin, including a small amount for some shutdown functions. Operating voltage range is GND to 28V.

DCIN (Pin 3): DC Power Input. The LTC4009 draws power from this pin when an external DC power source is present. This pin is typically isolated from the CLP pin by a diode and should be bypassed with a capacitance of 0.1µF or more. Operating voltage range is GND to 28V.

$\overline{\text{ICL}}$ (Pin 4): Active-Low Input Current Limit Indicator Output. This open-drain output pulls to GND when the charge current is reduced because of AC adapter input current limiting. This output should be left floating if not used.

DCDIV (Pin 5): AC Adapter Present Comparator Input. The LTC4009 senses voltage on this pin to determine when an adequate DC power source is present, or if an overvoltage condition exists. An external resistor divider programs these threshold levels relative to DCIN. Operating voltage range is GND to $INTV_{DD}$.

$\overline{\text{SHDN}}$ (Pin 6): Active-low Shutdown Input. Driving $\overline{\text{SHDN}}$ below 300mV unconditionally forces the LTC4009 into the shutdown state. This input has a 50kΩ internal pull-down to GND. Operating voltage range is GND to $INTV_{DD}$.

$\overline{\text{ACP}}$ (Pin 7): Active-Low AC Adapter Present Indicator Output. This open-drain output pulls to GND when adequate AC adapter (DC) voltage is present, based on the DCDIV input. This output should be left floating if not used.

$\overline{\text{CHRG}}$ (Pin 8): Active-Low Charge Indicator Output. This open-drain output provides three levels of information about charge status using a strong pull-down, 25µA weak pull-down or high impedance. Refer to the Operation and Applications Information sections for further details. This output should be left floating if not used.

FBDIV (Pin 9, LTC4009): Battery Voltage Feedback Resistor Divider Source. The LTC4009 connects this pin to BAT when charging is in progress. FBDIV is an open-drain PFET output to BAT with an operating voltage range of GND to BAT.

PIN FUNCTIONS

FVS0 (Pin 9, LTC4009-1/LTC4009-2): Battery Voltage Select Input (LSB). This pin is one of two pins used on the LTC4009-1 or LTC4009-2 to select one of four preset battery voltages. Selection is done by connecting to either GND or $INTV_{DD}$. Operating voltage range is GND to $INTV_{DD}$.

V_{FB} (Pin 10, LTC4009): Battery Voltage Feedback Input. An external resistor divider between FBDIV and GND with the center tap connected to V_{FB} programs the charger output voltage. In constant voltage mode, this pin is nominally at 1.2085V. Refer to the Applications Information section for complete details on programming battery float voltage. Operating voltage range is GND to 1.25V.

FVS1 (Pin 10, LTC4009-1/LTC4009-2): Battery Voltage Select Input (MSB). This pin is one of two pins used on the LTC4009-1 or LTC4009-2 to select one of four preset battery voltages. Selection is done by connecting to either GND or $INTV_{DD}$. Operating voltage range is GND to $INTV_{DD}$.

BAT (Pin 11): Battery Pack Connection. The LTC4009 uses the voltage on this pin to control PWM operation when charging. Operating voltage range is GND to CLN.

ITH (Pin 12): PWM Control Voltage and Compensation Node. The LTC4009 develops a voltage on this pin to control cycle-by-cycle peak inductor current. An external R-C network connected to ITH provides PWM loop compensation. Refer to the Applications Information section for further details on establishing loop stability. Operating voltage range is GND to $INTV_{DD}$.

PROG (Pin 13): Charge Current Programming and Monitoring Pin. An external resistance connected between PROG and GND, along with the current sense and PWM input resistors, programs the maximum charge current. The voltage on this pin can also provide a linearized indicator of charge current. Refer to the Applications Information section for complete details on current programming and monitoring. Operating voltage range is GND to $INTV_{DD}$.

CSN (Pin 14): Charge Current Sense Negative Input. Place an external input resistor (R_{IN}, Figure 1) between this pin and the negative side of the charge current sense resistor. Operating voltage ranges from (BAT – 50mV) to (BAT + 200mV).

CSP (Pin 15): Charge Current Sense Positive Input. Place an external input resistor (R_{IN}, Figure 1) between this pin and the positive side of the charge current sense resistor. Operating voltage ranges from (BAT – 50mV) to (BAT + 200mV).

BGATE (Pin 16): External Synchronous NFET Gate Control Output. This output provides gate drive to an external NMOS power transistor switch used for synchronous rectification to increase efficiency in the step-down DC/DC converter. Operating voltage is GND to $INTV_{DD}$. BGATE should be left floating if not used.

$INTV_{DD}$ (Pin 17): Internal 5V Regulator Output. This pin provides a means of bypassing the internal 5V regulator used to power the LTC4009 PWM FET drivers. This supply shuts down when the LTC4009 shuts down. Refer to the Application Information section for details if additional power is drawn from this pin by the application circuit.

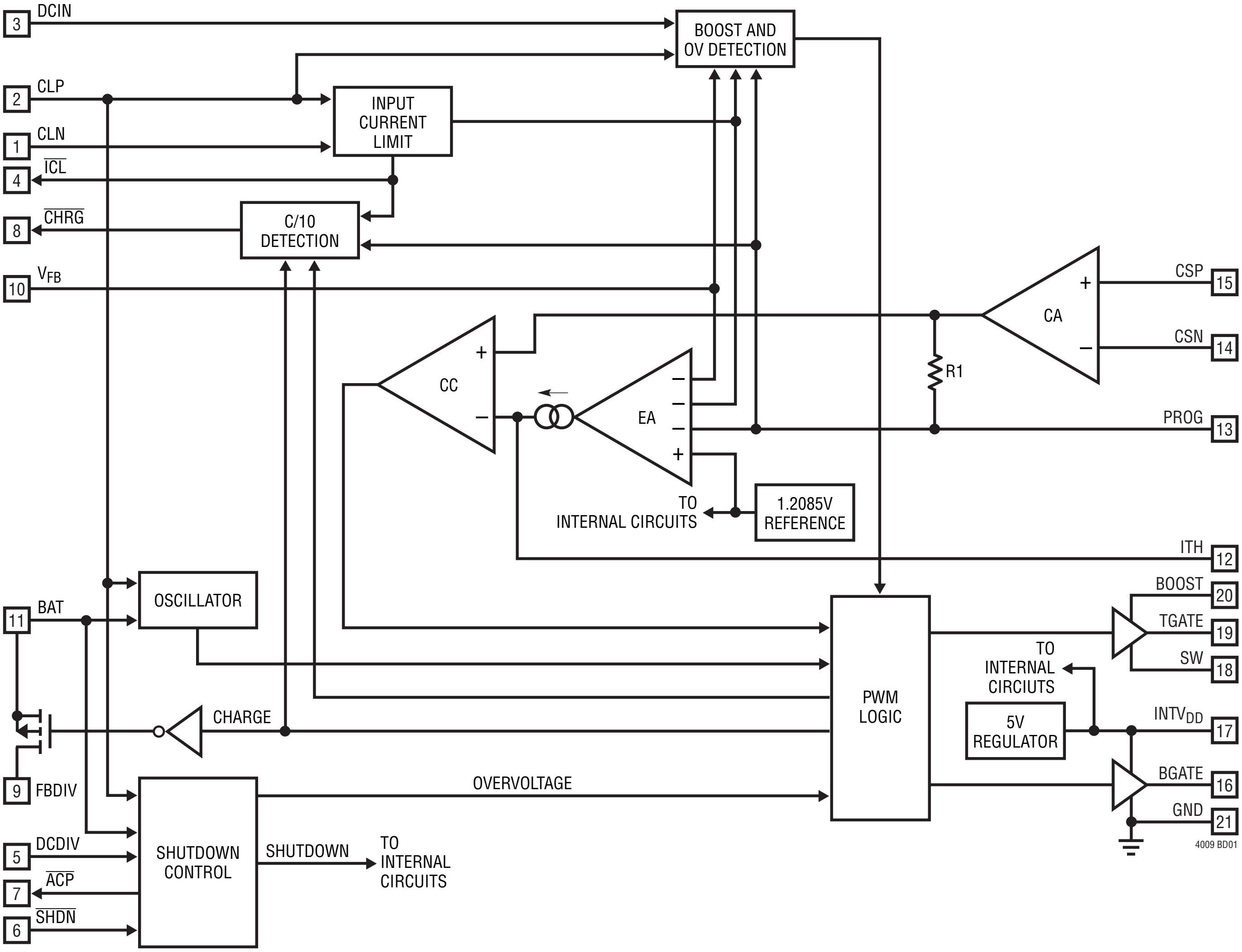
SW (Pin 18): PWM Switch Node. The LTC4009 uses the voltage on this pin as the source reference for its topside NFET (PWM switch) driver. Refer to the Applications Information section for additional PCB layout suggestions related to this critical circuit node. Operating voltage range is GND to CLN.

TGATE (Pin 19): External NFET Switch Gate Control Output. This output provides gate drive to an external NMOS power transistor switch used in the DC/DC converter. Operating voltage range is GND to (CLN + 5V).

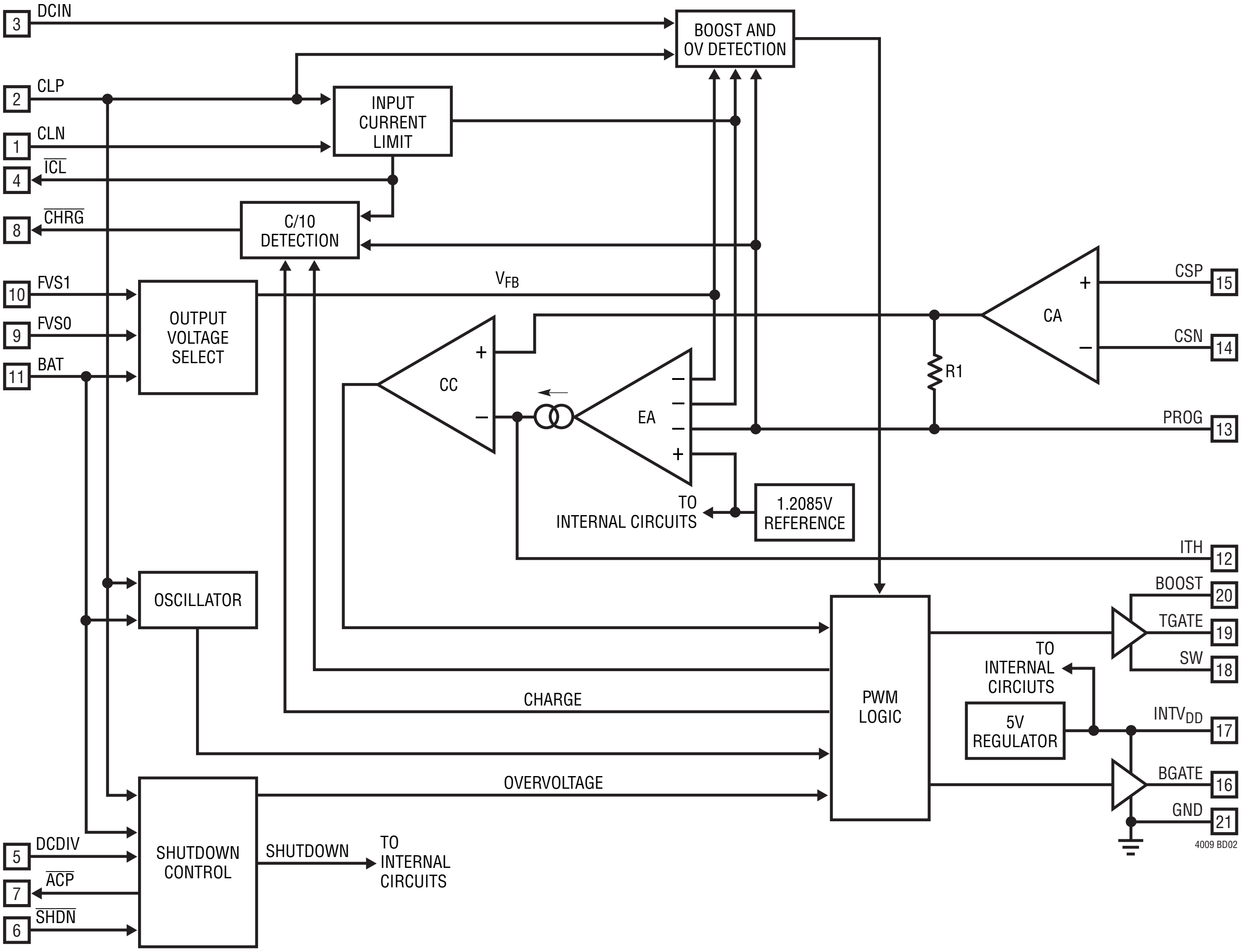
BOOST (Pin 20): TGATE Driver Supply Input. A bootstrap capacitor is returned to this pin from a charge network connected to SW and $INTV_{DD}$. Refer to the Applications Information section for complete details on circuit topology and component values. Operating voltage ranges from ($INTV_{DD}$ – 1V) to (CLN + 5V).

GND (Exposed Pad Pin 21): Ground. The package paddle provides a single-point ground for the internal voltage reference and other critical LTC4009 circuits. It must be soldered to a suitable PCB copper ground pad for proper electrical operation and to obtain the specified package thermal resistance.

BLOCK DIAGRAM (LTC4009)



BLOCK DIAGRAM (LTC4009-1/LTC4009-2)



OPERATION

Overview

The LTC4009 is a synchronous step-down (buck) current mode PWM battery charger controller. The maximum charge current is programmed by the combination of a charge current sense resistor (R_{SENSE}), matched input resistors (R_{IN}, Figure 1), and a programming resistor (R_{PROG}) between the PROG and GND pins. Battery voltage is programmed either with an external resistor divider between FBDIV and GND (LTC4009) or two digital battery voltage select pins (LTC4009-1/LTC4009-2). In addition, the PROG pin provides a linearized voltage output of the actual charge current.

The LTC4009 family does not have any built-in charge termination and is flexible enough for charging any type of battery chemistry. These are building block ICs intended for use with an external circuit, such as a microcontroller, capable of managing the entire algorithm required for the specific battery being charged. Each member of the LTC4009 family features a shutdown input and various state indicator outputs, allowing easy and direct management by a wide range of external (digital) charge controllers. Due to the popularity of rechargeable lithium-ion chemistries, the LTC4009-1 and LTC4009-2 also offer internal precision resistors that can be digitally selected to produce one of four preset output voltages for simplified design of those charger types.

Shutdown

The LTC4009 remains in shutdown until DCDIV exceeds 1.2V, and $\overline{\text{SHDN}}$ is driven above 1.4V. In shutdown, current drain from the battery is reduced to the lowest possible level, thereby increasing standby time. When in shutdown, the ITH pin is pulled to GND and the $\overline{\text{CHRG}}$, $\overline{\text{ICL}}$, FET gate drivers and $INTV_{DD}$ output are all disabled. The $\overline{\text{ACP}}$ status output indicates sensed adapter input voltage during all LTC4009 states. Charging can be stopped at any time by forcing $\overline{\text{SHDN}}$ below 300mV.

Soft-Start

Exiting the shutdown state enables the charger and releases the ITH pin. When enabled, switching will not begin until CLP exceeds BAT by 100mV and ITH exceeds a threshold that assures initial current will be positive (about 5% to 25% of the maximum programmed current). To limit inrush current, soft-start delay is created with the compensation values used on the ITH pin. Longer soft-start times can be realized by increasing the filter capacitor on ITH, if reduced loop bandwidth is acceptable. The actual charge current at the end of soft-start will depend on which loop (current, voltage or adapter limit) is in control of the PWM. If this current is below that required by the ITH start-up threshold, the resulting charge current transient duration depends on loop compensation but is typically less than 100µs.

Bulk Charge

When soft-start is complete, the LTC4009 begins sourcing the current programmed by the external components connected to CSP, CSN and PROG. Some batteries may require a small conditioning trickle current if they are heavily discharged. As shown in the Applications Information section, the LTC4009 can address this need through a variety of low current circuit techniques on the PROG pin. Once a suitable cell voltage has been reached, charge current can be switched to a higher, bulk charge value.

End-of-Charge and $\overline{\text{CHRG}}$ Output

As the battery approaches the programmed output voltage, charge current will begin to decrease. The open-drain $\overline{\text{CHRG}}$ output can indicate when the current drops to 10% of its programmed full-scale value by turning off the strong pull-down (open-drain FET) and turning on a weak 25µA pull-down current. This weak pull-down state is latched until the part enters shutdown or the sensed current rises to roughly C/6. C/10 indication will not be set if charge current has been reduced due to adapter input current limiting or DCIN/battery overvoltage. As the charge current approaches 0A, the PWM continues to operate in full continuous mode. This avoids generation of audible noise, allowing bulk ceramic capacitors to be used in the application.

OPERATION

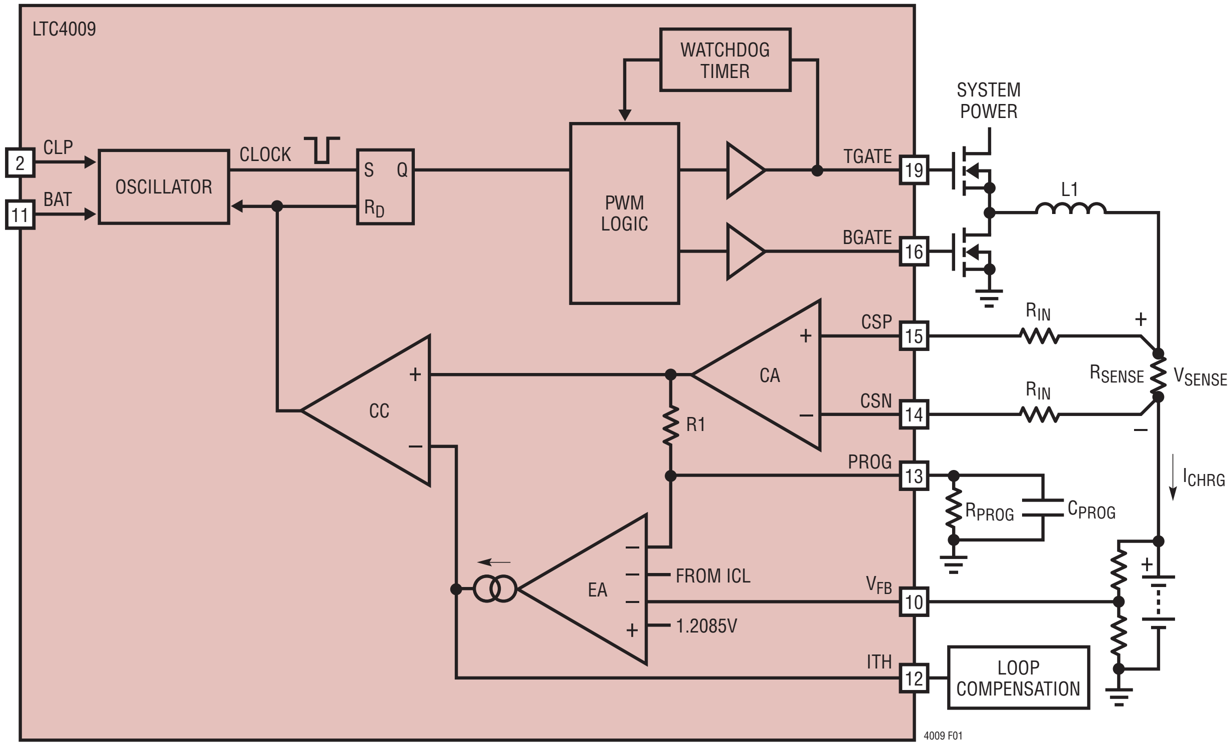


Figure 1. PWM Circuit Diagram

Charge Current Monitoring

When the LTC4009 is charging, the voltage on the PROG pin varies in direct proportion to the charge current. Referring to Figure 1, the nominal PROG voltage is given by

$$V_{PROG} = \frac{I_{CHRG} \cdot R_{SENSE} \cdot R_{PROG}}{R_{IN}} + 11.67\mu A \cdot R_{PROG}$$

Voltage tolerance on PROG is limited by the charge current accuracy specified in the Electrical Characteristics table. Refer to the Applications Information section on programming charge current for additional details.

Adapter Input Current Limit

The LTC4009 can monitor and limit current from the input DC supply, which is normally an AC adapter. When the programmed adapter input current is reached, charge current is reduced to maintain the desired maximum input current. The ITH and PROG pins will reflect the reduced charge current. This limit function avoids overloading the DC input source, allowing the product to operate at the same time the battery is charging without complex load management algorithms. The battery will automatically be charged at the maximum possible rate that the adapter will support, given the application's operating condition. The LTC4009 can only limit input current by reducing charge current, and in this case the charger uses nonsynchronous PWM operation to prevent boosting if the average charge current falls below about 25% of the maximum programmed current. Note that the $\overline{ICL}$ indicator output becomes active (low) at an adapter input current level just slightly less than that required for the internal amplifier to begin to assert control over the PWM loop.

If system load current equals or exceeds the input adapter current limit for more than a few milliseconds, the bootstrap capacitor between BOOST and SW can fully discharge due to normal pin leakage currents. In this case, the PWM will not restart until the system current has dropped to about 85% of the programmed input adapter limit value.

Charger Status Indicator Outputs

The LTC4009 open-drain indicator outputs provide valuable information about the IC's operating state and can

OPERATION

be used for a variety of purposes in applications. Table 1 summarizes the state of the three indicator outputs as a function of LTC4009 operation.

Table 1. LTC4009 Open-Drain Indicator Outputs

$\overline{\text{ACP}}$	$\overline{\text{CHRG}}$	$\overline{\text{ICL}}$	CHARGER STATE
Off	Off	Off	No DC Input (Shutdown)
On	Off	Off	Shutdown, Reverse Current or DCIN Overvoltage
On	On	Off	Bulk Charge
On	25µA	Off	Low Current Charge or Initial CLP-BAT < 100mV
On	On	On	Input Current Limit During Bulk Charge
On	25µA	On	Input Current Limit During Low Current Charge
On	Off	On	Input Current Limit During DCIN Overvoltage

PWM Controller

The LTC4009 uses a synchronous step-down architecture to produce high operating efficiency. The nominal operating frequency of 550kHz allows use of small filter components. The following conceptual discussion of basic PWM operation references Figure 1.

The voltage across the external charge current sense resistor R_{SENSE} is measured by current amplifier, CA. This instantaneous current (V_{SENSE}/R_{IN}) is fed to the PROG pin where it is averaged by an external capacitor and converted to a voltage by the programming resistor R_{PROG} between PROG and GND. The PROG voltage becomes the average charge current input signal to error amplifier, EA. EA also receives loop control information from the battery voltage feedback input V_{FB} and the adapter input current limit circuit. The ITH output of the error amplifier is a scaled control voltage for one input of the PWM comparator, CC. ITH sets a peak inductor current threshold, sensed by R1, to maintain the desired average current through R_{SENSE}. The current comparator output does this by switching the state of the RS latch at the appropriate time.

At the beginning of each oscillator cycle, the PWM clock sets the RS latch and turns on the external topside NFET (bottom-side synchronous NFET off) to refresh the current carried by the external inductor L1. The inductor current and voltage across R_{SENSE} begin to rise linearly. CA buffers this instantaneous voltage rise and applies it to CC with gain supplied by R1. When the voltage across R1 exceeds the peak level set by the ITH output of EA, the top FET turns off and the bottom FET turns on. The inductor current then ramps down linearly until the next rising PWM clock edge. This closes the loop and sources the correct inductor current to maintain the desired parameter (charge current, battery voltage, or input current). To produce a near constant frequency, the PWM oscillator implements the equation:

$$t_{OFF} = \frac{CLP - BAT}{CLP \bullet 550kHz}$$

Repetitive, closed-loop waveforms for stable PWM operation appear in Figure 2.

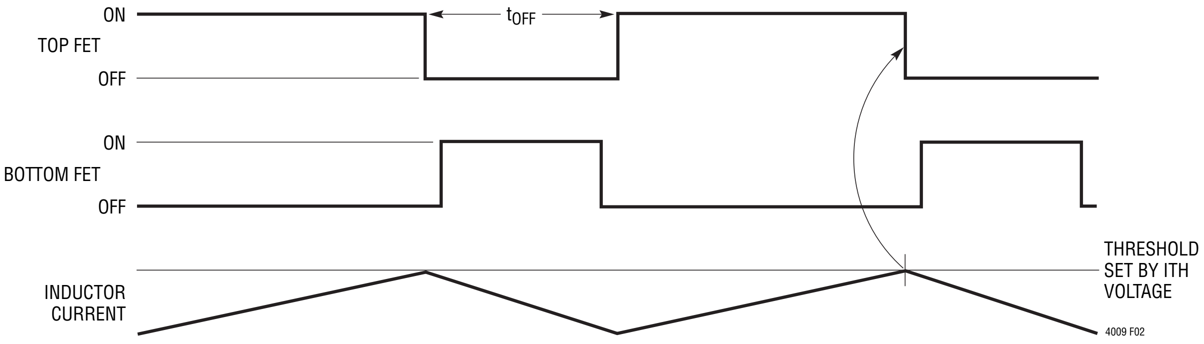


Figure 2. PWM Waveforms

OPERATION

PWM Watchdog Timer

As input and output conditions vary, the LTC4009 may need to utilize PWM duty cycles approaching 100%. In this case, operating frequency may be reduced well below 550kHz. An internal watchdog timer observes the activity on the TGATE pin. If TGATE is on for more than 40µs, the watchdog activates and forces the bottom NFET on (top NFET off) for about 100ns. This avoids a potential source of audible noise when using ceramic input or output capacitors and prevents the boost supply capacitor for the top gate driver from discharging. In low drop out operation, the actual charge current may not be able to reach the programmed full-scale value due to the watchdog function.

Overvoltage Protection

The LTC4009 also contains overvoltage detection that prevents transient battery voltage overshoots of more than about 6% above the programmed output voltage. When battery overvoltage is detected, both external MOSFETs are turned off until the overvoltage condition clears, at which time a new soft start sequence begins. This is useful for properly charging battery packs that use an internal switch to disconnect themselves for performing functions such as calibration or pulse mode charging.

Reverse Charge Current Protection (Anti-Boost)

Because the LTC4009 always attempts to operate synchronously in full continuous mode (to avoid audible noise from ceramic capacitors), reverse average charge current can occur during some invalid operating conditions. To avoid boosting a lightly loaded system supply during reverse operation, the LTC4009 monitors the voltage on CLP to determine if it rises 25mV above DCIN during charge. However, under heavier system loads, CLP may not boost above DCIN, even though reverse average current is flowing. In this case a second circuit monitors indication of reverse average current on PROG.

If the designer intends to replace the input diode with a MOSFET for improved efficiency, using the $\overline{\text{ACP}}$ signal of the LTC4009 to control the MOSFET is not recommended. In this case, the LTC4012 is strongly suggested, because it includes ideal diode control of the MOSFET, instead of driving it as a simple switch. This solution is the most effective at detecting boost conditions and quickly shutting down the IC. If for some reason the LTC4012 solution is not acceptable, and a MOSFET with external control is used to replace the input diode, and there are conditions involving very low reverse current under no system load with an AC adapter that cannot sink current, it may still be possible to boost the DCIN input supply. To cover this case, the LTC4009 monitors the resistor divider attached to the DCDIV pin and sets an input overvoltage fault if that voltage exceeds 1.825V.

If any of these circuits detects boost operation, The LTC4009 turns off both external MOSFETs until the reverse current condition clears. Once DCIN-CLP > 25mV, a new soft-start sequence begins.

APPLICATIONS INFORMATION

Programming Charge Current

The formula for charge current is:

$$I_{CHRG} = \frac{R_{IN}}{R_{SENSE}} \bullet \left(\frac{1.2085V}{R_{PROG}} - 11.67\mu A \right)$$

The LTC4009 operates best with 3.01k input resistors, although other resistors near this value can be used to accommodate standard sense resistor values. Refer to the subsequent discussion on inductor selection for other considerations that come into play when selecting input resistors R_{IN}.

R_{SENSE} should be chosen according to the following equation:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

where I_{MAX} is the desired maximum charge current I_{CHRG}. The 100mV target can be adjusted to some degree to obtain standard R_{SENSE} values and/or a desired R_{PROG} value, but target voltages lower than 100mV will cause a proportional reduction in current regulation accuracy.

The required minimum resistance between PROG and GND can be determined by applying the suggested expression for R_{SENSE} while solving the first equation given above for charge current with $I_{CHRG} = I_{MAX}$:

$$R_{PROG(MIN)} = \frac{1.2085V \bullet R_{IN}}{0.1V + 11.67\mu A \bullet R_{IN}}$$

If R_{IN} is chosen to be 3.01k with a sense voltage of 100mV, this equation indicates a minimum value for R_{PROG} of 26.9k. Table 6 gives some examples of recommended charge current programming component values based on these equations.

The resistance between PROG and GND can simply be set with a single a resistor, if only maximum charge current needs to be controlled during the desired charging algorithm. However, some batteries require a low charge current for initial conditioning when they are heavily discharged. The charge current can then be safely switched to a higher level after conditioning is complete. Figure 3 illustrates one method of doing this with 2-level control of the PROG pin resistance. Turning Q1 off reduces the charge current to $I_{MAX}/10$ for battery conditioning. When Q1 is on, the LTC4009 is programmed to allow full I_{MAX} current for bulk charge. This technique can be expanded through the use of additional digital control inputs for an arbitrary number of pre-programmed current values.

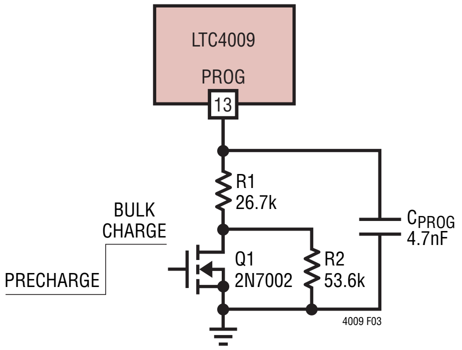


Figure 3. Programming 2-Level Charge Current

For a truly continuous range of maximum charge current control, pulse width modulation can be used as shown in Figure 4. The value of R_{PROG} controls the maximum value of charge current which can be programmed (Q1 continuously on). PWM of the Q1 gate voltage changes the value of R_{PROG} to produce lower currents. The frequency of this modulation should be higher than a few kHz, and C_{PROG} must be increased to reduce the ripple caused by switching Q1. In addition, it may be necessary to increase loop

APPLICATIONS INFORMATION

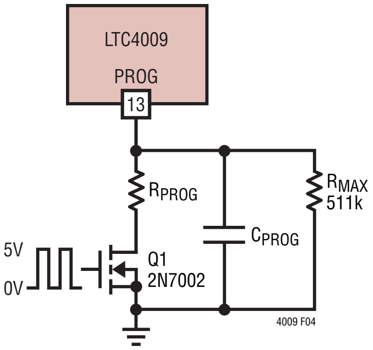


Figure 4. Programming PWM Current

compensation capacitance connected to ITH to maintain stability or prevent large current overshoot during start-up. Selecting a higher Q1 PWM frequency (≈10kHz) will reduce the need to change C_{PROG} or other compensation values. Charge current will be proportional to the duty cycle of the PWM input on the gate of Q1.

Programming LTC4009 Output Voltage

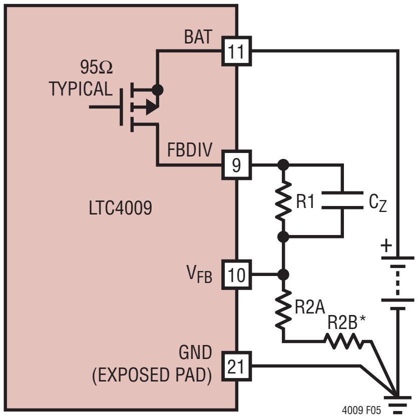
Figure 5 shows the external circuit for programming the charger voltage when using the LTC4009. The voltage is then governed by the following equation:

$$V_{BAT} = \frac{1.2085V \bullet (R1 + R2)}{R2}, \; R2 = R2A + R2B$$

See Table 2 for approximate resistor values for R2.

$$R1 = R2\left(\frac{V_{BAT}}{1.2085V} - 1\right), \; R2 = R2A + R2B$$

Selecting R2 to be less than 50k and the sum of R1 and R2 at least 200k or above, achieves the lowest possible error at the V_{FB} sense input. Note that sources of error such as R1 and R2 tolerance, FBDIV R_{ON} or V_{FB} input impedance are not included in the specifications given in the Electrical Characteristics. This leads to the possibility that very accurate (0.1%) external resistors might be required. Actually, the temperature rise of the LTC4009 will rarely exceed 50°C at the end of charge, because charge current will have tapered to a low level. This means that 0.25% resistors will normally provide the required level of overall accuracy. Table 2 gives recommended values for R1 and R2 for popular lithium-ion battery voltages. For values of R1 above 200k, addition of capacitor C_Z may improve transient response and loop stability. A value of 10pF is normally adequate.



*OPTIONAL TRIM RESISTOR

Figure 5. Programming LTC4009 Output Voltage

Table 2. Programming LTC4009 Output Voltage

V_{BAT} VOLTAGE	R1 (0.25%)	R2A (0.25%)	R2B (1%)*
4.1V	165k	69.0k	–
4.2V	167k	67.3k	200
8.2V	162k	28.0k	–
8.4V	169k	28.4k	–
12.3V	301k	32.8k	–
12.6V	294k	31.2k	–
16.4V	284k	22.6k	–
16.8V	271k	21.0k	–
20.5V	316k	19.8k	–
21.0V	298k	18.2k	–
24.6V	298k	15.4k	–
25.2V	397k	20.0k	–

*To obtain required accuracy requires series resistors for R2.

APPLICATIONS INFORMATION

Programming LTC4009-1/LTC4009-2 Output Voltage

The LTC4009-1/LTC4009-2 feature precision internal battery voltage feedback resistor taps configured for common lithium-ion voltages. All that is required to program the desired voltage is proper pin programming of FVS0 and FVS1 as shown in Table 3.

Table 3. LTC4009-1/LTC4009-2 Output Voltage Programming

V_{BAT} VOLTAGE			
LTC4009-1	**LTC4009-2**	**FVS1**	**FVS0**
4.1V	4.2V	GND	GND
8.2V	8.4V	GND	$INTV_{DD}$
12.3V	12.6V	$INTV_{DD}$	GND
16.4V	16.8V	$INTV_{DD}$	$INTV_{DD}$

Programming Input Current Limit

To set the input current limit, I_{LIM}, the minimum wall adapter current rating must be known. To account for the tolerance of the LTC4009 input current sense circuit, 5% should be subtracted from the adapter's minimum rated output. Refer to Figure 6 and program the input current limit function with the following equation.

$$R_{CL} = \frac{100mV}{I_{LIM}}$$

where I_{LIM} is the desired maximum current draw from the DC (adapter) input, including adjustments for tolerance, if any.

Often an AC adapter will include a rated current output margin of at least +10%. This can allow the adapter current limit value to simply be programmed to the actual minimum rated adapter output current. Table 4 shows some common R_{CL} current limit programming values.

A lowpass filter formed by R_F (5.1k) and C_F (0.1µF) is required to eliminate switching noise from the LTC4009 PWM and other system components. If input current limiting is not desired, CLN should be shorted to CLP while CLP remains connected to power.

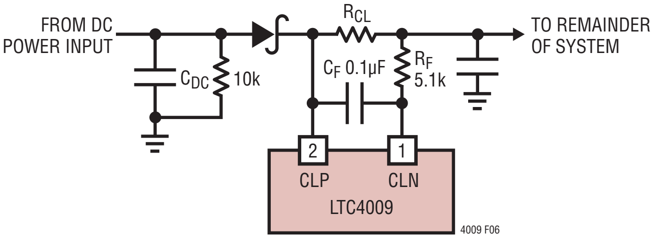


Figure 6. Programming Input Current Limit

Table 4. Common R_{CL} Values

ADAPTER RATING	R_{CL} VALUE (1%)	R_{CL} POWER DISSIPATION	R_{CL} POWER RATING
0.50A	0.200Ω	0.050W	0.25W
0.75A	0.133Ω	0.075W	0.25W
1.00A	0.100Ω	0.100W	0.25W
1.25A	0.080Ω	0.125W	0.25W
1.50A	0.067Ω	0.150W	0.25W
1.75A	0.057Ω	0.175W	0.25W
2.00A	0.050Ω	0.200W	0.25W

Figure 7 shows an optional circuit that can influence the parameters of the input current limit in two ways. The first option is to lower the power dissipation of R_{CL} at the expense of accuracy without changing the input current

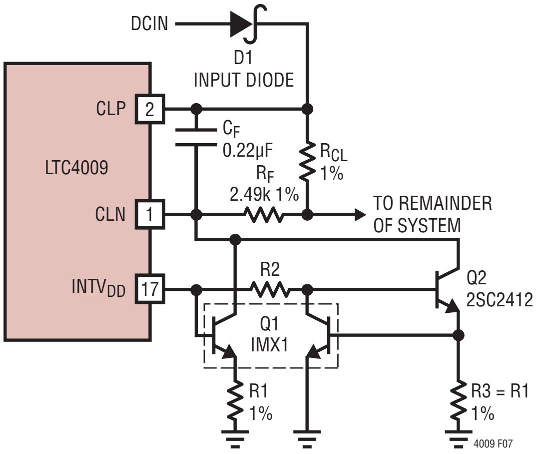


Figure 7. Adjusting Input Current Limit

APPLICATIONS INFORMATION

limit value. The second is to make the input current limit value programmable.

The overall accuracy of this circuit needs to be better than the power source current tolerance or be margined such that the worse-case error remains under the power source limits. The accuracy of the Figure 7 circuit is a function of the $INTV_{DD}$, V_{BE}, R_{CL}, R_F, R1 and R3 tolerances. To improve accuracy, the tolerance of R_F should be changed from 5.1k, 5% to a 2.49k 1% resistor. R_{CL} and the programming resistors R1 and R3 should also be 1% tolerance such that the dominant error is $INTV_{DD}$ (±3%). Bias resistor R2 can be 5%. When choosing NPN transistors, both need to have good gain (>100) at 10µA levels. Low gain NPNs will increase programming errors. Q1 must be a matched NPN pair. Since R_F has been reduced in value by half, the capacitor value of C_F should double to 0.22µF to remain effective at filtering out any noise.

If you wish to reduce R_{CL} power dissipation for a given current limit, the programming equation becomes:

$$R_{CL} = \frac{100\text{mV} - \left(\frac{5 \bullet 2.49\text{k}}{R1}\right)}{I_{LIM}}$$

If you wish to make the input current limit programmable, the equation becomes:

$$I_{LIM} = \frac{100\text{mV} - \left(\frac{5 \bullet 2.49\text{k}}{R1}\right)}{R_{CL}}$$

The equation governing R2 for both applications is based on the value of R1. R3 should always be equal to R1.

$$R2 = 0.875 \bullet R1$$

In many notebook applications, there are situations where two different I_{LIM} values are needed to allow two different power adapters or power sources to be used. In such cases, start by setting R_{LIM} for the high power I_{LIM} configuration and then use Figure 7 to set the lower I_{LIM} value. To toggle between the two I_{LIM} values, take the three ground connections shown in Figure 7, combine them into one common connection and use a small-signal NFET (2N7002) to open or close that common connection to circuit ground. When the NFET is off, the circuit is defeated (floating) allowing I_{LIM} to be the maximum value. When the NFET is on, the circuit will become active and I_{LIM} will drop to the lower set value.

Monitoring Charge Current

The PROG pin voltage can be used to indicate charge current where 1.2085V indicates full programmed current (1C) and zero charge current is approximately equal to $R_{PROG} \bullet 11.67\mu A$. PROG voltage varies in direct proportion to the charge current between this zero-current (offset) value and 1.2085V. When monitoring the PROG pin voltage, using a buffer amplifier as shown in Figure 8 will minimize charge current errors. The buffer amplifier may be powered from the $INTV_{DD}$ pin or any supply that is always on when the charger is on.

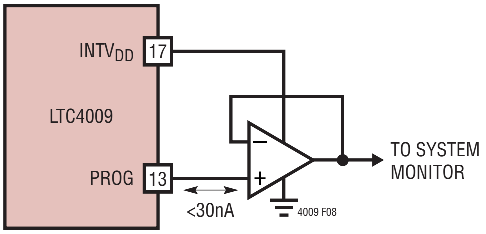


Figure 8. PROG Voltage Buffer

C/10 $\overline{\text{CHRG}}$ Indicator

The value chosen for R_{PROG} has a strong influence on charge current monitoring and the accuracy of the C/10 charge indicator output ($\overline{\text{CHRG}}$). The LTC4009 uses the voltage on the PROG pin to determine when charge current has dropped to the C/10 threshold. The nominal threshold of 400mV produces an accurate low charge current indication of C/10 as long as R_{PROG} = 26.7k, independent of all other current programming considerations. However, it may sometimes be necessary to deviate from this value to satisfy other application design goals.

APPLICATIONS INFORMATION

If R_{PROG} is greater than 26.7k, the actual level at which low charge current is detected will be less than C/10. The highest value of R_{PROG} that can be used while reliably indicating low charge current before reaching final V_{BAT} is 30.1k. R_{PROG} can safely be set to values higher than this, but low current indication will be lost.

If R_{PROG} is less than 26.7k, low charge current detection occurs at a level higher than C/10. More importantly, the LTC4009 becomes increasingly sensitive to reverse current. The lowest value of R_{PROG} that can be used without the risk of erroneous boost operation detection at end of charge is 26.1k. Values of R_{PROG} less than this should not be used. See the Operation section for more information about reverse current.

The nominal fractional value of I_{MAX} at which C/10 indication occurs is given by:

$$\frac{I_{C10}}{I_{MAX}} = \frac{400mV - \left(R_{PROG} \cdot 11.67\mu A\right)}{1.2085V - \left(R_{PROG} \cdot 11.67\mu A\right)}$$

Direct digital monitoring of C/10 indication is possible with an external application circuit like the one shown in Figure 9. The LTC4009 initially indicates C/10 until the PWM has started and the actual charge current can be determined (PROG pin voltage). The 0.1µF capacitor from $\overline{\text{CHRG}}$ to GND is used to filter this initial pulse, which is typically less than 2ms when starting toward a final charge current that is actually greater than C/10. If external circuitry is insensitive to, or can ignore, this momentary C/10 indication at start-up, the capacitor can be omitted.

By using two different value pull-up resistors, a microprocessor can detect three states from this pin (charging, C/10 and not charging). See Figure 10. When a digital output port (OUT) from the microprocessor drives one of the resistors and a second digital input port polls the network, the charge state can be determined as shown in Table 5.

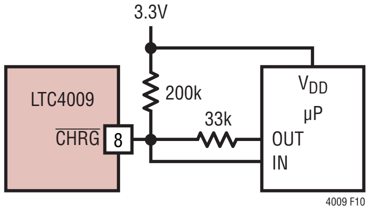


Figure 10. Microprocessor Status Interface

Table 5. Digital Read Back State (IN, Figure 10)

LTC4009 CHARGER STATE	OUT STATE	
	Hi-Z	**1**
Off	1	1
C/10 Charge	0	1
Bulk Charge	0	0

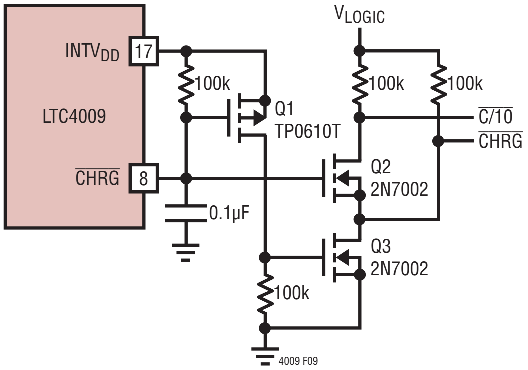


Figure 9. Digital C/10 Indicator

APPLICATIONS INFORMATION

Input and Output Capacitors

In addition to typical input supply bypassing (0.1µF) on DCIN, the relatively high ESR of aluminum electrolytic capacitors is helpful for reducing ringing when hot plugging the charger to the AC adapter. Refer to LTC Application Note 88 for more information.

The input capacitor between system power (drain of top FET, Figure 1) and GND is required to absorb all input PWM ripple current, therefore it must have adequate ripple current rating. Maximum RMS ripple current is typically one-half of the average battery charge current. Actual capacitance value is not critical, but using the highest possible voltage rating on PWM input capacitors will minimize problems. Consult with the manufacturer before use.

The output capacitor shown across the battery and ground must also absorb PWM output ripple current. The general formula for this capacitor current is:

$$I_{RMS} = \frac{0.29 \bullet V_{BAT} \bullet \left(1 - \frac{V_{BAT}}{V_{CLP}}\right)}{L1 \bullet f_{PWM}}$$

For example, I_{RMS} = 0.22A with:

V_{BAT} = 12.6V
V_{CLP} = 19V
L1 = 10µH
f_{PWM} = 550kHz

High capacity ceramic capacitors (20µF or more) available from a variety of manufacturers can be used for input/output capacitors. Other alternatives include OS-CON and POSCAP capacitors from Sanyo.

Low ESR solid tantalum capacitors have high ripple current rating in a relatively small surface mount package, but exercise caution when using tantalum for input or output bulk capacitors. High input surge current can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high surge currents. Select tantalum capacitors that have high surge current ratings or have been surge tested.

EMI considerations usually make it desirable to minimize ripple current in battery leads. Adding Ferrite beads or inductors can increase battery impedance at the nominal 550KHz switching frequency. Switching ripple current splits between the battery and the output capacitor in inverse relation to capacitor ESR and the battery impedance. If the ESR of the output capacitor is 0.2Ω and the battery impedance is raised to 4Ω with a ferrite bead, only 5% of the current ripple will flow to the battery.

Inductor Selection

Higher switching frequency generally results in lower efficiency because of MOSFET gate charge losses, but it allows smaller inductor and capacitor values to be used. A primary effect of the inductor value L1 is the amplitude of ripple current created. The inductor ripple current ΔI_L decreases with higher inductance and PWM operating frequency:

$$\Delta I_L = \frac{V_{BAT} \bullet \left(1 - \frac{V_{BAT}}{V_{CLP}}\right)}{L1 \bullet f_{PWM}}$$

Accepting larger values of ΔI_L allows the use of low inductance, but results in higher output voltage ripple and greater core losses. Lower charge currents generally call for larger inductor values.

APPLICATIONS INFORMATION

The LTC4009 limits maximum instantaneous peak inductor current during every PWM cycle. To avoid unstable switch waveforms, the ripple current must satisfy:

$$\Delta I_L < 2 \bullet \left(\frac{150mV}{R_{SENSE}} - I_{MAX} \right)$$

so choose:

$$L1 > \frac{0.125 \bullet V_{CLP}}{f_{PWM} \bullet \left(\frac{150mV}{R_{SENSE}} - I_{MAX} \right)}$$

For C-grade parts, a reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{MAX}$. For I-grade parts, use $\Delta I_L = 0.2 \bullet I_{MAX}$ **only** if the IC will actually be used to charge batteries over the wider I-grade temperature range. The voltage compliance of internal LTC4009 circuits also imposes limits on ripple current. Select R_{IN} (in Figure 1) to avoid average current errors in high ripple designs. The following equation can be used for guidance:

$$\frac{R_{SENSE} \bullet \Delta I_L}{50\mu A} \le R_{IN} \le \frac{R_{SENSE} \bullet \Delta I_L}{20\mu A}$$

R_{IN} should not be less than 2.37k or more than 6.04k. Values of R_{IN} greater than 3.01k may cause some reduction in programmed current accuracy. Use these equations and guidelines, as represented in Table 6, to help select the correct inductor value. This table was developed for C-grade parts to maintain maximum ΔI_L near $0.6 \bullet I_{MAX}$ with f_{PWM} at 550kHz and $V_{BAT} = 0.5 \bullet V_{CLP}$ (the point of maximum ΔI_L), assuming that inductor value could also vary by 25% at I_{MAX}. For I-grade parts, reduce maximum ΔI_L to less than $0.4 \bullet I_{MAX}$, but **only** if the IC will actually be used to charge batteries over the wider I-grade temperature range. In that case, a good starting point can be found by multiplying the inductor values shown in Table 6 by a factor of 1.6 and rounding up to the nearest standard value.

Table 6. Minimum Typical Inductor Values

V_{CLP}	L1 (Typ)	I_{MAX}	R_{SENSE}	R_{IN}	R_{PROG}
<10V	≥10µH	1A	100mΩ	3.01k	26.7k
10V to 20V	≥20µH	1A	100mΩ	3.01k	26.7k
>20V	≥28µH	1A	100mΩ	3.01k	26.7k
<10V	≥5.1µH	2A	50mΩ	3.01k	26.7k
10V to 20V	≥10µH	2A	50mΩ	3.01k	26.7k
>20V	≥14µH	2A	50mΩ	3.01k	26.7k

To guarantee that a chosen inductor is optimized in any given application, use the design equations provided and perform bench evaluation in the target application, particularly at duty cycles below 20% or above 80% where PWM frequency can be much less than the nominal value of 550kHz.

TGATE BOOST Supply

Use the external components shown in Figure 11 to develop a bootstrapped BOOST supply for the TGATE FET driver. A good set of equations governing selection of the two capacitors is:

$$C1 = \frac{20 \bullet Q_G}{4.5V}, \ C2 = 20 \bullet C1$$

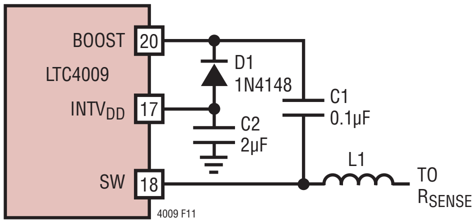


Figure 11. TGATE Boost Supply

APPLICATIONS INFORMATION

where Q_G is the rated gate charge of the top external NFET with $V_{GS} = 4.5V$. The maximum average diode current is then given by:

$$I_D = Q_G \bullet 665kHz$$

To improve efficiency by increasing V_{GS} applied to the top FET, substitute a Schottky diode with low reverse leakage for D1.

PWM jitter has been observed in some designs operating at higher V_{IN}/V_{OUT} ratios. This jitter does not substantially affect DC charge current accuracy. A series resistor with a value of 5Ω to 20Ω can be inserted between the cathode of D1 and the BOOST pin to remove this jitter if present. A resistor case size of 0603 or larger is recommended to lower ESL and achieve the best results.

FET Selection

Two external power MOSFETs must be selected for use with the charger: an N-channel power switch (top FET) and an N-channel synchronous rectifier (bottom FET). Peak gate-to-source drive levels are internally set to about 5V. Consequently, logic-level FETs must be used. In addition to the fundamental DC current, selection criteria for these MOSFETs also include channel resistance $R_{DS(ON)}$, total gate charge Q_G, reverse transfer capacitance C_{RSS}, maximum rated drain-source voltage BV_{DSS} and switching characteristics such as $t_{d(ON/OFF)}$. Power dissipation for each external FET is given by:

$$P_{D(TOP)} = \frac{V_{BAT} \bullet I_{MAX}{}^2 \bullet (1+\delta\Delta T) R_{DS(ON)}}{V_{CLP}} + k \bullet V_{CLP}{}^2 \bullet I_{MAX} \bullet C_{RSS} \bullet 665kHz$$

$$P_{D(BOT)} = \frac{(V_{CLP} - V_{BAT}) \bullet I_{MAX}{}^2 \bullet (1+\delta\Delta T) R_{DS(ON)}}{V_{CLP}}$$

where δ is the temperature dependency of $R_{DS(ON)}$, ΔT is the temperature rise above the point specified in the FET data sheet for $R_{DS(ON)}$ and k is a constant inversely related to the internal LTC4009 top gate driver. The term (1 + δΔT) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ curve versus temperature, but δ of 0.005/°C can be used as a suitable approximation for logic-level FETs if other data is not available. $C_{RSS} = Q_{GD}/dV_{DS}$ is usually specified in the MOSFET characteristics. The constant k = 2 can be used in estimating top FET dissipation. The LTC4009 is designed to work best with external FET switches with a total gate charge at 5V of 15nC or less.

For $V_{CLP} < 20V$, high charge current efficiency generally improves with larger FETs, while for $V_{CLP} > 20V$, top gate transition losses increase rapidly to the point that using a topside NFET with higher $R_{DS(ON)}$ but lower C_{RSS} can actually provide higher efficiency. If the charger will be operated with a duty cycle above 85%, overall efficiency is normally improved by using a larger top FET.

The synchronous (bottom) FET losses are greatest at high input voltage or during a short circuit, which forces a low side duty cycle of nearly 100%. Increasing the size of this FET lowers its losses but increases power dissipation in the LTC4009. Using asymmetrical FETs will normally achieve cost savings while allowing optimum efficiency.

Select FETs with BV_{DSS} that exceeds the maximum V_{CLP} voltage that will occur. Both FETs are subjected to this level of stress during operation. Many logic-level MOSFETs are limited to 30V or less.

APPLICATIONS INFORMATION

The LTC4009 uses an improved adaptive TGATE and BGATE drive that is insensitive to MOSFET inertial delays, $t_{d(ON/OFF)}$, to avoid overlap conduction losses. Switching characteristics from power MOSFET data sheets apply only to a specific test fixture, so there is no substitute for bench evaluation of external FETs in the target application. In general, MOSFETs with lower inertial delays will yield higher efficiency.

Diode Selection

A Schottky diode in parallel with the bottom FET and/or top FET in an LTC4009 application clamps SW during the non-overlap times between conduction of the top and bottom FET switches. This prevents the body diode of the MOSFETs from forward biasing and storing charge, which could reduce efficiency as much as 1%. One or both diodes can be omitted if the efficiency loss can be tolerated. A 1A Schottky is generally a good size for 3A chargers due to the low duty cycle of the non-overlap times. Larger diodes can actually result in additional efficiency (transition) losses due to larger junction capacitance.

Loop Compensation and Soft-Start

The three separate PWM control loops of the LTC4009 can be compensated by a single set of components attached between the ITH pin and GND. As shown in the typical LTC4009 application, a 6.04k resistor in series with a capacitor of at least 0.1µF provides adequate loop compensation for the majority of applications.

The LTC4009 can be soft-started with the compensation capacitor on the ITH pin. At start-up, ITH will quickly rise to about 0.25V, then ramp up at a rate set by the compensation capacitor and the 40µA ITH bias current. The full programmed charge current will be reached when ITH reaches approximately 2V. With a 0.1µF capacitor, the time to reach full charge current is usually greater than 1.5ms. This capacitor can be increased if longer start-up times are required, but loop bandwidth and dynamic response will be reduced.

$INTV_{DD}$ Regulator Output

Bypass the $INTV_{DD}$ regulator output to GND with a low ESR X5R or X7R ceramic capacitor with a value of 0.47µF or larger. The capacitor used to build the BOOST supply (C2 in Figure 11) can serve as this bypass. Do not draw more than 30mA from this regulator for the host system, governed by IC power dissipation.

Calculating IC Power Dissipation

The user should ensure that the maximum rated junction temperature is not exceeded under all operating conditions. The thermal resistance of the LTC4009 package (θ_{JA}) is 37°C/W, provided the Exposed Pad is in good thermal contact with the PCB. The actual thermal resistance in the application will depend on forced air cooling and other heat sinking means, especially the amount of copper on the PCB to which the LTC4009 is attached. The following formula may be used to estimate the maximum average power dissipation P_D (in watts) of the LTC4009, which is dependent upon the gate charge of the external MOSFETs. This gate charge, which is a function of both gate and drain voltage swings, is determined from specifications or graphs in the manufacturer's data sheet. For the equation below, find the gate charge for each transistor assuming 5V gate swing and a drain voltage swing equal to the maximum V_{CLP} voltage. Maximum LTC4009 power dissipation under normal operating conditions is then given by:

$$P_D = DCIN(2.8mA + I_{DD} + 665kHz(Q_{TGATE} + Q_{BGATE})) - 5I_{DD}$$

where:

I_{DD} = Average external $INTV_{DD}$ load current, if any

Q_{TGATE} = Gate charge of external top FET in Coulombs

Q_{BGATE} = Gate charge of external bottom FET in Coulombs

APPLICATIONS INFORMATION

PCB Layout Considerations

To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the LTC4009 is essential. Refer to Figure 12. For maximum efficiency, the switch node rise and fall times should be minimized. The following PCB design priority list will help insure proper topology. Layout the PCB using this specific order.

1. Input capacitors should be placed as close as possible to switching FET supply and ground connections with the shortest copper traces possible. The switching FETs must be on the same layer of copper as the input capacitors. Vias should not be used to make these connections.
2. Place the LTC4009 close to the switching FET gate terminals, keeping the connecting traces short to produce clean drive signals. This rule also applies to IC supply and ground pins that connect to the switching FET source pins. The IC can be placed on the opposite side of the PCB from the switching FETs.
3. Place the inductor input as close as possible to the switching FETs. Minimize the surface area of the switch node. Make the trace width the minimum needed to support the programmed charge current. Use no copper fills or pours. Avoid running the connection on multiple copper layers in parallel. Minimize capacitance from the switch node to any other trace or plane.
4. Place the charge current sense resistor immediately adjacent to the inductor output, and orient it such that current sense traces to the LTC4009 are not long. These feedback traces need to be run together as a single pair with the smallest spacing possible on any given layer on which they are routed. Locate any filter component on these traces next to the LTC4009, and not at the sense resistor location.
5. Place output capacitors adjacent to the sense resistor output and ground.
6. Output capacitor ground connections must feed into the same copper that connects to the input capacitor ground before connecting back to system ground.
7. Connection of switching ground to system ground, or any internal ground plane, should be single-point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection.
8. Route analog ground as a trace tied back to the LTC4009 GND paddle before connecting to any other ground. Avoid using the system ground plane. A useful CAD technique is to make analog ground a separate ground net and use a 0Ω resistor to connect analog ground to system ground.
9. A good rule of thumb for via count in a given high current path is to use 0.5A per via. Be consistent when applying this rule.

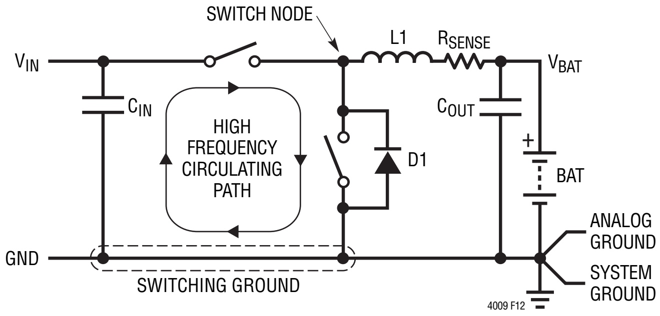


Figure 12. High Speed Switching Path

APPLICATIONS INFORMATION

10. If possible, place all the parts listed above on the same PCB layer.
11. Copper fills or pours are good for all power connections except as noted above in Rule 3. Copper planes on multiple layers can also be used in parallel. This helps with thermal management and lowers trace inductance, which further improves EMI performance.
12. For best current programming accuracy, provide a Kelvin connection from R_{SENSE} to CSP and CSN. See Figure 13 for an example.
13. It is important to minimize parasitic capacitance on the CSP and CSN pins. The traces connecting these pins to their respective resistors should be as short as possible.

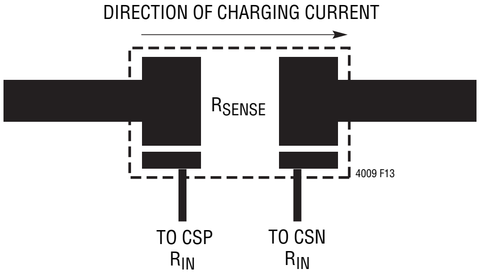
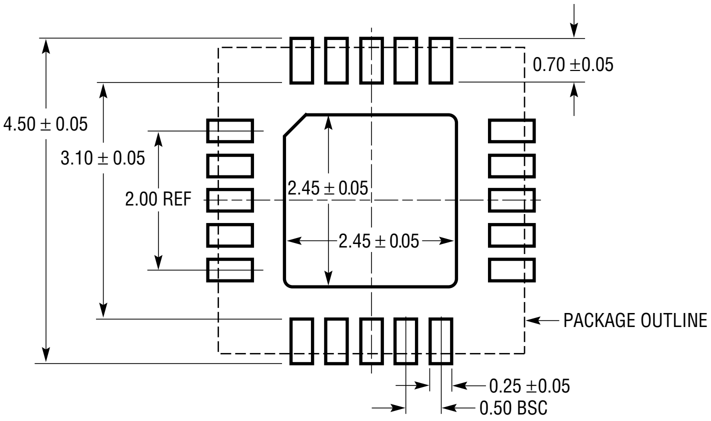


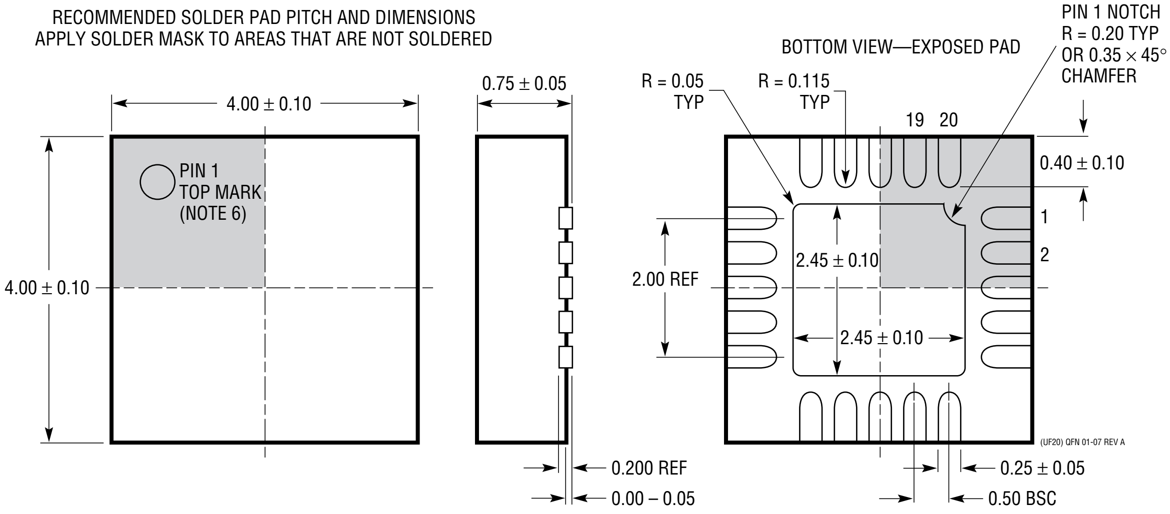
Figure 13. Kelvin Sensing of Charge Current

PACKAGE DESCRIPTION

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev D)

REV	DATE	DESCRIPTION	PAGE NUMBER
D	3/10	I-Grade Parts Added. Reflected Throughout the Data Sheet	1 to 28