Standalone Linear NiMH/NiCd Fast Battery Charger

FEATURES

- **Complete Fast Charger Controller for Single, 2-, 3- or 4-Series Cell NiMH/NiCd Batteries**
- **No Firmware or Microcontroller Required**
- **Termination by –ΔV, Maximum Voltage or Maximum Time**
- **No Sense Resistor or Blocking Diode Required**
- **Automatic Recharge Keeps Batteries Charged**
- **Programmable Fast Charge Current: 0.4A to 2A**
- **Accurate Charge Current: ±5% at 2A**
- Fast Charge Current Programmable Beyond 2A with External Sense Resistor
- Automatic Detection of Battery
- Precharge for Heavily Discharged Batteries
- Optional Temperature Qualified Charging
- Charge and AC Present Status Outputs Can Drive LED
- Automatic Sleep Mode with Input Supply Removal
- Negligible Battery Drain in Sleep Mode: <1μA
- Manual Shutdown
- Input Supply Range: 4.5V to 10V
- Available in 16-Lead DFN and TSSOP Packages

APPLICATIONS

- Portable Computers, Cellular Phones and PDAs
- Medical Equipment
- Charging Docks and Cradles
- Portable Consumer Electronics

DESCRIPTION

The LTC®4060 is a complete fast charging system for NiMH or NiCd batteries. Just a few external components are needed to design a standalone linear charging system.

An external PNP transistor provides charge current that is user programmable with a resistor. A small external capacitor sets the maximum charge time. No external current sense resistor is needed, and no blocking diode is required.

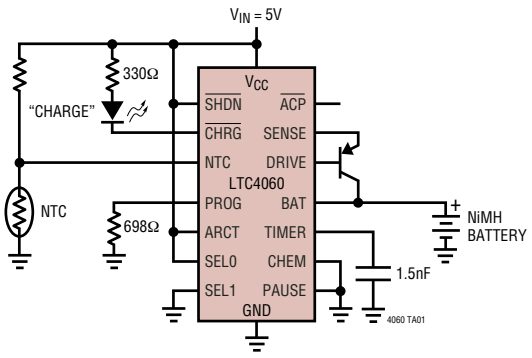
The IC automatically senses the DC input supply and battery insertion or removal. Heavily discharged batteries are initially charged at a C/5 rate before a fast charge is applied. Fast charge is terminated using the –ΔV detection method. Backup termination consists of a programmable timer and battery overvoltage detector. An optional external NTC thermistor can be used for temperature-based qualification of charging. An optional programmable recharge feature automatically recharges batteries after discharge.

Manual shutdown is accomplished with the $\overline{\text{SHDN}}$ pin, while removing input power automatically puts the LTC4060 into sleep mode. During shutdown or sleep mode, battery drain is <1μA.

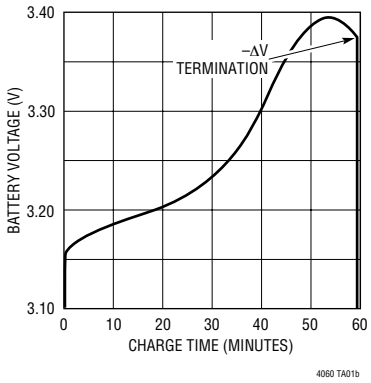
The LTC4060 is available in both low profile (0.75mm) 16-pin 5mm × 3mm DFN and 16-lead TSSOP packages. Both feature exposed metal die mount pads for optimum thermal performance.

TYPICAL APPLICATION

2-Cell, 2A Standalone NiMH Fast Charger with Optional Thermistor and Charge Indicator



2-Cell NiMH Charging Profile



ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.3V to 11V

Input Voltage

SHDN, NTC, SEL0, SEL1, PROG, ARCT, BAT, CHEM, TIMER, PAUSE ..... –0.3V to V_{CC} + 0.3V

Output Voltage

CHRG, ACP, DRIVE ..... –0.3V to V_{CC} + 0.3V

Output Current (SENSE) ..... –2.2A

Short-Circuit Duration (DRIVE) ..... Indefinite

Operating Ambient Temperature Range (Note 2) ..... –40°C to 85°C

Operating Junction Temperature (Note 3) ..... 125°C

Storage Temperature Range

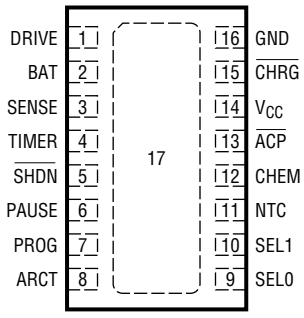
TSSOP Package ..... –65°C to 150°C

DFN Package ..... –65°C to 125°C

Lead Temperature (Soldering, 10 sec)

TSSOP Package ..... 300°C

PACKAGE/ORDER INFORMATION

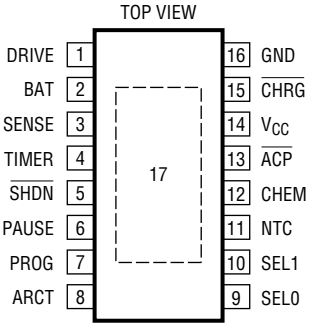


DHC16 PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W

EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB TO OBTAIN
θ_{JA} = 37°C/W OTHERWISE θ_{JA} = 140°C

ORDER PART NUMBER
LTC4060EDHC
DHC PART MARKING
4060



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 37°C/W

EXPOSED PAD (PIN 17) IS GND
MUST BE SOLDERED TO PCB TO OBTAIN
θ_{JA} = 37°C/W OTHERWISE θ_{JA} = 135°C

ORDER PART NUMBER
LTC4060EFE
FE PART MARKING
4060EFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{BAT} = 2.8V, GND = 0V unless otherwise specified. All currents into the device pins are positive and all currents out of the device pins are negative. All voltages are referenced to GND unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Supply							
V_{CC}	Operating Voltage Range (Note 4)		●	4.50		10	V
I_{CC}	V_{CC} Supply Current (Note 9)	I_{PROG} = 2mA (R_{PROG} = 698Ω), PAUSE = V_{CC}			2.9	4.3	mA
I_{SD}	V_{CC} Supply Shutdown Current	$\overline{SHDN}$ = 0V			250	325	µA
I_{BSD}	Battery Pin Leakage Current in Shutdown (Note 5)	V_{BAT} = 2.8V, $\overline{SHDN}$ = 0V		–1	0	1	µA
I_{BSL}	Battery Pin Leakage Current in Sleep (Note 6)	V_{CC} = 0V, V_{BAT} = 5.6V		–1	0	1	µA
V_{UVI1}	Undervoltage Lockout Exit Threshold	SEL0 = 0, SEL1 = 0 and SEL0 = V_{CC}, SEL1 = 0, V_{CC} Increasing	●	4.25	4.36	4.47	V
V_{UVD1}	Undervoltage Lockout Entry Threshold	SEL0 = 0, SEL1 = 0 and SEL0 = V_{CC}, SEL1 = 0, V_{CC} Decreasing	●	4.15	4.26	4.37	V

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{BAT} = 2.8V, GND = 0V unless otherwise specified. All currents into the device pins are positive and all currents out of the device pins are negative. All voltages are referenced to GND unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{UVI2}	Undervoltage Lockout Exit Threshold	SEL0 = 0, SEL1 = V_{CC}, V_{CC} Increasing	●	6.67	6.81	6.95	V
V_{UVD2}	Undervoltage Lockout Entry Threshold	SEL0 = 0, SEL1 = V_{CC}, V_{CC} Decreasing	●	6.57	6.71	6.85	V
V_{UVI3}	Undervoltage Lockout Exit Threshold	SEL0 = V_{CC}, SEL1 = V_{CC}, V_{CC} Increasing	●	8.28	8.47	8.65	V
V_{UVD3}	Undervoltage Lockout Entry Threshold	SEL0 = V_{CC}, SEL1 = V_{CC}, V_{CC} Decreasing	●	8.18	8.37	8.55	V
V_{UVH}	Undervoltage Lockout Hysteresis	For All SEL0, SEL1 Options			100		mV
Charging Performance							
I_{FCH}	High Fast Charge Current (Notes 7, 10)	R_{PROG} = 698Ω, 5V < V_{CC} < 10V	●	1.9	2	2.1	A
I_{FCL}	Low Fast Charge Current (Note 7)	R_{PROG} = 3480Ω, 4.5V < V_{CC} < 10V	●	0.35	0.4	0.45	A
I_{PCH}	High Precharge Current (Note 7)	R_{PROG} = 698Ω, 4.5V < V_{CC} < 10V		320	400	480	mA
I_{PCL}	Low Precharge Current (Note 7)	R_{PROG} = 3480Ω, 4.5V < V_{CC} < 10V		40	80	120	mA
I_{BRD}	Battery Removal Detection Bias Current	4.5V < V_{CC} < 10V, V_{BAT} = V_{CC} – 0.4V	●	–450	–300	–160	µA
V_{BR}	Battery Removal Threshold Voltage (Note 8)	V_{CELL} Increasing, 4.5V < V_{CC} < 10V	●	1.95	2.05	2.15	V
V_{BRH}	Battery Removal Threshold Hysteresis Voltage (Note 8)	V_{CELL} Decreasing			50		mV
V_{BOV}	Battery Overvoltage Threshold (Note 8)	V_{CELL} Increasing, 4.5V < V_{CC} < 10V	●	1.85	1.95	2.05	V
V_{BOVH}	Battery Overvoltage Threshold Hysteresis (Note 8)	V_{CELL} Decreasing			50		mV
V_{FCQ}	Fast Charge Qualification Threshold Voltage (Note 8)	V_{CELL} Increasing, 4.5V < V_{CC} < 10V		840	900	960	mV
V_{FCQH}	Fast Charge Qualification Threshold Hysteresis Voltage (Note 8)	V_{CELL} Decreasing			50		mV
V_{IDT}	Initial Delay Hold-Off Threshold Voltage (Note 8)	V_{CELL} Increasing, 4.5V < V_{CC} < 10V		1.24	1.3	1.36	V
V_{IDTH}	Initial Delay Hold-Off Threshold Hysteresis Voltage (Note 8)	V_{CELL} Decreasing			50		mV
V_{MDV}	–ΔV Termination (Note 8)	CHEM = V_{CC} (NiCd) CHEM = 0V (NiMH)	● ●	11 5	16 8	21 14	mV mV
V_{PROG}	Program Pin Voltage	4.5V < V_{CC} < 10V, R_{PROG} = 635Ω and 3480Ω	●	1.45	1.5	1.54	V
V_{ART}	Automatic Recharge Programmed Threshold Voltage Accuracy (Note 8)	V_{CELL} Decreasing, V_{ARCT} = 1.1V, 4.5V < V_{CC} < 10V	●	1.065	1.1	1.135	V
V_{ARDT}	Automatic Recharge Default Threshold Voltage Accuracy (Note 8)	V_{CELL} Decreasing, V_{ARCT} = V_{CC}, 4.5V < V_{CC} < 10V	●	1.235	1.3	1.365	V
V_{ARH}	Automatic Recharge Threshold Voltage Hysteresis (Note 8)	V_{CELL} Increasing			50		mV
V_{ARDEF}	Automatic Recharge Pin Default Enable Threshold Voltage			V_{CC} – 0.8		V_{CC} – 0.2	V
V_{ARDIS}	Automatic Recharge Pin Disable Threshold Voltage			250		650	mV
I_{ARL}	Automatic Recharge Pin Pull-Down Current	V_{ARCT} = 1.3V	●	0.15		1.5	µA
V_{CLD}	NTC Pin Cold Threshold Voltage	V_{NTC} Decreasing, 4.5V < V_{CC} < 10V	●	0.83 • V_{CC}	0.86 • V_{CC}	0.89 • V_{CC}	V
V_{CLDH}	NTC Pin Cold Threshold Hysteresis Voltage	V_{NTC} Increasing			150		mV
V_{HTI}	NTC Pin Hot Charge Initiation Threshold Voltage	V_{NTC} Decreasing, 4.5V < V_{CC} < 10V	●	0.47 • V_{CC}	0.5 • V_{CC}	0.53 • V_{CC}	V

ELECTRICAL CHARACTERISTICS

The ● indicates specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{BAT} = 2.8V, GND = 0V unless otherwise specified. All currents into the device pins are positive and all currents out of the device pins are negative. All voltages are referenced to GND unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{HTIH}	NTC Pin Hot Charge Initiation Hysteresis Voltage	V_{NTC} Increasing			100		mV
V_{HTC}	NTC Pin Hot Charge Cutoff Threshold Voltage	V_{NTC} Decreasing, 4.5V ≤ V_{CC} ≤ 10V	●	0.37 • V_{CC}	0.4 • V_{CC}	0.43 • V_{CC}	V
V_{HTCH}	NTC Pin Hot Charge Cutoff Hysteresis Voltage	V_{NTC} Increasing			100		mV
V_{NDIS}	NTC Pin Disable Threshold Voltage			25		250	mV
I_{NL}	NTC Pin Pull-Down Current	V_{NTC} = 2.5V	●	0.15		1.5	µA
t_{ACC}	Timer Accuracy	R_{PROG} = 698Ω, C_{TIMER} = 1.2nF and R_{PROG} = 3480Ω, C_{TIMER} = 470pF		–15	0	15	%
Output Drivers							
I_{DRV}	Drive Pin Sink Current	V_{DRIVE} = 4V	●	40	70	120	mA
R_{DRV}	Drive Pin Resistance to V_{CC}	V_{DRIVE} = 4V, Not Charging			4700		Ω
V_{OL}	$\overline{ACP}$, $\overline{CHRG}$ Output Pins Low Voltage	$I_{\overline{ACP}}$ = $I_{\overline{CHRG}}$ = 10mA				0.8	V
I_{OH}	$\overline{ACP}$, $\overline{CHRG}$ Output Pins High Leakage Current	Outputs Inactive, $V_{\overline{CHRG}}$ = $V_{\overline{ACP}}$ = V_{CC}		–2		2	µA
Control Inputs							
V_{IT}	$\overline{SHDN}$, SEL0, SEL1, CHEM, PAUSE Pins Digital Input Threshold Voltage	V_{CC} = 10V		350		650	mV
V_{ITH}	$\overline{SHDN}$, SEL0, SEL1, CHEM, PAUSE Pins Digital Input Hysteresis Voltage				50		mV
I_{IPD}	$\overline{SHDN}$, SEL0, SEL1, CHEM Pins Digital Input Pull-Down Current	V_{CC} = 10V, V_{IN} = V_{CC}		0.4		2	µA
I_{IPU}	PAUSE Pin Digital Input Pull-Up Current	V_{IN} = GND		–2		–0.4	µA

Note 1: Absolute Maximum Ratings only indicate limits for survivability. Operating the device beyond these limits may result in permanent damage. Continuous or extended application of these maximum levels may adversely affect device reliability.

Note 2: The LTC4060 is guaranteed to meet performance specifications from 0°C to 70°C ambient temperature range and 0°C to 85°C junction temperature range. Specifications over the –40°C to 85°C operating ambient temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Overtemperature protection is activated at a temperature of approximately 145°C, which is above the specified maximum operating junction temperature. Continuous operation above the specified maximum operation temperature may result in device degradation or failure. Operating junction temperature T_J (in °C) is calculated from the ambient temperature T_A and the average power dissipation P_D (in watts) by the formula:

$$T_J = T_A + \theta_{JA} \bullet P_D$$

Note 4: Short duration drops below the minimum V_{CC} specification of several microseconds or less are ignored by the undervoltage detection circuit.

Note 5: Assumes that the external PNP pass transistor has negligible B-C reverse leakage current when the collector is biased at 2.8V (V_{BAT} for two charged cells in series) and the base is biased at V_{CC}.

Note 6: Assumes that the external PNP pass transistor has negligible B-E reverse leakage current when the emitter is biased at 0V (V_{CC}) and the base is biased at 5.6V (V_{BAT} for four charged cells in series).

Note 7: The charge current specified is the regulated current through the internal current sense resistor that flows into the external PNP pass transistor's emitter. Actual battery charging current is slightly less and depends upon PNP alpha.

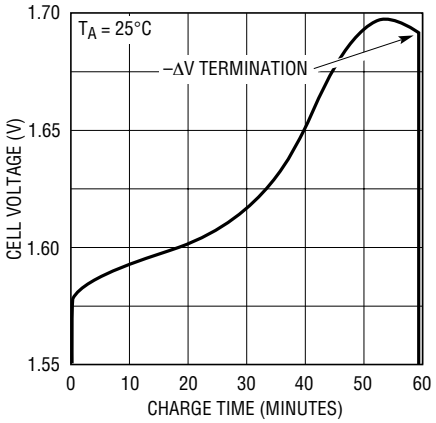
Note 8: Given as a per cell voltage (V_{BAT}/Number of Cells).

Note 9: Supply current includes the current programming resistor current of 2mA. The charger is paused and not charging the battery.

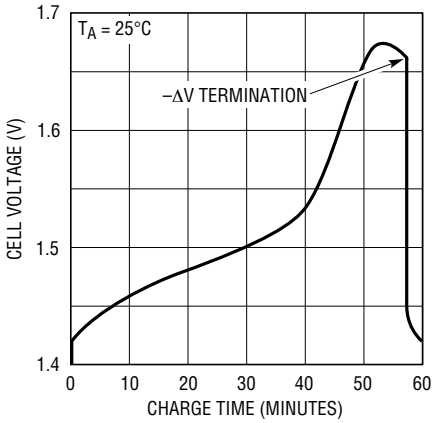
Note 10: The minimum V_{CC} supply is set at 5V during this test to compensate for voltage drops due to test socket contact resistance and 2A of current. This ensures that the supply voltage delivered to the device under test does not fall below the UVLO entry threshold. Specification at the minimum V_{CC} of 4.5V is assured by design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

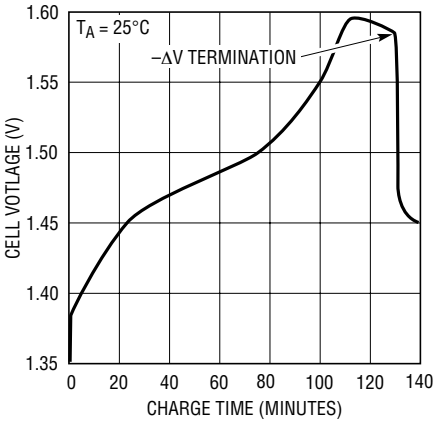
NiMH Battery Charging Characteristics at 1C Rate



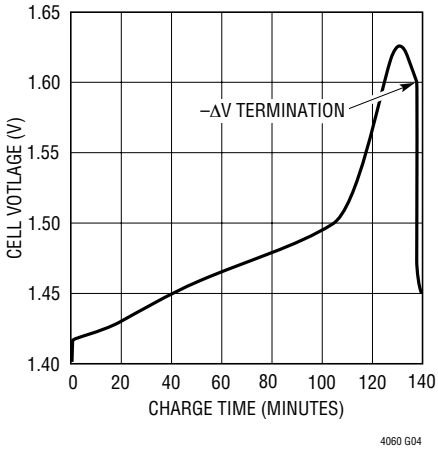
NiCd Battery Charging Characteristics at 1C Rate



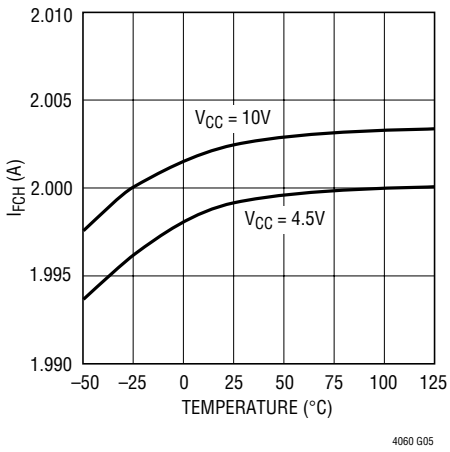
NiMH Battery Charging Characteristics at C/2 Rate



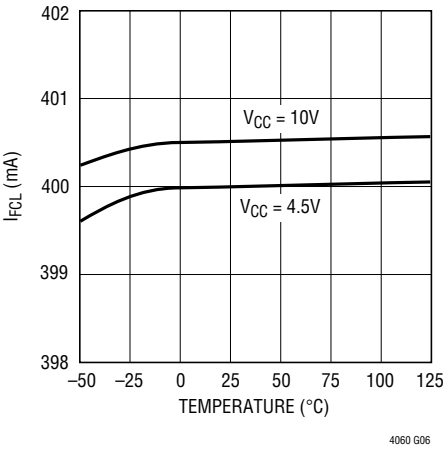
NiCd Battery Charging Characteristics at C/2 Rate



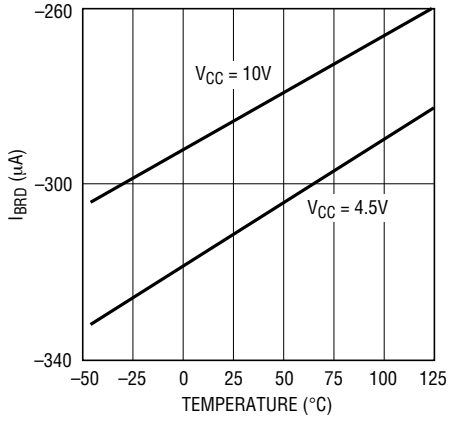
I_{FCH} vs Temperature and Supply Voltage



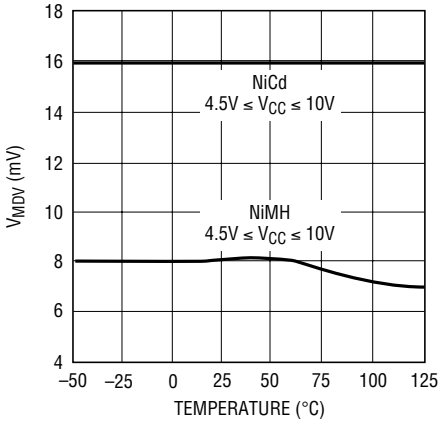
I_{FCL} vs Temperature and Supply Voltage



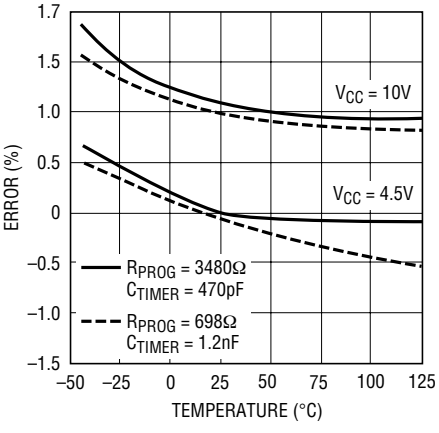
I_{BRD} vs Temperature and Supply Voltage



V_{MDV} vs Temperature and Supply Voltage



t_{ACC} vs Temperature and Supply Voltage



PIN FUNCTIONS

DRIVE (Pin 1): Base Drive Output for the External PNP Pass Transistor. Provides a controlled sink current that drives the base of the PNP. This pin has current limit protection for the LTC4060.

BAT (Pin 2): Battery Voltage Sense Input Pin. The LTC4060 uses the voltage on this pin to monitor battery voltage and control the battery current during charging. An internal resistor divider is connected to this pin which is disconnected when in shutdown or when no power is applied to V_{CC}.

SENSE (Pin 3): Charge Current Sense Node Input. Current from V_{CC} passes through the internal current sense resistor and reappears at the SENSE pin to supply current to the external PNP emitter. The PNP collector provides charge current directly to the battery.

TIMER (Pin 4): Charge Timer Input. A capacitor connected between TIMER and GND along with a resistor connected from PROG to GND programs the charge cycle timing limits.

$\overline{\text{SHDN}}$ (Pin 5): Active Low Shutdown Control Logic Input. When pulled low, charging stops and the LTC4060 supply current is minimized.

PAUSE (Pin 6): Pause Enable Logic Input. The charger can be paused, turning off the charge current, disabling termination and stopping the timer when this pin is high. A low level will resume the charging process.

PROG (Pin 7): Charge Current Programming Input. Provides a virtual reference of 1.5V for an external resistor (R_{PROG}) tied between this pin and GND that programs the battery charge current. The fast charge current will be 930 times the current through this resistor. This voltage is also usable as system voltage reference.

ARCT (Pin 8): Autorecharge Threshold Programming Input. When the average cell voltage falls below this threshold, charging is reinitiated. The voltage on this pin is conveniently derived by using two series PROG pin resistors and connecting to their common. Connecting ARCT to V_{CC} invokes a default threshold of 1.3V. Connecting ARCT to GND inhibits autorecharge.

SEL0, SEL1 (Pins 9, 10): Number of Cells Selection Logic Input. For single cell, connect both pins to GND. For two cells, connect SEL1 to GND and SEL0 to V_{CC}. For three cells, SEL1 connects to V_{CC} and SEL0 to GND. For four cells, connect both pins to V_{CC}.

NTC (Pin 11): Battery Temperature Input. An external NTC thermistor network may be connected to NTC to provide temperature-based charge qualification. Connecting NTC to GND inhibits this function.

CHEM (Pin 12): Battery Chemistry Selection Logic Input. When connected to a high level NiCd fast charge $-\Delta V$ termination parameters are used. A low level selects NiMH parameters.

$\overline{\text{ACP}}$ (Pin 13): Open-Drain Power Supply Status Output. When V_{CC} is greater than the undervoltage lockout threshold, the $\overline{\text{ACP}}$ pin will pull to ground. Otherwise the pin is high impedance. This output is capable of driving an LED.

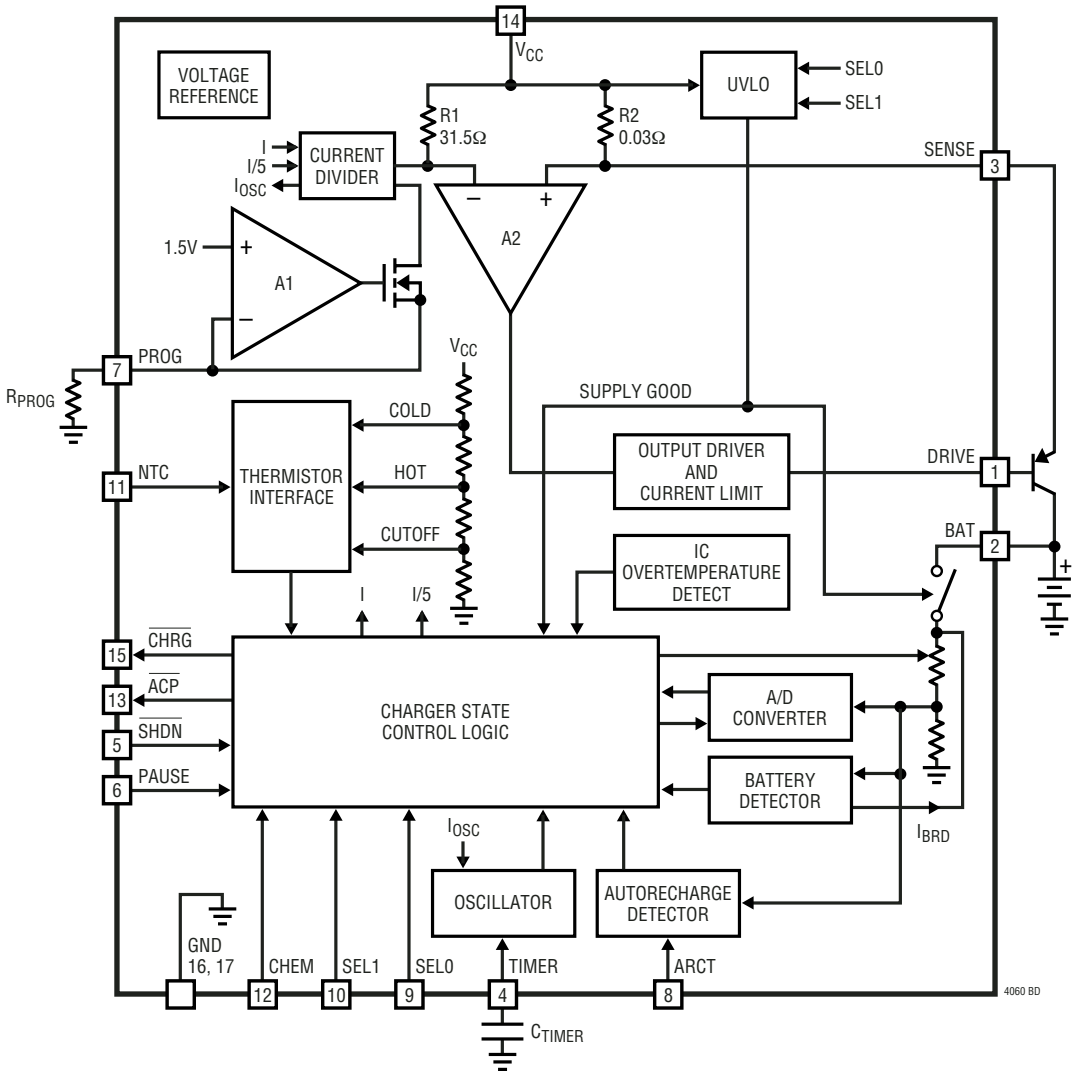
V_{CC} (Pin 14): Power Input. This pin can be bypassed to ground with a capacitance of 1μF.

$\overline{\text{CHRG}}$ (Pin 15): Open-Drain Charge Indicator Status Output. The LTC4060 indicates it is providing charge to the battery by driving this pin to GND. If charging is paused or suspended due to abnormal battery temperature, the pin remains pulled to GND. Otherwise the pin is high impedance. This output can drive an LED.

GND (Pin 16): Ground. This pin provides a ground for the internal voltage reference and other circuits. All voltage thresholds are referenced to this pin.

Exposed Pad (Pin 17): Thermal Connection. Internally connected to GND. Solder to PCB ground for optimum thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC4060 is a complete linear fast charging system for NiMH or NiCd batteries. Operation can be understood by referring to the Block Diagram, State Diagram (Figure 1) and application circuit (Figure 2). While in the unpowered sleep mode, the battery is disconnected from any internal loading. The sleep mode is exited and the shutdown mode is entered when V_{CC} rises above the UVLO (Undervoltage Lock Out) exit threshold. The UVLO thresholds are dependent upon the number of series cells programmed by the SEL0 and SEL1 pins. When shutdown occurs the $\overline{ACP}$ pin goes from a high to low impedance state. The shutdown mode is exited and the charge qualification mode entered when all of the following conditions are met: 1) there is no manual shutdown command from $\overline{SHDN}$, 2) the battery overvoltage detector does not detect a battery overvoltage, 3) the battery removal detector detects a battery in place, 4) pause is inactive and 5) the IC's junction temperature is normal. Once in the charge qualification mode the thermistor interface monitors an optional thermistor network to determine if the battery temperature is within charging limits. If the temperature is found within limits charging can begin. While charging, the $\overline{CHRG}$ pin pulls to GND which can drive an LED.

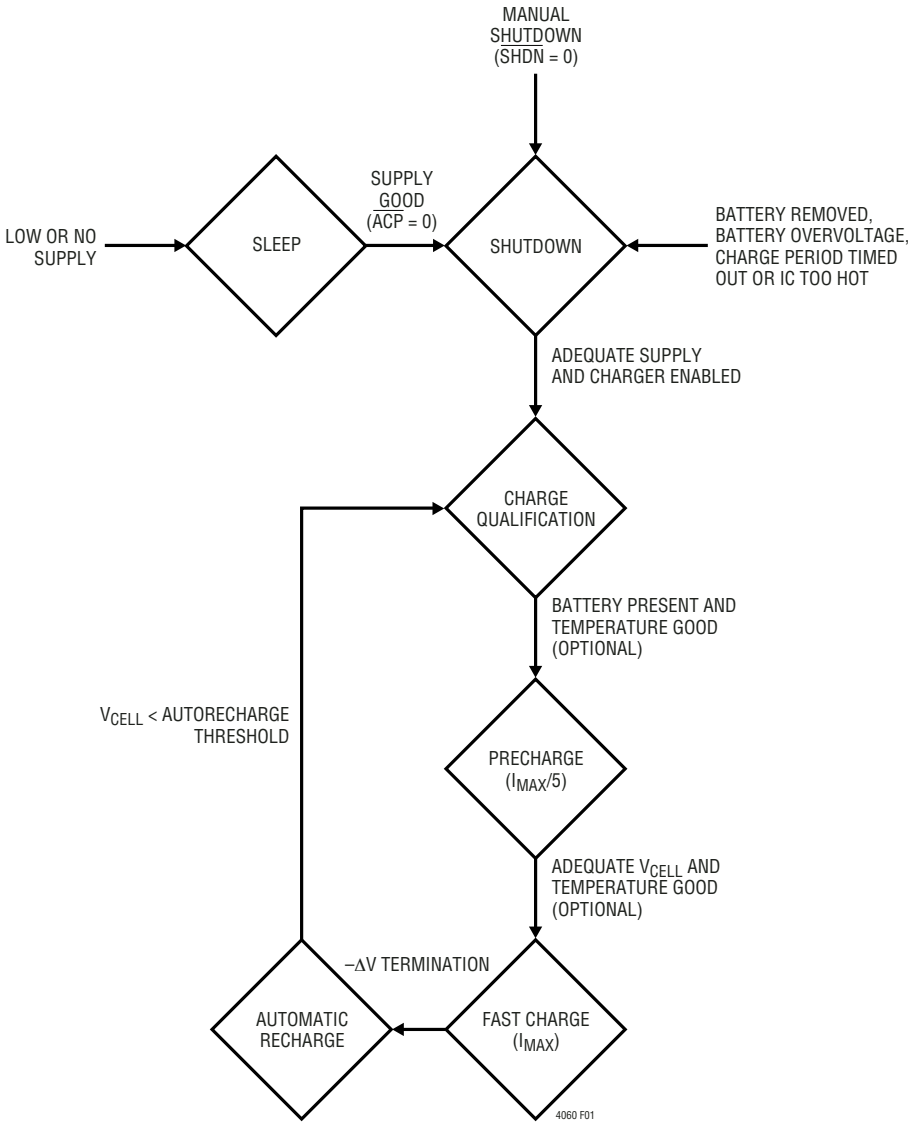


Figure 1. LTC4060 Basic State Diagram

OPERATION

The charge current is set with an external current programming resistor connected between the PROG pin and GND. In the Block Diagram, amplifier A1 will cause a virtual 1.5V to appear on the PROG pin and thus, all of the programming resistor's current will flow through the N-channel FET to the current divider. The current divider is controlled by the charger state control logic to produce a voltage across R1, appropriate either for precharge (I/5) or for fast charge (I), depending on the cell voltage. The current divider also produces a constant current I_{OSC}, that along with an external capacitor tied to the TIMER pin, sets the Oscillator's clock frequency. During charging, the external PNP transistor's collector will provide the battery charge current. The PNP's emitter current flows into the SENSE pin and through the internal current sense resistor R2 (0.03Ω). This current is slightly more than the collector current since it includes the base current. Amplifier A2 and the output driver will drive the base of the external PNP through the DRIVE pin to force the same reference voltage that appears across R1 to appear across the R2. The precision ratio between R1 and R2, along with the current programming resistor, accurately determines the charge current.

When charging begins, the charger state control logic will enable precharge of the battery. When the cell voltage exceeds the fast charge qualification threshold, fast charge begins. If the cell voltage exceeds the initial delay hold off threshold voltage just prior to precharge, then the A/D converter immediately monitors for a –ΔV event to terminate charging while in fast charge. Otherwise, the fast charge voltage stabilization hold off period must expire before the A/D converter monitors for a –ΔV event from which to terminate charging. The –ΔV magnitude for termination is selected for either NiMH or NiCd by the CHEM pin. Should the battery temperature become too hot or too cold, charging will be suspended by the charger state control logic until the temperature enters normal limits. A termination timer puts the charger into shutdown mode if the programmed time has expired. After charging has ended, the optional autorecharge detector function monitors for the battery voltage to drop to either a default or externally programmed cell voltage before automatically restarting a charge cycle.

The $\overline{SHDN}$ pin can be used to return the charger to a shutdown and reset state. The PAUSE pin can be used to pause the charge current and internal clocks for any interval desired.

Fault conditions, such as overheating of the IC due to excessive PNP base current drive, are monitored and limited by the IC overtemperature detection and output driver and current limit blocks.

When either V_{CC} is removed or manual shutdown is entered, the charger will draw only tiny leakage currents from the battery, thus maximizing standby time. With V_{CC} removed, the external PNP's base is connected to the battery by the charger. In manual shutdown, the base is connected to V_{CC} by the charger.

Undervoltage Lockout

An internal undervoltage lockout circuit (UVLO) monitors the input voltage and keeps the charger in the inactive sleep mode until V_{CC} rises above the undervoltage exit threshold. The $\overline{ACP}$ pin is high impedance while in the sleep mode and becomes low impedance to ground when in the active mode. The threshold is dependent upon the number of series cells selected by the SEL0 and SEL1 pins (see V_{UVI1-3} and V_{UVD1-3} in the Electrical Characteristics table). The UVLO circuit has a built-in hysteresis of 100mV. The thresholds are chosen to provide a minimum voltage drop of approximately 600mV between minimum V_{CC} and BAT at a battery cell voltage of 1.8V. This helps to protect against excessive saturation in the external power PNP when the supply voltage is near its minimum. While inactive the LTC4060 reduces battery current to just a negligible leakage current (I_{BSL}).

Manual Shutdown Control

The LTC4060 can be forced into a low quiescent current shutdown while V_{CC} is present by applying a low level to the $\overline{SHDN}$ pin. In manual shutdown, charging is inhibited, the internal timer is reset and oscillator disabled, $\overline{CHRG}$ status output is high impedance and $\overline{ACP}$ continues to provide the correct status. The LTC4060 will draw low current from the supply (I_{SD}), and only a negligible leakage current is applied to the battery (I_{BSD}). If a high level is

OPERATION

applied to the $\overline{SHDN}$ pin, shutdown ends and charge qualification is entered.

Charge Qualification

After exiting the sleep or shutdown modes the LTC4060 will check for the presence of a battery and for proper battery temperature (if a thermistor is used) before initiating charging.

When V_{CELL} (V_{BAT}/Number of Cells) is below 2.05V (V_{BR}), a battery is assumed to be present. Should V_{CELL} rise above 1.95V (V_{BOV}) for a time greater than the battery overvoltage event delay shown in the far right column of Table 1, then a battery overvoltage condition is detected and charging stops. Once stopped in this way, qualification can be reinitiated after V_{CELL} has fallen below 1.9V ($V_{BOV} – V_{BOVH}$) only by removing and replacing the battery (or replacing the battery if the overvoltage condition is a result of battery removal), toggling the $\overline{SHDN}$ pin low to high or removing and reapplying power to the charger.

If the NTC pin voltage is above the temperature disable threshold (V_{NDIS}), the LTC4060 verifies that the thermistor temperature is between 5°C and 45°C. Charging will not initiate until these temperature limits are met.

The LTC4060 continues to qualify important voltage and temperature parameters during all charging states. If V_{CC} drops below the undervoltage lockout threshold, sleep mode is entered.

If the internal die temperature becomes excessive, charging stops and the part enters the shutdown state. Once in the shutdown state charge qualification can be reinitiated only when the die temperature drops to normal and then by removing and replacing the battery or toggling the $\overline{SHDN}$ pin low to high or removing and reapplying power to the charger.

Precharge

The state that is entered when qualified charging begins is precharge. The $\overline{CHRG}$ status output is set low and remains low during both precharge and fast charge. If the voltage on V_{CELL} is below the 900mV (V_{FCQ}) fast charge qualification voltage, the LTC4060 charges using one-fifth the maximum programmed charge current. The cell voltage is continuously checked to determine when the battery is ready to accept a fast charge. Until this voltage reaches V_{FCQ}, the LTC4060 remains in precharge.

If an external thermistor indicates that the sensed temperature is beyond a range of 5°C to 45°C charging is suspended, the charge timer is paused and the $\overline{CHRG}$ status output remains low. Normal charging resumes from the previous state when the sensed temperature rises above 5°C or falls below 45°C.

Fast Charge

When the average cell voltage exceeds V_{FCQ}, the LTC4060 transitions from the precharge to the fast charge state and

Table 1. LTC4060 Time Limit Programming Examples

FAST CHARGE CURRENT	R_{PROG}	C_{TIMER}	TYPICAL FAST CHARGE RATE (C)	BATTERY VOLTAGE STABILIZATION HOLD OFF (MINUTES)	CHARGE TIME LIMIT (t_{MAX}) (HOURS)	BATTERY VOLTAGE SAMPLING INTERVAL (SECONDS)	AUTOMATIC RECHARGE ENTRY DELAY (SECONDS)	UVLO EXIT, BATTERY INSERTION/REMOVAL/OVERVOLTAGE, FAST CHARGE ENTRY AND THERMISTOR EVENT DELAYS (ms)
2A	698Ω	1nF	1.5	4.6 to 5.7	1.1	15	15 to 31	175 to 260
2A	698Ω	1.5nF	1	6.9 to 8.4	1.6	23	23 to 46	260 to 390
2A	698Ω	1.8nF	0.75	8.4 to 10.3	2	28	28 to 56	320 to 480
2A	698Ω	2.7nF	0.5	12.6 to 15.4	3	42	42 to 84	480 to 720
400mA	3480Ω	180pF	1.5	4.2 to 5.2	1	14	14 to 28	160 to 240
400mA	3480Ω	270pF	1	6.3 to 7.7	1.5	21	21 to 42	240 to 360
400mA	3480Ω	390pF	0.75	8.9 to 11	2.1	30	30 to 60	340 to 510
400mA	3480Ω	560pF	0.5	12.6 to 15.4	3	42	42 to 84	480 to 720

OPERATION

charging begins at the maximum current set by the external programming resistor connected between the PROG pin and GND.

If an external thermistor indicates sensed temperature is beyond a range of 5°C to 55°C charging is suspended, the charge timer is paused and the $\overline{CHRG}$ status output remains low. Normal charging resumes from the previous state when the sensed temperature rises above 5°C or falls below 45°C. Voltage-based termination (–ΔV) is then reset and immediately enabled. If voltage-based termination was imminent when the temperature limits were exceeded, charge termination will occur.

Charge Termination

Once fast charge begins and after an initial battery voltage stabilization hold-off period shown in Table 1, voltage-based termination (–ΔV) is enabled. This period is used to prevent falsely terminating on a –ΔV event that can occur almost immediately after initiating charging on some heavily discharged or stored batteries. However, if V_{CELL} was measured to be above 1.3V (V_{IDT}) immediately prior to the precharge cycle, then a mostly charged battery is assumed and voltage-based termination (–ΔV) is enabled without delay.

An internal 1.5mV resolution A/D converter measures the cell voltage after each battery voltage sampling interval indicated in Table 1. The peak cell voltage is stored and compared to the current cell voltage. When the cell voltage has dropped by at least V_{MDV} (magnitude selected by the CHEM pin) from the peak for four consecutive battery voltage sampling intervals, charging is terminated.

Back-up termination is provided by the charge time limiter, whose time limit is indicated in Table 1, and by a battery overvoltage detector. Once terminated by back-up termination, charge qualification can be reinitiated only by removing and replacing the battery or toggling the $\overline{SHDN}$ pin low to high or removing and reapplying power to the charger.

Automatic Recharge

Once charging is complete, the optional programmable automatic recharge state can be entered. This state, if enabled, will automatically restart the charger from the charge qualification state without user intervention whenever the battery cell voltage drops below a set level. With the advent of low memory effect NiMH and improved NiCd cells an automatic recharge feature is practical and eliminates the need for very slow trickle charging.

The $\overline{CHRG}$ status output is high impedance in the automatic recharge state until charging begins. If the V_{CELL} voltage drops below the voltage set on the ARCT pin for at least the automatic recharge entry delay time as shown in Table 1, the charge qualification state is entered and charging will begin anew in fast charge. An easy way of setting the voltage on the ARCT pin is by using two series current programming resistors and connecting their common to the ARCT pin as shown in Figure 2. The PROG pin will provide a constant 1.5V (V_{PROG}). The programmable voltage range of the ARCT pin is approximately 0.8V to 1.6V. A preprogrammed recharge threshold of 1.3V (V_{ARDT}) is selected when the ARCT pin is connected to V_{CC} (V_{ARDEF}). Automatic recharge is disabled when the ARCT pin is connected to ground (V_{ARDIS}).

Pause

After charging is initiated, the PAUSE pin may be used to pause operation at any time. Whenever the voltage on the PAUSE pin is a logic high, the charge timer and all other timers pause, charging is stopped and the fast charge termination algorithm is inhibited. The $\overline{CHRG}$ status output remains at GND. If voltage-based termination was imminent before pause, charge termination will occur. Otherwise, when pause ends, the charge timer and all other timers resume timing, charging restarts and voltage-based termination (–ΔV) is reset and immediately enabled. If the battery is removed while the PAUSE pin is a logic high, then battery removal is detected and shutdown is entered. If the battery is replaced while the PAUSE pin is a logic high, it will not be detected until pause is turned off.

For pause periods or a series of periods where the battery capacity could be significantly depleted, consider using shutdown instead of pause to avoid having the safety timer expire before the battery can be fully charged. Shutdown resets the safety timer.

OPERATION

Battery Chemistry Selection

The desired battery chemistry is selected by programming the CHEM pin to the proper voltage. When wired to GND, a set of parameters specific to charging NiMH cells is selected. When CHEM is connected to V_{CC}, charging is optimized for NiCd cells. The various charging parameters are detailed in Table 2.

Cell Selection

The number of series cells is selected using the SEL0 and SEL1 pins. For one cell, both pins connect to GND. For two cells, SEL0 connects to V_{CC} and SEL1 to GND. For three cells, SEL0 connects to GND and SEL1 to V_{CC}. For four cells, both connect to V_{CC}.

Insertion and Removal of Batteries

The LTC4060 automatically senses the insertion or removal of a battery by monitoring the V_{CELL} pin voltage. Either the charge current, or if not charging then an internal pull-up current (I_{BRD}), will pull V_{CELL} up when the battery is removed. When this voltage rises above 2.05V (V_{BR}) for a time greater than the battery removal event delay shown in Table 1, the LTC4060 considers the battery to be absent. Inserting a battery, causing V_{CELL} to fall below both V_{BR} and 1.95V (V_{BOV}) for a period longer than the battery insertion event delay shown in Table 1, results in the LTC4060 recognizing a battery present and initiates a completely new charge cycle beginning with charge qualification. All battery currents are inhibited while in shutdown.

Table 2. LTC4060 Charging Parameters

STATE	CHEM	CHARGE TIME LIMIT	T_{MIN}	T_{MAX}	I_{CHRG}	TYPICAL TERMINATION CONDITION
Precharge	Both	t_{MAX}	5°C	45°C	$I_{MAX}/5$	$V_{CELL} \geq 0.9V$
Fast Charge	NiCd	t_{MAX}	5°C	55°C	I_{MAX}	–16mV Per Cell After Initial $t_{MAX}/12$ Delay
	NiMH	t_{MAX}	5°C	55°C	I_{MAX}	–8mV Per Cell After Initial $t_{MAX}/12$ Delay

APPLICATIONS INFORMATION

Programming Charge Current

The battery charge current is set with an external program resistor connected from the PROG pin to GND. The formula for the battery fast charge current or I_{MAX} is:

$$I_{MAX} = (I_{PROG}) \bullet 930 = \left(\frac{1.5V}{R_{PROG}}\right) \bullet 930$$

or

$$R_{PROG} = \frac{1395}{I_{MAX}}$$

where R_{PROG} is the total resistance from the PROG pin to ground. For example, if 1A of fast charge current is required:

$$R_{PROG} = \frac{1395}{1A} = 1.4k\ 1\%\ \text{Resistor}$$

Under precharge conditions, the current is reduced to 20% of the fast charge value (I_{MAX}).The LTC4060 is designed for a maximum current of 2A. This translates to a maximum PROG pin current of 2.15mA and a minimum program resistor of 698Ω. Reduced accuracy at low current limits the useful fast charge current to a minimum of approximately 200mA. Errors in the charge current can be statistically approximated as follows:

One Sigma Error ≅ 7mA

For best stability over temperature and time, 1% metal-film resistors are recommended. Capacitance on the PROG pin should be limited to about 75pF to insure adequate AC phase margin for its amplifier.

Different charge currents can be programmed by various means such as by switching in different program resistors. A voltage DAC connected through a resistor to the PROG pin or a current DAC connected in parallel with a

APPLICATIONS INFORMATION

resistor to the PROG pin can also be used to program current. Note that this will alter the timer periods unless alternate TIMER pin capacitors are also programmed through an analog switch.

The PROG pin provides a reference voltage of 1.5V (V_{PROG}) that may be tapped for system use. Current loading on PROG is multiplied by 930 and appears as increased I_{MAX}. This may be compensated by adjustment of R_{PROG}. Total PROG pin current must be limited to 2.3mA otherwise absolute maximum ratings will be exceeded. When the LTC4060 is in the shutdown mode, the PROG pin is forced to ground potential to save power.

Programming the Timer

All LTC4060 internal timing is derived from the internal oscillator that is programmed with an external capacitor at the TIMER pin. The time periods shown in Table 1 scale directly with the timer period. The programmable safety timer is used to put a time limit on the entire charge cycle for the case when charging has not otherwise terminated.

The time limit is programmed by an external capacitor at the TIMER pin and is also dependent on the current set by the programming resistor connected to the PROG pin. The time limit is determined by the following equation:

$$t_{MAX}\ (\text{Hours}) = 1.567 \bullet 10^6 \bullet R_{PROG}\ (\Omega) \bullet C_{TIMER}\ (\text{F})$$

$$C_{TIMER}\ (\text{F}) = \frac{t_{MAX}\ (\text{Hours})}{1.567 \bullet 10^6 \bullet R_{PROG}\ (\Omega)}$$

Some typical timing values are detailed in Table 1. The timer begins at the start of a charge cycle. After the time-out occurs, the charge current stops and the $\overline{CHRG}$ output assumes a high impedance state to indicate that the charging has stopped.

Excessively short time-out periods may not allow enough time for the battery to receive full charge or may result in premature $-\Delta V$ termination due to too short a battery voltage stabilization hold-off period. Excessively long time-out periods may indicate too low a charge current which may not allow voltage-based termination ($-\Delta V$) to work properly. Time-out limits of less than 0.75 hour for faster 2C charge rates, or more than 3.5 hours for slower C/2 charge rates, are generally not recommended. Consult the battery manufacturer for recommended periods.

An external timing source can also be used to drive the TIMER pin for precise or programmed control. The high level must be between 2.5V and V_{CC} and the low level must be between 0V and 0.25V. Also, the driving source must be able to overdrive the internal current source and sink which is 5% of the current through R_{PROG}.

Battery Temperature Sensing

Temperature sensing is optional in LTC4060 applications. To disable temperature qualification of all charging operations, the NTC pin must be wired to ground. A circuit for temperature sensing using a thermistor with a negative temperature coefficient (NTC) is shown in Figure 2. Internally derived V_{CC} proportional voltages (V_{CLD}, V_{HTI}, V_{HTC}) are compared to the voltage on the NTC input pin to test the temperature thresholds. The battery temperature is measured by placing the thermistor close to the battery pack. In Figure 2, a common 10k NTC thermistor such as a Murata NTH4G series NTH4G39A103F can be used. R_{HOT} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 45°C ($V_{NTC} = V_{HTI} = 0.5 \bullet V_{CC}$ typ). Another temperature may be chosen to suit the battery requirements. The LTC4060 will not initiate a charge cycle or continue with a precharge if the value of the thermistor falls below 4.42k which is a temperature rising to approximately 45°C. However, once fast charging is in progress, it will not be stopped until the thermistor drops below 3k which is a temperature rising to approximately 55°C ($V_{NTC} = V_{HTC} = 0.4 \bullet V_{CC}$ typ). Once reaching this charge cutoff threshold, charging is suspended until the value of the thermistor rises above approximately 4.8k (falling temperature) or approximately 43°C (45°C – 2°C hysteresis at V_{CC} = 5V) and then charging is resumed. Hysteresis avoids possible oscillation about the trip points. Note that the comparator hysteresis voltages are constant and when V_{CC} increases the signal level from the thermistor increases thus making the temperature hysteresis look smaller.

During suspension the charge current is turned off and the safety timer is frozen. The LTC4060 is also designed to suspend when the thermistor rises above 34k (falling

APPLICATIONS INFORMATION

temperature) at approximately 0°C (5°C – 5°C hysteresis at V_{CC} = 5V) and then resume when the thermistor falls below 27k (rising temperature) which will be approximately 5°C (V_{NTC} = V_{CLD} = 0.86 • V_{CC} typ).

Many thermistors with an R_{COLD} to R_{HOT} ratio of approximately 7 will work. For lower power dissipation higher values of thermistor resistance can be used. The Murata NTH4G series offers resistances of up to 100k at 25°C.

It is important that the thermistor be placed in close contact with the battery and away from the external PNP pass transistor to avoid excessive temperature errors on the sensed battery temperature. Furthermore, since V_{CC} is a high current path into the LTC4060, it is essential to minimize voltage drops between the V_{CC} supply pin and the top of R_{HOT} by Kelvin connecting R_{HOT} directly to the V_{CC} pin.

Power Requirements

The DC power input to the V_{CC} pin must always be within proper limits while charging a battery. Voltages beyond the absolute maximum ratings may damage the charger and voltages falling below the UVLO entry thresholds, as programmed by the SEL0 and SEL1 pins, will likely cause the charger to enter the shutdown state (when the UVLO exit threshold is exceeded charging will begin anew). While the LTC4060 is designed to reject 60Hz or 120Hz supply ripple, certain precautions are required. The instantaneous ripple voltage must always be within the above mentioned limits. Ripple voltage seen across the collector-base junction of the external PNP pass transistor will slightly modulate its beta and hence its base current. Since the emitter current is precisely regulated by the LTC4060, any modulation of base current will appear at the collector. This slightly modulated battery charge current into a battery will usually produce an insignificant modulation voltage at the battery. However, if excessive wire impedance to the battery from the PNP exists, then it may be helpful to Kelvin connect the BAT pin to a convenient point closest to the battery to reduce ripple magnitude entering the LTC4060's battery monitoring circuits. The battery ground impedance should also be managed to limit ripple voltage at the BAT pin. Excessive ripple into the BAT pin may cause the charger to deviate from specified performance.

V_{CC} Bypass Capacitor

A 1µF capacitor located close to the LTC4060 will usually provide adequate input bypassing. However, caution must be exercised when using multilayer ceramic capacitors. Because of the self-resonance and high Q characteristics of some types of ceramic capacitors, along with wiring inductance, high voltage transients can be generated under some conditions such as connecting or disconnecting a supply input to a hot power source. To reduce the Q and prevent these transients from exceeding the absolute maximum voltage rating, consider adding about 1Ω of resistance in series with the ceramic input capacitor.

BAT Bypass Capacitor

This optional capacitor, connected between BAT and GND, can be used to help filter excessive contact bounce during the battery monitoring or charging process. The value will depend upon the contact bounce open duration, but is typically 10µF. Another purpose of this capacitor is to bypass transient battery load events that might otherwise disrupt monitoring or charging. Should the battery connections not be subject to excessive contact bounce or excessive battery voltage transients, then no BAT pin capacitor is required. The same caution mentioned above for the V_{CC} bypass capacitor applies.

External PNP Transistor

The external PNP pass transistor must have adequate beta and breakdown voltages, low saturation voltage and sufficient power dissipation capability that may include heat sinking.

To provide 2A of charge current with the minimum available base current drive of 40mA (I_{DRV} min) requires a minimum PNP beta of 50.

The transistor's collector to emitter breakdown voltage must be high enough to withstand the difference between the maximum supply voltage and minimum battery voltage. Almost any transistor will meet this requirement. Additionally, when no power is supplied to the charger (V_{IN} = 0V and V_{SENSE} = 0V), the transistor's emitter to base breakdown voltage must be high enough to prevent a leakage path at the maximum battery voltage while not

APPLICATIONS INFORMATION

charging (the DRIVE pin is internally switched to the BAT pin). Most transistors will meet this requirement as well.

With low supply voltages, the PNP saturation voltage (V_{CESAT}) becomes important. The V_{CESAT} must be less than the minimum supply voltage minus the maximum voltage drop across the internal current sense resistor and bond wires (approximately 0.08Ω) and maximum battery voltage presented to the charger accounting for wire I • R drops.

$$V_{CESAT}(V) < V_{DD(MIN)} - (I_{BAT(MAX)} \bullet 0.08\Omega + V_{BAT(MAX)})$$

For example, if it were desired to have a programmed charge current of 2A with a minimum supply voltage of 4.75V and a maximum battery voltage of 3.6V (2 series cells at 1.8V each), then the minimum operating V_{CESAT} is:

$$V_{CESAT}(V) = 4.75 - (2 \bullet 0.08 + 3.6) = 0.99V$$

If the PNP transistor cannot achieve the saturation voltage required, base current will dramatically increase. This is to be avoided for a number of reasons: DRIVE pin current may reach current limit resulting in the LTC4060 characteristics going out of specifications, excessive power dissipation may force the IC into thermal shutdown, or the battery could discharge because some of the current from the DRIVE pin could be pulled from the battery through the forward biased PNP collector base junction.

The actual battery fast charge current (I_{BAT}) is slightly less than the regulated charge current because the charger senses the emitter current and the battery charge current will be reduced by the base current. In terms of β (I_C/I_B) I_{BAT} can be calculated as follows:

$$I_{BAT}(A) = 930 \bullet I_{PROG}\left(\frac{\beta}{\beta + 1}\right)$$

If β = 100 then I_{BAT} is 1% low. The 1% loss can be easily compensated for by increasing I_{PROG} by 1%.

Another important factor to consider when choosing the PNP pass transistor is its power handling capability. The transistor's data sheet will usually give the maximum rated power dissipation at a given ambient temperature with a power derating for elevated temperature operation. The maximum power dissipation of the PNP when charging is:

$$P_{D(MAX)}(W) = I_{MAX}(V_{DD(MAX)} - V_{BAT(MIN)})$$

$V_{DD(MAX)}$ is the maximum supply voltage and $V_{BAT(MIN)}$ is the minimum battery voltage when discharged, but not less than 0.9V/cell since less than 0.9V/cell invokes precharge current levels.

Thermal Considerations

Internal overtemperature protection is provided to prevent excessive LTC4060 die temperature during a fault condition. If the internal die temperature exceeds approximately 145°C, charging stops and the part enters the shutdown state. The faults can be generated from insuffient heat sinking, a shorted DRIVE pin or from excessive DRIVE pin current to the base of an external PNP transistor if it's in deep saturation from a very low V_{CE}. Once in the shutdown state, charge qualification can be reinitiated only by removing and replacing the battery or toggling the $\overline{SHDN}$ pin low to high or removing and reapplying power to the charger. This protection is not designed to prevent overheating of the PNP pass transistor. Indirectly though, self-heating of the PNP thermally conducting to the LTC4060 can result in the IC's junction temperature rising above 145°C, thus cutting off the PNP's base current. This action will limit the PNP's junction temperature to some temperature well above 145°C. The user should insure that the maximum rated junction temperature is not exceeded under any normal operating condition. See Package/Order Information for the θ_{JA} of the LTC4060 Exposed Pad packages. The actual thermal resistance in the application will vary depending on forced air cooling, use of the Exposed Pad and other heat sinking means, especially the amount of copper on the PCB to which the LTC4060 is attached. The majority of the power dissipated within the LTC4060 is in the current sense resitor and DRIVE pin driver as given below:

$$P_D = (I_{BAT})^2 \bullet 0.08 + I_{DRIVE}(V_{CC} - V_{EB})$$

$$T_J = T_A + \theta_{JA} \bullet P_D$$

V_{EB} is the emitter to base voltage of the external PNP.

TYPICAL APPLICATIONS

Full Featured 2A Charger Application

Figure 2 shows an application that utilizes the optional temperature sensing and optional externally programmable automatic recharge features. It also has LEDs to indicate charging status and the presence of sufficient input supply voltage.

The PROG pin has a total resistance of 691Ω to ground that programs the fast-charge current at the PNP's emitter to 2.02A (2A at the collector for beta of 100). The ARCT pin voltage is programmed to 1.25V. When the battery cell voltage falls below this automatic recharge will begin. Optional capacitor C_{BAT} filters excessive contact bounce. This circuit can be modified to charge a 4A-Hr battery at a C/2 rate simply by doubling the C_{TIMER} capacitance.

Power Path Control

Proper power path control is an important consideration when fast charging nickel cells. This control ensures the system load remains powered at all times, but that normal system operation and associated load transients do not adversely affect the charging procedure. Figure 3 illustrates a 1A charger with power path control. When V_{IN} is applied the forward biased Schottky diode will power the load while the P-channel FET will disconnect the battery from the load. When V_{IN} is removed, the FET will turn-on to provide a low loss switch from the battery to the load, and the diode will isolate V_{IN}. The $\overline{ACP}$ output signals the presense of V_{IN}.

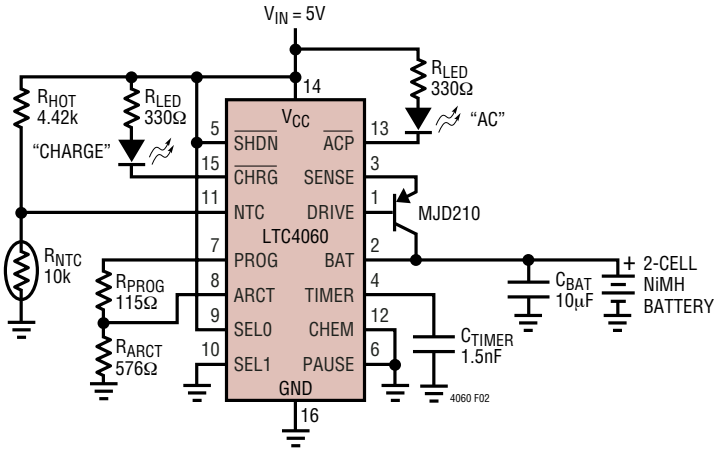


Figure 2. Full Featured 2A Charger Application

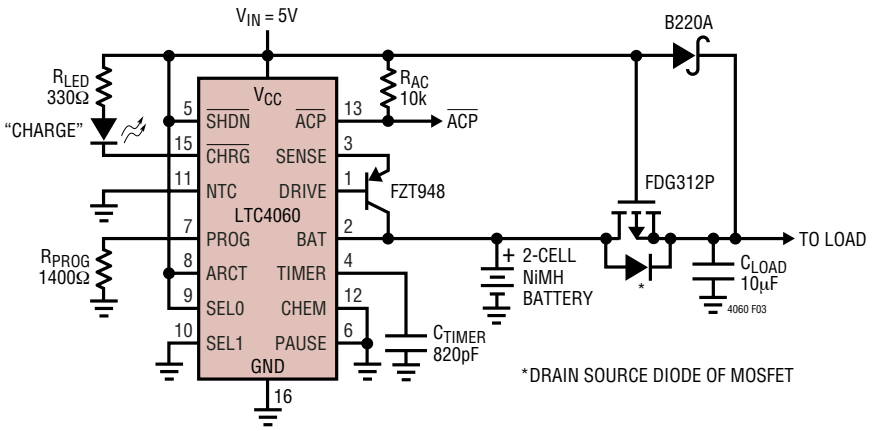


Figure 3. 1A Charger Application with Power Path Control

TYPICAL APPLICATIONS

Trickle Charge

The trickle charge function is normally not required due to the automatic recharge feature. However, the LTC4060 does provide a modest pull-up current (I_{BRD}) as part of its battery removal detection method. If additional current is required for trickle charge or to support battery removal detection with current loads greater than I_{BRD}, then the simple circuit of Figure 4 will facilitate that. The diode insures no reverse discharge current when V_{IN} is removed and the resistor sets the trickle current.

Extending Charge Current

Extending the charge current beyond 2A can be accomplished by paralleling an external current sense resistor, R_{ISET}, with the internal current sense resistor as shown in Figure 5. Bond wire, lead frame and PCB interconnect resistance and mismatches in the two sense resistor's value will cause charge current variability to increase in proportion to the extension in current. Resistor R_{ISET} should be connected directly to the LTC4060 to reduce errors. The total current sense resistor, bond wire and lead frame resistance is approximately 0.08Ω (T.C. ≅ 3500ppm/°C). The formula for extended fast charge current is:

$$I_{MAX(EXT)} = I_{MAX} \bullet \left(1 + \frac{0.08}{R_{ISET}}\right)$$

$$= 2A \bullet 1.5 = 3A$$

for R_{ISET} = 0.16Ω and R_{PROG} = 698Ω.

Adequate PNP beta is required to meet the DRIVE pin capability and the increased PNP power dissipation will require additional heat sinking.

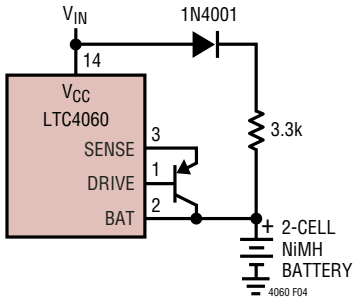


Figure 4. Adding Trickle Charge

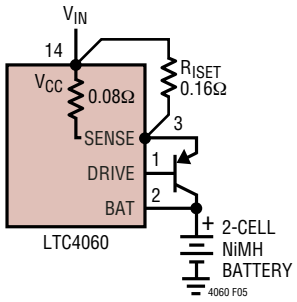
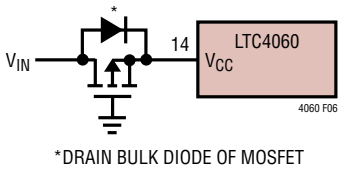


Figure 5. Extended Charge Current Operation

TYPICAL APPLICATIONS

Reverse Input Voltage Protection

In some applications protection from reverse supply voltage is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases, where the voltage drop must be kept very low, a P-channel FET as shown in Figure 6 can be used.

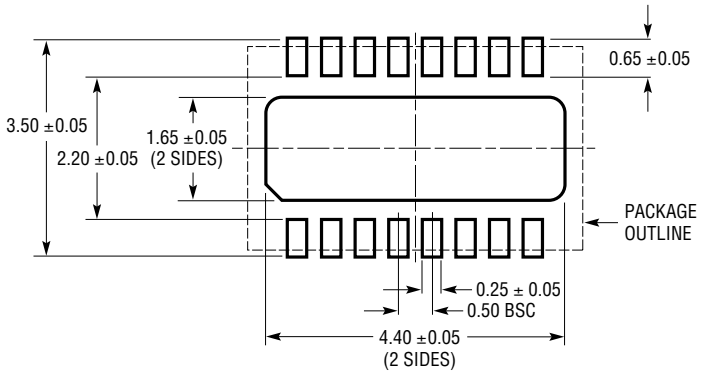


*DRAIN BULK DIODE OF MOSFET

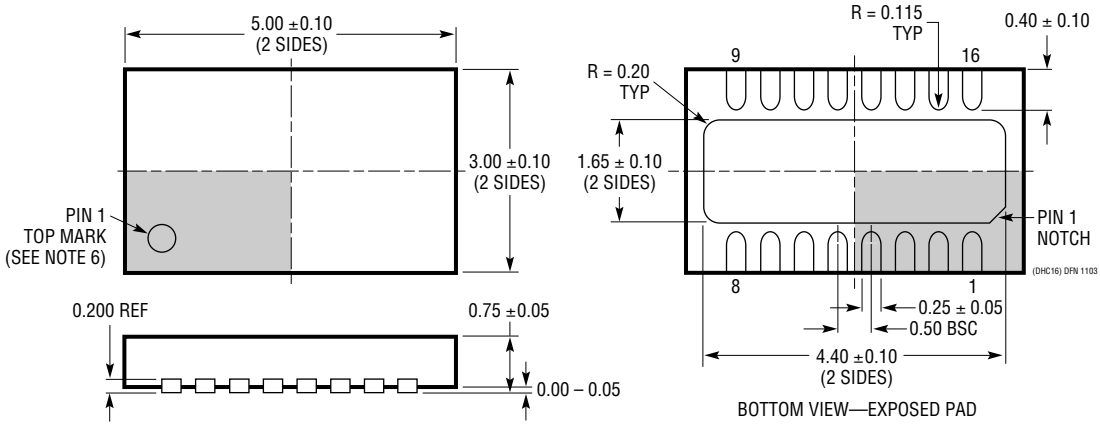
Figure 6. Low Loss Reverse Input Voltage Protection

PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE