USB Power Controller and Li-Ion Linear Charger with Low Loss Ideal Diode

FEATURES

- **Seamless Transition Between Input Power Sources: Li-Ion Battery, USB and 5V Wall Adapter**
- **Low Loss (50mΩ) Ideal Diode Path from BAT to OUT**
- **Programmable Charge Current Detection ($\overline{CHRG}$)**
- **Load Dependent Charging Guarantees USB Input Current Compliance**
- **Analog Gas Gauge Function**
- Charges Single Cell Li-Ion Batteries Directly from USB Port
- Constant-Current/Constant-Voltage Operation with Thermal Feedback to Maximize Charging Rate Without Risk of Overheating*
- Selectable 100% or 20% Current Limit (e.g., 500mA/100mA)
- Termination Timer Adapts to Actual Charge Current
- Preset 4.2V Charge Voltage with 0.8% Accuracy (4.1V for LTC4066-1)
- NTC Thermistor Input for Temperature Qualified Charging
- Thin Profile (0.75mm) 24-Lead 4mm × 4mm QFN Package
- Ultrathin Profile (0.55mm) 24-Lead 4mm × 4mm UTQFN Package (LTC4066 Only)

APPLICATIONS

- Portable USB Devices
- GPS, Cameras, Broadband Wireless Modems
- Mulitple Input Chargers

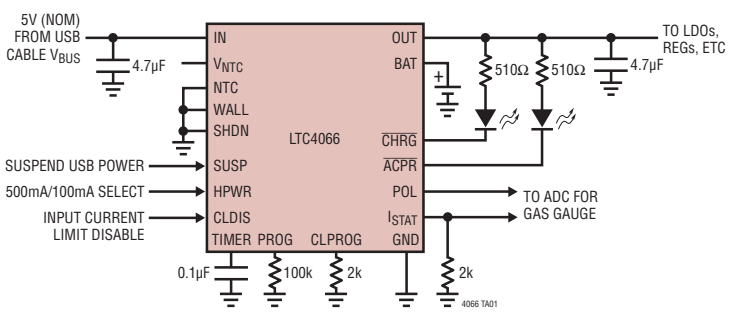
DESCRIPTION

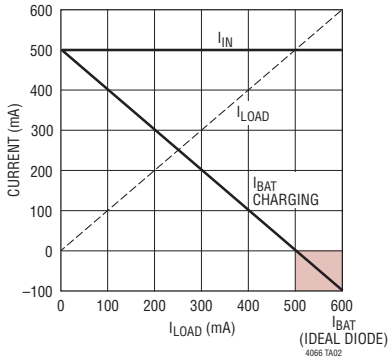
The LTC®4066/LTC4066-1 are USB power managers and Li-Ion battery chargers designed to work in portable battery-powered applications. The parts control the total current used by the USB peripheral for operation and battery charging. The total input current can be limited to 100mA, 500mA or "unlimited" (i.e., above 2A). Battery charge current is automatically reduced such that the sum of the load current and the charge current does not exceed the programmed input current limit.

The LTC4066/LTC4066-1 include a standalone constant-current/constant-voltage linear charger for single cell Li-ion batteries. The float voltage applied to the battery is held to a tight 0.8% tolerance, and charge current is programmable using an external resistor to ground. A programmable end-of-charge status output ($\overline{CHRG}$) indicates full charge. BAT pin charge and discharge currents can be monitored via an analog output (I_{STAT}). Total charge time is programmable by an external capacitor to ground. When the battery drops 100mV below the float voltage, automatic recharging of the battery occurs. Also featured is an NTC thermistor input used to monitor battery temperature while charging.

The LTC4066/LTC4066-1 are available in a 24-pin thin profile (0.75mm) 4mm×4mm QFN package. The LTC4066 is also available in a 24-pin ultrathin profile (0.55mm) 4mm × 4mm UTQFN package.

TYPICAL APPLICATION





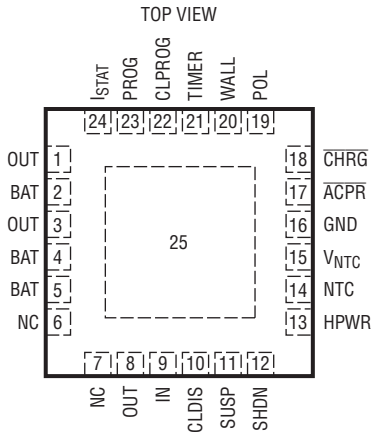
ABSOLUTE MAXIMUM RATINGS (Notes 1 to 6)

Terminal Voltage
- t < 1ms and Duty Cycle < 1%
- IN, OUT ..... –0.3V to 7V
- Steady State
- IN, OUT, BAT ..... –0.3V to 6V
- NTC, V_{NTC}, TIMER, PROG, CLPROG, I_{STAT} ..... –0.3V to (V_{CC} + 0.3V)
- $\overline{CHRG}$, HPWR, SUSP, SHDN, WALL, $\overline{ACPR}$, POL, CLDIS ..... –0.3V to 6V

Pin Current (DC)
- IN (Note 7) 2.7A
- OUT, BAT (Note 7) 5A

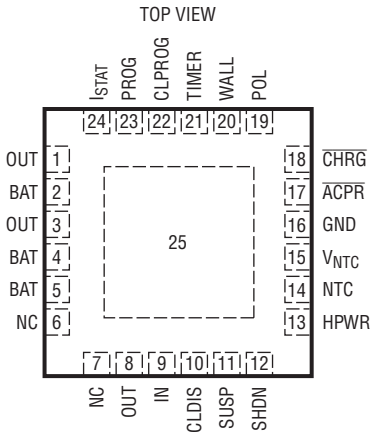
Operating Temperature Range ..... –40°C to 85°C
Maximum Operating Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN #) IS GND, MUST BE SOLDERED TO PCB



PF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC UTQFN

T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN #) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4066EUF#PBF	LTC4066EUF#TRPBF	4066	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC4066EUF-1#PBF	LTC4066EUF-1#TRPBF	40661	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC4066EPF#PBF	LTC4066EPF#TRPBF	4066T	24-Lead (4mm × 4mm) Plastic UTQFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{BAT} = 3.7V, HPWR = 5V, WALL = 0V, R_{PROG} = 100k, R_{CLPROG} = R_{ISTAT} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Voltage	IN and OUT	●	4.35		5.5	V
V_{BAT}	Input Voltage	BAT	●			4.3	V
I_{IN}	Input Supply Current	I_{BAT} = I_{ISTAT} = 0 (Note 8) Suspend Mode; SUSP = 2V Suspend Mode; SUSP = 2V, Wall = 2V, V_{OUT} = 4.8V Shutdown; SHDN = 2V	● ● ● ●		0.5 50 50 10	1.2 100 100 20	mA µA µA µA
I_{OUT}	Output Supply Current	V_{OUT} = 5V, V_{IN} = 0V, V_{BAT} = 4.3V, TIMER = 0V	●		400	800	µA
BAT	Battery Drain Current	V_{BAT} = 4.3V, Charging Stopped Suspend Mode; SUSP = 2V Shutdown; SHDN = 2V V_{IN} = 0V, BAT Powers OUT, No Load	● ● ● ●		15 15 2.5 55	27 27 5 100	µA µA µA µA
$I_{IN(MAX)}$	Maximum Input Current Limit	(Note 9)		1.9	2.6		A
V_{UVLO}	Input or Output Undervoltage Lockout	V_{IN} Powers Part, Rising Threshold V_{OUT} Powers Part, Rising Threshold	● ●	3.6 3.6	3.8 3.8	4 4	V V
ΔV_{UVLO}	Input or Output Undervoltage Lockout	V_{IN} Rising – V_{IN} Falling or V_{OUT} Rising – V_{OUT} Falling			125		mV
Current Limit							
I_{LIM}	Current Limit	R_{CLPROG} = 2k, HPWR = 5V R_{CLPROG} = 2k, HPWR = 0V	● ●	475 90	500 100	525 110	mA mA
R_{ON}	ON Resistance V_{IN} to V_{OUT}	HPWR = 5V, 400mA Load HPWR = 0V, 80mA Load			0.16 0.16		Ω Ω
V_{CLPROG}	CLPROG Pin Voltage	R_{CLPROG} = 2k R_{CLPROG} = 1k	●	0.980 0.980	1.000 1.000	1.020 1.020	V V
I_{SS}	Soft-Start Inrush Current	IN or OUT			10		mA/µs
V_{ALEN}	Automatic Current Limit Enable Threshold Voltage	(V_{IN} – V_{OUT}) V_{IN} Rising (V_{IN} – V_{OUT}) V_{IN} Falling		25 –85	50 –60	75 –25	mV mV
Battery Charger							
V_{FLOAT}	Regulated Output Voltage	(0°C to 85°C), I_{BAT} = 2mA I_{BAT} = 2mA	 ●	4.165 4.158	4.200 4.200	4.235 4.242	V V
		(0°C to 85°C), I_{BAT} = 2mA (LTC4066-1) I_{BAT} = 2mA (LTC4066-1)	 ●	4.066 4.059	4.100 4.100	4.134 4.141	V V
I_{BAT}	Current Mode Charge Current	R_{PROG} = 100k, No Load R_{PROG} = 50k, No Load	● ●	460 920	500 1000	540 1080	mA mA
$I_{BAT(MAX)}$	Maximum Charge Current	(Note 9)			1.5		A
V_{PROG}	PROG Pin Voltage	R_{PROG} = 100k R_{PROG} = 50k	● ●	0.980 0.980	1.000 1.000	1.020 1.020	V V
k_{ISTAT}	Ratio of I_{BAT} (Charging) to I_{STAT} Pin Current	I_{BAT} = 50mA I_{BAT} = 100mA I_{BAT} = 500mA I_{BAT} = 1000mA	● ● ● ●	875 900 925 950	1000 1000 1000 1000	1125 1100 1075 1050	mA/mA mA/mA mA/mA mA/mA
V_{EOC}	End-of-Charge I_{STAT} Pin Voltage	V_{BAT} = V_{FLOAT} (4.2V, 4.1V for LTC4066-1)	●	94	100	106	mV
I_{TRIKL}	Trickle Charge Current	V_{BAT} = 2V, R_{PROG} = 100k		35	50	60	mA
V_{TRIKL}	Trickle Charge Threshold Voltage		●	2.8	2.9	3	V
V_{CEN}	Charger Enable Threshold Voltage	(V_{OUT} – V_{BAT}) High to Low, V_{BAT} = 4V (V_{OUT} – V_{BAT}) Low to High, V_{BAT} = 4V			60 90		mV mV
V_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT} – V_{RECHRG}	●	60	100	130	mV
t_{TIMER}	TIMER Accuracy	V_{BAT} = 4.2V (4.1V for LTC4066-1)		–10		10	%
	Recharge Time	Percent of Total Charge Time			50		%
	Low-Battery Trickle Charge Time	Percent of Total Charge Time, V_{BAT} < 2.8V			25		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_{BAT} = 3.7V, HPWR = 5V, WALL = 0V, R_{PROG} = 100k, R_{CLPROG} = R_{ISTAT} = 2k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
T_{LIM}	Junction Temperature in Constant Temperature Mode				105		°C
Ideal Diode							
R_{FWD}	Incremental Resistance, V_{ON} Regulation	I_{BAT} = 500mA			27		mΩ
$R_{DIO(ON)}$	On-Resistance V_{BAT} to V_{OUT}	I_{BAT} = 3A			45		mΩ
V_{FWD}	Voltage Forward Drop (V_{BAT} – V_{OUT})	I_{BAT} = 5mA I_{BAT} = 200mA I_{BAT} = 2A	●	10	30 47 95	50	mV mV mV
$k_{DIO,ISTAT}$	Ratio of I_{BAT} (Discharging Through Ideal Diode) to I_{STAT} Pin Current	I_{BAT} = 5mA I_{BAT} = 20mA		850 850	1000 1000	1150 1150	mA/mA mA/mA
V_{OFF}	Diode Disable Battery Voltage				2.8		V
I_{FWD}	Load Current Limit for V_{ON} Regulation	V_{BAT} = 3.5V			2.5		A
$I_{D(MAX)}$	Diode Current Limit			3.8	5.2		A
Logic							
V_{OL}	Output Low Voltage ($\overline{CHRG}$, $\overline{ACPR}$, POL)	I_{SINK} = 5mA	●		0.1	0.25	V
V_{IH}	Enable Input High Voltage	SUSP, SHDN, HPWR, CLDIS Pin	●	1.2			V
V_{IL}	Enable Input Low Voltage	SUSP, SHDN, HPWR, CLDIS Pin	●			0.4	V
I_{PULLDN}	Logic Input Pull-Down Current	SUSP, SHDN, HPWR, CLDIS			2		µA
$V_{CHG,SD}$	Charger Shutdown Threshold Voltage on TIMER		●	0.15		0.4	V
$I_{CHG,SD}$	Charger Shutdown Pull-Up Current on TIMER	V_{TIMER} = 0V	●	2	4		µA
V_{WALL}	Wall Input Threshold Voltage	V_{WALL} Rising Threshold	●	1.200	1.225	1.250	V
$V_{WALL,HYS}$	Wall Input Hysteresis	V_{WALL} Rising – V_{WALL} Falling Threshold			35		mV
I_{WALL}	Wall Input Leakage Current	V_{WALL} = 1V			0	±50	nA
NTC							
I_{VNTC}	V_{NTC} Pin Current	V_{VNTC} = 2.5V		1.5	2.5	3.5	mA
V_{VNTC}	V_{NTC} Bias Voltage	I_{VNTC} = 500µA	●	4.4	4.85		V
I_{NTC}	NTC Input Leakage Current	V_{NTC} = 1V			0	±1	µA
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis			0.74 • V_{VNTC} 0.02 • V_{VNTC}		V V
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis			0.29 • V_{VNTC} 0.01 • V_{VNTC}		V V
V_{DIS}	NTC Disable Voltage	NTC Input Voltage to GND (Falling) Hysteresis	●	75	100 35	125	mV mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: V_{CC} is the greater of V_{IN}, V_{OUT} or V_{BAT}.

Note 3: Pins 1, 3 and 8 (OUT) should be tied together with a low impedance to ensure that the difference between the three pins does not exceed 50mV. Pins 2, 4 and 5 (BAT) should be tied together with a low impedance to ensure that the difference between the three pins does not exceed 50mV.

Note 4: All voltage values are with respect to GND.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: The LTC4066/LTC4066-1 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

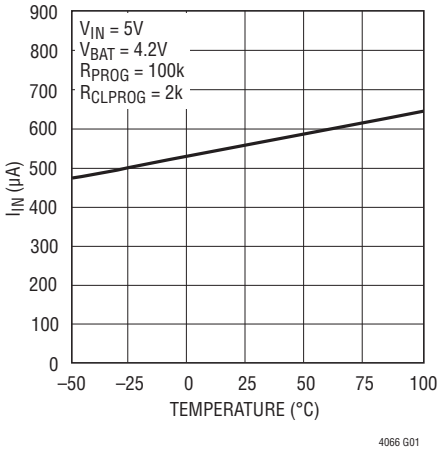
Note 7: Guaranteed by long term current density limitations.

Note 8: Total input current is equal to this specification plus 1.003 × I_{BAT} where I_{BAT} is the charge current.

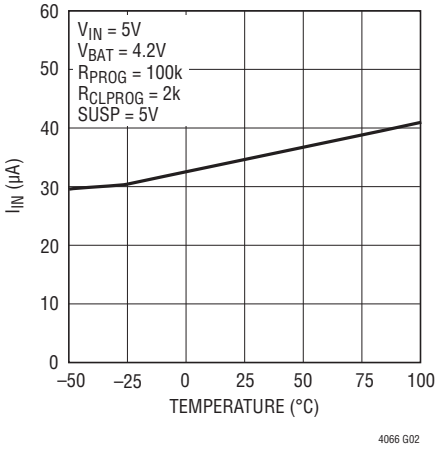
Note 9: Accuracy of programmed current may degrade for currents greater than 1.5A.

TYPICAL PERFORMANCE CHARACTERISTICS

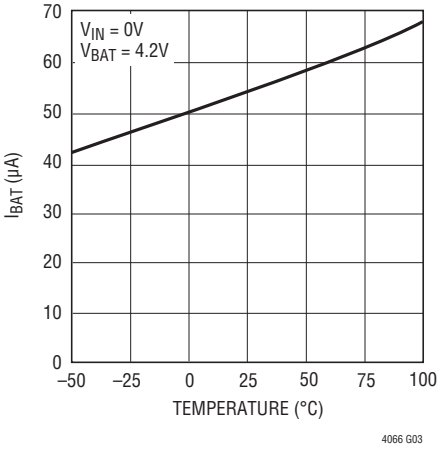
Input Supply Current vs Temperature



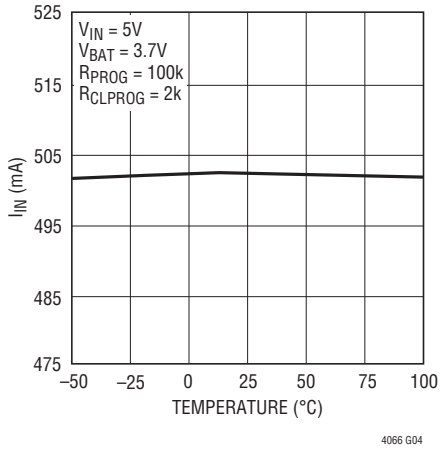
Input Supply Current vs Temperature (Suspend Mode)



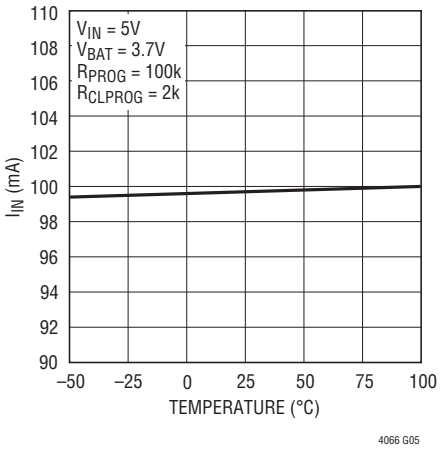
Battery Drain Current vs Temperature (BAT Powers OUT, No Load)



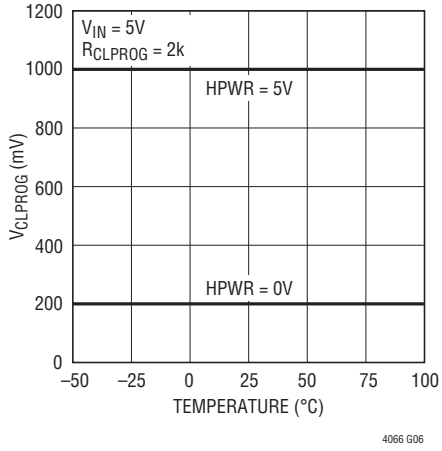
Input Current Limit vs Temperature, HPWP = 5V



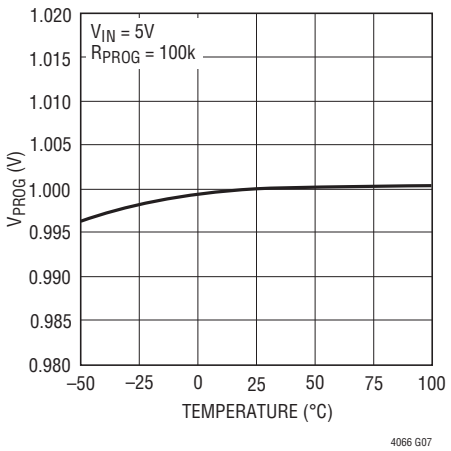
Input Current Limit vs Temperature, HPWR = 0V



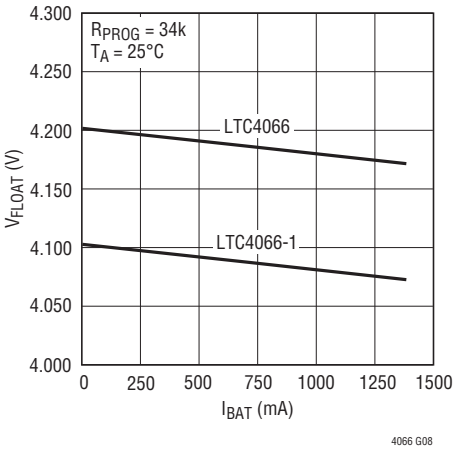
CLPROG Pin Voltage vs Temperature



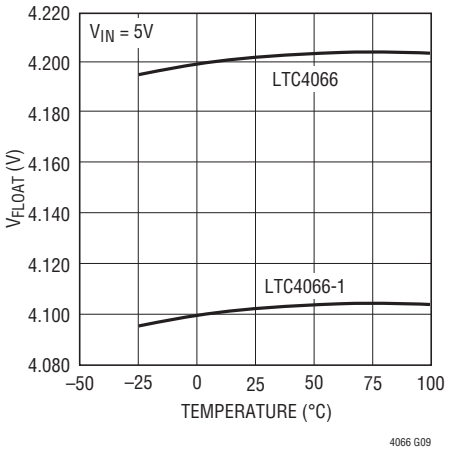
PROG Pin Voltage vs Temperatrue



V_{FLOAT} Load Regulation

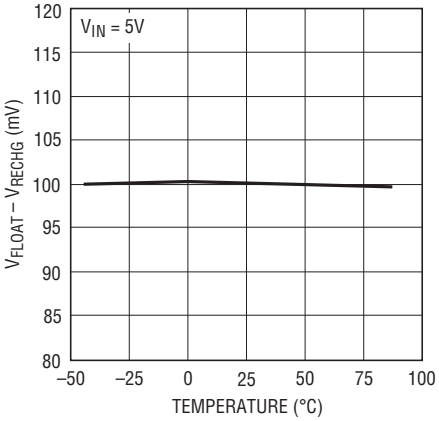


Battery Regulation (Float) Voltage vs Temperature

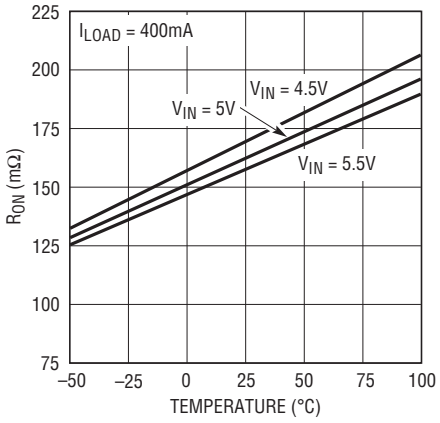


TYPICAL PERFORMANCE CHARACTERISTICS

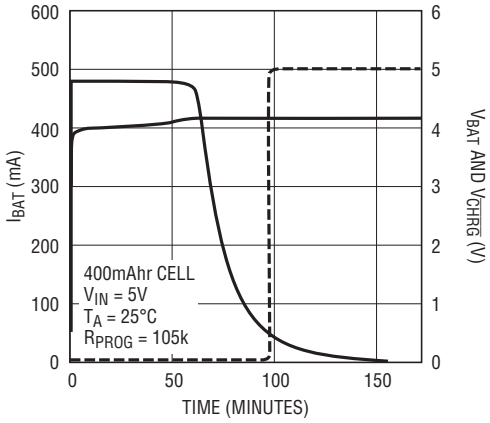
Regulated Output Voltage–Recharge Threshold Voltage vs Temperature



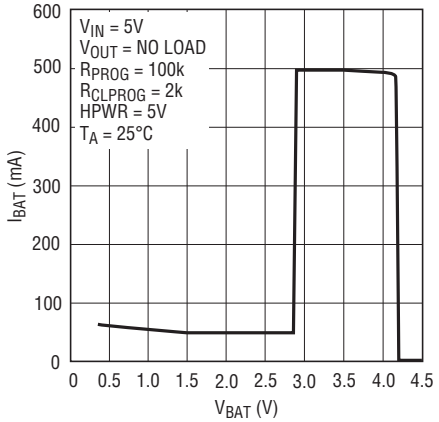
Input R_{ON} vs Temperature



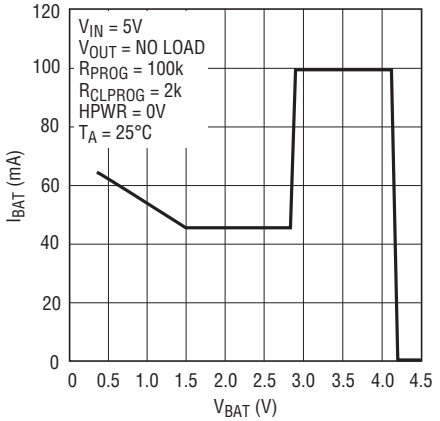
Battery Current and Voltage vs Time (LTC4066)



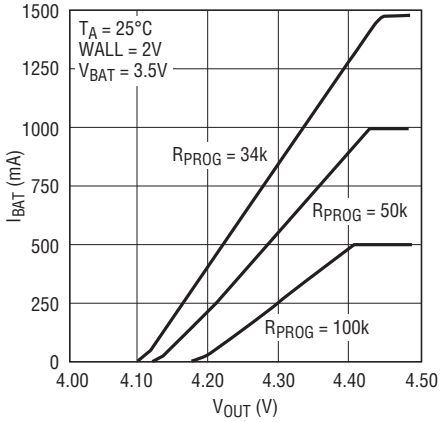
Charging from USB, I_{BAT} vs V_{BAT} (LTC4066)



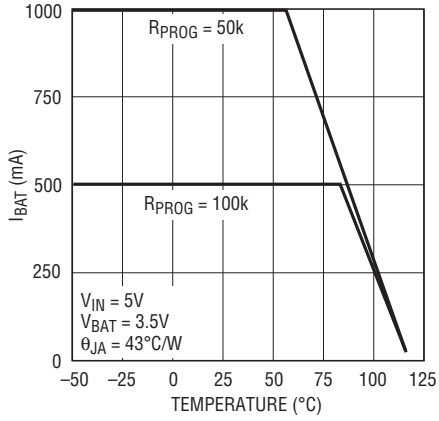
Charging from USB, Low Power, I_{BAT} vs V_{BAT} (LTC4066)



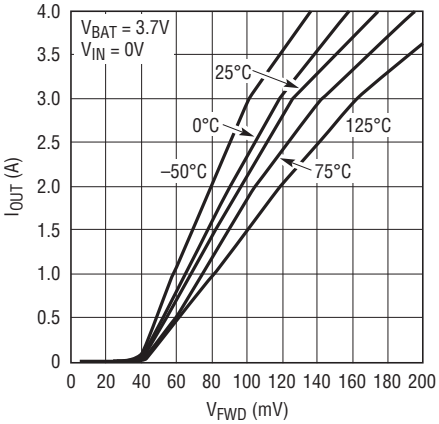
Undervoltage Current Limit I_{BAT} vs V_{OUT}



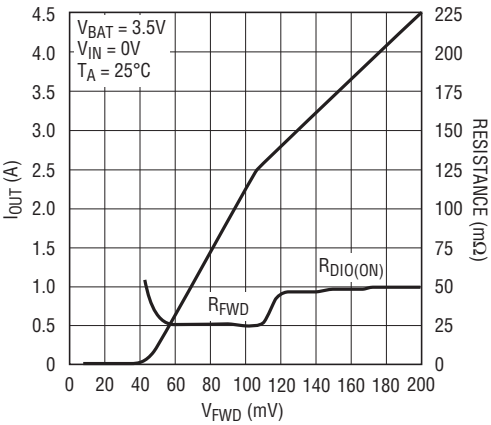
Charge Current vs Temperature (Thermal Regulation)



Ideal Diode Current vs Forward Voltage and Temperature

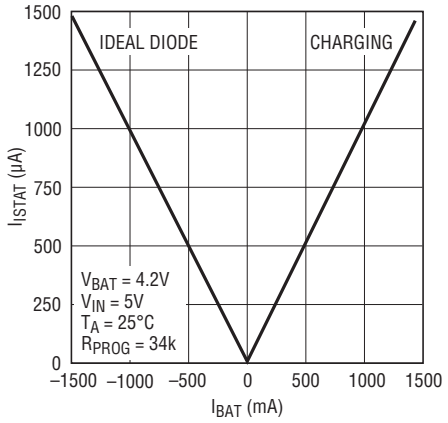


Ideal Diode Resistance and Current vs Forward Voltage

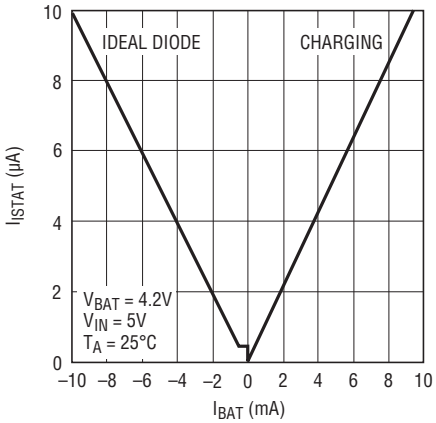


TYPICAL PERFORMANCE CHARACTERISTICS

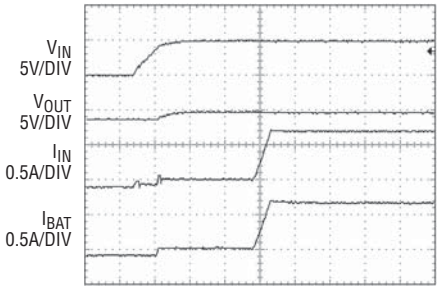
I_{STAT} Pin Current vs Battery Current



I_{STAT} Pin Current vs Battery Current (Low Currents)

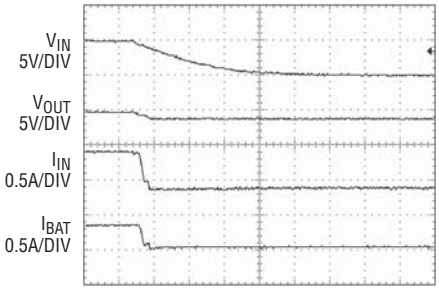


Input Connect Waveforms



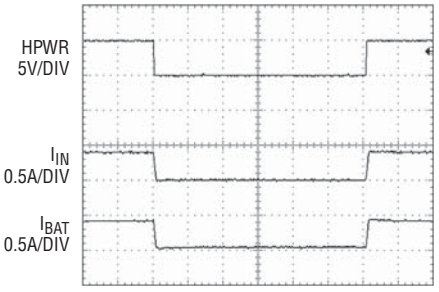
V_{BAT} = 3.85V 1ms/DIV
I_{OUT} = 100mA

Input Disconnect Waveforms



V_{BAT} = 3.85V 1ms/DIV
I_{OUT} = 100mA

Response to HPWR

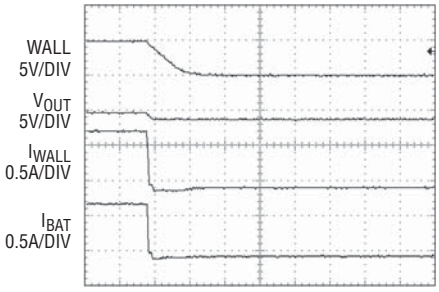


V_{BAT} = 3.85V 1ms/DIV
I_{OUT} = 50mA

WALL Connect Waveforms, V_{IN} = 0V

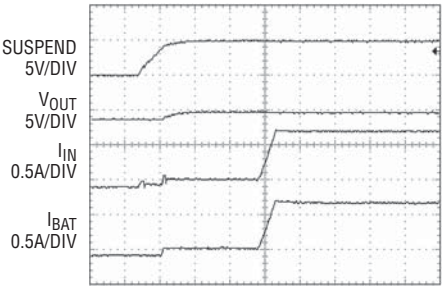
V_{BAT} = 3.85V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 71.5k

WALL Disconnect Waveforms, V_{IN} = 0V



V_{BAT} = 3.85V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 71.5k

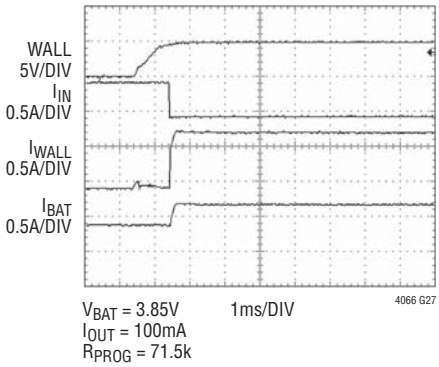
Respond to Suspend



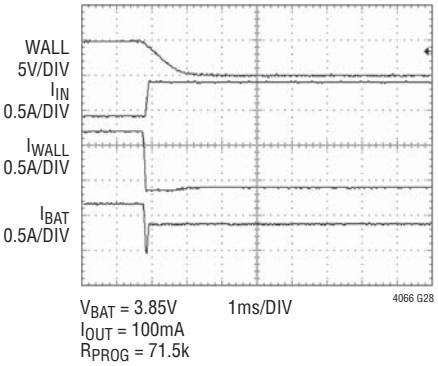
V_{BAT} = 3.85V 1ms/DIV
I_{OUT} = 50mA

TYPICAL PERFORMANCE CHARACTERISTICS

WALL Connect Waveforms, V_{IN} = 5V



WALL Disconnect Waveforms, V_{IN} = 5V



PIN FUNCTIONS

OUT (Pins 1, 3, 8): Voltage Output. This pin is used to provide controlled power to a USB device from either USB V_{BUS} (IN) or the battery (BAT) when the USB is not present. This pin can also be used as an input for battery charging when the USB is not present and a wall adapter is applied to this pin. OUT should be bypassed with at least 4.7µF to GND. Connect Pins 1, 3 and 8 with a resistance no greater than 10mΩ.

BAT (Pins 2, 4, 5): Connect to a single cell Li-Ion battery. This pin is used as an output when charging the battery, and as an input when supplying power to OUT. When the OUT pin potential drops below the BAT pin potential, an ideal diode function connects BAT to OUT and prevents V_{OUT} from dropping more than 50mV below V_{BAT}. A precision internal resistor divider sets the final float (charging) potential on this pin. The internal resistor divider is disconnected when IN and OUT are in undervoltage lockout. Connect Pins 2, 4 and 5 with a resistance no greater than 10mΩ.

IN (Pin 9): Input Supply. Connect to USB supply, V_{BUS}. Input current to this pin is limited to either 20% or 100% of the current programmed by the CLPROG pin as determined by the state of the HPWR pin. The input current limit can also be disabled by pulling CLDIS high. Charge current (to BAT pin) supplied through the input is set to the current programmed by the PROG pin but will be limited by the input current limit if charge current is set greater than the input current limit.

CLDIS (Pin 10): Current Limit Disable. This logic input is used to disable the input current limit programmed by CLPROG. A voltage greater than 1.2V on the pin will set the current limit to $I_{IN(MAX)}$ (typically 2.6A). A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

SUSP (Pin 11): Suspend Mode Input. Pulling this pin above 1.2V will disable the power path from IN to OUT. The supply current from IN will be reduced to comply with the USB specification for Suspend mode. Both the ability to charge the battery from OUT and the ideal diode function (from BAT to OUT) will remain active. Suspend mode will reset the charge timer if V_{OUT} is less than V_{BAT} while in suspend mode. If V_{OUT} is kept greater than V_{BAT}, such as when a wall adapter is present, the charge timer will not be reset when the part is put in suspend. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

PIN FUNCTIONS

SHDN (Pin 12): Shutdown Input. Pulling this pin greater than 1.2V will disable the entire part and place it in a low supply current mode of operation. All power paths will be disabled. A weak pull-down current is internally applied to this pin to ensure it is enabled at power-up when the pin is not being driven externally.

HPWR (Pin 13): High Power Select. This logic input is used to control the input current limit. A voltage greater than 1.2V on the pin will set the input current limit to 100% of the current programmed by the CLPROG pin. A voltage less than 0.4V on the pin will set the input current limit to 20% of the current programmed by the CLPROG pin. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the pin is not being driven externally.

NTC (Pin 14): Input to the NTC Thermistor Monitoring Circuits. Under normal operation, tie a thermistor from the NTC pin to ground and a resistor of equal value from NTC to V_{NTC}. When the voltage on this pin is above 0.74 • V_{VNTC} (Cold, 0°C) or below 0.29 • V_{VNTC} (Hot, 50°C) the timer is suspended, but not cleared, the charging is disabled and the $\overline{CHRG}$ pin remains in its former state. When the voltage on NTC comes back between 0.74 • V_{VNTC} and 0.29 • V_{VNTC}, the timer continues where it left off and charging is re-enabled if the battery voltage is below the recharge threshold. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. Connect the NTC pin to ground to disable this feature. This will disable all of the LTC4066/LTC4066-1 NTC functions.

V_{NTC} (Pin 15): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

GND (Pin 16), Exposed Pad (Pin 25): Ground. The Exposed Pad is ground and must be soldered to the PC board for maximum heat transfer. The Exposed Pad must be electrically connected to the GND pin.

$\overline{ACPR}$ (Pin 17): Wall Adapter Present Output. Active low open-drain output pin. A low on this pin indicates that the wall adapter input comparator has had its input pulled above the input threshold. This feature is disabled if the part is shut down or if no power is present on IN or OUT or BAT (i.e., below UVLO thresholds).

$\overline{CHRG}$ (Pin 18): Open-Drain Charge Status Output. When the battery is being charged, the $\overline{CHRG}$ pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below a programmable current level or the input supply or output supply is removed, the $\overline{CHRG}$ pin is forced to a high impedance state.

POL (Pin 19): Battery Current Status Polarity Pin. This open-drain output pin indicates whether the current flowing out of the I_{STAT} pin represents one-thousandth of the current flowing into or out of the BAT pins. The POL pin will pull down when current is flowing out of the BAT pin (i.e., charging) and will assume a high impedance state when current is flowing into the BAT pin (i.e., ideal diode).

WALL (Pin 20): Wall Adapter Present Input. Pulling this pin above 1.225V will disconnect the power path from IN to OUT. The $\overline{ACPR}$ pin will also be pulled low to indicate that a wall adapter has been detected.

TIMER (Pin 21): Timer Capacitor. Placing a capacitor, C_{TIMER}, to GND sets the timer period. The timer period is:

$$t_{TIMER}(Hours) = \frac{C_{TIMER} \bullet R_{PROG} \bullet 3Hours}{0.1\mu F \bullet 100k}$$

Charge time is increased if charge current is reduced due to load current, thermal regulation and current limit selection (HPWR). Shorting the TIMER pin to GND disables the battery charging functions.

PIN FUNCTIONS

CLPROG (Pin 22): Current Limit Program and Input Current Monitor. Connecting a resistor, R_{CLPROG}, to ground programs the input to output current limit. The current limit is programmed as follows:

$$I_{CL}(A) = \frac{1000V}{R_{CLPROG}}$$

In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

The voltage on the CLPROG pin is always proportional to the current flowing through the IN to OUT power path. This current can be calculated as follows:

$$I_{IN}(A) = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

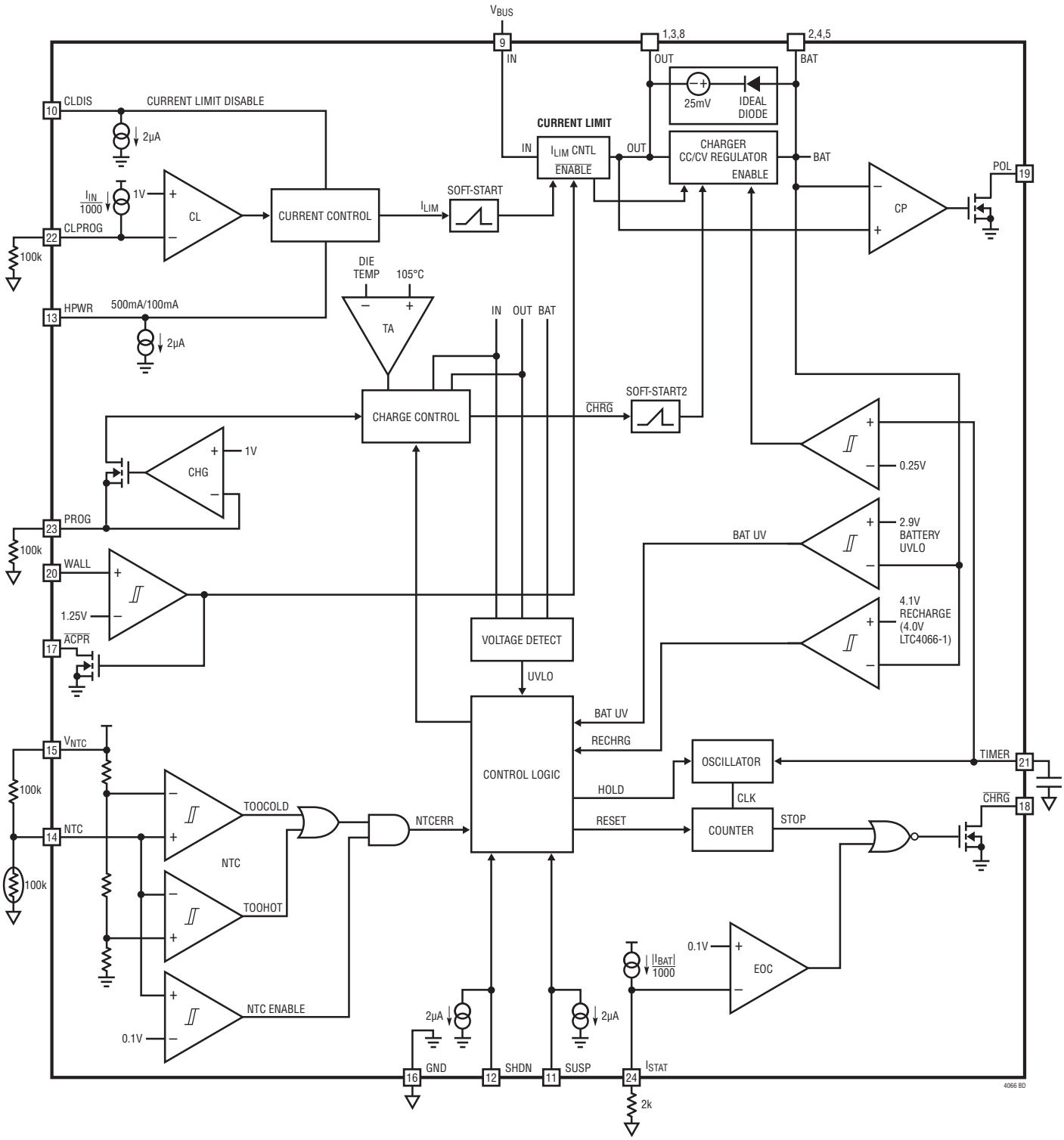
PROG (Pin 23): Charge Current Program. Connecting a resistor, R_{PROG}, to ground programs the battery charge current. The battery charge current is programmed as follows:

$$I_{CHG}(A) = \frac{50,000V}{R_{PROG}}$$

I_{STAT} (Pin 24): Battery Current Status Pin. One-thousandth of the current flowing into or out of the BAT pins flows out of this pin. The POL polarity pin indicates which direction current is flowing. If the current flowing into the BAT pins drops below 1mA, then the I_{STAT} pin will continue to source 1µA. The I_{STAT} pin also programs the charge current level at which the $\overline{CHRG}$ pin transitions to its high impedance state. When the I_{STAT} voltage drops below 0.1V while charging in constant voltage mode the $\overline{CHRG}$ pin will transition to a high impedance state. This corresponds to a BAT current of:

$$I_{BAT}(A) = \frac{0.1V}{R_{ISTAT}} \bullet 1000$$

BLOCK DIAGRAM



OPERATION

The LTC4066/LTC4066-1 are complete PowerPath™ controllers for battery-powered USB applications. The LTC4066/LTC4066-1 are designed to receive power from a USB source, a wall adapter or a battery. It can then deliver power to an application connected to the OUT pin and a battery connected to the BAT pin (assuming that an external supply other than the battery is present). Power supplies that have limited current resources (such as USB V_{BUS} supplies) should be connected to the IN pin which has a programmable current limit. Battery charge current will be adjusted to ensure that the sum of the charge current and load current does not exceed the programmed input current limit.

An ideal diode function provides power from the battery when output/load current exceeds the input current limit or when input power is removed. Powering the load through the ideal diode instead of connecting the load directly to the battery allows a fully charged battery to remain fully charged until external power is removed. Once external power is removed, the output drops until the ideal diode is forward biased. The forward biased ideal diode will then provide the output power to the load from the battery.

Furthermore, powering switching regulator loads from the OUT pin (rather than directly from the battery), results in shorter battery charge times. This is due to the fact that switching regulators typically require constant input power. When this power is drawn from the OUT pin voltage (rather than the lower BAT pin voltage) the current consumed by the switching regulator is lower, leaving more current available to charge the battery.

The LTC4066/LTC4066-1 also have the ability to receive power from a wall adapter. Wall adapter power can be connected to the output (load side) of the LTC4066/LTC4066-1 through an external device such as a power Schottky or FET, as shown in Figure 1. The LTC4066/LTC4066-1 have the unique ability to use the output, which is powered by the wall adapter, as a path to charge the battery while providing power to the load. A wall adapter comparator on the LTC4066/LTC4066-1 can be configured to detect the presence of the wall adapter and shut off the connection to the USB to prevent reverse conduction out to the USB bus.

PowerPath is a trademark of Linear Technology Corporation.

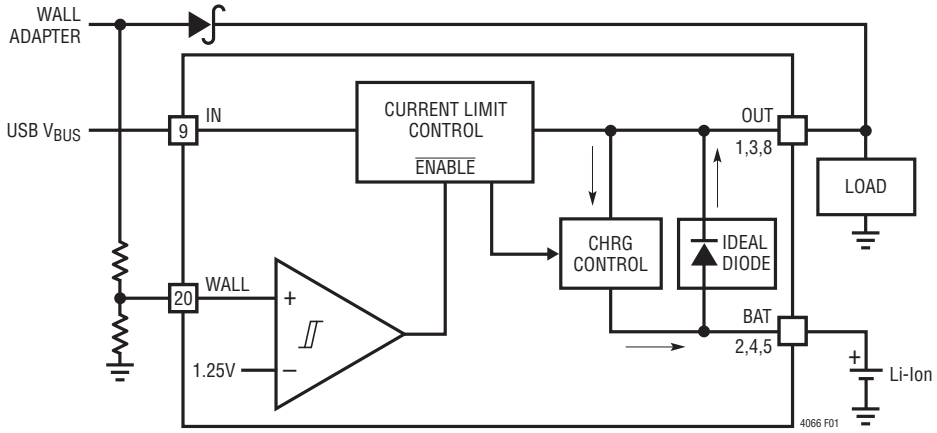


Figure 1. Simplified Block Diagram—PowerPath

OPERATION

Table 1. Operating Modes—PowerPath States
Current Limited Input Power (IN to OUT)

WALL PRESENT	SHUTDOWN	SUSPEND	V_{IN} > 3.8V	V_{IN} > (V_{OUT} + 100mV)	V_{IN} > (V_{BAT} + 100mV)	CURRENT LIMIT ENABLED
Y	X	X	X	X	X	N
X	Y	X	X	X	X	N
X	X	Y	X	X	X	N
X	X	X	N	X	X	N
X	X	X	X	N	X	N
X	X	X	X	X	N	N
N	N	N	Y	Y	Y	Y

Battery Charger (OUT to BAT)

WALL PRESENT	SHUTDOWN	SUSPEND	V_{OUT} > 4.35V	V_{OUT} > (V_{BAT} + 100mV)	CHARGER ENABLED
X	Y	X	X	X	N
X	X	X	N	X	N
X	X	X	X	N	N
X	N	X	Y	Y	Y

Ideal Diode (BAT to OUT)

WALL PRESENT	SHUTDOWN	SUSPEND	V_{BAT} > 2.8V	V_{BAT} > V_{OUT}	V_{IN}	DIODE ENABLED
X	Y	X	X	X	X	N
X	X	X	N	X	X	N
X	X	X	X	N	X	N
X	N	X	Y	Y	X	Y

Table 2. Operating Modes—Pin Currents vs Programmed Currents (Powered from IN)

PROGRAMMING	OUTPUT CURRENT	BATTERY CURRENT	INPUT CURRENT
$I_{CL} = I_{CHG}$	$I_{OUT} < I_{CL}$ $I_{OUT} = I_{CL} = I_{CHG}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CHG} - I_{OUT}$ $I_{BAT} = 0$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$
$I_{CL} > I_{CHG}$	$I_{OUT} < (I_{CL} - I_{CHG})$ $I_{OUT} > (I_{CL} - I_{CHG})$ $I_{OUT} = I_{CL}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CHG}$ $I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = 0$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CHG} + I_{OUT}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$
$I_{CL} < I_{CHG}$	$I_{OUT} < I_{CL}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$

OPERATION

Operatinal State Diagram

APPLICATIONS INFORMATION

USB Current Limit and Charge Current Control

The current limit and charger control circuits of the LTC4066/LTC4066-1 are designed to limit input current as well as control battery charge current as a function of I_{OUT}. The programmed input current limit, I_{CL}, is defined as:

$$I_{CL} = \left(\frac{1000}{R_{CLPROG}} \bullet V_{CLPROG}\right) = \frac{1000V}{R_{CLPROG}}$$

The programmed battery charge current, I_{CHG}, is defined as:

$$I_{CHG} = \left(\frac{50,000}{R_{PROG}} \bullet V_{PROG}\right) = \frac{50,000V}{R_{PROG}}$$

Input current, I_{IN}, is equal to the sum of the BAT pin output current and the OUT pin output current:

$$I_{IN} = I_{OUT} + I_{BAT}$$

The current limiting circuitry in the LTC4066/LTC4066-1 can and should be configured to limit current to 500mA for USB applications (selectable using the HPWR pin and programmed using the CLPROG pin).

The LTC4066/LTC4066-1 reduce battery charge current such that the sum of the battery charge current and the load current does not exceed the programmed input current limit (one-fifth of the programmed input current limit when HPWR is low, see Figure 2). The battery charge current goes to zero when load current exceeds the programmed input current limit (one-fifth of the limit when HPWR is low). If the load current is greater than the current limit, the output voltage will drop to just under the battery voltage where the ideal diode circuit will take over and the excess load current will be drawn from the battery.

Programming Current Limit

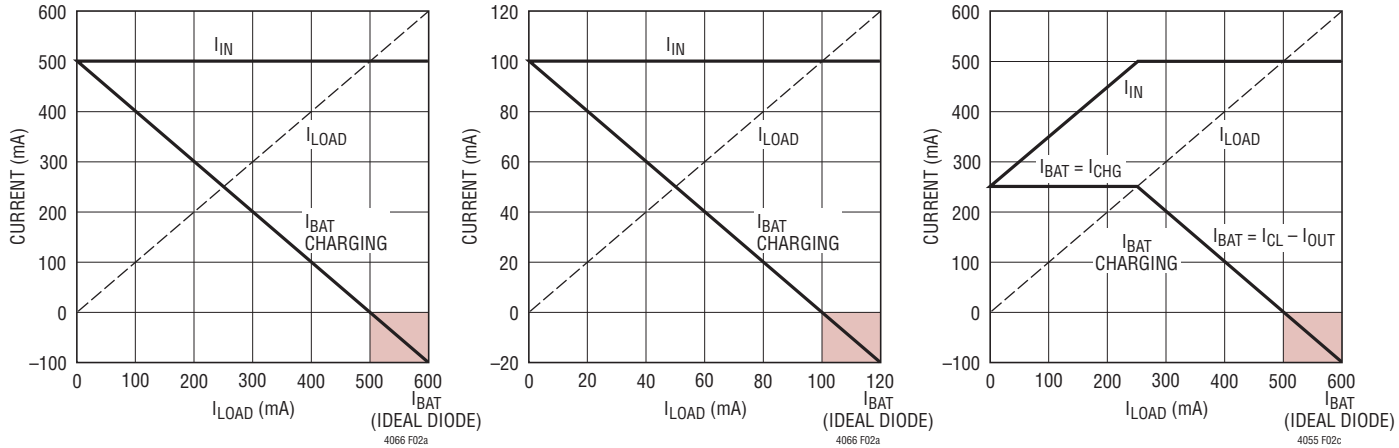
The formula for input current limit is:

$$I_{CL} = \left(\frac{1000}{R_{CLPROG}} \bullet V_{CLPROG}\right) = \frac{1000V}{R_{CLPROG}}$$

where V_{CLPROG} is the CLPROG pin voltage and R_{CLPROG} is the total resistance from the CLPROG pin to ground.

For example, if typical 500mA current limit is required, calculate:

$$R_{CLPROG} = \frac{1V}{500mA} \bullet 1000 = 2k$$



(2a) High Power Mode/Full Charge R_{PROG} = 100k and R_{CLPROG} = 2k

(2b) Low Power Mode/Full Charge R_{PROG} = 100k and R_{CLPROG} = 2k

(2c) High Power Mode with I_{CL} = 500mA and I_{CHG} = 250mA R_{PROG} = 200k and R_{CLPROG} = 2k

Figure 2. Input and Battery Currents as a Function of Load Current

APPLICATIONS INFORMATION

In USB applications, the minimum value for R_{CLPROG} should be 2.1k. This will prevent the application current from exceeding 500mA due to LTC4066/LTC4066-1 tolerances and quiescent currents. A 2.1k CLPROG resistor will give a typical current limit of 476mA in high power mode (HPWR = 1) or 95mA in low power mode (HPWR = 0).

V_{CLPROG} will typically servo to 1V; however, if $I_{OUT} + I_{BAT} < I_{CL}$ then V_{CLPROG} will track the input current according to the following equation:

$$I_{IN} = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

For best stability over temperature and time, 1% metal film resistors are recommended.

Ideal Diode from BAT to OUT

If a battery is the only power supply available or if the load current exceeds the programmed input current limit, then the battery will automatically deliver power to the load via an ideal diode circuit between the BAT and OUT pins. The ideal diode circuit (along with the recommended 4.7µF capacitor on the OUT pin) allows the LTC4066/LTC4066-1 to handle large transient loads and wall adapter or USB V_{BUS} connect/disconnect scenarios without the need for large bulk capacitors. The ideal diode responds within a few microseconds and prevents the OUT pin voltage from dipping below the BAT pin voltage by more than 50mV.

Forward regulation for the ideal diode from BAT to OUT has three operational ranges, depending on the magnitude of the diode load current. For small load currents, the LTC4066/LTC4066-1 will provide a constant voltage drop; this operating mode is referred to as "constant V_{ON}" regulation. As the current exceeds I_{FWD} the voltage drop will increase linearly with the current with a slope of $1/R_{DIO(ON)}$; this operating mode is referred to as "constant R_{ON}" regulation. As the current increases further, exceeding I_{MAX}, the forward voltage drop will increase rapidly; this operating mode is referred to as "constant I_{ON}" regulation. The characteristics for parameters R_{FWD}, R_{ON}, V_{FWD} and I_{FWD} are specified with the aid of Figure 3.

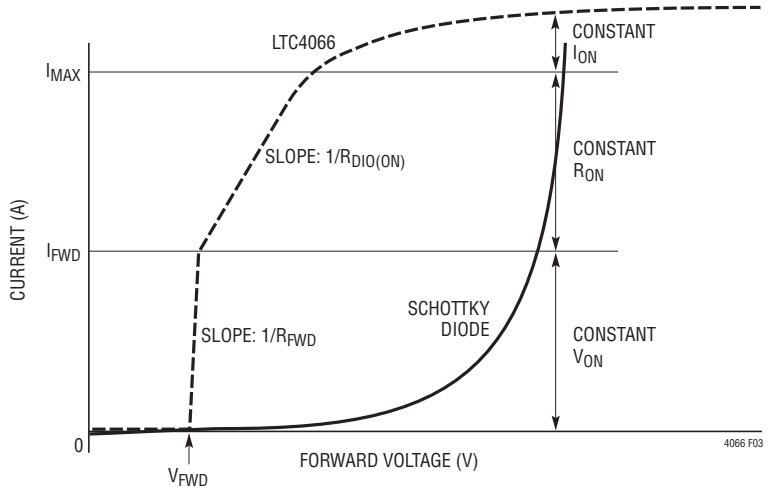


Figure 3. LTC4066/LTC4066-1 vs Schottky Diode Forward Voltage Drop

APPLICATIONS INFORMATION

Battery Charger

The battery charger circuits of the LTC4066/LTC4066-1 are designed for charging single cell lithium-ion batteries. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage charge algorithm with programmable current and a programmable timer for charge termination. Charge current can be programmed up to 1.5A. The final float voltage accuracy is ±0.8% typical. No blocking diode or sense resistor is required when powering the IN pin. The $\overline{CHRG}$ open-drain status output provides information regarding the charging status of the LTC4066/LTC4066-1 at all times. An NTC input provides the option of charge qualification using battery temperature.

An internal thermal limit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature protects the LTC4066/LTC4066-1 from excessive temperature, and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LTC4066/LTC4066-1. Another benefit of the LTC4066/LTC4066-1 thermal limit is that charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

The charge cycle begins when the voltage at the OUT pin rises above the output UVLO level and the battery voltage is below the recharge threshold. No charge current actually flows until the OUT voltage is greater than the output UVLO level and 100mV above the BAT voltage. At the beginning of the charge cycle, if the battery voltage is below 2.8V, the charger goes into trickle charge mode to bring the cell voltage up to a safe level for charging. The charger goes into the fast charge constant-current mode once the voltage on the BAT pin rises above 2.8V. In constant-current mode, the charge current is set by R_{PROG}. When the battery approaches the final float voltage, the charge current begins to decrease as the LTC4066/LTC4066-1 switches to constant-voltage mode. When the charge current drops below a level programmed by the I_{STAT} pin while in constant-voltage mode the $\overline{CHRG}$ pin assumes a high impedance state.

An external capacitor on the TIMER pin sets the total minimum charge time. When this time elapses the charge cycle terminates and the $\overline{CHRG}$ pin assumes a high impedance state, if it has not already done so. While charging in constant-current mode, if the charge current is decreased by thermal regulation or in order to maintain the programmed input current limit the charge time is automatically increased. In other words, the charge time is extended inversely proportional to charge current delivered to the battery. For Li-Ion and similar batteries that require accurate final float potential, the internal bandgap reference, voltage amplifier and the resistor divider provide regulation with ±0.8% accuracy.

Trickle Charge and Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is low (below 2.8V) the charger goes into trickle charge reducing the charge current to 10% of the full-scale current. If the low-battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated and the $\overline{CHRG}$ pin output assumes a high impedance state. If for any reason the battery voltage rises above ~2.8V, the charge cycle will be restarted. To restart the charge cycle (i.e., when the dead battery is replaced with a discharged battery), simply remove the input voltage and reapply it, cycle the TIMER pin to 0V or cycle the SHDN pin to 0V.

APPLICATIONS INFORMATION

Programming Charge Current

The formula for the battery charge current is:

$$I_{CHG} = (I_{PROG}) \bullet 50,000 = \frac{V_{PROG}}{R_{PROG}} \bullet 50,000$$

where V_{PROG} is the PROG pin voltage and R_{PROG} is the total resistance from the PROG pin to ground. Keep in mind that when the LTC4066/LTC4066-1 are powered from the IN pin, the programmed input current limit takes precedence over the charge current. In such a scenario, the charge current cannot exceed the programmed input current limit.

For example, if typical 500mA charge current is required, calculate:

$$R_{PROG} = \left(\frac{1V}{500mA}\right) \bullet 50,000 = 100k$$

For best stability over temperature and time, 1% metal film resistors are recommended. Under trickle charge conditions, this current is reduced to 10% of the full-scale value.

Monitoring Charge Current

The I_{STAT} and POL pins provide a means for monitoring the BAT pin current. The I_{STAT} pin sources a current equal to one-thousandth of the absolute value of the current flowing in the BAT pin. The POL pin indicates the polarity of the BAT pin current. When current is flowing from OUT to BAT (i.e., charging), the POL pin pulls to ground. When current is flowing from BAT to OUT (ideal diode), the POL pin assumes a high impedance. If a resistor, R_{ISTAT}, is placed from the I_{STAT} pin to ground, then the formula for BAT current is:

$$|I_{BAT}| = \frac{V_{ISTAT}}{R_{ISTAT}} \bullet 1000$$

where V_{ISTAT} is the I_{STAT} pin voltage and R_{ISTAT} is the total resistance from the I_{STAT} pin to ground. These pins enable a true gas gauge function to be performed on the battery with an external ADC and integrator. See Gas Gauge for more information.

The Charge Timer

The programmable charge timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin. The charge time is typically:

$$t_{TIMER}(Hours) = \frac{C_{TIMER} \bullet R_{PROG} \bullet 3Hours}{0.1\mu F \bullet 100k}$$

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied or when leaving shutdown and the voltage on the battery is less than the recharge threshold. At power-up or exiting shutdown with the battery voltage less than the recharge threshold, the charge time is a full cycle. If the battery is greater than the recharge threshold, the timer will not start and charging is prevented. If after power-up the battery voltage drops below the recharge threshold, or if after a charge cycle the battery voltage is still below the recharge threshold, the charge time is set to one-half of a full cycle.

The LTC4066/LTC4066-1 have a feature that extends charge time automatically. Charge time is extended if the charge current in constant-current mode is reduced due to load current or thermal regulation. This change in charge time is inversely proportional to the change in charge current. As the LTC4066/LTC4066-1 approach constant-voltage mode the charge current begins to drop. This change in charge current is due to normal charging operation and does not affect the timer duration.

APPLICATIONS INFORMATION

Consider, for example, a USB charge condition where R_{CLPROG} = 2k, R_{PROG} = 100k and C_{TIMER} = 0.1µF. This corresponds to a three hour charge cycle. However, if the HPWR input is set to a logic low, then the input current limit will be reduced from 500mA to 100mA. With no additional system load, this means the charge current will be reduced to 100mA. Therefore, the termination timer will automatically slow down by a factor of five until the charger reaches constant voltage mode (i.e., V_{BAT} = 4.2V, 4.1V for LTC4066-1) or HPWR is returned to a logic high. The charge cycle is automatically lengthened to account for the reduced charge current. The exact time of the charge cycle will depend on how long the charger remains in constant current mode and/or how long the HPWR pin remains a logic low.

Once a time-out occurs and the voltage on the battery is greater than the recharge threshold, the charge current stops, and the $\overline{CHRG}$ output assumes a high impedance state if it has not already done so.

Connecting the TIMER pin to ground disables the battery charger.

$\overline{CHRG}$ Status Output Pin

When the charge cycle starts, the $\overline{CHRG}$ pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. When the charge current drops below a programmable threshold while in constant-voltage mode, the pin assumes a high impedance state (but charge current continues to flow until the charge time elapses). If this state is not reached before the end of the programmable charge time, the pin will assume a high impedance state when a time-out occurs.

The current level at which the $\overline{CHRG}$ pin changes state is programmed by the I_{STAT} pin. As described in Monitoring Charge Current and Gas Gauge, the I_{STAT} pin sources a current proportional to the BAT pin current. The LTC4066/LTC4066-1 monitor the voltage on the I_{STAT} pin and turns off the $\overline{CHRG}$ N-channel pull-down when V_{ISTAT} drops below 100mV while in constant-voltage mode. The $\overline{CHRG}$ current detection threshold can be calculated by the following equation:

$$I_{DETECT} = \frac{0.1V}{R_{ISTAT}} \bullet 1000 = \frac{100V}{R_{ISTAT}}$$

For example, to program the $\overline{CHRG}$ pin to change state at a battery charge current of 100mA, choose:

$$R_{ISTAT} = \frac{100V}{100mA} = 1k$$

Note: The end-of-charge (EOC) comparator that monitors the I_{STAT} pin voltage for 100mV latches its decision. Therefore, the first time V_{ISTAT} drops below 100mV (i.e., I_{BAT} drops below $100V/R_{ISTAT}$) while in constant voltage mode will toggle $\overline{CHRG}$ to a high impedance state. If, for some reason, the charge current rises back above the threshold, the $\overline{CHRG}$ pin will not resume the strong pull-down state. The EOC latch can be reset by toggling the SHDN pin or toggling the input power to the part. The EOC latch will also be reset if the BAT pin voltage falls below the recharge threshold.

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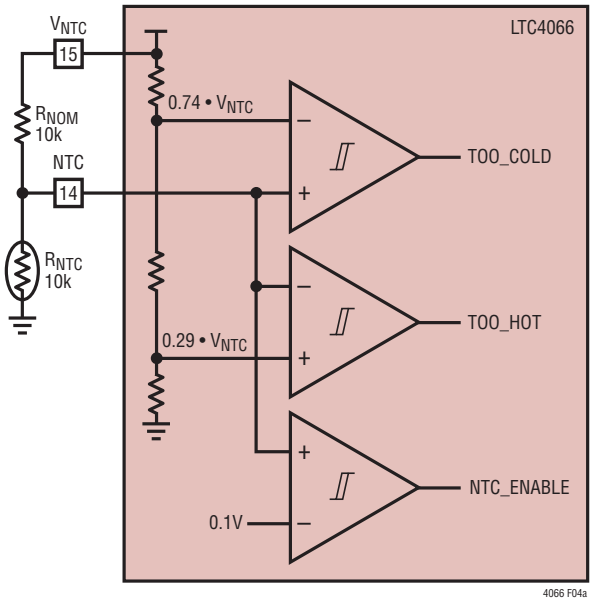
NTC Thermistor

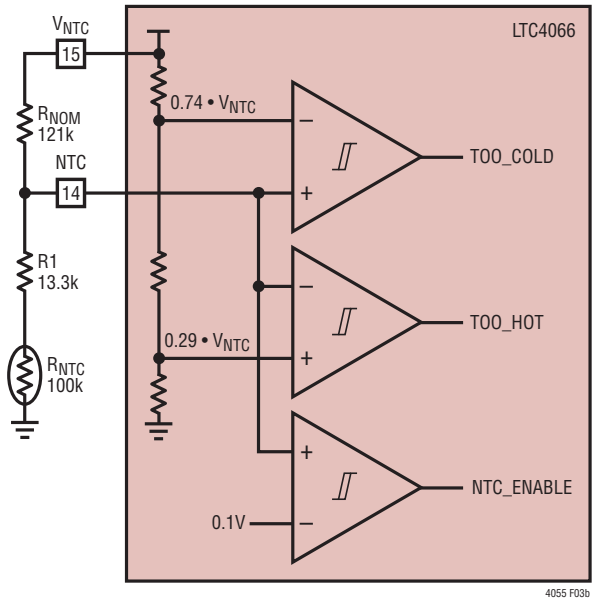
The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 4. To use this feature, connect the NTC thermistor (R_{NTC}) between the NTC pin and ground and a resistor (R_{NOM}) from the NTC pin to V_{NTC}. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (this value is 10k for a Vishay NTHS0603N02N1002J thermistor). The LTC4066/LTC4066-1 go into hold mode when the resistance (R_{HOT}) of the NTC thermistor drops to 0.41 times the value of R_{NOM} or approximately 4.1k, which should be at 50°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4066/LTC4066-1 are designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of R_{NOM}. This resistance is R_{COLD}. For a Vishay NTHS0603N02N1002J thermistor, this value is 28.2k which corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin can disable the NTC function.

Thermistors

The LTC4066/LTC4066-1 NTC trip points were designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's "R-T Curve 2". The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 2" characteristic in a variety of sizes. Furthermore, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 7.0 will also work (Vishay Dale R-T Curve 2 shows a ratio of R_{COLD} to R_{HOT} of 2.815/0.4086 = 6.89).



(4a)



(4b)

Figure 4. NTC Circuits

APPLICATIONS INFORMATION

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 2." Using these directly in the manor spelled out previously in the NTC Thermistor section will give temperature trip points of approximately 3°C and 47°C, a delta of 44°C. This delta in temperature can be moved in either direction by changing the value of R_{NOM} with respect to R_{NTC}. Increasing R_{NOM} will move both trip points to lower temperatures. Likewise a decrease in R_{NOM} with respect to R_{NTC} will move the trip points to higher temperatures. To calculate R_{NOM} for a shift to lower temperature for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25°C$$

where R_{COLD} is the resistance ratio of R_{NTC} at the desired cold temperature trip point. If you want to shift the trip points to higher temperatures, use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.4086} \bullet R_{NTC} \text{ at } 25°C$$

where R_{HOT} is the resistance ratio of R_{NTC} at the desired hot temperature trip point.

Here is an example using a 100k R-T Curve 1 Thermistor from Vishay Dale. The difference between the trip points is 44°C, from before, and we want the cold trip point to be 0°C, which would put the hot trip point at 44°C. The R_{NOM} needed is calculated as follows:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \bullet R_{NTC} \text{ at } 25°C$$

$$= \frac{3.266}{2.815} \bullet 100k\Omega = 116k\Omega$$

The nearest 1% value for R_{NOM} is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 44°C respectively. To extend the delta between the cold and hot trip points, a resistor (R1) can be added in series with R_{NTC} (see Figure 3b). The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086}$$

$$R1 = \left(\frac{0.4086}{2.815 - 0.4086}\right) \bullet (R_{COLD} - R_{HOT}) - R_{HOT}$$

where R_{NOM} is the value of the bias resistor, R_{HOT} and R_{COLD} are the values of R_{NTC} at the desired temperature trip points. Continuing the example from before with a desired hot trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086} = \frac{100k \bullet (3.266 - 0.3602)}{2.815 - 0.4086}$$

$$= 120.8k\Omega, \text{ 121k nearest 1\%}$$

$$R1 = 100k \bullet \left[\left(\frac{0.4086}{2.815 - 0.4086}\right) \bullet (3.266 - 0.3602) - 0.3602\right]$$

$$= 13.3k\Omega, \text{ 13.3k is nearest 1\%}$$

The final solution is as shown if Figure 3b where R_{NOM} = 121k, R1 = 13.3k and R_{NTC} = 100k at 25°C.

Gas Gauge

The extremely low impedance of the ideal diode between BAT and OUT (typically 50mΩ) allows users to connect all of their loads to the OUT pin. Such a configuration puts the LTC4066/LTC4066-1 in a unique position whereby it can monitor all of the current that flows into and out of the battery. Two output pins, I_{STAT} and POL, are provided to enable users to monitor and integrate the battery current for a true gas gauge function.

APPLICATIONS INFORMATION

Any time a battery is connected to the BAT pin and the SHDN pin is low, the BAT pin current can be monitored with the following equation:

$$|I_{BAT}| = \frac{V_{ISTAT}}{R_{ISTAT}} \bullet 1000$$

where $|I_{BAT}|$ is the absolute value of the BAT pin current, V_{ISTAT} is the voltage on the I_{STAT} pin and R_{ISTAT} is the total resistance from the I_{STAT} pin to ground.

The POL pin has two states: high impedance and strong pull-down. High impedance indicates that current is flowing from BAT to OUT (ideal diode function) and strong pull-down indicates that current is flowing from OUT to BAT (charging). If an external ADC is used to convert the I_{STAT} voltage, then the POL pin can be thought of as a sign bit.

When the ideal diode function is operating, the I_{STAT} pin cannot monitor ideal diode load currents less than about 1mA. For any ideal diode load current less than 1mA, the I_{STAT} pin will source a constant current of approximately 1µA. However, when the battery charger function is operating, the I_{STAT} pin will continue to source one-thousandth of the battery charge current even if the charge current drops to less than 1mA.

When choosing the value of R_{ISTAT}, two details must be considered. For the battery charger function, the value of R_{ISTAT} programs the charge current below which the $\overline{CHRG}$ pin transitions to its high impedance state (see $\overline{CHRG}$ Status Output Pin). Furthermore, the available common mode range on the I_{STAT} pin needed to maintain an accurate ratio between I_{BAT} and I_{ISTAT} is limited. When charging, the I_{STAT} pin voltage should not exceed approximately V_{OUT} – 0.5V. When the ideal diode is functioning, the I_{STAT} pin voltage should not exceed approximately V_{BAT} – 0.5V (for the typical minimum operating voltage for the ideal diode this value would be 2.8V – 0.5V = 2.3V). Typically, it is this second case that is the limiting situation since V_{BAT} is typically lower than V_{OUT} (while charging) and transient ideal diode loads tend to be greater than typical charge currents (causing a higher voltage on the I_{STAT} pin). Therefore, choosing a value of R_{ISTAT} based on the $\overline{CHRG}$ detection current may limit the maximum ideal diode load current that can be sensed accurately. Consider an example:

a) Desired charge current = 850mA

b) Desired $\overline{CHRG}$ detection current = 100mA

c) Maximum transient ideal diode current = 1.5A

Calculate:

a) R_{PROG} = (1V/850mA) • 50,000 = 59k

b) R_{ISTAT} = 100V/100mA = 1k

c) $V_{ISTAT(MAX)}$ = 1.5A/1000 • 1k = 1.5V

In this example, there is no common mode problem because the maximum I_{STAT} voltage (1.5V) is well below the 2.3V minimum. However, if, instead of 100mA, the desired $\overline{CHRG}$ detection current was lowered to 40mA, then the desired R_{ISTAT} resistor would increase to 2.5k (100V/40mA) and the maximum I_{STAT} voltage would increase to 3.75V (assuming no change in the 1.5A maximum ideal diode current). Therefore, ideal diode currents greater than 920mA (2.3V/2.5k • 1000) might not be reported accurately. To calculate the maximum ideal diode current that will be reported accurately:

$$I_{DMON(MAX)} = \frac{V_{BAT} - 0.5V}{R_{ISTAT}}$$

APPLICATIONS INFORMATION

Current Limit Undervoltage Lockout

An internal undervoltage lockout circuit monitors the input voltage and disables the input current limit circuits until V_{IN} rises above the undervoltage lockout threshold. The current limit UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the current limit UVLO circuit disables the current limit (i.e., forces the input power path to a high impedance state) if V_{OUT} exceeds V_{IN}. If the current limit UVLO comparator is tripped, the current limit circuits will not come out of shutdown until V_{OUT} falls 50mV below the V_{IN} voltage.

Charger Undervoltage Lockout

An internal undervoltage lockout circuit monitors the V_{OUT} voltage and disables the battery charger circuits until V_{OUT} rises above the undervoltage lockout threshold. The battery charger UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the charger UVLO circuit keeps the charger shutdown if V_{BAT} exceeds V_{OUT}. If the charger UVLO comparator is tripped, the charger circuits will not come out of shutdown until V_{OUT} exceeds V_{BAT} by 50mV.

Shutdown

The LTC4066/LTC4066-1 can be shutdown by forcing the SHDN pin greater than 1.2V. In shutdown, the currents drawn from IN, OUT and BAT are decreased to less than 2.5µA and the internal battery charge timer and end-of-charge comparator output are reset. All power paths are put in a high impedance state.

Suspend

The LTC4066/LTC4066-1 can be put in suspend mode by forcing the SUSP pin greater than 1.2V. In suspend mode the ideal diode function from BAT to OUT is kept alive. If power is applied to the OUT pin externally (i.e., a wall adapter is present) then charging will be unaffected. Current drawn from the IN pin is reduced to 50µA. Suspend mode is intended to comply with the USB Power Specification mode of the same name.

Selecting WALL Input Resistors

The WALL input pin identifies the presence of a wall adapter. This information is used to disconnect the input pin, IN, from the OUT pin in order to prevent back conduction to whatever may be connected to the input. It also forces the $\overline{ACPR}$ pin low when the voltage at the WALL pin exceeds the input threshold. The WALL pin has a 1.225V rising threshold and approximately 30mV of hysteresis.

The wall adapter detection threshold is set by the following equation:

$$V_{TH}(Adapter) = V_{WALL} \bullet \left(1 + \frac{R1}{R2}\right)$$

$$V_{HYST}(Adapter) = V_{WALL(HYST)} \bullet \left(1 + \frac{R1}{R2}\right)$$

where V_{TH}(Adapter) is the wall adapter detection threshold, V_{WALL} is the WALL pin rising threshold (typically 1.225V), R1 is the resistor from the wall adapter input to WALL and R2 is the resistor from WALL to GND.

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Consider an example where the V_{TH}(Adapter) is to be set somewhere around 4.5V. Resistance on the WALL pin should be kept relatively low (~10k) in order to prevent false tripping of the wall comparator due to leakages associated with the switching element used to connect the adapter to OUT. Pick R2 to be 10k and solve for R1:

$$R1 = R2 \bullet \left(\frac{V_{TH}(Adapter)}{V_{WALL}} - 1 \right)$$

$$R1 = 10k \bullet \left(\frac{4.5V}{1.225V} - 1 \right) = 10k \bullet 2.67 = 26.7k$$

The nearest 1% resistor is 26.7k. Therefore, R1 = 26.7k and the rising trip point should be 4.50V.

$$V_{HYST}(Adapter) \approx 30mV \bullet \left(1 + \frac{26.7k}{10k} \right) \approx 110.1mV$$

The hysteresis is going to be approximately 110mV for this example.

Power Dissipation

The conditions that cause the LTC4066/LTC4066-1 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the part. For high charge currents and a wall adapter applied to V_{OUT}, the LTC4066/LTC4066-1 power dissipation is approximately:

$$P_D = (V_{OUT} - V_{BAT}) \bullet I_{BAT}$$

where P_D is the power dissipated, V_{OUT} is the supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the battery charge current. It is not necessary to perform any worst-case power dissipation scenarios because the LTC4066/LTC4066-1 will automatically reduce the charge current to maintain the die temperature at approximately 105°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 105°C - P_D \bullet \theta_{JA}$$

$$T_A = 105°C - (V_{OUT} - V_{BAT}) \bullet I_{BAT} \bullet \theta_{JA}$$

Example: Consider an LTC4066/LTC4066-1 operating from a wall adapter with 5V at V_{OUT} providing 0.8A to a 3V Li-Ion battery. The ambient temperature above which the LTC4066/LTC4066-1 will begin to reduce the 0.8A charge current, is approximately:

$$T_A = 105°C - (5V - 3V) \bullet 0.8A \bullet 37°C/W$$

$$T_A = 105°C - 1.6W \bullet 37°C/W = 105°C - 59°C = 46°C$$

The LTC4066/LTC4066-1 can be used above 46°C, but the charge current will be reduced below 0.8A. The charge current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{105°C - T_A}{(V_{OUT} - V_{BAT}) \bullet \theta_{JA}}$$

Consider the above example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{BAT} = \frac{105°C - 55°C}{(5V - 3V) \bullet 37°C/W} = \frac{50°C}{74°C/A} = 0.675A$$

Board Layout Considerations

In order to be able to deliver maximum charge current under all conditions, it is critical that the Exposed Pad on the backside of the LTC4066/LTC4066-1 package is soldered to the board. Correctly soldered to a 2500mm^2 double-sided 1oz. copper board, the LTC4066/LTC4066-1 has a thermal resistance of approximately 37°C/W. Failure

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to make thermal contact between the Exposed Pad on the backside of the package and the copper board will result in thermal resistances far greater than 37°C/W. As an example, a correctly soldered LTC4066/LTC4066-1 can deliver over 1A to a battery from a 5V supply at room temperature. Without a backside thermal connection, this number could drop to less than 500mA.

Furthermore, Pins 6 and 7 are "true No Connect" pins. Therefore, they can be used to improve the amount of metal used to connect to Pin 5 or Pin 8.

V_{IN} and Wall Adapter Bypass Capacitor

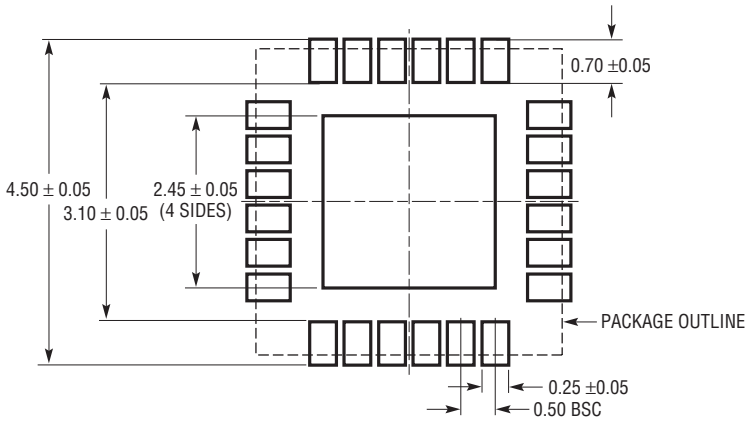
Many types of capacitors can be used for input bypassing. However, caution must be exercised when using multilayer ceramic capacitors. Because of the self resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a hot power source. For more information, refer to Application Note 88.

Stability

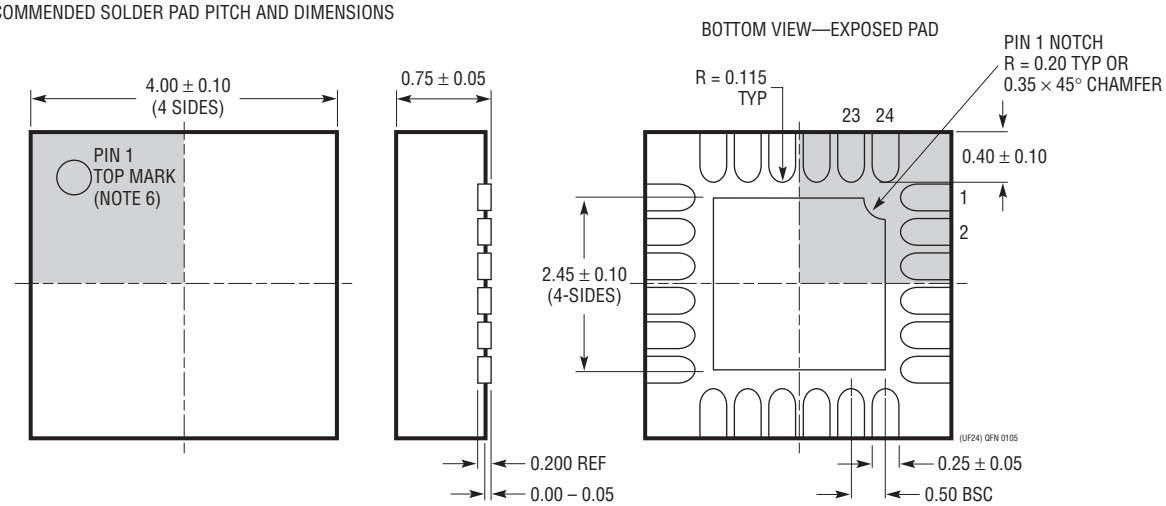
The constant-voltage mode feedback loop is stable without any compensation when a battery is connected. However, a 4.7µF capacitor with a 1Ω series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



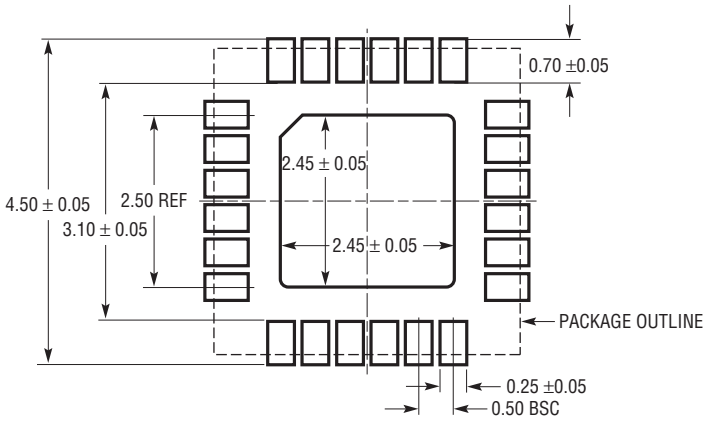
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



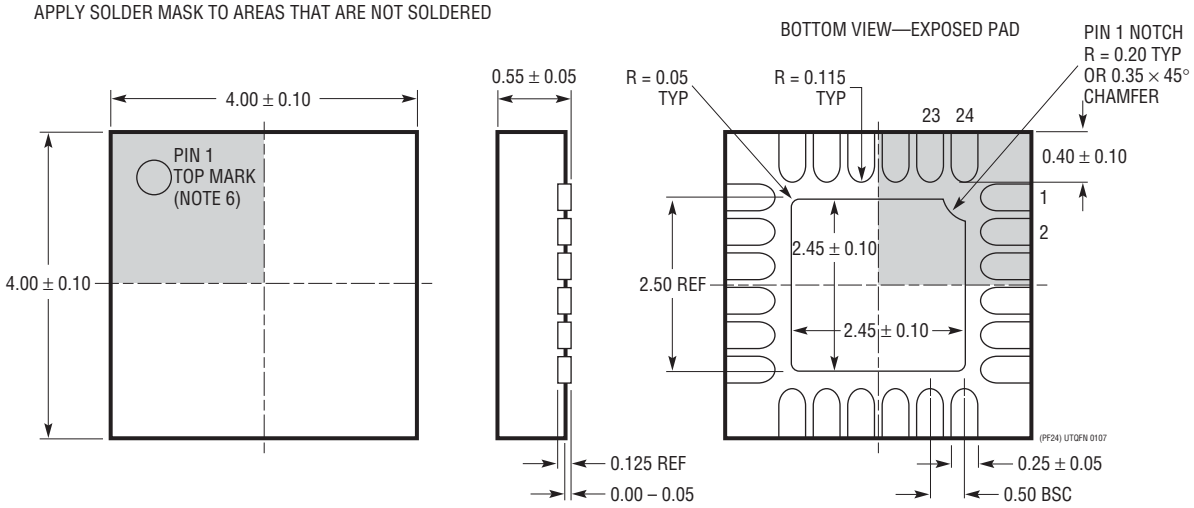
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

PF Package
24-Lead Plastic UTQFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1748 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE