Li-Ion/Polymer Shunt Battery Charger System

FEATURES

- **Low Operating Current (450nA)**
- **1% Float Voltage Accuracy Over Full Temperature and Shunt Current Range**
- **50mA Maximum Internal Shunt Current (500mA with External PFET)**
- **Pin Selectable Float Voltage Options: 4.0V, 4.1V, 4.2V**
- **Ultralow Power Pulsed NTC Float Conditioning for Li-Ion/Polymer Protection**
- Suitable for Intermittent, Continuous and Very Low Power Charging Sources
- Low and High Battery Status Outputs
- Simple Low Voltage Load Disconnect Application
- Thermally Enhanced, Low Profile (0.75mm) 8-Lead (2mm × 3mm) DFN and MSOP Packages

APPLICATIONS

- Low Power Li-Ion/Polymer Battery Back-Up
- Solar Power Systems with Back-Up
- Memory Back-Up
- Embedded Automotive
- Thin Film Batteries
- Energy Scavenging/Harvesting

DESCRIPTION

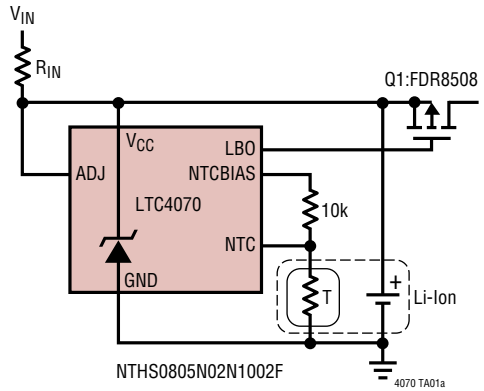
The LTC®4070 allows simple charging of Li-Ion/Polymer batteries from very low current, intermittent or continuous charging sources. The 450nA to 50mA operating current makes charging possible from previously unusable sources. With the addition of an external pass device, shunt current may be boosted to 500mA. Stacked cell high voltage battery packs are inherently balanced with shunt charging. With its low operating current, the LTC4070 is well suited to charge thin film batteries in energy harvesting applications where charging sources may be intermittent or very low power. The unique architecture of the LTC4070 allows for an extremely simple battery charger solution; requiring just one external resistor.

The LTC4070 offers a pin selectable float voltage with 1% accuracy across the full range of operating temperature and shunt current. The integrated thermal battery qualifier extends battery lifetime and improves reliability by automatically reducing the battery float voltage at NTC thermistor temperatures above 40°C. The LTC4070 also provides both low and high battery status outputs. For applications requiring pack protection, see LTC4071.

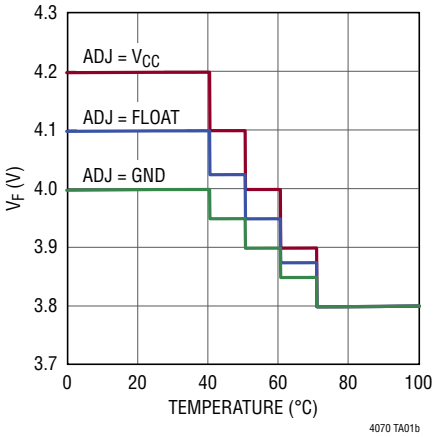
The device is offered in two thermally enhanced packages, a compact low profile (0.75mm) 8-lead (2mm × 3mm) DFN and an 8-lead MSOP package.

TYPICAL APPLICATION

Simple Shunt Charger with Load Disconnect and NTC Conditioning



NTC Overtemperature Battery Float Voltage Qualifying

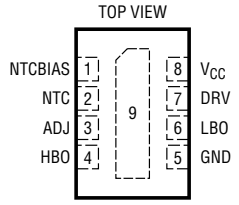


Rev. D

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

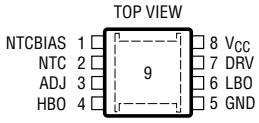
I_{CC} ..... ±60mA
ADJ, NTC, NTCBIAS, DRV, LBO, HBO
Voltages ..... –0.3V to V_{CC} + 0.3V
Operating Junction Temperature Range .. –40°C to 125°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Peak Reflow Temperature ..... 260°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS NOT INTERNALLY CONNECTED,
MUST BE SOLDERED TO PCB, GND TO OBTAIN θ_{JA}



MS8E PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 9) IS NOT INTERNALLY CONNECTED,
MUST BE SOLDERED TO PCB, GND TO OBTAIN θ_{JA}

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4070EDDB#TRMPBF	LTC4070EDDB#TRPBF	LFPD	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC4070IDDB#TRMPBF	LTC4070IDDB#TRPBF	LFPD	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LTC4070EMS8E#TRMPBF	LTC4070EMS8E#TRPBF	LTFMT	8-Lead Plastic MSOP	–40°C to 125°C
LTC4070IMS8E#TRMPBF	LTC4070IMS8E#TRPBF	LTFMT	8-Lead Plastic MSOP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range. V_{NTC} = V_{CC}, T_A = 25°C unless otherwise specified. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FLOAT}	Programmable Float Voltage 10µA ≤ I_{CC} ≤ 50mA	V_{ADJ} = 0V V_{ADJ} = Float V_{ADJ} = V_{CC}	● ● ●	3.96 4.06 4.16	4.0 4.1 4.2	4.04 4.14 4.24	V V V
I_{CCMAX}	Maximum Shunt Current	V_{CC} > V_{FLOAT}	●	50			mA
I_{CCQ}	V_{CC} Operating Current	V_{HBO} Low	●		450	1040	nA
I_{CCQLB}	Low Bat V_{CC} Operating Current	V_{CC} = 3.1V			300		nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range. $V_{NTC} = V_{CC}$, $T_A = 25°C$ unless otherwise specified. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
High Battery Status							
V_{HBTH}	HBO Threshold ($V_{FLOAT} - V_{CC}$)	V_{CC} Rising	●	15	40	60	mV
V_{HBHY}	Hysteresis				100		mV
Low Battery Status							
V_{LBTH}	LBO Threshold	V_{CC} Falling	●	3.08	3.2	3.34	V
V_{LBHY}	Hysteresis			220	290	350	mV
Status Outputs HBO/LBO							
V_{OL}	CMOS Output Low	I_{SINK} = 1mA, V_{CC} = 3.7V	●			0.5	V
V_{OH}	CMOS Output High	V_{LBO}: V_{CC} = 3.1V, I_{SOURCE} = –100µA V_{HBO}: I_{CC} = 1.5mA, I_{SOURCE} = –500µA	●	V_{CC} – 0.6			V
3-State Selection Input: ADJ							
V_{ADJ}	ADJ Input Level	Input Logic Low Level	●			0.3	V
		Input Logic High Level	●	V_{CC} – 0.3			V
$I_{ADJ(Z)}$	Allowable ADJ Leakage Current in Floating State		●			±3	µA
NTC							
I_{NTC}	NTC Leakage Current	0V< NTC < V_{CC}		–50	0	50	nA
$I_{NTCBIAS}$	Average NTCBIAS Sink Current	Pulsed Duty Cycle < 0.002%			30		pA
$\Delta V_{FLOAT(NTC)}$	Delta Float Voltage per NTC Comparator Step	I_{CC} = 1mA, NTC Falling Below One of the NTC_{TH} Thresholds ADJ = 0V ADJ = Float ADJ = V_{CC}			 –50 –75 –100		 mV mV mV
NTC_{TH1}	NTC Comparator Falling Thresholds	V_{NTC} as % of $V_{NTCBIAS}$ Amplitude		35.5	36.5	37.5	%
NTC_{TH2}				28.0	29.0	30.0	%
NTC_{TH3}				21.8	22.8	23.8	%
NTC_{TH4}				16.8	17.8	18.8	%
NTC_{HY}	Hysteresis				30		mV
Drive Output							
$I_{DRV(SOURCE)}$	DRV Output Source Current	V_{CC} = 3.1V, V_{DRV} = 0V			–1		mA
$I_{DRV(SINK)}$	DRV Output Sink Current	I_{CC} = 1mA, R_{DRV} = 475k (Note 3)			3		µA

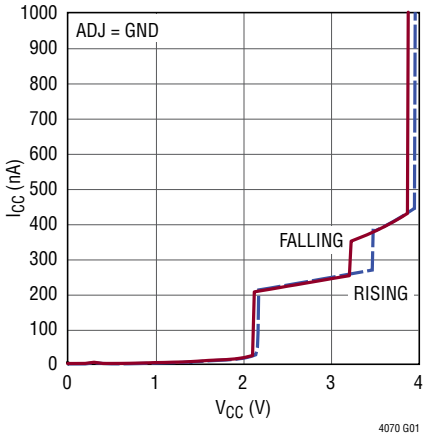
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4070 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4070E is guaranteed to meet performance specifications for junction temperatures from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4070I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

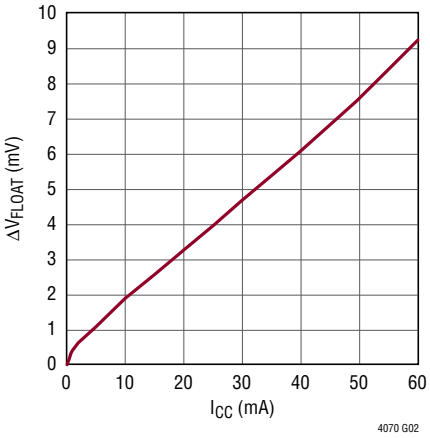
Note 3: The $I_{DRV(SNK)}$ current is tested by pulling the DRV pin up to V_{CC} through a 475k resistor, R_{DRV}. Pulling the DRV pin up to V_{CC} with low impedance disables the regulator.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

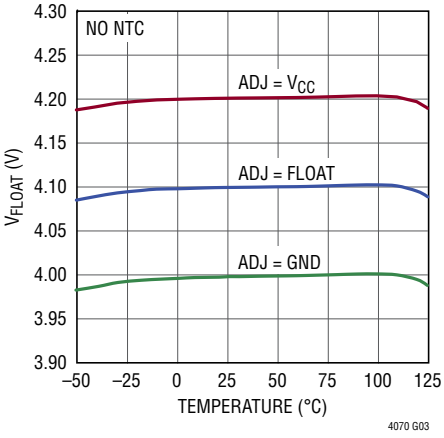
Battery Discharge I_{CC} vs V_{CC}



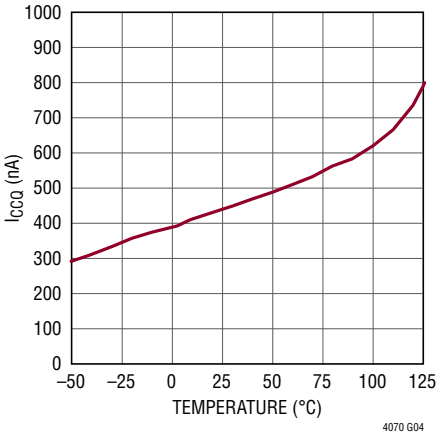
Load Regulation ΔV_{FLOAT} vs I_{CC}



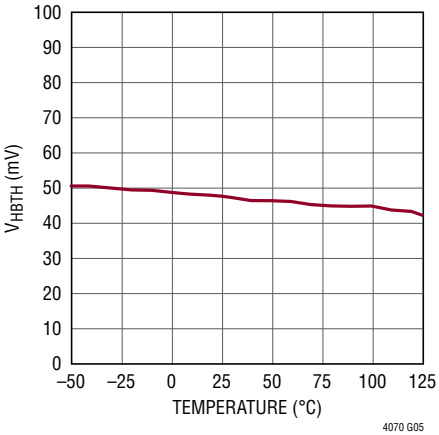
V_{FLOAT} vs Temperature, I_{CC} = 1mA



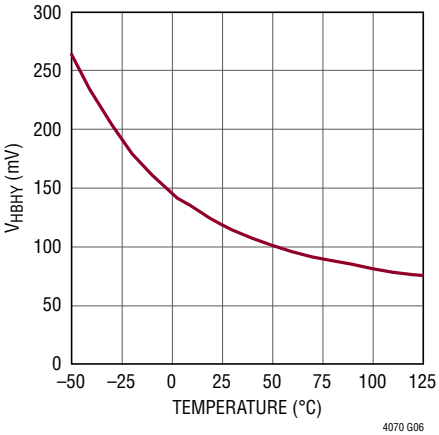
I_{CCQ} vs Temperature (ADJ = V_{CC})



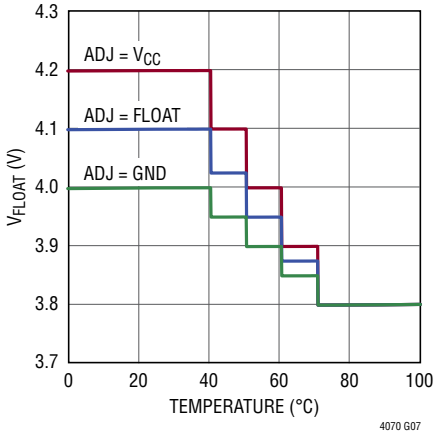
V_{HBTH} V_{CC} Rising vs Temperature (ADJ = V_{CC})



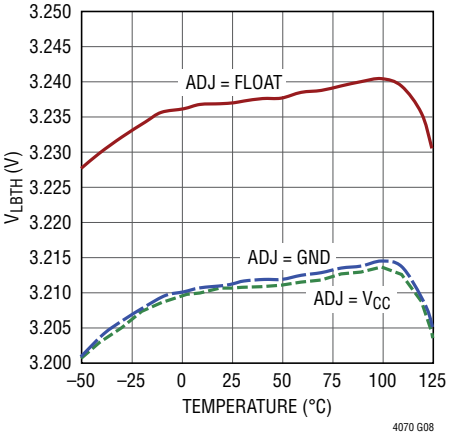
V_{HBHY} vs Temperature (ADJ = V_{CC})



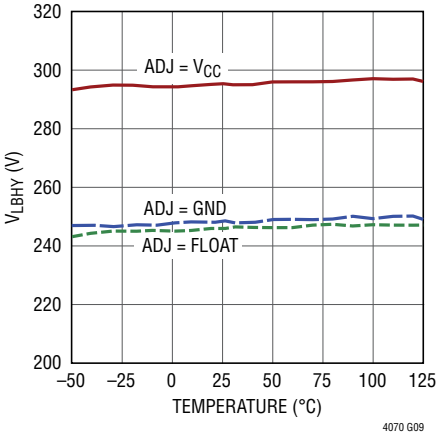
V_{FLOAT} vs NTC Temperature, I_{CC} = 1mA



V_{LBTH} V_{CC} Falling vs Temperature

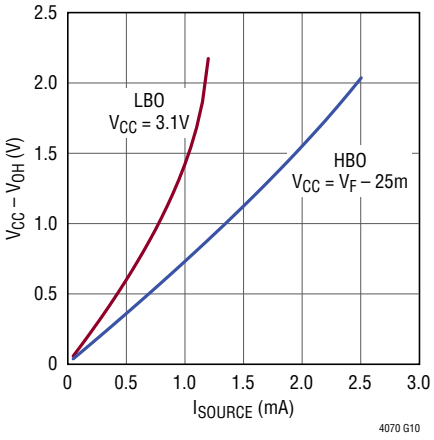


V_{LBHY} vs Temperature

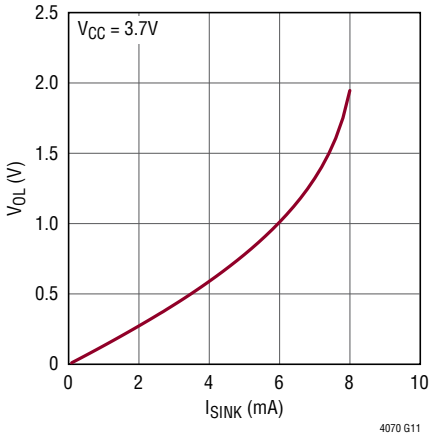


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

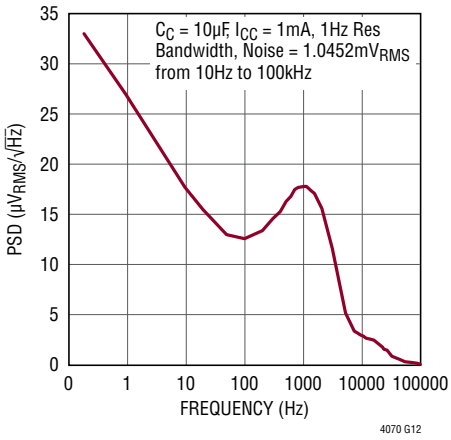
V_{OH} LBO/HBO vs I_{SOURCE}



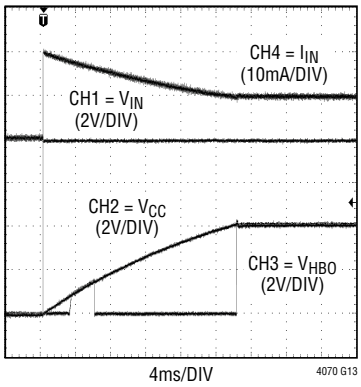
V_{OL} LBO/HBO vs I_{SINK}



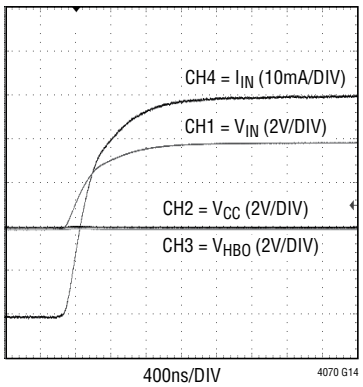
Power Spectral Density



Hot Plug Transient, C_C = 330µF, R_{IN} = 81Ω



Step Response with 800mAHr Battery, R_{IN} = 81Ω



PIN FUNCTIONS

NTCBIAS (Pin 1): NTC Bias Pin. Connect a resistor from NTCBIAS to NTC, and a thermistor from NTC to GND. Float NTCBIAS when not in use. Minimize parasitic capacitance on this pin.

NTC (Pin 2): Input to the Negative Temperature Coefficient Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery to determine the temperature of the battery. If the battery temperature is too high, the float voltage is reduced. Connect a low drift bias resistor from NTCBIAS to NTC and a thermistor from NTC to GND. When not in use, connect NTC to V_{CC}. Minimize parasitic capacitance on this pin.

ADJ (Pin 3): Float Voltage Adjust Pin. Connect ADJ to GND to program 4.0V float voltage. Disconnect ADJ to program 4.1V float voltage. Connect ADJ to V_{CC} to program 4.2V float voltage. The float voltage is also adjusted by the NTC thermistor.

PIN FUNCTIONS

HBO (Pin 4): High Battery Monitor Output (Active High). HBO is a CMOS output that indicates that the battery is almost fully charged and current is being shunted away from BAT. This pin is driven high when V_{CC} rises to within V_{HBTH} of the effective float voltage. The absolute value of this threshold depends on ADJ and NTC, both of which affect the float voltage. HBO is driven low when V_{CC} falls by more than (V_{HBTH} + V_{HBHY}) below the float voltage. Refer to Table 1 for the effective float voltage.

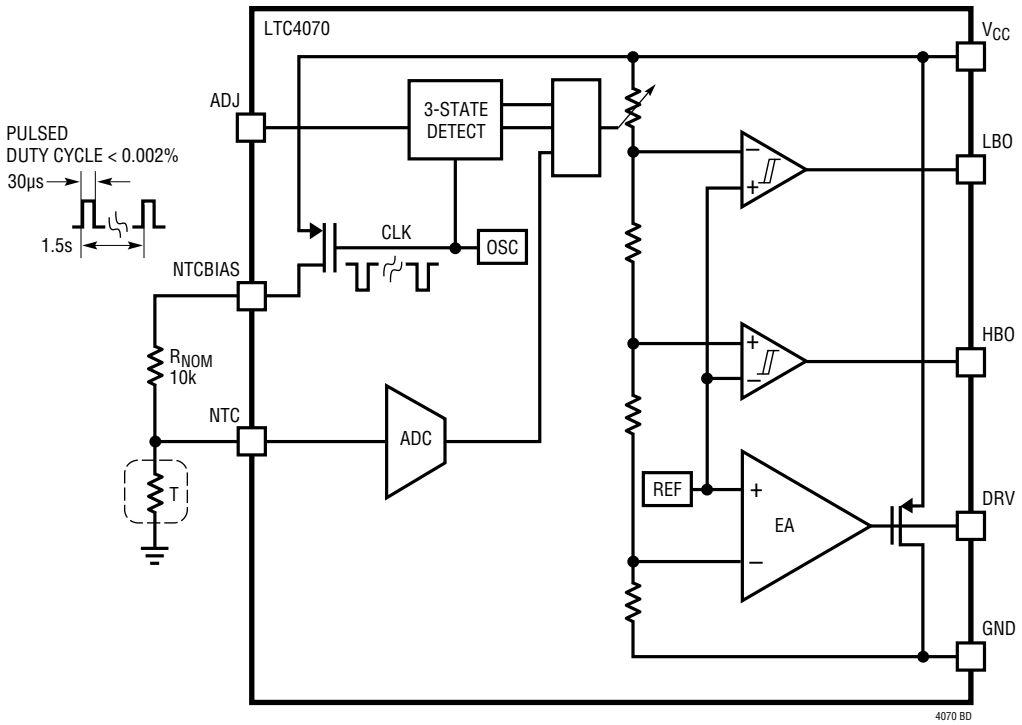
GND (Pin 5, Exposed Pad Pin 9): Ground. The exposed package pad must be connected to PCB ground for rated thermal performance.

LBO (Pin 6): Low Battery Monitor Output (Active High). LBO is a CMOS output that indicates when the battery is discharged below 3.2V or rises above 3.5V. This pin is driven high if $V_{CC} < V_{LBTH}$, and is driven low if $V_{CC} > (V_{LBTH} + V_{LBHY})$.

DRV (Pin 7): External Drive Output. Connect to the gate of an external PFET to increase shunt current for applications which require more than 50mA charge current. Minimize capacitance and leakage current on this pin. When not in use, float DRV.

V_{CC} (Pin 8): Input Supply Pin. The input supply voltage is regulated to 4.0V, 4.1V, or 4.2V depending on the ADJ pin state (see the ADJ pin description for more detail). This pin can sink up to 50mA in order to keep the voltage regulation within accuracy limits. When no battery is present, decouple to GND with a capacitor, C_{IN}, of at least 0.1µF.

BLOCK DIAGRAM



OPERATION

The LTC4070 provides a simple, reliable, and high performance battery protection and charging solution by preventing the battery voltage from exceeding a programmed level. Its shunt architecture requires just one resistor between the input supply and the battery to handle a wide range of battery applications. When the input supply is removed and the battery voltage is below the high battery output threshold, the LTC4070 consumes just 450nA from the battery.

While the battery voltage is below the programmed float voltage, the charge rate is determined by the input voltage, the battery voltage, and the input resistor:

$$I_{CHG} = \frac{(V_{IN} - V_{BAT})}{R_{IN}}$$

As the battery voltage approaches the float voltage, the LTC4070 shunts current away from the battery thereby reducing the charge current. The LTC4070 can shunt up to 50mA with float voltage accuracy of ±1% over temperature. The shunt current limits the maximum charge current, but the 50mA internal capability can be increased by adding an external P-channel MOSFET.

Adjustable Float Voltage, V_{FLOAT}

A built-in 3-state decoder connected to the ADJ pin provides three programmable float voltages: 4.0V, 4.1V, or 4.2V. The float voltage is programmed to 4.0V when ADJ is tied to GND, 4.1V when ADJ is floating, and 4.2V when ADJ is tied to V_{CC}. The state of the ADJ pin is sampled about once every 1.5 seconds. When it is being sampled, the LTC4070 applies a relatively low impedance voltage at the ADJ pin. This technique prevents low level board leakage from corrupting the programmed float voltage.

NTC Qualified Float Voltage, $\Delta V_{FLOAT(NTC)}$

The NTC pin voltage is compared against an internal resistor divider tied to the NTCBIAS pin. This divider has tap points that are matched to the NTC thermistor resistance/temperature conversion table for a Vishay thermistor with a $B_{25/85}$ value of 3490 at temperatures of 40°C, 50°C, 60°C, and 70°C.

Battery temperature conditioning adjusts the float voltage down to V_{FLOAT_EFF} when the NTC thermistor indicates that the battery temperature is too high. For a 10k thermistor with a $B_{25/85}$ value of 3490 such as the Vishay NTHS0402N02N1002F, and a 10k NTCBIAS resistor, each 10°C increase in temperature above 40°C causes the float voltage to drop by a fixed amount, $\Delta V_{FLOAT(NTC)}$, depending on ADJ. If ADJ is at GND, the float voltage steps down by 50mV for each 10°C temperature increment. If ADJ is floating, the step size is 75mV. And if ADJ is at V_{CC}, the step size is 100mV. Refer to Table 1 for the range of V_{FLOAT_EFF} programming.

Table 1. NTC Qualified Float Voltage

ADJ	$\Delta V_{FLOAT(NTC)}$	TEMPERATURE	V_{NTC} AS % OF NTCBIAS	V_{FLOAT_EFF}
GND	50mV	T < 40°C	$V_{NTC} > 36.5\%$	4.000V
		40°C ≤ T < 50°C	$29.0\% < V_{NTC} \leq 36.5\%$	3.950V
		50°C ≤ T < 60°C	$22.8\% < V_{NTC} \leq 29.0\%$	3.900V
		60°C ≤ T < 70°C	$17.8\% < V_{NTC} \leq 22.8\%$	3.850V
		70°C < T	$V_{NTC} \leq 17.8\%$	3.800V
Float	75mV	T < 40°C	$V_{NTC} > 36.5\%$	4.100V
		40°C ≤ T < 50°C	$29.0\% < V_{NTC} \leq 36.5\%$	4.025V
		50°C ≤ T < 60°C	$22.8\% < V_{NTC} \leq 29.0\%$	3.950V
		60°C ≤ T < 70°C	$17.8\% < V_{NTC} \leq 22.8\%$	3.875V
		70°C ≤ T	$V_{NTC} \leq 17.8\%$	3.800V
V_{CC}	100mV	T < 40°C	$V_{NTC} > 36.5\%$	4.200V
		40°C ≤ T < 50°C	$29.0\% < V_{NTC} \leq 36.5\%$	4.100V
		50°C ≤ T < 60°C	$22.8\% < V_{NTC} \leq 29.0\%$	4.000V
		60°C ≤ T < 70°C	$17.8\% < V_{NTC} \leq 22.8\%$	3.900V
		70°C ≤ T	$V_{NTC} \leq 17.8\%$	3.800V

For all ADJ pin settings the lowest float voltage setting is $3.8V = V_{FLOAT} - 4 \bullet \Delta V_{FLOAT(NTC)} = V_{FLOAT\_MIN}$. This occurs at NTC thermistor temperatures above 70°C, or if the NTC pin is grounded.

To conserve power in the NTCBIAS and NTC resistors, the NTCBIAS pin is sampled at a low duty cycle at the same time that the ADJ pin state is sampled.

High Battery Status Output: HBO

The HBO pin pulls high when V_{CC} rises to within V_{HBTH} of the programmed float voltage, V_{FLOAT_EFF}, including NTC qualified float voltage adjustments.

If V_{CC} drops below the float voltage by more than $V_{HBTH} + V_{HBHY}$ the HBO pin pulls low to indicate that the battery is not at full charge. The input supply current of the LTC4070 drops to less than 450nA (typ) as the LTC4070 no longer shunts current to protect the battery. The NTCBIAS sample clock slows to conserve power, and the DRV pin is pulled up to V_{CC}.

OPERATION

For example, if the NTC thermistor requires the float voltage to be dropped by 100mV (ADJ = V_{CC} and 0.29•$V_{NTCBIAS}$ < V_{NTC} < 0.36•$V_{NTCBIAS}$) then the HBO rising threshold is detected when V_{CC} rises past $V_{FLOAT} – \Delta V_{FLOAT(NTC)} – V_{HBTH}$ = 4.2V – 100mV – 40mV = 4.06V. The HBO falling threshold in this case is detected when V_{CC} falls below $V_{FLOAT} – \Delta V_{FLOAT(NTC)} – V_{HBTH} – V_{HBHY}$ = 4.2V – 100mV – 40mV – 100mV = 3.96V.

Low Battery Status Output: LBO

When the battery voltage drops below 3.2V, the LBO pin pulls high. Otherwise, the LBO pin pulls low when the battery voltage exceeds about 3.5V.

While the low battery condition persists, NTC and ADJ pins are no longer sampled—the functions are disabled—and total supply consumption for the LTC4070 drops to less than 300nA (typ).

APPLICATIONS INFORMATION

General Charging Considerations

The LTC4070 uses a different charging methodology from previous chargers. Most Li-Ion chargers terminate the charging after a period of time. The LTC4070 does not have a discrete charge termination. Extensive measurements on Li-Ion cells show that the cell charge current drops to nanoamps with the shunt charge control circuit effectively terminating the charge. For long cell life, operate the charger at 100mV lower charge voltage normally used.

The simplest application of the LTC4070 is shown in Figure 1. This application requires only an external resistor to program the charge/shunt current. Assume the wall adapter voltage (V_{WALL}) is 12V and the minimum battery voltage (V_{BAT_MIN}) is 3V, then the maximum charge current is calculated as:

$$I_{MAX\_CHARGE} = \frac{\left(V_{WALL} - V_{BAT\_MIN}\right)}{R_{IN}}$$

$$= \frac{(12V - 3V)}{162\Omega} = 55.5mA$$

Care must be taken in selecting the input resistor. Power dissipated in RIN under full charge current is given by the following equation:

$$P_{DISS} = \frac{\left(V_{WALL} - V_{BAT\_MIN}\right)^2}{R_{IN}} = \frac{(12V - 3V)^2}{162\Omega} = 0.5W$$

The charge current decreases as the battery voltage increases. If the rising battery voltage is 40mV less than the programmed float voltage, the LTC4070 consumes only 450nA of current, and all of the input current flows into the battery. As the battery voltage reaches the float voltage, the LTC4070 shunts current from the wall adapter and regulates the battery voltage to V_{FLOAT}. The more shunt current the LTC4070 sinks, the less charge current the battery gets. Eventually, the LTC4070 shunts all the current from the battery; up to the maximum shunt current. The maximum shunt current in this case, with no NTC adjustment, is determined by the input resistor and is calculated as:

$$I_{SHUNT\_MAX} = \frac{\left(V_{WALL} - V_{FLOAT}\right)}{R_{IN}} = \frac{(12V - 4.1V)}{162\Omega} = 49mA$$

At this point the power dissipated in the input resistor is 388mW.

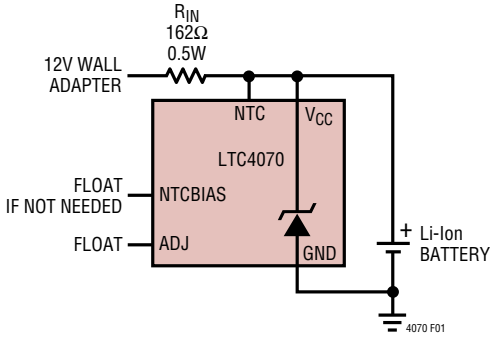


Figure 1. Single-Cell Battery Charger

APPLICATIONS INFORMATION

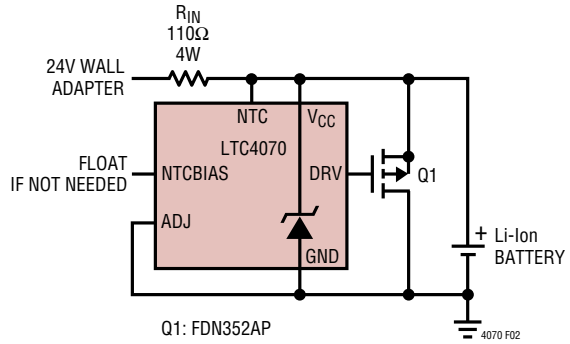


Figure 2. Single-Cell Charger with Boosted Drive

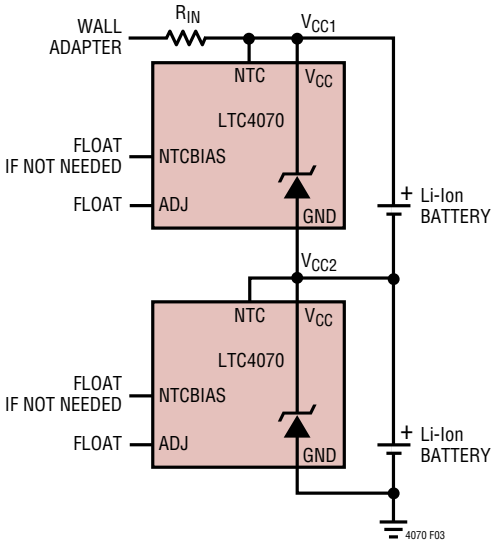


Figure 3. 2-Cell Battery Charger

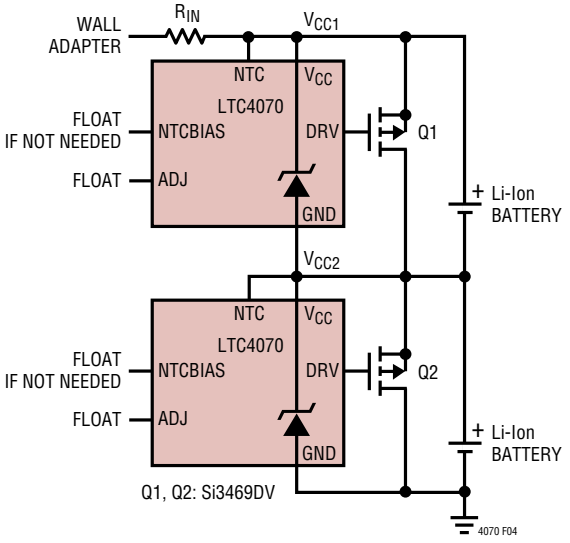


Figure 4. 2-Cell Battery Charger with Boosted Drive

Figure 2 shows a charge circuit that can boost the charge current as well as the shunt current with an external P-channel MOSFET, Q1. In this case, if the wall adapter voltage (V_{WALL}) is 24V and the minimum battery voltage (V_{BAT}) is 3V, then the initial charge current is set to 191mA by selecting R_{IN} = 110Ω. Note that this resistor dissipates over 4W of power, so select the resistor taking power rating into account. When the battery voltage reaches the float voltage, the LTC4070 and the external P-channel MOSFET begin to shunt current from the wall adapter. Eventually, the LTC4070 and the external P-channel MOSFET shunts all available current (182mA) and no current flows to the battery. Take the full shunt current and power into account when selecting the external MOSFET.

The LTC4070 can also be used to regulate series-connected battery stacks as illustrated in Figure 3 and Figure 4. Here two LTC4070 devices are used to charge two batteries in series; with or without boosted drive. A single resistor sets the maximum charge/shunt current. The GND pin of the top device is simply connected to the V_{CC} pin of the bottom device. Care must be taken in observing the status output pins of the top device as these signals are not ground referenced. Also, the wall adapter must have a high enough voltage rating to charge both cells.

NTC Protection

The LTC4070 measures battery temperature with a negative temperature coefficient thermistor thermally coupled to the battery. NTC thermistors have temperature characteristics which are specified in resistance-temperature conversion tables. Internal NTC circuitry protects the battery from excessive heat by reducing the float voltage for each 10°C rise in temperature above 40°C (assuming a Vishay thermistor with a $B_{25/85}$ value of 3490).

The LTC4070 uses a ratio of resistor values to measure battery temperature. The LTC4070 contains an internal fixed resistor voltage divider from NTCBIAS to GND with four tap points; NTC_{TH1}-NTC_{TH4}. The voltages at these tap points are periodically compared against the voltage at the NTC pin to measure battery temperature. To conserve power, the battery temperature is measured periodically by biasing the NTCBIAS pin to V_{CC} about once every 1.5 seconds.

APPLICATIONS INFORMATION

The voltage at the NTC pin depends on the ratio of the NTC thermistor value, R_{NTC}, and a bias resistor, R_{NOM}. Choose R_{NOM} equal to the value of the thermistor at 25°C. R_{NOM} is 10k for a Vishay NTHS0402N02N1002F thermistor with a $B_{25/85}$ value of 3490. R_{NOM} must be connected from NTCBIAS to NTC. The ratio of the NTC pin voltage to the NTCBIAS voltage is:

$$\frac{R_{NTC}}{(R_{NTC} + R_{NOM})}$$

When the thermistor temperature rises, the resistance drops; and the resistor divider between R_{NOM} and the thermistor lowers the voltage at the NTC pin.

An NTC thermistor with higher $B_{25/85}$ values may also be used with the LTC4070. However the temperature trip points are shifted due to the higher negative temperature coefficient of the thermistor. To correct for this difference add a resistor, R_{FIX}, in series with the higher $B_{25/85}$ value thermistor to shift the ratio,

$$\frac{R_{FIX} + R_{NTC}}{(R_{FIX} + R_{NTC} + R_{NOM})}$$

up to the internal resistive divider tap points: NTC_{TH1} through NTC_{TH4}. For a 100k thermistor with a $B_{25/85}$ value of 3950 NTHS0402N01N1003F, at 70°C (with R_{NOM} = 100k) choose R_{FIX} = 3.92kΩ. The temperature trip points are found by looking up the thermistor R/T values plus R_{FIX} that correspond to the ratios for NTC_{TH1} = 36.5%, NTC_{TH2} = 29.0%, NTC_{TH3} = 22.8%, and NTC_{TH4} = 17.8%. Selecting R_{FIX} = 3.92k results in trip points of 39.9°C, 49.4°C, 59.2°C and 69.6°C.

Another technique may be used without adding an additional component. Instead decrease R_{NOM} to adjust the NTC_{TH} thresholds for a given R/T thermistor profile. For example, if R_{NOM} = 88.7k (with the same 100k thermistor) then the temperature trip points are 41.0°C, 49.8°C, 58.5°C, and 67.3°C.

When using the NTC features of the LTC4070 it is important to keep in mind that the maximum shunt current increases as the float voltage, V_{FLOAT_EFF} drops with NTC conditioning. Reviewing the Typical Applications with a 12V wall adapter in Figure 1; the input resistor, R_{IN}, should be increased to 165Ω such that the maximum shunt current does not exceed 50mA at the lowest possible float voltage due to NTC conditioning, V_{FLOAT_MIN} = 3.8V.

Thermal Considerations

At maximum shunt current, the LTC4070 may dissipate up to 205mW. The thermal dissipation of the package should be taken into account when operating at maximum shunt current so as not to exceed the absolute maximum junction temperature of the device. With θ_{JA} of 40°C/W, in the MSOP package, at maximum shunt current of 50mA the junction temperature rise is about 8°C above ambient. With θ_{JA} of 76°C/W in the DFN package, at maximum shunt current of 50mA the junction temperature rise is about 16°C above ambient.

Operation with an External PFET to Boost Shunt Current

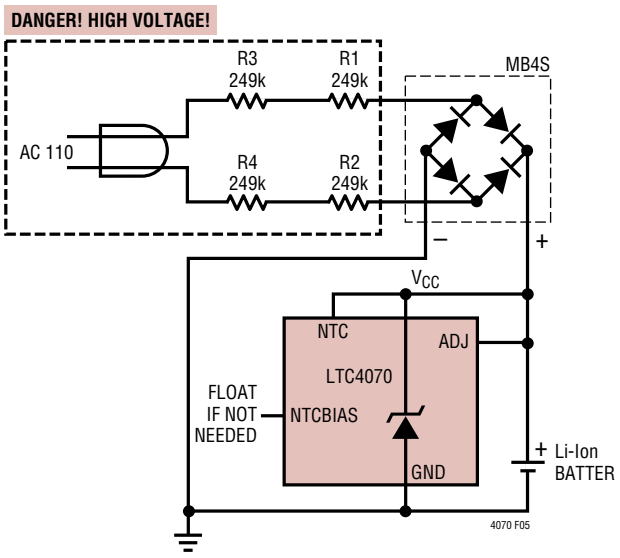
Recommended External Shunt PFETS lists recommended devices to increase the maximum shunt current. Due to the requirement for low capacitance on the DRV pin node, it is recommended that only low gate charge and high threshold PFET devices be used. Also it is recommended that careful PCB layout be used to keep leakage at the DRV pin to a minimum as the $I_{DRV(SINK)}$ current is typically 3µA.

Refer to device manufacturers data sheets for maximum continuous power dissipation and thermal resistance when selecting an external PFET for a particular application.

Table 2. Recommended External Shunt PFETS

DEVICE	VENDOR	Q_{GS}	$V_{TH(MIN)}$	$R_{DS(ON)}$
FDN352AP	Fairchild	0.50nC	–0.8V	0.33
Si3467DV	Vishay	1.7nC	–1.0V	0.073
Si3469DV	Vishay	3.8nC	–1.0V	0.041
DMP2130LDM	Diodes Inc.	2.0nC	–0.6V	0.094
DMP3015LSS	Diodes Inc.	7.2nC	–1.0V	0.014

TYPICAL APPLICATIONS



DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN AC LINE-CONNECTED CIRCUITS! BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF AC LINE-CONNECTED CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. ALL TESTING PERFORMED ON AN AC LINE-CONNECTED CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE AC LINE AND THE CIRCUIT. USERS AND CONSTRUCTORS OF AC LINE-CONNECTED CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK.

Figure 5. 4.2V AC Line Charging, UL Leakage Okay

The LTC4070 can be used to charge a battery to a 4.2V float voltage from an AC line with a bridge rectifier as shown in the simple schematic in Figure 5. In this example, the four input 249k resistors are sized for acceptable UL leakage in the event that one of the resistors short. Here, the LTC4070 will fully charge the battery from the AC line while meeting the UL specification with only 104µA of available charge current.

A photovoltaic (PV) application for the LTC4070 is illustrated in Figure 6. In this application, transistor Q1 has been added to further reduce the already low quiescent current of the LTC4070 to achieve extremely low battery discharge when the PV cells are not charging the battery. In long battery life applications, Q1 isolates the battery from the LTC4070 when Q1's base voltage falls. Under normal operation, the PV cells provide current through the V_{BE} and V_{BC} diodes of Q1. While the battery is charging, the majority of PV current flows to the battery. When V_{CC} reaches the programmed float voltage, in this case 4.1V with ADJ floating, then the LTC4070 shunts base-collector junction current from Q1, effectively reducing the battery charging current to zero and saturating Q1. In the event that the thermistor temperature rises and the float voltage drops, the LTC4070 shunts more current, and Q1 is forced to operate in reverse active mode until the battery voltage falls. Once equilibrium is achieved, the difference between V_{BAT} and V_{CC} should be less than a few mV, depending on the magnitude of the shunt current.

Add a series input resistor, R_{IN}, to limit the current from high current solar cells. Solar cells are limited in current normally, so for small cells no resistor is needed. With high current PV cells, select R_{IN} taking into account the PV cell's open-circuit voltage and short-circuit current, the temperature coefficient of the V_{BC} and V_{BE} diodes and the maximum collector current and operating junction temperature of Q1. Using an isolating transistor reduces discharge current to a few nanoamps, and may be extended to other applications as well.

The PV application schematic in Figure 6 also illustrates using the LTC4070 with a 10k, 5% curve 2 type NTC thermistor, NTHS0402N02N1002F. Here R_{NOM} is 10k, and the rising temperature trip points are 40°C, 50°C, 60°C and 70°C.

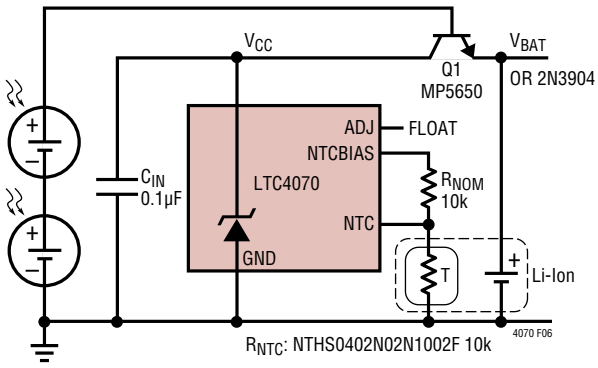


Figure 6. Photovoltaic Charger with Extremely Low Leakage When Not Charging

TYPICAL APPLICATIONS

The LTC4070 status pins have sufficient drive strength to use with an LED, for a visual indication of charging status. Consider the application in Figure 7, where red LED D1 is connected to the LBO pin and turns off when the battery voltage is below V_{LBTH}. Note that LED D1 discharges the battery until V_{CC} falls below V_{LBTH}. Green LED D2, connected to the HBO pin turns on while the battery is charging. When the battery voltage rises to within V_{HBTH} of the float voltage including NTC qualification, V_{FLOAT_EFF}, D2 turns off to indicate that the battery is no longer charging. Optionally, a low leakage diode D3 is placed between the cathode of D2 and the battery. This diode stops D2 from discharging the battery when the input supply is not present.

In this application, R_{IN} = 205Ω, is sized for a maximum shunt current of 50mA that occurs at the maximum input voltage of 15V and the minimum NTC qualified float voltage of 3.8V, assuming the voltage drop on diode D3 is 1.1V. Without the optional D3, R_{IN} increases to 226Ω.

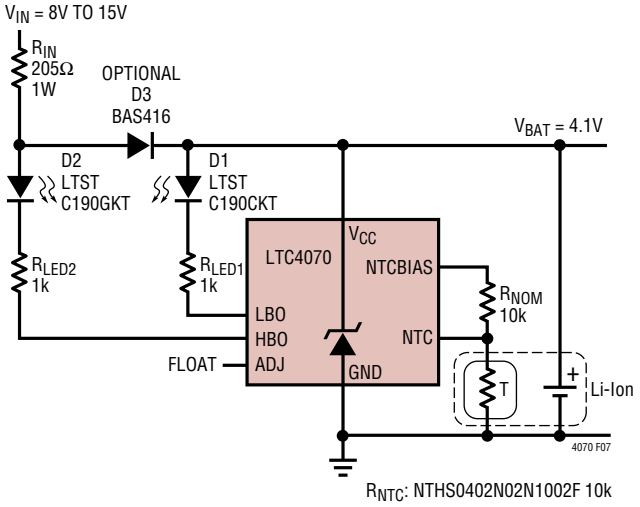


Figure 7. Single Cell Charger with LED Status and NTC Qualified Float Voltage

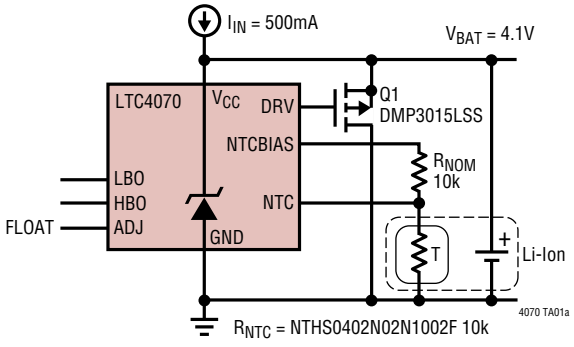


Figure 8. Replace Three NiMH with Lithium

Figure 8 illustrates an application to replace three NiMH cells with a single Li-Ion cell. This simple application replaces the NiMH charging solution without the need for a charge termination or cell balancing scheme. NiMH charging can be done without termination, but that algorithm limits the charge rate to C/10. The LTC4070 application allows the Li-Ion battery to be charged faster without concern of over-charging.

Figure 9, 12V Wall Adapter Charging with 205mA, illustrates the use of an external PFET transistor to boost the maximum shunt current. If the battery voltage is 3.6V the battery receives the full charge current of about 205mA. If the battery temperature is below 40°C, the float voltage rises to 4.1V (ADJ = floating) then Q1 and the LTC4070 shunts 192mA away from the battery. If the battery temperature rises, the shunt current increases to regulate the float voltage 75mV lower per 10°C rise in battery temperature, as described in Table 1. At a maximum shunt current of 200mA the minimum float voltage is held at 3.8V when the battery temperature is above 70°C.

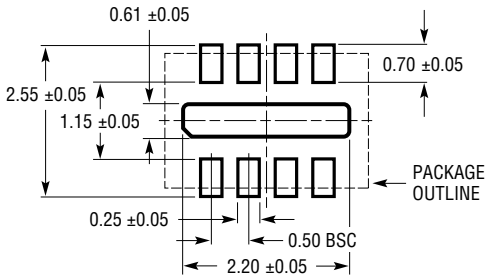
This example illustrates an alternative use of a LED, D1, to observe the HBO status pin. This LED turns on to provide a visual indication that the battery is fully charged, and shunts about 1.5mA when the battery rises to within 40mV of the desired float voltage. LED D1 discharges the battery, when no supply is present, until V_{CC} falls by more than V_{HBTH} + V_{HBHY} below the float voltage. When using an LED with the HBO pin in this configuration, it is important to limit the LED current with a resistor, R_{LED} as shown. Otherwise the step in current through R_{IN} that occurs when the LED turns on may pull V_{CC} below the HBO hysteresis. To prevent that situation, the ratio of R_{IN} to R_{LED} should be selected to meet the following relation:

$$\frac{R_{IN}}{R_{LED}}\left(V_{CC} - V_{LED}\right) < V_{HBHY} - 50mV$$

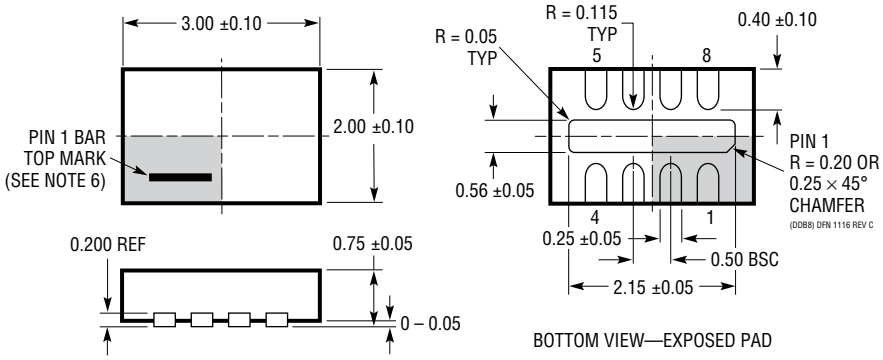
where V_{LED} is the forward voltage drop of the LED and a margin of 50mV is subtracted from the HBO hysteresis. A V_{LED} value of 1.1V is assumed for this example. Refer to the LED data sheet for the forward voltage drop at the applied current level.

PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

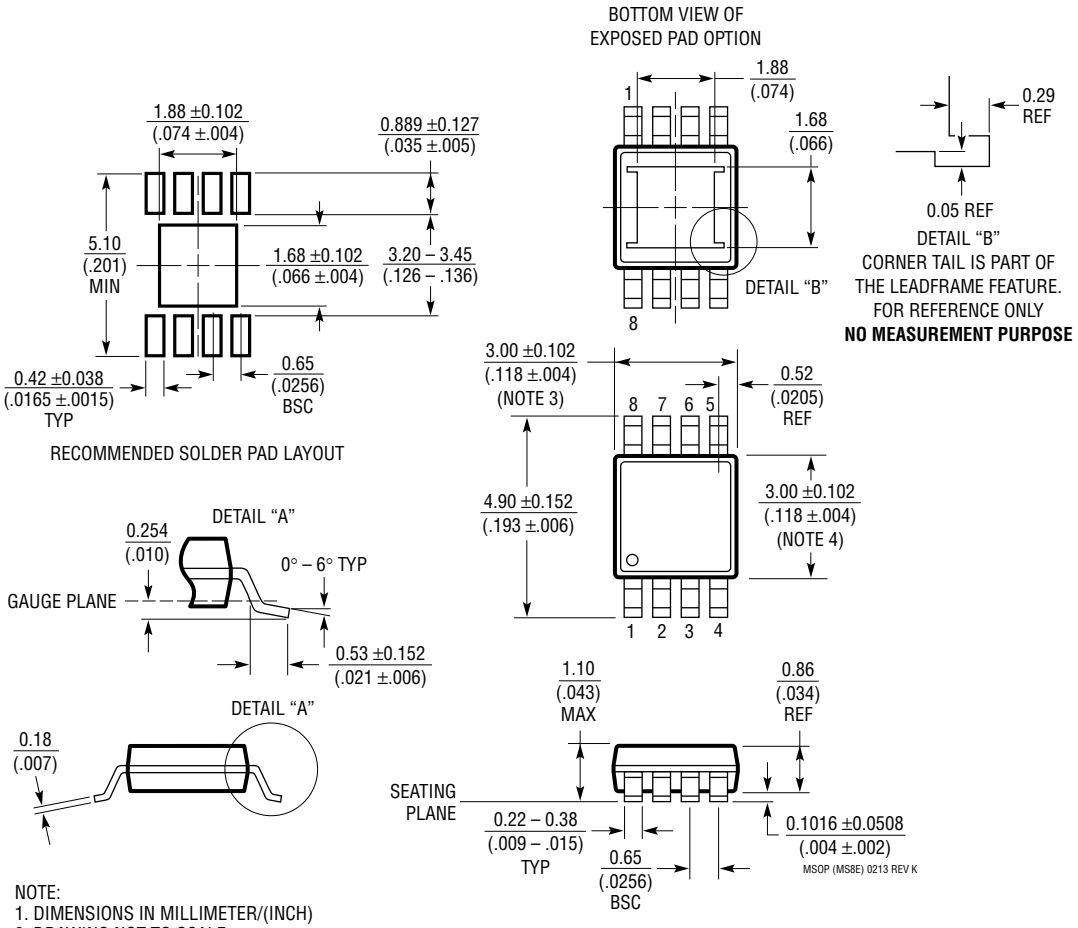


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/10	Change Q1's Part Number on Figure 6	12
B	9/10	Updated Description section	1
		Temperature Range updated in Order Information section	2
		Updated Note 2	3
		Text updated in "NTC Qualified Float Voltage, $\Delta V_{FLOAT(NTC)}$" section	7
		Text updated in "NTC Protection" section	9, 10
		Updated Related Parts section	16
C	4/11	Updated Vishay thermistor part number.	1, 7, 10, 11, 12, 16
D	2/20	Revised Order Information table	2