# Li-Ion/Polymer Shunt Battery Charger System with Low Battery Disconnect

## FEATURES

- **Charger Plus Pack Protection in One IC**
- **Low Operating Current (550nA)**
- **Near Zero Current (<0.1nA) Low Battery Disconnect Function to Protect Batteries from Over-Discharge**
- **Pin Selectable Low Battery Disconnect Level: 2.7V or 3.2V**
- 1% Float Voltage Accuracy Over Temperature
- 50mA Maximum Internal Shunt Current
- Pin Selectable Float Voltage Options: 4.0V, 4.1V, 4.2V
- Ultralow Power Pulsed NTC Float Conditioning for Li-Ion/Polymer Protection
- Suitable for Intermittent, Continuous and Very Low Power Charging Sources
- High Battery Status Output
- Thermally Enhanced, Low Profile (0.75mm) 8-Lead (2mm × 3mm) DFN and MSOP Packages

## APPLICATIONS

- Low Capacity, Li-Ion/Polymer Battery Back-Up
- Thin Film Batteries
- Energy Scavenging/Harvesting
- Solar Power Systems with Back-Up
- Memory Back-Up
- Embedded Automotive

## DESCRIPTION

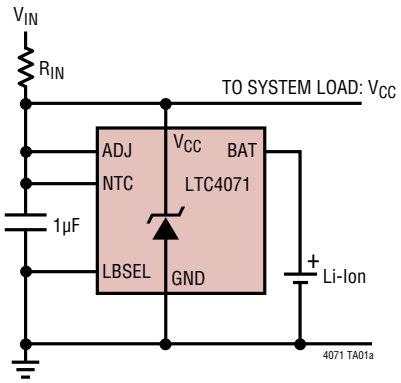
The LTC®4071 allows simple charging of Li-Ion/Polymer batteries from very low current, intermittent or continuous charging sources. A near-zero current low battery latching disconnect function protects even the lowest capacity batteries from deep discharge and potentially irreparable damage. The 550nA to 50mA operating current makes charging possible from previously unusable sources. With its low operating current the LTC4071 is well suited to charge low capacity Li-Ion or thin film batteries in energy harvesting applications. The unique architecture of the LTC4071 allows for an extremely simple battery charger solution, requiring just one external resistor.

The LTC4071 offers a pin selectable float voltage with ±1% accuracy. The integrated thermal battery qualifier extends battery lifetime and improves reliability by automatically reducing the battery float voltage at NTC thermistor temperatures above 40°C. The LTC4071 also provides two pin selectable low battery disconnect levels and a high battery status output.

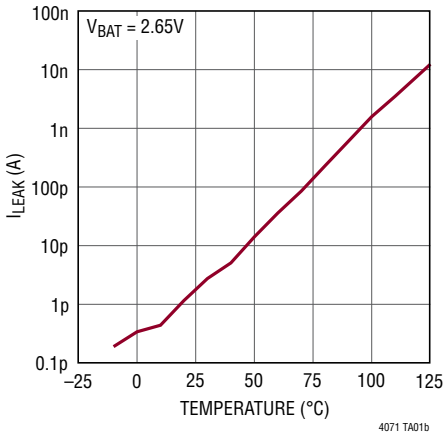
The device is offered in two thermally enhanced packages, a compact low profile (0.75mm) 8-lead (2mm × 3mm) DFN and an 8-lead MSOP package.

All registered trademarks and trademarks are the property of their respective owners.

## TYPICAL APPLICATION




**Battery Disconnect $I_{LEAK}$ vs Temperature**

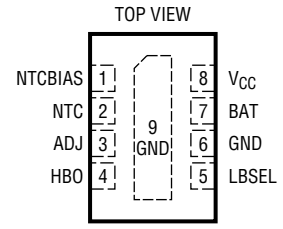



Rev. D

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

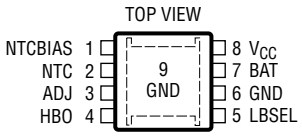
$I_{CC}$, $I_{BAT}$ ..... ±60mA Continuous
$I_{BAT}$ ..... 400mA for Single Pulse < 10ms
$I_{CC}$ ..... –400mA for Single Pulse < 10ms
ADJ, NTC, NTCBIAS, HBO Voltages .. –0.3V to $V_{CC}$ + 0.3V
LBSEL Voltage ..... –0.3V to 6V
Operating Junction Temperature Range .. –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Peak Reflow Temperature ..... 260°C

## PIN CONFIGURATION




DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 76°C/W
EXPOSED PAD (PIN 9) IS NOT INTERNALLY CONNECTED,
MUST BE SOLDERED TO PCB, GND TO OBTAIN $\theta_{JA}$




MS8E PACKAGE
8-LEAD PLASTIC MSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 40°C/W
EXPOSED PAD (PIN 9) IS NOT INTERNALLY CONNECTED,
MUST BE SOLDERED TO PCB, GND TO OBTAIN $\theta_{JA}$

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | TAPE AND REEL (MINI) | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|---|
| | LTC4071EDD#TRPBF | LTC4071EDD#TRMPBF | LFXF | 8-Lead Plastic DFN | –40°C to 125°C |
| | LTC4071IDD#TRPBF | LTC4071IDD#TRMPBF | LFXF | 8-Lead Plastic DFN | –40°C to 125°C |
| LTC4071EMS8E#PBF | LTC4071EMS8E#TRPBF | | LTFXG | 8-Lead Plastic MSOP | –40°C to 125°C |
| LTC4071IMS8E#PBF | LTC4071IMS8E#TRPBF | | LTFXG | 8-Lead Plastic MSOP | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range. Conditions are $V_{NTC}$ = $V_{ADJ}$ = $V_{CC}$, $V_{LBSEL}$ = GND, $T_A$ = 25°C unless otherwise specified. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND unless otherwise noted. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{FLOAT}$ | Programmable Float Voltage<br>10µA ≤ $I_{CC}$ ≤ 25mA | $V_{ADJ}$ = 0V, 0°C < Temp < 125°C<br>$V_{ADJ}$ = 0V | <br>● | 3.96<br>3.88 | 4.0<br>4.0 | 4.04<br>4.04 | V<br>V |
| | | $V_{ADJ}$ = Float, 0°C < Temp < 125°C<br>$V_{ADJ}$ = Float | <br>● | 4.06<br>3.98 | 4.1<br>4.1 | 4.14<br>4.14 | V<br>V |
| | | $V_{ADJ}$ = $V_{CC}$, 0°C < Temp < 125°C<br>$V_{ADJ}$ = $V_{CC}$ | <br>● | 4.16<br>4.07 | 4.2<br>4.2 | 4.24<br>4.24 | V<br>V |
| $I_{CCMAX}$ | Maximum Shunt Current | $V_{CC}$ > $V_{FLOAT}$ | ● | 50 | | | mA |
| $I_{CCQ}$ | $V_{CC}$ Operating Current | $V_{HBO}$ Low, ADJ = $V_{CC}$ | ● | | 550 | 1200 | nA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating junction temperature range. Conditions are $V_{NTC} = V_{ADJ} = V_{CC}$, $V_{LBSEL}$ = GND, $T_J$ = 25°C unless otherwise specified. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND unless otherwise noted. (Note 2)**

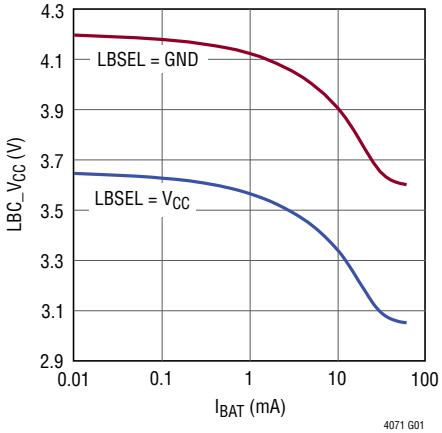
| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Low Battery Disconnect** | | | | | | | |
| $I_{LEAK}$ | Battery Disconnect Leakage Current | $V_{CC} < V_{BAT}$ = 2.65V | ● | | 0.01<br>0.01 | 25 | nA<br>nA |
| $R_{DSON}$ | Resistance of $V_{CC}$ – BAT Switch | $I_{BAT}$ = –1mA, $V_{HBO}$ High | | | 4 | 6 | Ω |
| $V_{LBD}$ | Low Battery Disconnect | $V_{BAT}$ Falling, $I_{BAT}$ = –1mA, LBSEL = $V_{CC}$, 0°C < Temp < 125°C | | 2.60 | 2.70 | 2.79 | V |
| | | $V_{BAT}$ Falling, $I_{BAT}$ = –1mA, LBSEL = $V_{CC}$ | ● | 2.52 | 2.70 | 2.79 | V |
| | | $V_{BAT}$ Falling, $I_{BAT}$ = –1mA, LBSEL = GND, 0°C < Temp < 125°C | | 3.05 | 3.20 | 3.28 | V |
| | | $V_{BAT}$ Falling, $I_{BAT}$ = –1mA, LBSEL = GND | ● | 2.95 | 3.20 | 3.28 | V |
| $V_{LBC\_BAT}$ | Low Battery Connect | $V_{BAT}$ Rising, $I_{BAT}$ = –1mA, LBSEL = $V_{CC}$ | | | 2.97 | | V |
| | | $V_{BAT}$ Rising, $I_{BAT}$ = –1mA, LBSEL = GND | | | 3.53 | | V |
| $V_{LBC\_VCC}$ | Low Battery Connect | $V_{CC}$ Rising, LBSEL = $V_{CC}$<br>$V_{CC}$ Rising, LBSEL = GND | | | 3.6<br>4.19 | | V<br>V |
| **High Battery Status** | | | | | | | |
| $V_{HBTH}$ | HBO Threshold ($V_{FLOAT}$ – $V_{CC}$) | $V_{CC}$ Rising | ● | 15 | 40 | 75 | mV |
| $V_{HBHY}$ | Hysteresis | | | | 100 | | mV |
| **Status Output: HBO** | | | | | | | |
| $V_{OL}$ | CMOS Output Low | $I_{SINK}$ = 1mA, $V_{CC}$ = 3.7V | | | | 0.5 | V |
| $V_{OH}$ | CMOS Output High | $I_{SOURCE}$ = –0.5mA, $I_{CC}$ = 1.5mA | | $V_{CC}$ – 0.6 | | | V |
| **Selection Inputs: ADJ, LBSEL** | | | | | | | |
| $V_{ADJ\_IL}$ | ADJ $V_{IL}$ | Input Logic Low Level | ● | | | 0.3 | V |
| $V_{ADJ\_IH}$ | ADJ $V_{IH}$ | Input Logic High Level | ● | $V_{CC}$ – 0.3 | | | V |
| $I_{ADJ(Z)}$ | Allowable ADJ Leakage Current in Floating State | | ● | | | ±3 | µA |
| $V_{LBSEL\_IL}$ | LBSEL $V_{IL}$ | Input Logic Low Level | ● | | | 250 | mV |
| $V_{LBSEL\_IH}$ | LBSEL $V_{IH}$ | Input Logic High Level | ● | 1.4 | | | V |
| $I_{LBSEL}$ | LBSEL Leakage Current | 0 ≤ LBSEL ≤ $V_{CC}$ | ● | –5 | 0 | 5 | nA |
| **NTC** | | | | | | | |
| $I_{NTC}$ | NTC Leakage Current | 0V ≤ NTC ≤ $V_{CC}$ | ● | –5 | 0 | 5 | nA |
| $I_{NTCBIAS}$ | Average NTCBIAS Sink Current | Pulsed Duty Cycle < 0.002% | | | 30 | 50 | pA |
| $NTC_{TH1}$ | NTC Comparator Falling Thresholds | $V_{NTC}$ as Percentage of $V_{NTCBIAS}$ Amplitude | | 35.5 | 36.5 | 38 | % |
| $NTC_{TH2}$ | | | | 28.0 | 29.0 | 30.5 | % |
| $NTC_{TH3}$ | | | | 21.8 | 22.8 | 23.8 | % |
| $NTC_{TH4}$ | | | | 16.8 | 17.8 | 18.8 | % |
| $NTC_{HY}$ | Hysteresis | | | | 30 | | mV |
| $\Delta V_{FLOAT(NTC)}$ | Delta Float Voltage per NTC Comparator Step | NTC Falling Below One of the $NTC_{TH}$ Thresholds<br>ADJ = 0V<br>ADJ = Floating<br>ADJ = $V_{CC}$ | | <br>–57<br>–82<br>–107 | <br>–50<br>–75<br>–100 | <br>–43<br>–68<br>–93 | <br>mV<br>mV<br>mV |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

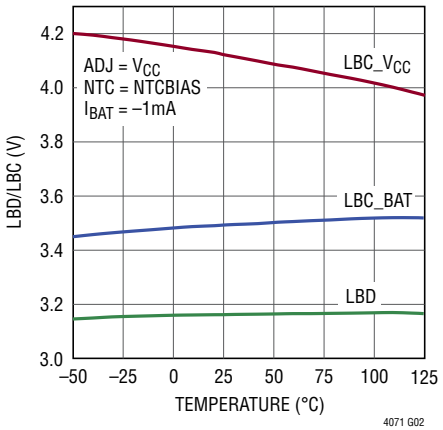
**Note 2:** The LTC4071 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4071E is guaranteed to meet performance specifications for junction temperatures from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4071I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operation conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

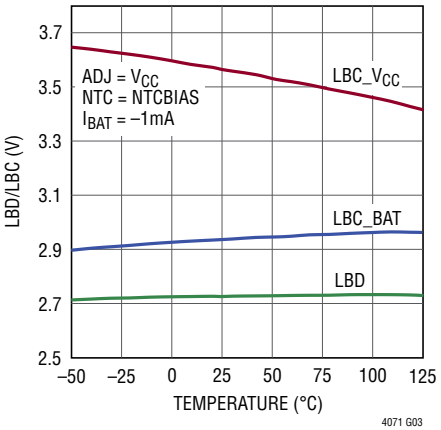
### LBC vs $I_{BAT}$



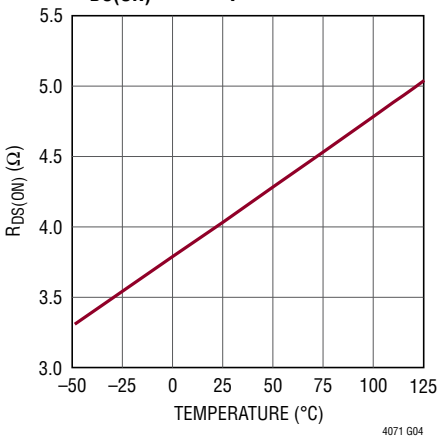

### LBD/LBC vs Temperature (LBSEL = GND)



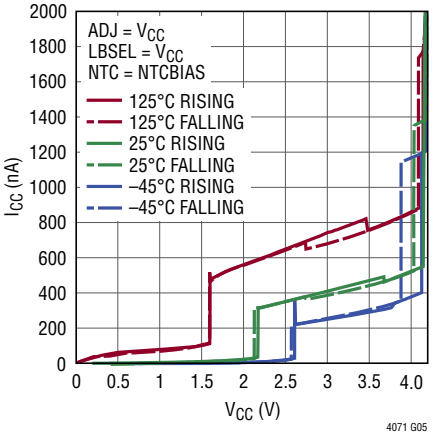

### LBD/LBC vs Temperature (LBSEL = $V_{CC}$)



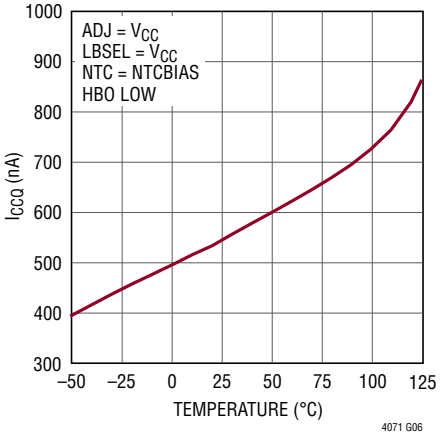

### $R_{DS(ON)}$ vs Temperature



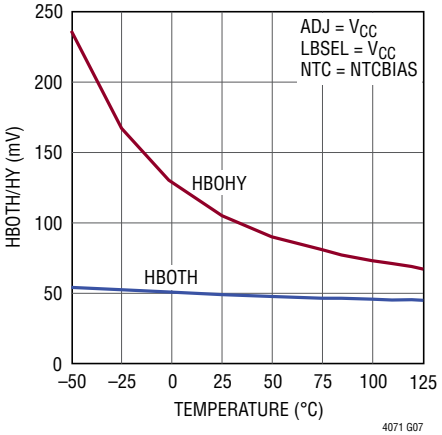

### $I_{CC}$ vs $V_{CC}$



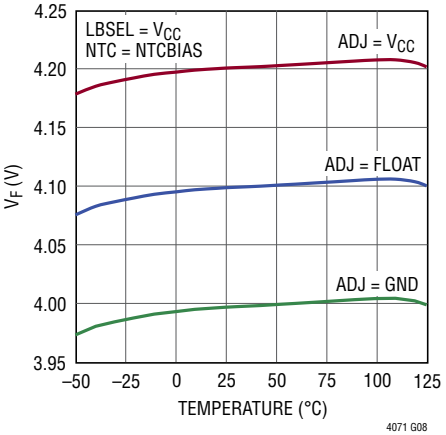

### $I_{CCQ}$ vs Temperature



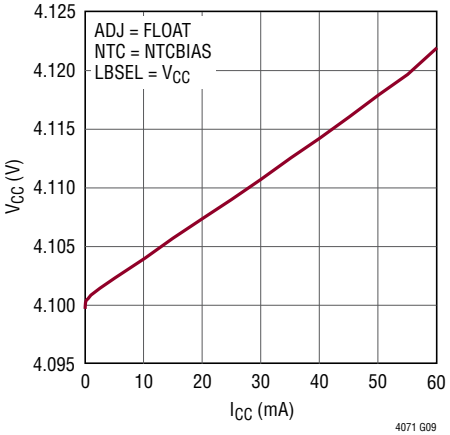

### HBO Thresholds vs Temperature




### $V_F$ vs Temperature

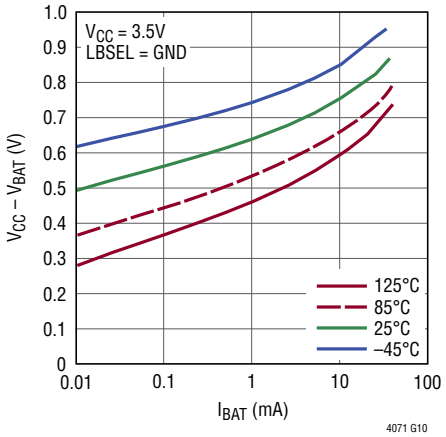



### Load Regulation

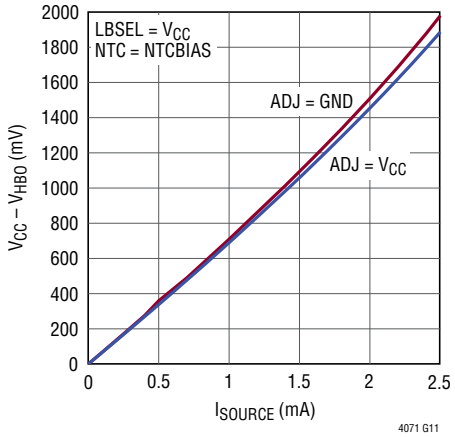


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C, unless otherwise noted.

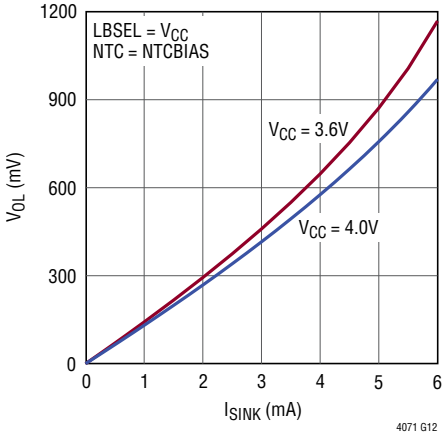
### MP1 Body Diode



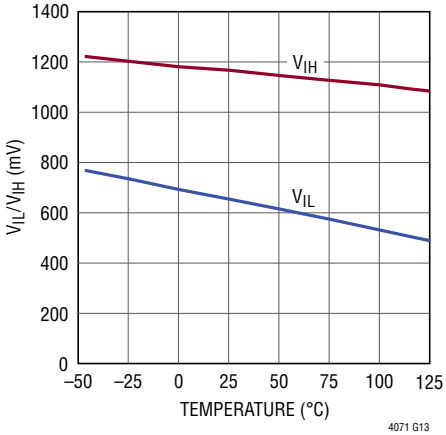

### HBO $V_{OH}$



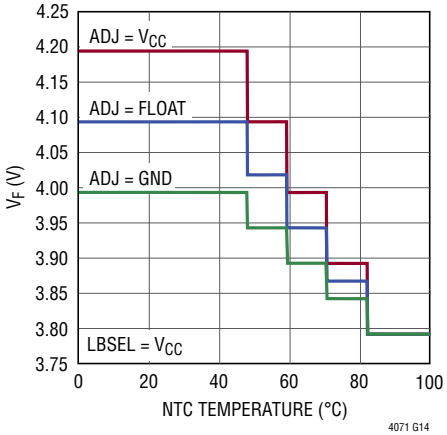

### HBO $V_{OL}$



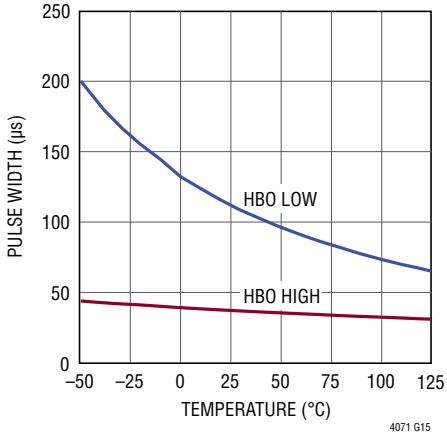

### LBSEL $V_{IL}$/$V_{IH}$ vs Temperature



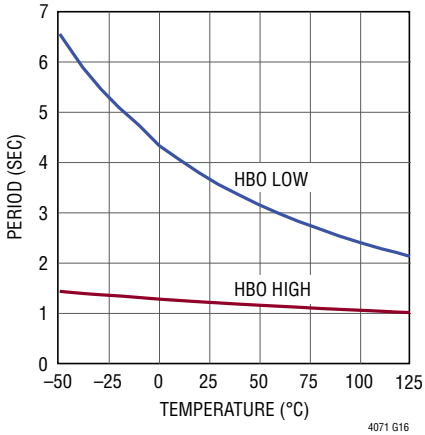

### $V_F$ vs NTC Temperature




### NTCBIAS Pulse Width vs Temperature




### NTCBIAS Period vs Temperature



## PIN FUNCTIONS

**NTCBIAS (Pin 1):** NTC Bias Pin. Connect a resistor from NTCBIAS to NTC, and a thermistor from NTC to GND. Float NTCBIAS when not in use. Minimize parasitic capacitance on this pin.

**NTC (Pin 2):** Input to the Negative Temperature Coefficient Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery to determine the temperature of the battery. If the battery temperature is too high, the float voltage is reduced. Connect a low drift bias resistor from NTCBIAS to NTC and a thermistor from NTC to GND. When not in use, connect NTC to $V_{CC}$. Minimize parasitic capacitance on this pin.

**ADJ (Pin 3):** Float Voltage Adjust Pin. Connect ADJ to GND to program 4.0V float voltage. Disconnect ADJ to program 4.1V float voltage. Connect ADJ to $V_{CC}$ to program 4.2V float voltage. The float voltage is also adjusted by the NTC thermistor.

**HBO (Pin 4):** High Battery Monitor Output (Active High). HBO is a CMOS output that indicates that the battery is almost fully charged and current is being shunted away from $V_{CC}$. This pin is driven high when $V_{CC}$ rises to within $V_{HBTH}$ of the effective float voltage, $V_{FLOAT\_EFF}$. The absolute value of this threshold depends on ADJ and NTC both of which affect the float voltage. HBO is driven low when $V_{CC}$ falls by more than ($V_{HBTH}$ + $V_{HBHY}$) below the effective float voltage. Refer to Table 1 for the effective float voltage.

**LBSEL (Pin 5):** Low Battery Disconnect Select Pin. Connect LBSEL to GND to select a low battery disconnect level of 3.2V, connect LBSEL to $V_{CC}$ to select a low battery disconnect level of 2.7V. Do not float.

**GND (Pin 6, Exposed Pad Pin 9):** Ground. The exposed package pad has no internal electrical connection but must be connected to PCB ground for maximum heat transfer.

**BAT (Pin 7):** Battery Pin. Battery charge current is sourced from $V_{CC}$ through this pin when an external supply is present. BAT supplies current to $V_{CC}$ from this pin when no other source of power is available. If BAT falls below $V_{LBD}$ this pin disconnects the battery from $V_{CC}$ protecting the battery from discharge by the load when no external power supply is present.

**$V_{CC}$ (Pin 8):** Input Supply Pin. Attach system load to this pin. The input supply voltage is regulated to 4.0V, 4.1V, or 4.2V depending on the ADJ pin state (see the ADJ pin description for more detail). This pin can sink up to 50mA in order to keep the voltage regulation within accuracy limits. Decouple to GND with a capacitor, $C_{IN}$, of at least 0.1µF, use a larger decoupling cap to handle high peak load currents.

## BLOCK DIAGRAM

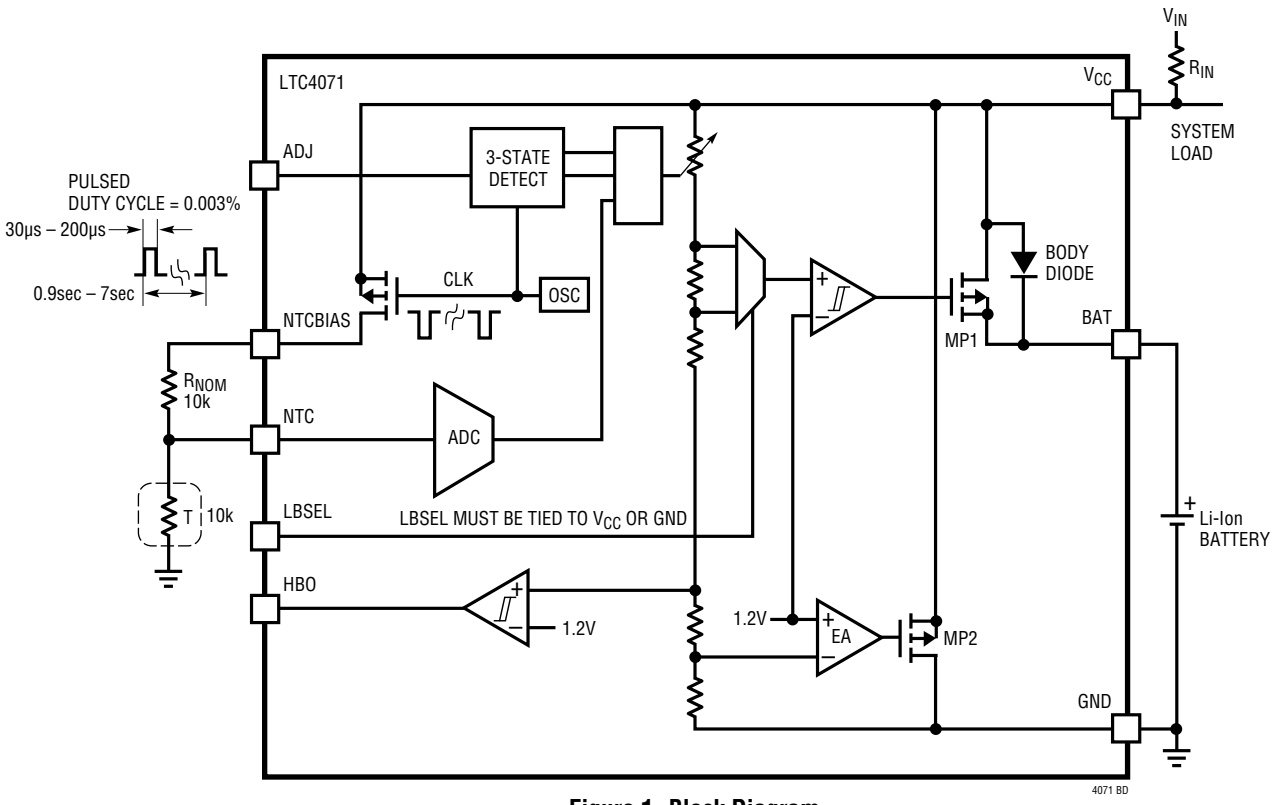



**Figure 1. Block Diagram**

## OPERATION

The LTC4071 provides a simple, reliable, and high performance battery protection and charging solution by preventing the battery voltage from exceeding a programmed level. Its shunt architecture requires just one resistor from the input supply to charge and protect the battery in a wide range of battery applications. When the input supply is removed and the battery voltage is below the high battery output threshold, the LTC4071 consumes just 550nA from the battery. If the battery voltage falls below the programmable low battery disconnect level, the battery disconnects from $V_{CC}$, protecting the battery from overdischarge either by the load connected to $V_{CC}$ or from the LTC4071 quiescent current.

When an input supply is present the battery charges through the body diode of the internal disconnect PFET, MP1, until the battery voltage rises above the low-battery connect threshold. Select an input voltage large enough for $V_{CC}$ to reach $V_{LBC\_VCC}$ to ensure that MP1 turns on. The user may detect the connected state by observing periodic pulses at the NTCBIAS pin that only occur once $V_{CC}$ has risen above $V_{LBC\_VCC}$, and cease once $V_{CC}$ falls below $V_{LBD}$. Depending on the capacity of the battery and the input decoupling capacitor, the $V_{CC}$ voltage generally falls to $V_{BAT}$ when MP1 turns on; rather than $V_{BAT}$ rising to $V_{CC}$. The internal PFET then reconnects the battery to $V_{CC}$ and the charge rate is determined by the input voltage, the battery voltage, and the input resistor:

$$I_{CHG} = \frac{(V_{IN} - V_{BAT})}{R_{IN}}$$

As the battery voltage approaches the float voltage, the LTC4071 shunts current away from the battery thereby reducing the charge current. The LTC4071 can shunt up to 50mA. The shunt current limits the maximum charge current.

## OPERATION

In cases where the input supply may be shorted to GND when not supplying power, for example with a solar cell, add a diode in series with $R_{IN}$ to prevent the input from loading the battery. For more information, refer to the photovoltaic charger example in the Applications Information section.

### Adjustable Float Voltage, $V_{FLOAT}$

A built-in 3-state decoder connected to the ADJ pin provides three programmable float voltages: 4.0V, 4.1V, or 4.2V. The float voltage is programmed to 4.0V when ADJ is tied to GND, 4.1V when ADJ is floating (disconnected), and 4.2V when ADJ is tied to $V_{CC}$. The state of the ADJ pin (and NTC pins) is sampled for about 36µs about once every 1.2 seconds when HBO is high, and when HBO is low the sampling rate reduces to about once every 3.6 seconds with the same duty cycle. If $V_{CC}$ falls below $V_{LBD}$, the sampling stops. When it is being sampled, the LTC4071 applies a relatively low impedance voltage at the ADJ pin. This technique prevents low level board leakage from corrupting the programmed float voltage.

### NTC Qualified Float Voltage, $\Delta V_{FLOAT(NTC)}$

The NTC pin voltage is compared against an internal resistor divider tied to the NTCBIAS pin. This divider has tap points that are matched to the NTC thermistor resistance/temperature conversion table for a Vishay curve 2 thermistor at temperatures of 40°C, 50°C, 60°C, and 70°C. The curve 2 thermistor is also designated by a B25/85 value of 3490.

Battery temperature conditioning adjusts the float voltage down to $V_{FLOAT\_EFF}$ when the NTC thermistor indicates that the battery temperature is too high. For a 10k curve 2 thermistor and a 10k NTCBIAS resistor, each 10°C increase in temperature above 40°C causes the float voltage to drop by a fixed amount, $\Delta V_{FLOAT(NTC)}$, depending on ADJ. If ADJ is at GND, the float voltage steps down by 50mV for each 10°C temperature increment. If ADJ is floating, the step size is 75mV. And if ADJ is at $V_{CC}$, the step size is 100mV. Refer to Table 1 for the range of $V_{FLOAT\_EFF}$ programming.

**Table 1. NTC Qualified Float Voltage**

| ADJ | $\Delta V_{FLOAT(NTC)}$ | TEMPERATURE | $V_{NTC}$ AS % OF NTCBIAS | $V_{FLOAT\_EFF}$ |
|---|---|---|---|---|
| GND | 50mV | T < 40°C | $V_{NTC} > 36.5$ | 4.000 |
| | | 40°C ≤ T < 50°C | $29.0 < V_{NTC} \le 36.5$ | 3.950 |
| | | 50°C ≤ T < 60°C | $22.8 < V_{NTC} \le 29.0$ | 3.900 |
| | | 60°C ≤ T < 70°C | $17.8 < V_{NTC} \le 22.8$ | 3.850 |
| | | 70°C < T | $V_{NTC} \le 17.8$ | 3.800 |
| Floating | 75mV | T < 40°C | $V_{NTC} > 36.5$ | 4.100 |
| | | 40°C ≤ T < 50°C | $29.0 < V_{NTC} \le 36.5$ | 4.025 |
| | | 50°C ≤ T < 60°C | $22.8 < V_{NTC} \le 29.0$ | 3.950 |
| | | 60°C ≤ T < 70°C | $17.8 < V_{NTC} \le 22.8$ | 3.875 |
| | | 70°C < T | $V_{NTC} \le 17.8$ | 3.800 |
| $V_{CC}$ | 100mV | T < 40°C | $V_{NTC} > 36.5$ | 4.200 |
| | | 40°C ≤ T < 50°C | $29.0 < V_{NTC} \le 36.5$ | 4.100 |
| | | 50°C ≤ T < 60°C | $22.8 < V_{NTC} \le 29.0$ | 4.000 |
| | | 60°C ≤ T < 70°C | $17.8 < V_{NTC} \le 22.8$ | 3.900 |
| | | 70°C < T | $V_{NTC} \le 17.8$ | 3.800 |

For all ADJ pin settings the lowest float voltage setting is:

$$3.8V = V_{FLOAT\_MIN} = V_{FLOAT} - 4 \bullet \Delta V_{FLOAT(NTC)}.$$

This occurs at NTC thermistor temperatures above 70°C, or if the NTC pin is grounded.

To conserve power in the NTCBIAS and NTC resistors, the NTCBIAS pin is sampled at a low duty cycle at the same time that the ADJ pin state is sampled.

### High Battery Status Output: HBO

The HBO pin pulls high when $V_{CC}$ rises to within $V_{HBTH}$ of the programmed float voltage, $V_{FLOAT\_EFF}$, including NTC qualified float voltage adjustments assuming $V_{CC}$ has risen above $V_{LBC\_VCC}$.

If $V_{CC}$ drops below the float voltage by more than $V_{HBTH} + V_{HBHY}$ the HBO pin pulls low to indicate that the battery is not at full charge. The input supply current to the LTC4071 drops to less than 550nA (typ) as the LTC4071 no longer shunts current to protect the battery. And the NTCBIAS sample clock slows to conserve power.

For example, if the NTC thermistor requires the float voltage to be dropped by 100mV (ADJ = $V_{CC}$ and $0.29 \bullet V_{NTCBIAS} < V_{NTC} < 0.36 \bullet V_{NTCBIAS}$) then the HBO rising threshold is detected when $V_{CC}$ rises past:

$$V_{FLOAT} - \Delta V_{FLOAT(NTC)} - V_{HBTH}$$
$$= 4.2V - 100mV - 40mV = 3.96V.$$

## OPERATION

### Low Battery Disconnect/Connect: LBD/LBC

The low battery disconnect ($V_{LBD}$) and connect ($V_{LBC}$) voltage levels are programmed by the LBSEL pin. As shown in the Block Diagram the battery disconnects from $V_{CC}$ by shutting off MP1 when the BAT voltage falls below $V_{LBD}$. This disconnect function protects Li-Ion batteries from permanent damage due to deep discharge. If the voltage of a Li-Ion cell drops below a certain level, the cell may be permanently damaged. Disconnecting the battery from $V_{CC}$ prevents the load at $V_{CC}$ as well as the LTC4071 quiescent current from further discharging the battery.

Once disconnected the $V_{CC}$ voltage collapses towards ground. When an input supply is reconnected the battery charges through the internal body diode of MP1. The input supply voltage should be larger than $V_{LBC\_VCC}$ to ensure that MP1 is turned on. When the $V_{CC}$ voltage reaches $V_{LBC\_VCC}$, MP1 turns on and connects $V_{CC}$ and BAT. While disconnected, the BAT pin voltage is indirectly sensed through MP1's body diode. Therefore $V_{LBC}$ varies with charge current and junction temperature. Please see the Typical Performance Characteristics section for more information.

### Low Battery Select: LBSEL

The low battery discharge cutoff voltage level is programmed by the LBSEL pin.

The LBSEL pin allows the user to trade-off battery runtime and maximum shelf life. A lower battery disconnect threshold maximizes run time by allowing the battery to fully discharge before the disconnect event. Conversely, by increasing the low battery disconnect threshold more capacity remains following the disconnect event which extends the shelf life of the battery. For maximum run time, tie LBSEL to $V_{CC}$ so that the battery disconnects at $V_{CC}$ = 2.7V. For extended shelf life, tie LBSEL to GND so that the battery disconnects at $V_{CC}$ = 3.2V. If a high peak current event is expected, users may temporarily select the lower disconnect threshold. This avoids disconnecting the battery too early when the load works against the battery series resistance and temporarily reduces $V_{CC}$.

## APPLICATIONS INFORMATION

### General Charging Considerations

The LTC4071 uses a different charging methodology from previous chargers. Most Li-Ion chargers terminate the charging after a period of time. The LTC4071 does not have a discrete charge termination. Extensive measurements on Li-Ion cells show that the cell charge current drops to very low levels with the shunt charge control circuit effectively terminating the charge. For improved battery lifetime choose 4.0V or 4.1V float voltage.

The battery disconnect function requires some care in selecting the input supply compliance for charging a battery while powering a load at $V_{CC}$. The internal battery disconnect switch remains off while charging the battery through the body diode of the internal switch until $V_{CC}$ exceeds $V_{LBC\_VCC}$. If the source voltage compliance is not greater than $V_{LBC\_VCC}$, then the battery will never reconnect to $V_{CC}$ and the system load will not be able to run on battery power. Users may detect that the battery is connected by monitoring the NTCBIAS pin as it will periodically pulse high once $V_{CC}$ has risen above $V_{LBC\_VCC}$, and stops pulsing once $V_{CC}$ falls below $V_{LBD}$.

The simplest application of the LTC4071 is shown in Figure 2. This application requires only an external resistor to program the charge/shunt current. Assume the wall

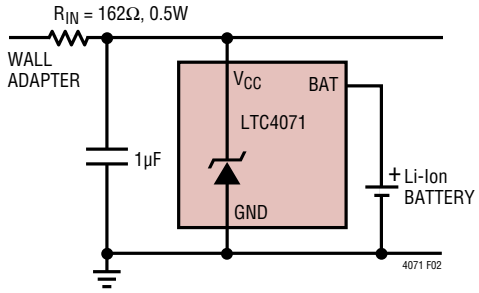



**Figure 2. Single-Cell Battery Charger**

adapter voltage ($V_{WALL}$) is 12V and the maximum charge current is calculated as:

$$I_{MAX\_CHARGE} = \frac{\left(V_{WALL} - V_{BAT\_MIN}\right)}{R_{IN}}$$

$$= \frac{\left(12V - 3.2V\right)}{162\Omega} = 54mA$$

Care must be taken in selecting the input resistor. Power dissipated in $R_{IN}$ under full charge current is given by the following equation:

$$P_{DISS} = \frac{\left(V_{WALL} - V_{BAT\_MIN}\right)^2}{R_{IN}} = \frac{\left(12V - 3.2V\right)^2}{162\Omega} = 0.48W$$

The charge current decreases as the battery voltage increases. If the battery voltage is 40mV less than the programmed float voltage the LTC4071 consumes only 550nA of current, and all of the excess input current flows into the battery. As the battery voltage reaches the float voltage, the LTC4071 shunts current from the wall adapter and regulates the battery voltage to $V_{FLOAT} = V_{CC}$. The more shunt current the LTC4071 sinks, the less charge current the battery gets. Eventually, the LTC4071 shunts all the current flowing through $R_{IN}$; up to the maximum shunt current. The maximum shunt current in this case, with no NTC adjustment is determined by the input resistor and is calculated as:

$$I_{SHUNT\_MAX} = \frac{\left(V_{WALL} - V_{FLOAT}\right)}{R_{IN}} = \frac{\left(12V - 4.1V\right)}{162\Omega} = 49mA$$

At this point the power dissipated in the input resistor is 388mW.

The LTC4071 can also be used to regulate series-connected battery stacks as illustrated in Figure 3. Here two LTC4071 devices are used to charge two batteries in series. A single resistor sets the maximum charge/shunt current.

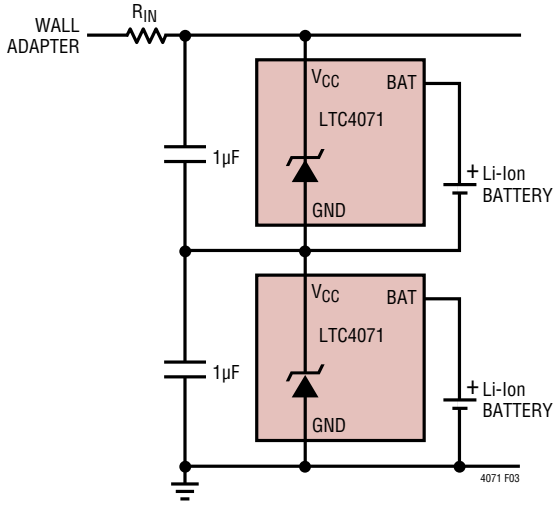



**Figure 3. 2-Cell Battery Charger**

## APPLICATIONS INFORMATION

The GND pin of the top device is simply connected to the $V_{CC}$ pin of the bottom device. Care must be taken in observing the HBO status output pin of the top device as this signal is no longer ground referenced. Likewise for the control inputs of the top device; tie ADJ and LBSEL of the top device to the local GND or $V_{CC}$ pins. Also, the wall adapter must have a high enough voltage rating to charge both cells.

### NTC Protection

The LTC4071 measures battery temperature with a negative temperature coefficient thermistor thermally coupled to the battery. NTC thermistors have temperature characteristics which are specified in resistance-temperature conversion tables. Internal NTC circuitry protects the battery from excessive heat by reducing the float voltage for each 10°C rise in temperature above 40°C (assuming a Vishay thermistor with a $B_{25/85}$ value of 3490).

The LTC4071 uses a ratio of resistor values to measure battery temperature. The LTC4071 contains an internal fixed resistor voltage divider from NTCBIAS to GND with four tap points; $NTC_{TH1}$–$NTC_{TH4}$. The voltages at these tap points are periodically compared against the voltage at the NTC pin to measure battery temperature. To conserve power, the battery temperature is measured periodically by biasing the NTCBIAS pin to $V_{CC}$ about once every 1.5 seconds.

The voltage at the NTC pin depends on the ratio of NTC thermistor value, $R_{NTC}$, and a bias resistor, $R_{NOM}$. Choose $R_{NOM}$ equal to the value of the thermistor at 25°C. $R_{NOM}$ is 10k for a Vishay NTHS0402N02N1002F thermistor with a $B_{25/85}$ value of 3490. $R_{NOM}$ must be connected from NTCBIAS to NTC. The ratio of the NTC pin voltage to the NTCBIAS voltage when it is pulsed to $V_{CC}$ is:

$$\frac{R_{NTC}}{\left(R_{NTC}+R_{NOM}\right)}$$

When the thermistor temperature rises, the resistance drops; and the resistor divider between $R_{NOM}$ and the thermistor lowers the voltage at the NTC pin.

An NTC thermistor with a different $B_{25/85}$ value may also be used with the LTC4071. However the temperature trip points are shifted due to the higher negative temperature coefficient of the thermistor. To correct for this difference add a resistor, $R_{FIX}$, in series with the thermistor to shift the ratio:

$$\frac{R_{FIX}+R_{NTC}}{\left(R_{FIX}+R_{NTC}+R_{NOM}\right)}$$

Up to the internal resistive divider tap points: $NTC_{TH1}$ through $NTC_{TH4}$. For a 100k thermistor with a $B_{25/85}$ value of 3950, e.g. NTHS0402N01N1003F, at 70°C (with $R_{NOM}$ = 100k) choose $R_{FIX}$ = 3.92k. The temperature trip points are found by looking up the curve 1 thermistor R/T values plus $R_{FIX}$ that correspond to the ratios for $NTC_{TH1}$ = 36.5%, $NTC_{TH2}$ = 29%, $NTC_{TH3}$ = 22.8%, and $NTC_{TH4}$ = 17.8%. Selecting $R_{FIX}$ = 3.92k results in trip points of 39.9°C, 49.4°C, 59.2°C and 69.6°C.

Another technique may be used without adding an additional component. Instead decrease $R_{NOM}$ to adjust the $NTC_{TH}$ thresholds for a given R/T thermistor profile. For example, if $R_{NOM}$ = 88.7k (with the same 100k thermistor) then the temperature trip points are 41.0°C, 49.8°C, 58.5°C and 67.3°C.

When using the NTC features of the LTC4071 it is important to keep in mind that the maximum shunt current increases as the float voltage, $V_{FLOAT\_EFF}$ drops with NTC conditioning. Reviewing the single-cell battery charger application with a 12V wall adapter in Figure 2; the input resistor should be increased to 165Ω such that the maximum shunt current does not exceed 50mA at the lowest possible float voltage due to NTC conditioning, $V_{FLOAT\_MIN}$ = 3.8V.

### Thermal Considerations

At maximum shunt current, the LTC4071 may dissipate up to 205mW. The thermal dissipation of the package should be taken into account when operating at maximum shunt current so as not to exceed the absolute maximum junction temperature of the device. With $\theta_{JA}$ of 40°C/W, in the MSOP package, at maximum shunt current of 50mA the junction temperature rise is about 8°C above ambient. With $\theta_{JA}$ of 76°C/W in the DFN package, at maximum shunt current of 50mA the junction temperature rise is about 16°C above ambient. The junction temperature, $T_J$, is calculated depending on ambient temperature,

## APPLICATIONS INFORMATION

$T_A$, power dissipation, PD (in W), and $\theta_{JA}$ is the thermal impedance of the package (in °C/W):

$$T_J = T_A + (PD \times \theta_{JA}).$$

The application shown in Figure 4 illustrates how to prevent triggering the low-battery disconnect function under large pulsed loads due to the high ESR of thin-film batteries.

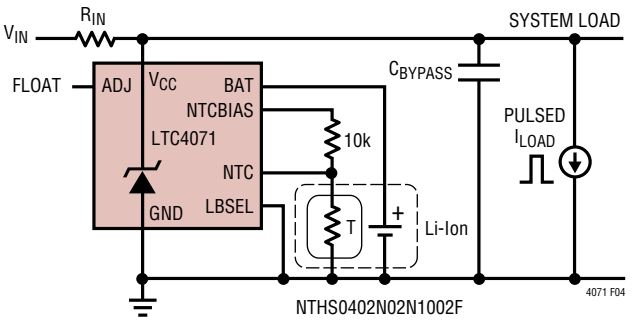



**Figure 4. Adding a Decoupling Capacitor for Large Load Transients**

Table 2 lists some thin-film batteries, their capacities and their equivalent series resistance. The ESR causes $V_{BAT}$ and $V_{CC}$ to droop as a product of the load current amplitude multiplied by the ESR. This droop may trigger the low-battery disconnect while the battery itself may still have ample capacity. Adding a bypass capacitor to $V_{CC}$ prevents large low duty cycle load transients from pulling down on $V_{CC}$.

**Table 2. Low Capacity Li-Ion and Thin-Film Batteries**

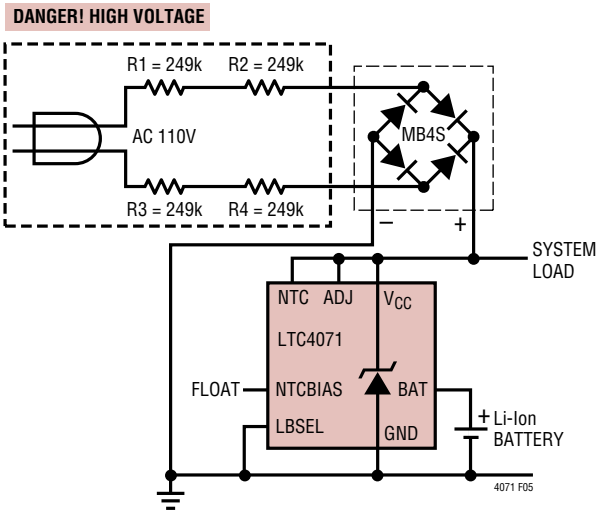
| VENDOR | P/N | CAPACITY | RESISTANCE | $V_{MIN}$ |
|---|---|---|---|---|
| CYMBET | CBC012 | 12µAh | 5k to 10k | 3.0V |
| CYMBET | CBC050 | 50µAh | 1500Ω to 3k | 3.0V |
| GS NanoTech | N/A | 500µAh | 40Ω | 3.0V |
| APS-Autec | LIR2025 | 20mAh | 0.75Ω | 3.0V |
| APS-Autec | LIR1025 | 6mAh | 30Ω | 2.75V |
| IPS | MEC225-1P | 0.13mAh | 210Ω to 260Ω | 2.1V |
| IPS | MEC220-4P | 0.4mAh | 100Ω to 120Ω | 2.1V |
| IPS | MEC201-10P | 1.0mAh | 34Ω to 45Ω | 2.1V |
| IPS | MEC202-25P | 2.5mAh | 15Ω to 20Ω | 2.1V |
| GM Battery | GMB031009 | 8mAh | 10Ω to 20Ω | 2.75V |

For example, given a 0.1% duty cycle 5ms load pulse of 20mA and a 1.0mAh IPS MEC201-10P solid-state thin-film battery with an equivalent series resistance of 35Ω, the voltage drop at $V_{CC}$ can be as high as 0.7V while the load is on. However once the load pulse ends, the battery voltage recovers, as the capacity of the battery should provide roughly 50 hours of use for an equivalent 0.1%•20mA = 20µA load. To prevent load pulses from tripping the low battery disconnect, add a decoupling capacitor from $V_{CC}$ to GND. The size of this capacitor can be calculated based on how much margin is required from the LBD threshold as well as the amplitude and pulse width of the load transient. For a 1.0mAh battery with a state-of-charge of 3.8V, the margin from LBD is 600mV with LBSEL tied to GND. For a square-wave load pulse of 20mA with a pulse width of 5ms, the minimum size of the decoupling cap required to hold $V_{CC}$ above LBD is calculated as follows:

$$C_{BYPASS} = \frac{20mA \bullet 5ms}{600mV} = 166.6\mu F$$

Take care to select a bypass capacitor with low leakage.

The LTC4071 can be used to charge a battery to a 4.2V float voltage from an AC line with a bridge rectifier as shown in the simple schematic in Figure 5. In this example,




**DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN AC LINE-CONNECTED CIRCUITS! BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF AC LINE-CONNECTED CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. ALL TESTING PERFORMED ON AC LINE-CONNECTED CIRCUITS MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE AC LINE AND THE CIRCUIT. USERS AND CONSTRUCTORS OF AC LINE-CONNECTED CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK.**

**Figure 5. 4.2V AC Line Charging, UL Leakage Okay**

## APPLICATIONS INFORMATION

the four input 249k resistors are sized for acceptable UL leakage in the event that one of the resistors short. Here, the LTC4071 will fully charge the battery from the AC line while meeting the UL specification with 104µA of available charge current.

A simple photovoltaic (PV) application for the LTC4071 is illustrated in Figure 6. At low $V_{CC}$ voltage, PV current flows to both the system at $V_{CC}$ as well as the battery.

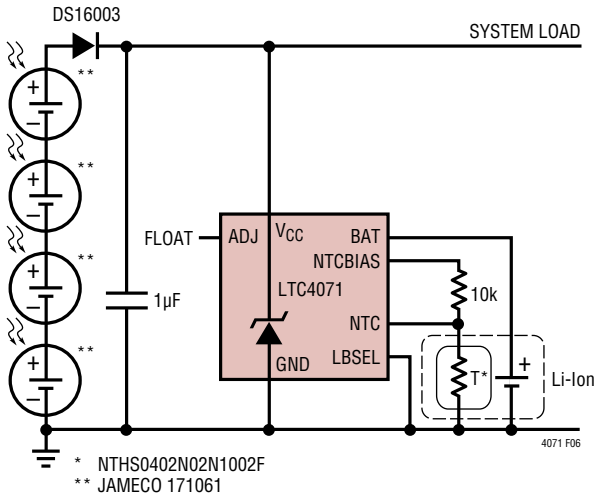



**Figure 6. Simple Photovoltaic Charger**

When $V_{CC}$ reaches the programmed float voltage (4.1V with ADJ floating) then the LTC4071 shunts excess current not used by the load, limiting $V_{CC}$ to 4.1V and effectively reducing the battery charge current to zero. If the PV cells stop supplying current, the battery supports the load at $V_{CC}$ through the LTC4071. Add a diode in series with the PV cells to prevent reverse leakage of the PV cells from draining the battery. If the battery discharges to the point where $V_{CC}$ falls below $V_{LBD}$ (3.2V with LBSEL tied to GND) the LTC4071 disconnects the load from the battery to protect the battery from over discharge.

Typically, solar cells are inherently limited in current, but this circuit may require a resistor, $R_{IN}$, in series with the LTC4071 for high current solar cells. Select $R_{IN}$ such that the LTC4071 never needs to shunt more than 50mA.

The simple schematic in Figure 7 illustrates a complete piezoelectric energy harvesting application using the LTC4071 to charge and protect Li-Ion cells along with the LTC3588-1 to rectify and regulate energy generated from a piezoelectric generator to a fixed 3.3V load.

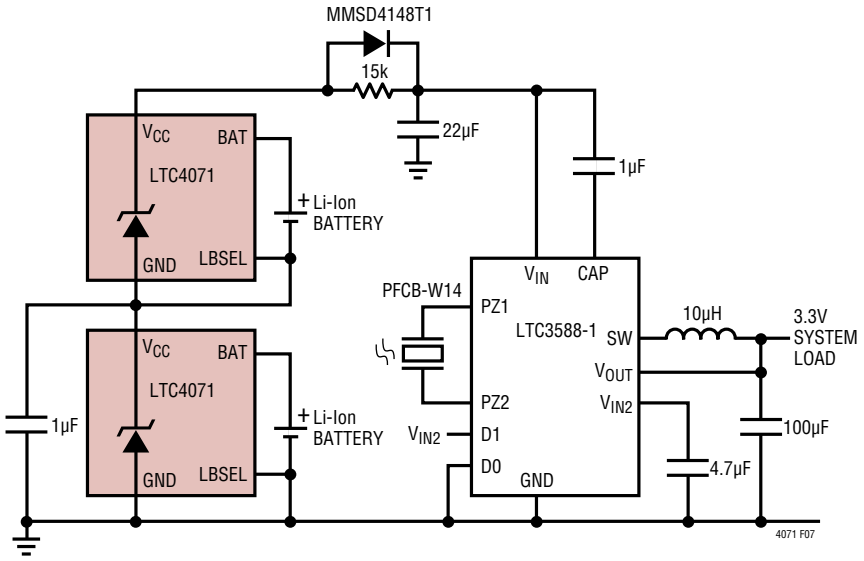



**Figure 7. Piezoelectric Energy Harvester with Battery Backup**

## APPLICATIONS INFORMATION

This system has two modes of operation, charging where the batteries are being charged from energy harvested from the piezoelectric generator while the load is negligible. And discharging, where the load is pulling current from the batteries, but insufficient energy is being harvested to power the load.

This application allows the load to periodically draw more current than would otherwise be available from the piezoelectric generator by storing excess charge in a stack of two Li-Ion cells. Each Li-Ion cell is protected from overcharge and over discharge by a LTC4071 shunt regulator. The two LTC4071s regulate $V_{IN}$ of the LTC3588-1 to 8.2V (with both ADJ pins floating) shunting any excess current that is not used by the load once the batteries achieve their float voltages. When the load requires more current than is available from the piezoelectric generator, the voltage at $V_{IN}$ droops and current is supplied from the two Li-Ion cells to power the step-down switching regulator. If the load pulls enough current to discharge the batteries below $V_{LBD}$, the LTC4071s disconnect the batteries, and $V_{IN}$ collapses until the piezoelectric generator resumes supplying current.

The application in Figure 8 illustrates how to implement "ship-mode," where a battery is co-packaged with the LTC4071 and then the entire device is latched-off, leaving the battery fully charged but with the LTC4071 switched off. The co-packaged battery and LTC4071 can then be stored with a long shelf-life before being activated for normal use.

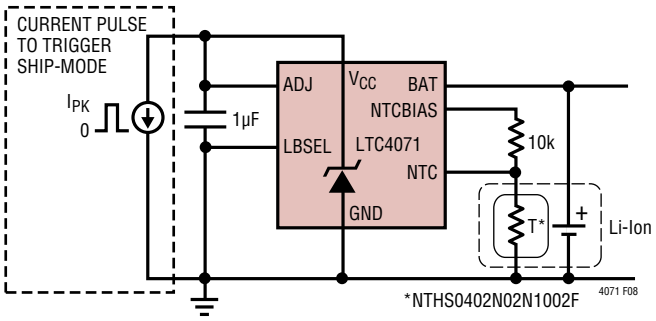



**Figure 8. LTC4071 Ship-Mode Application for Extended Shelf Life**

Ship-mode is triggered by pulling enough current through the LTC4071 so as to drop $V_{CC}$ below the LBD threshold. The current pulse amplitude should be less than 400mA with a duration of less than 10ms. The peak current necessary, $I_{PK}$, depends on the equivalent series resistance of the battery, $B_{ESR}$, summed with the $R_{DSON}$ of the BAT-$V_{CC}$ FET, the battery voltage, $V_{BAT}$ and the selected disconnect voltage, $V_{LBD}$:

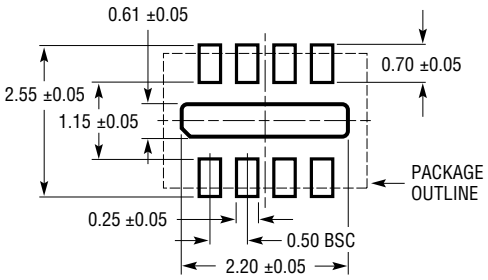
$$I_{PK} = \frac{V_{BAT} - V_{LBD}}{R_{DSON} + BESR}$$

Users may test that ship mode has been triggered by simply checking if $V_{CC}$ is at GND and that there are no longer any NTCBIAS pulses.

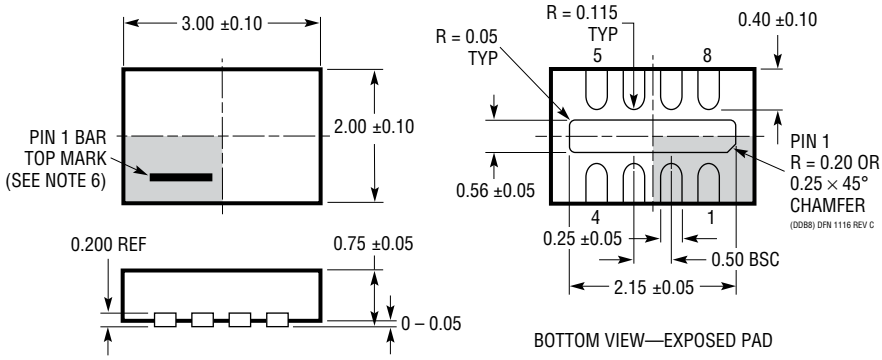
Re-activation of the LTC4071 and the battery requires either applying power normally, or briefly shorting $V_{CC}$ to BAT to turn it on.

# PACKAGE DESCRIPTION

**DDB Package**
**8-Lead Plastic DFN (3mm × 2mm)**
(Reference LTC DWG # 05-08-1702 Rev C)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

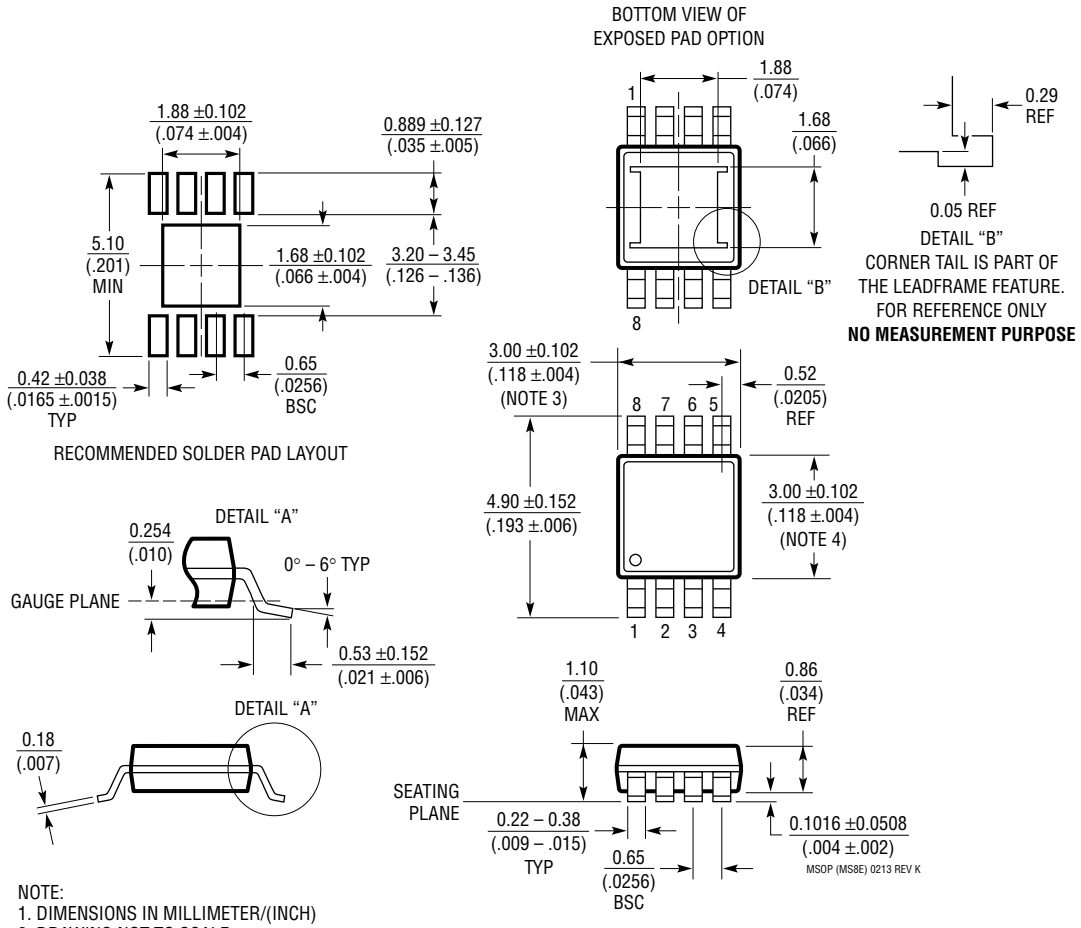



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**MS8E Package**
**8-Lead Plastic MSOP, Exposed Die Pad**
(Reference LTC DWG # 05-08-1662 Rev K)




NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 10/10 | $V_{LBD}$ specification replaced in Electrical Characteristics section. | 3 |
| B | 4/11 | Updated Vishay thermistor part number. | 11, 12, 13, 14, 18 |
| C | 10/11 | Under Note 2, replaced “=” with “≈”. | 3 |
| | | Updated IPS MFR’s part numbers. | 12 |
| | | Updated the application example. | 12 |
| | | Updated MFR part number on the Typical Application circuit MEC201-10P. | 18 |
| D | 2/20 | Revised Order Information table | 2 |



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.