500mA Li-Ion Charger with NTC Input and 300mA Synchronous Buck

FEATURES

Battery Charger:

- **Constant-Current/Constant-Voltage Operation with Thermal Feedback to Maximize Charge Rate without Risk of Overheating**
- **Internal 4.5-Hour Safety Timer for Termination**
- **Charge Current Programmable Up to 500mA with 5% Accuracy**
- **NTC Thermistor Input for Temperature Qualified Charging**
- C/10 Charge Current Detection Output
- 5µA Supply Current in Shutdown Mode

Switching Regulator:

- **High Efficiency Synchronous Buck Converter**
- **300mA Output Current (Constant-Frequency Mode)**
- 2.7V to 4.5V Input Range (Powered from BAT Pin)
- 0.8V to V_{BAT} Output Range
- MODE Pin Selects Fixed (2.25MHz) Constant-Frequency PWM Mode or Low I_{CC} (23µA) Burst Mode® Operation
- 2µA BAT Current in Shutdown Mode
- 10-Lead, Low Profile (0.75 mm) 3mm × 3mm DFN Package

APPLICATIONS

- Wireless Headsets
- Bluetooth Applications
- Portable MP3 Players
- Multifunction Wristwatches

DESCRIPTION

The LTC®4081 is a complete constant-current/constant-voltage linear battery charger for a single-cell 4.2V lithium-ion/polymer battery with an integrated 300mA synchronous buck converter. A 3mm × 3mm DFN package and low external component count make the LTC4081 especially suitable for portable applications. Furthermore, the LTC4081 is specifically designed to work within USB power specifications.

The $\overline{CHRG}$ pin indicates when charge current has dropped to ten percent of its programmed value (C/10). An internal 4.5-hour timer terminates the charge cycle. The full-featured LTC4081 battery charger also includes trickle charge, automatic recharge, soft-start (to limit inrush current) and an NTC thermistor input used to monitor battery temperature.

The LTC4081 integrates a synchronous buck converter that is powered from the BAT pin. It has an adjustable output voltage and can deliver up to 300mA of load current. The buck converter also features low current high efficiency Burst Mode operation that can be selected by the MODE pin.

The LTC4081 is available in a 10-lead, low profile (0.75mm) 3mm × 3mm DFN package.

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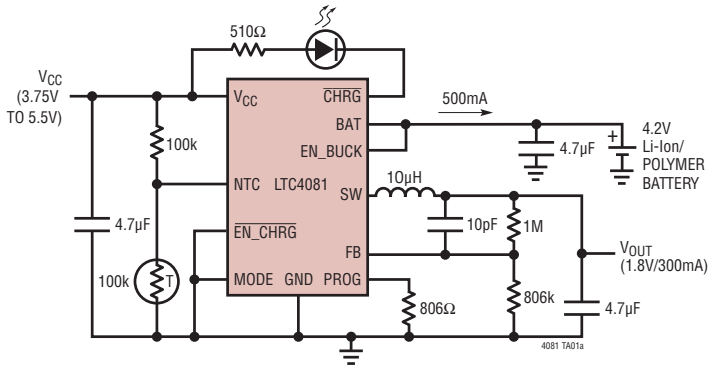
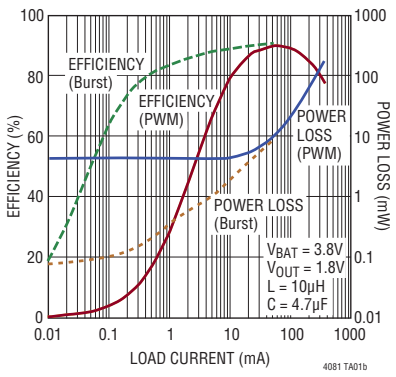
TYPICAL APPLICATION

Li-Ion Battery Charger with 1.8V Buck Regulator



Buck Efficiency vs Load Current (V_{OUT} = 1.8V)

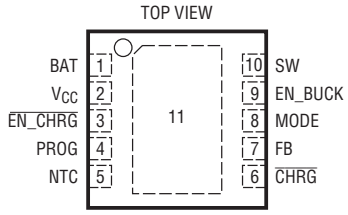


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC}, t < 1ms and Duty Cycle < 1% ..... –0.3V to 7V
V_{CC} Steady State ..... –0.3V to 6V
BAT, $\overline{CHRG}$ ..... –0.3V to 6V
$\overline{EN_CHRG}$, PROG, NTC ..... –0.3V to V_{CC} + 0.3V
MODE, EN_BUCK ..... –0.3V to V_{BAT} + 0.3V
FB ..... –0.3V to 2V

BAT Short-Circuit Duration ..... Continuous
BAT Pin Current 800mA
PROG Pin Current 2mA
Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) .... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 110°C, θ_{JA} = 43°C/W (NOTE 3)
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4081EDD#PBF	LTC4081EDD#TRPBF	LDBX	10-Lead (3mm × 3mm) DFN	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, V_{BAT} = 3.8V, $V_{\overline{EN_CHRG}}$ = 0V, V_{NTC} = 0V, V_{EN_BUCK} = V_{BAT}, V_{MODE} = 0V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Battery Charger Supply Voltage	(Note 4)	●	3.75	5	5.5	V
V_{BAT}	Input Voltage for the Switching Regulator	(Note 5)	●	2.7	3.8	4.5	V
I_{CC}	Quiescent Supply Current (Charger On, Switching Regulator Off)	V_{BAT} = 4.5V (Forces I_{BAT} and I_{PROG} = 0), V_{EN_BUCK} = 0	●		110	300	µA
I_{CC_SD}	Supply Current in Shutdown (Both Battery Charger and Switching Regulator Off)	$V_{\overline{EN_CHRG}}$ = 5V, V_{EN_BUCK} = 0, V_{CC} > V_{BAT} $V_{\overline{EN_CHRG}}$ = 4V, V_{EN_BUCK} = 0, V_{CC} (3.5V) < V_{BAT} (4V)	●		5 2	10	µA µA
I_{BAT_SD}	Battery Current in Shutdown (Both Battery Charger and Switching Regulator Off)	$V_{\overline{EN_CHRG}}$ = 5V, V_{EN_BUCK} = 0, V_{CC} > V_{BAT} $V_{\overline{EN_CHRG}}$ = 4V, V_{EN_BUCK} = 0, V_{CC} (3.5V) < V_{BAT} (4V)	●		0.6 2	5	µA µA

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
V_{FLOAT}	V_{BAT} Regulated Output Voltage	I_{BAT} = 2mA I_{BAT} = 2mA, 4.3V < V_{CC} < 5.5V	 ●	4.179 4.158	4.2 4.2	4.221 4.242	V V
I_{BAT}	Current Mode Charge Current	R_{PROG} = 4k; Current Mode; V_{EN_BUCK} = 0 R_{PROG} = 0.8k; Current Mode; V_{EN_BUCK} = 0	● ●	90 475	100 500	110 525	mA mA
V_{UVLO_CHRG}	V_{CC} Undervoltage Lockout Voltage	V_{CC} Rising V_{CC} Falling	● ●	3.5 2.8	3.6 3.0	3.7 3.2	V V
V_{PROG}	PROG Pin Servo Voltage	0.8k ≤ R_{PROG} ≤ 4k	●	0.98	1.0	1.02	V
V_{ASD}	Automatic Shutdown Threshold Voltage	(V_{CC} – V_{BAT}), V_{CC} Low to High (V_{CC} – V_{BAT}), V_{CC} High to Low		60 15	82 32	100 45	mV mV
t_{SS_CHRG}	Battery Charger Soft-Start Time				180		µs
I_{TRKL}	Trickle Charge Current	V_{BAT} = 2V, R_{PROG} = 0.8k		35	50	65	mA
V_{TRKL}	Trickle Charge Threshold Voltage	V_{BAT} Rising	●	2.75	2.9	3.05	V
V_{TRHYS}	Trickle Charge Threshold Voltage Hysteresis			100	150	350	mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT} – V_{BAT}, 0°C < T_A < 85°C		70	100	130	mV
ΔV_{UVCL1}, ΔV_{UVCL2}	(V_{CC} – V_{BAT}) Undervoltage Current Limit Threshold Voltage	I_{BAT} = 0.9 I_{CHG} I_{BAT} = 0.1 I_{CHG}		180 90	300 130		mV mV
t_{TIMER}	Charge Termination Timer		●	3	4.5	6	hrs
	Recharge Time		●	1.5	2.25	3	hrs
	Low-Battery Charge Time	V_{BAT} = 2.5V	●	0.75	1.125	1.5	hrs
$I_{C/10}$	End of Charge Indication Current Level	R_{PROG} = 2k (Note 6)	●	0.085	0.1	0.115	mA/mA
T_{LIM}	Junction Temperature in Constant-Temperature Mode				115		°C
R_{ON_CHRG}	Power FET On-Resistance (Between V_{CC} and BAT)	I_{BAT} = 350mA, V_{CC} = 4V			700		mΩ
f_{BADBAT}	Defective Battery Detection $\overline{CHRG}$ Pulse Frequency	V_{BAT} = 2V			2		Hz
D_{BADBAT}	Defective Battery Detection $\overline{CHRG}$ Pulse Frequency Duty Ratio	V_{BAT} = 2V			75		%
I_{NTC}	NTC Pin Current	V_{NTC} = 2.5V				1	µA
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Voltage Threshold Hysteresis			0.76 • V_{CC} 0.015 • V_{CC}		V V
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Voltage Threshold Hysteresis			0.35 • V_{CC} 0.017 • V_{CC}		V V
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold; V_{CC} = 5V Hysteresis			82 50		mV mV
f_{NTC}	Fault Temperature $\overline{CHRG}$ Pulse Frequency				2		Hz
D_{NTC}	Fault Temperature $\overline{CHRG}$ Pulse Frequency Duty Ratio				25		%

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, V_{BAT} = 3.8V, $V_{\overline{EN_CHRG}}$ = 0V, V_{NTC} = 0V, V_{EN_BUCK} = V_{BAT}, V_{MODE} = 0V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck Converter							
V_{FB}	FB Servo Voltage		●	0.78	0.80	0.82	V
I_{FB}	FB Pin Input Current	V_{FB} = 0.85V		–50		50	nA
f_{OSC}	Switching Frequency		●	1.8	2.25	2.75	MHz
$I_{BAT_NL_CF}$	No-Load Battery Current (Continuous Frequency Mode)	No-Load for Regulator, $V_{\overline{EN_CHRG}}$ = 5V, L = 10µH, C = 4.7µF			1.9		mA
$I_{BAT_NL_BM}$	No-Load Battery Current (Burst Mode Operation)	No-Load for Regulator, $V_{\overline{EN_CHRG}}$ = 5V, MODE = V_{BAT}, L = 10µH, C = 4.7µF			23		µA
I_{BAT_SLP}	Battery Current in SLEEP Mode	$V_{\overline{EN_CHRG}}$ = 5V, MODE = V_{BAT}, V_{OUT} > Regulation Voltage	●	10	15	20	µA
V_{UVLO_BUCK}	Buck Undervoltage Lockout Voltage	V_{BAT} Rising V_{BAT} Falling	● ●	2.6 2.4	2.7 2.5	2.8 2.6	V V
R_{ON_P}	PMOS Switch On-Resistance				0.95		Ω
R_{ON_N}	NMOS Switch On-Resistance				0.85		Ω
I_{LIM_P}	PMOS Switch Current Limit			375	520	700	mA
I_{LIM_N}	NMOS Switch Current Limit				700		mA
I_{ZERO_CF}	NMOS Zero Current in Normal Mode				15		mA
I_{PEAK}	Peak Current in Burst Mode Operation	MODE = V_{BAT}		50	100	150	mA
I_{ZERO_BM}	Zero Current in Burst Mode Operation	MODE = V_{BAT}		20	35	50	mA
t_{SS_BUCK}	Buck Soft-Start Time	From the Rising Edge of EN_BUCK to 90% of Buck Regulated Output			400		µs
Logic							
V_{IH}	Input High Voltage	$\overline{EN_CHRG}$, EN_BUCK, MODE Pin Low to High	●			1.2	V
V_{IL}	Input Low Voltage	$\overline{EN_CHRG}$, EN_BUCK, MODE Pin High to Low	●	0.4			V
V_{OL}	Output Low Voltage ($\overline{CHRG}$)	I_{SINK} = 5mA	●		60	105	mV
I_{IH}	Input Current High	EN_BUCK, MODE Pins at 5.5V, V_{BAT} = 5V	●	–1		1	µA
I_{IL}	Input Current Low	$\overline{EN_CHRG}$, EN_BUCK, MODE Pins at GND	●	–1		1	µA
$R_{\overline{EN_CHRG}}$	$\overline{EN_CHRG}$ Pin Input Resistance	$V_{\overline{EN_CHRG}}$ = 5V		1	1.45	3.3	MΩ
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Leakage Current	V_{BAT} = 4.5V, $V_{\overline{EN_CHRG}}$ = 5V	●			1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4081 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much higher than 43°C/W.

Note 4: Although the LTC4081 charger functions properly at 3.75V, full charge current requires an input voltage greater than the desired final battery voltage per ΔV_{UVCL1} specification.

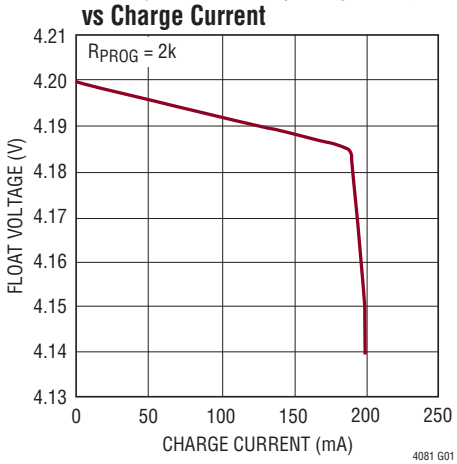
Note 5: The 2.8V maximum buck undervoltage lockout (V_{UVLO_BUCK}) exit threshold must first be exceeded before the minimum V_{BAT} specification applies.

Note 6: $I_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

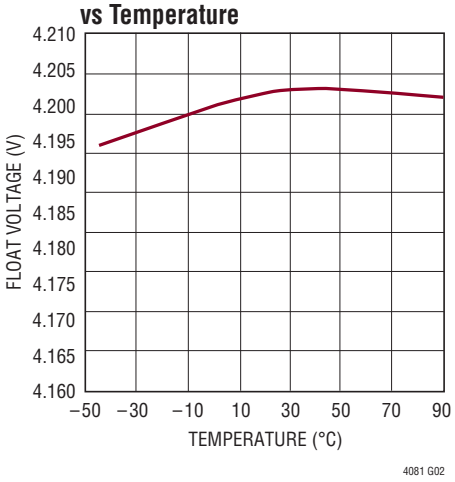
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise specified)

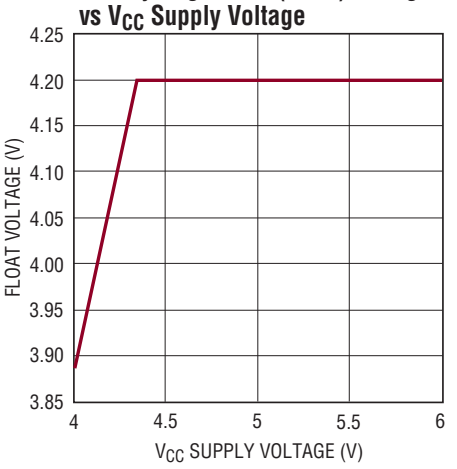
Battery Regulation (Float) Voltage vs Charge Current



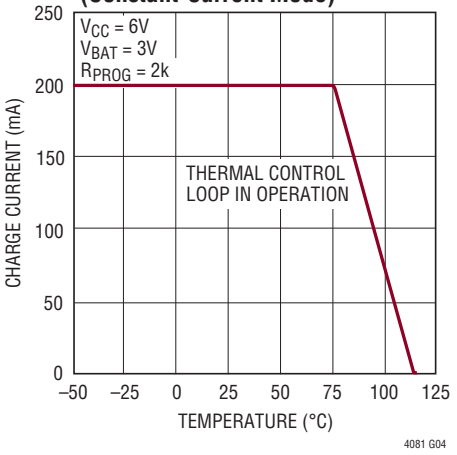
Battery Regulation (Float) Voltage vs Temperature



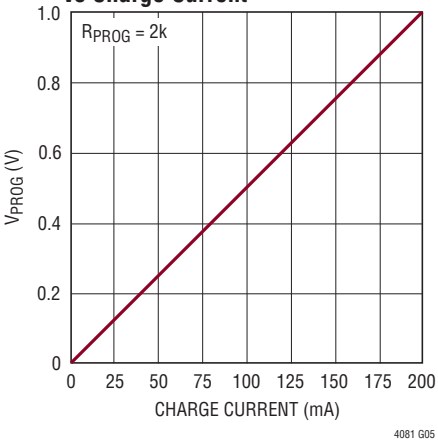
Battery Regulation (Float) Voltage vs V_{CC} Supply Voltage



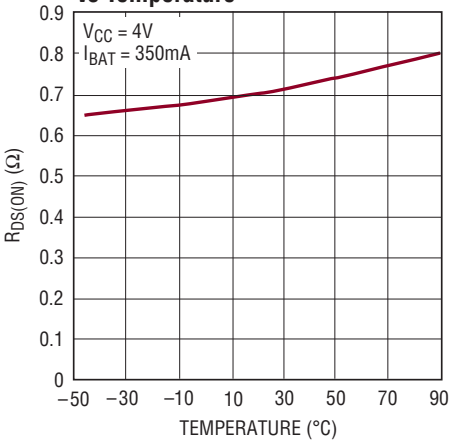
Charge Current vs Temperature with Thermal Regulation (Constant-Current Mode)



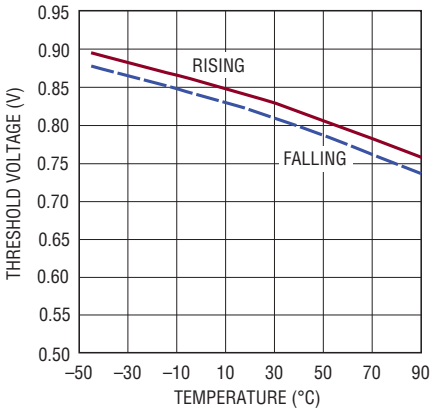
PROG Pin Voltage vs Charge Current



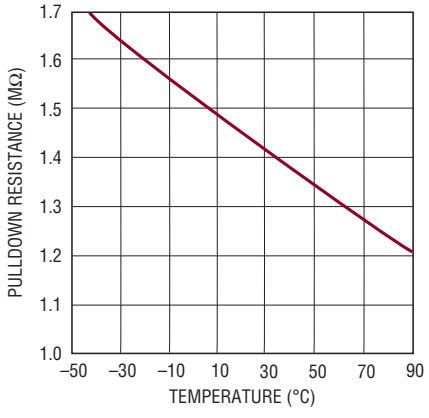
Charger FET On-Resistance vs Temperature



$\overline{EN_CHRG}$, EN_BUCK and MODE Pin Threshold Voltage vs Temperature



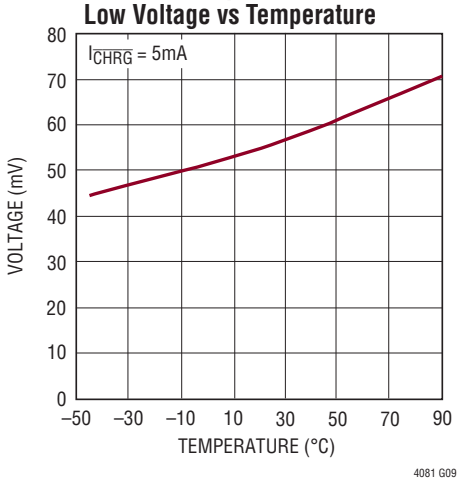
$\overline{EN_CHRG}$ Pin Pull-Down Resistance vs Temperature



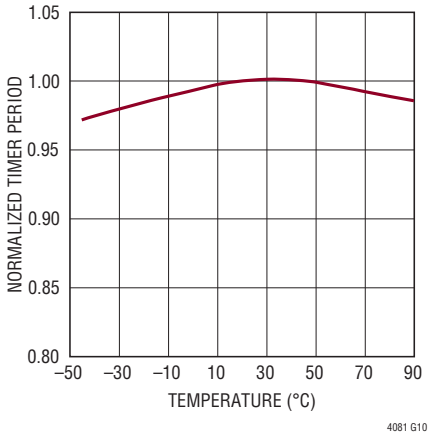
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise specified)

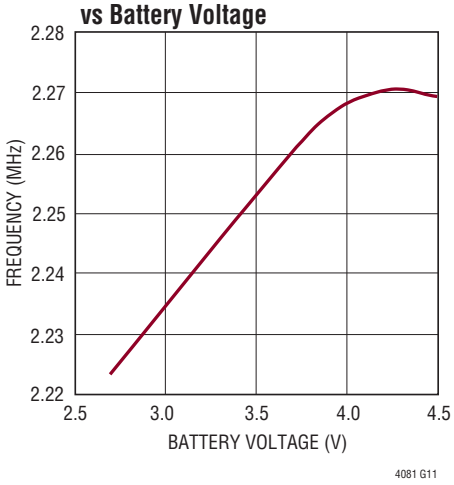
$\overline{CHRG}$ Pin Output Low Voltage vs Temperature



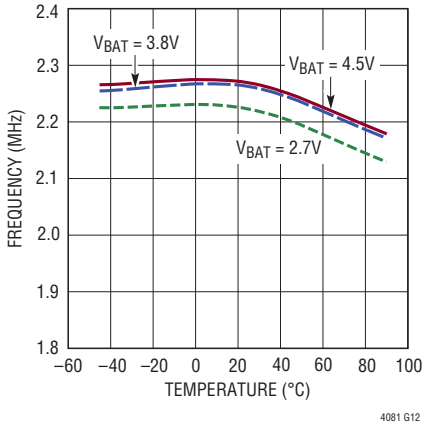
Normalized Charge Termination Time vs Temperature



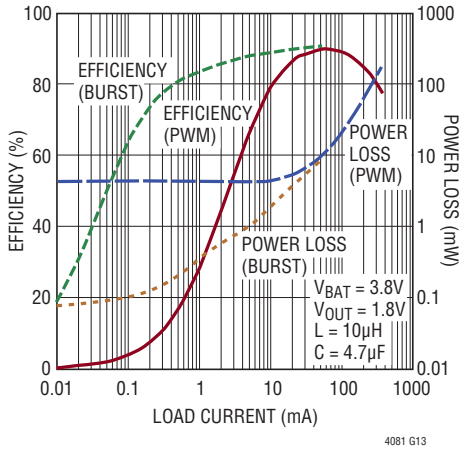
Buck Oscillator Frequency vs Battery Voltage



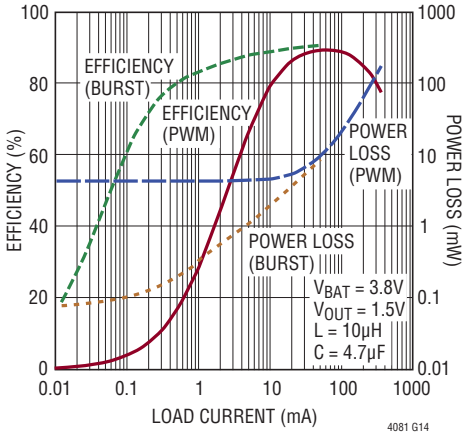
Buck Oscillator Frequency vs Temperature



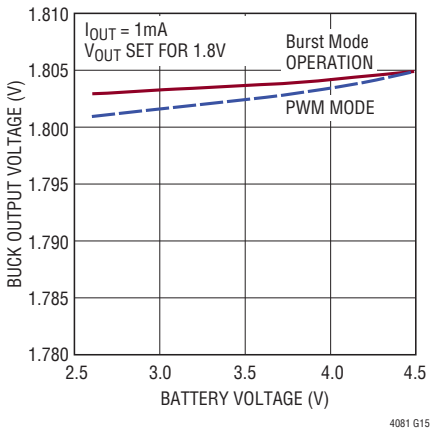
Buck Efficiency vs Load Current (V_{OUT} = 1.8V)



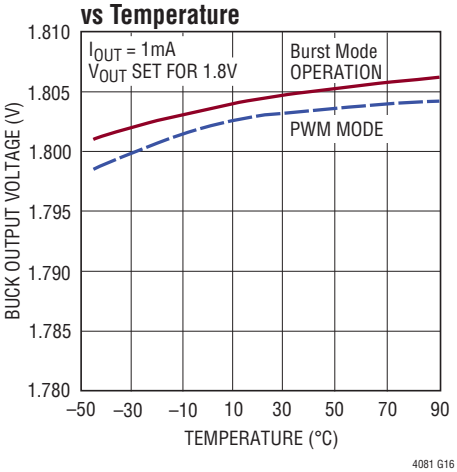
Buck Efficiency vs Load Current (V_{OUT} = 1.5V)



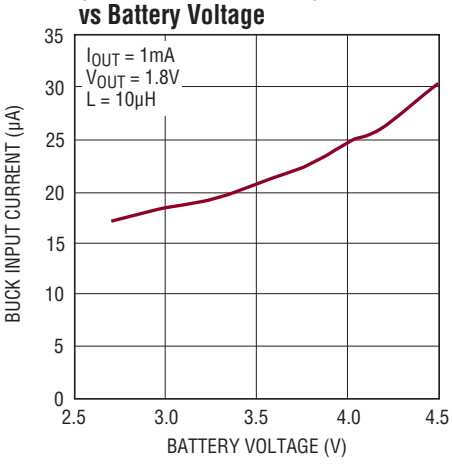
Buck Output Voltage vs Battery Voltage



Buck Output Voltage vs Temperature



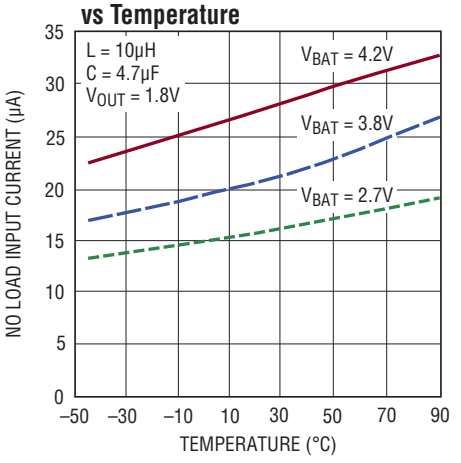
No-Load Buck Input Current (Burst Mode Operation) vs Battery Voltage



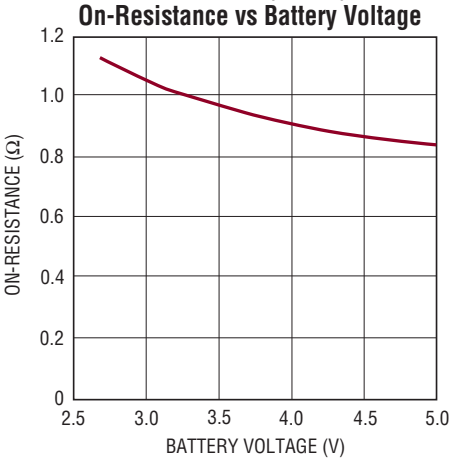
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise specified)

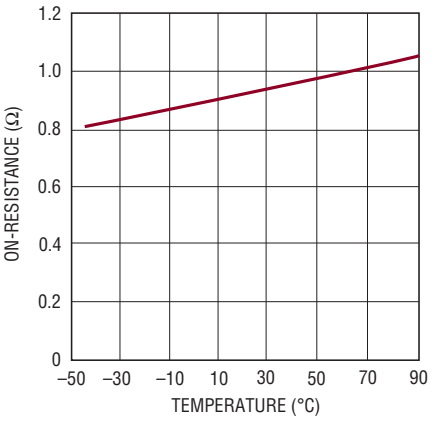
No-Load Buck Input Current (Burst Mode Operation) vs Temperature



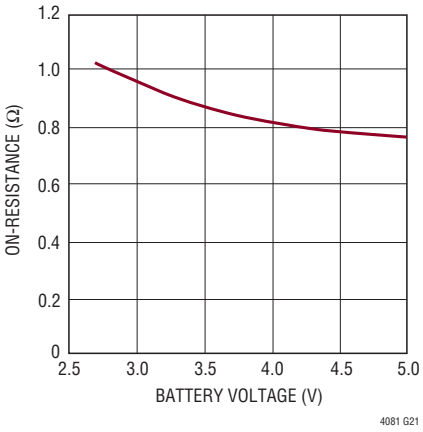
Buck Main Switch (PMOS) On-Resistance vs Battery Voltage



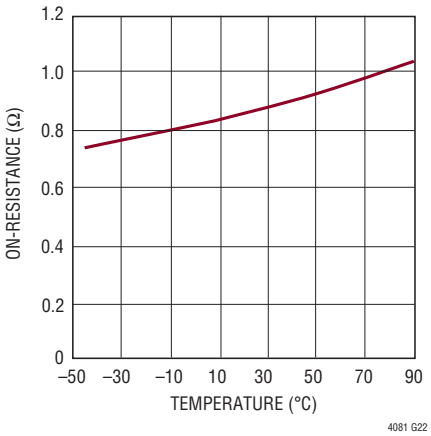
Buck Main Switch (PMOS) On-Resistance vs Temperature



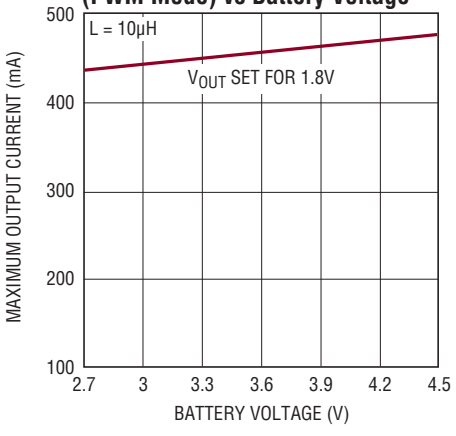
Buck Synchronous Switch (NMOS) On-Resistance vs Battery Voltage



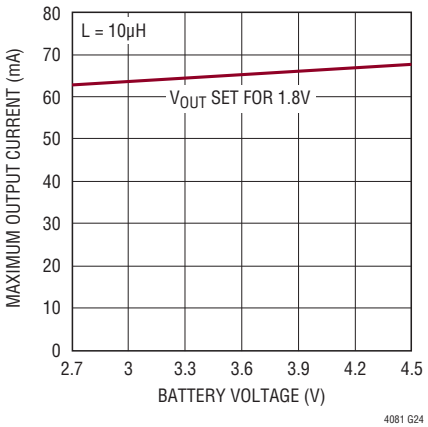
Buck Synchronous Switch (NMOS) On-Resistance vs Temperature



Maximum Output Current (PWM Mode) vs Battery Voltage



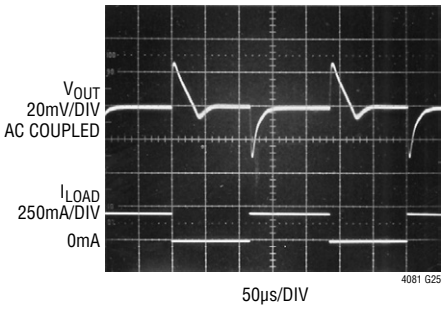
Maximum Output Current (Burst Mode Operation) vs Battery Voltage



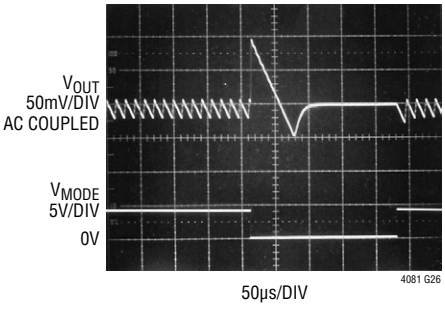
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5V, V_{BAT} = 3.8V, unless otherwise specified)

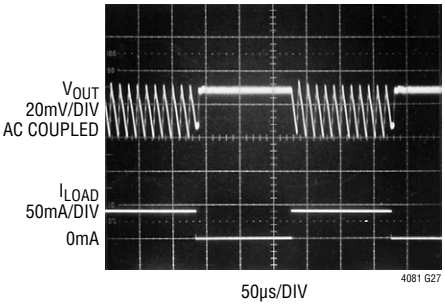
Output Voltage Transient Step Response (PWM Mode)



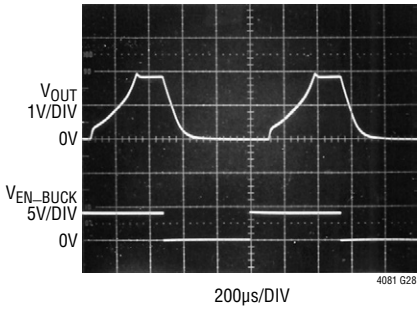
Output Voltage Waveform when Switching Between Burst and PWM Mode (I_{LOAD} = 10mA)



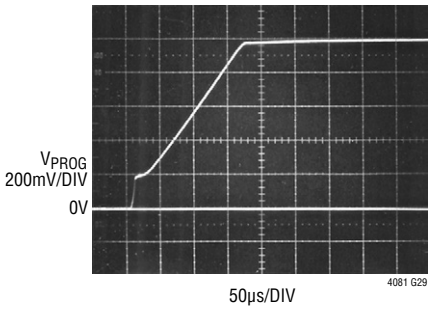
Output Voltage Transient Step Response (Burst Mode Operation)



Buck V_{OUT} Soft-Start (I_{LOAD} = 50mA)



Charger V_{PROG} Soft-Start



PIN FUNCTIONS

BAT (Pin 1): Charge Current Output and Buck Regulator Input. Provides charge current to the battery and regulates the final float voltage to 4.2V. An internal precision resistor divider from this pin sets the float voltage and is disconnected in charger shutdown mode. This pin must be decoupled with a low ESR capacitor for low noise buck operation.

V_{CC} (Pin 2): Positive Input Supply Voltage. This pin provides power to the battery charger. V_{CC} can range from 3.75V to 5.5V. This pin should be bypassed with at least a 1µF capacitor. When V_{CC} is less than 32mV above the BAT pin voltage, the battery charger enters shutdown mode.

$\overline{\text{EN_CHRG}}$ (Pin 3): Enable Input Pin for the Battery Charger. Pulling this pin above the manual shutdown threshold (V_{IH}) puts the LTC4081 charger in shutdown mode, thus stopping the charge cycle. In battery charger shutdown mode, the LTC4081 has less than 10µA supply current and less than 5µA battery drain current provided the regulator is not running. Enable is the default state, but the pin should be tied to GND if unused.

PROG (Pin 4): Charge Current Program and Charge Current Monitor Pin. Connecting a 1% resistor, R_{PROG}, to ground programs the charge current. When charging in constant-current mode, this pin servos to 1V. In all modes, the voltage on this pin can be used to measure the charge current using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 400$$

NTC (Pin 5): Input to the NTC (negative temperature coefficient) Thermistor Temperature Monitoring Circuit. For normal operation, connect a thermistor from the NTC pin to ground and a resistor of equal value from the NTC pin to V_{CC}. When the voltage at this pin drops below 0.35 • V_{CC} at hot temperatures or rises above 0.76 • V_{CC} at cold, charging is suspended, the internal timer is frozen and the $\overline{\text{CHRG}}$ pin output will start to pulse at 2Hz. Pulling this pin below 0.016 • V_{CC} disables the NTC feature. There is approximately 3°C of temperature hysteresis associated with each of the input comparator's thresholds.

$\overline{\text{CHRG}}$ (Pin 6): Open-Drain Charge Status Output. The charge status indicator pin has three states: pull-down, high impedance state, and pulsing at 2Hz. This output can be used as a logic interface or as an LED driver. When the battery is being charged, the $\overline{\text{CHRG}}$ pin is pulled low by an internal N-channel MOSFET. When the charge current drops to 10% of the full-scale current, the $\overline{\text{CHRG}}$ pin is forced to a high impedance state. When the battery voltage remains below 2.9V for one quarter of the full charge time, the battery is considered defective, and the $\overline{\text{CHRG}}$ pin pulses at a frequency of 2Hz with 75% duty cycle. When the NTC pin voltage rises above 0.76 • V_{CC} or drops below 0.35 • V_{CC}, the $\overline{\text{CHRG}}$ pin pulses at a frequency of 2Hz (25% duty cycle).

FB (Pin 7): Feedback Pin for the Buck Regulator. A resistor divider from the regulator's output to the FB pin programs the output voltage. Servo value for this pin is 0.8V.

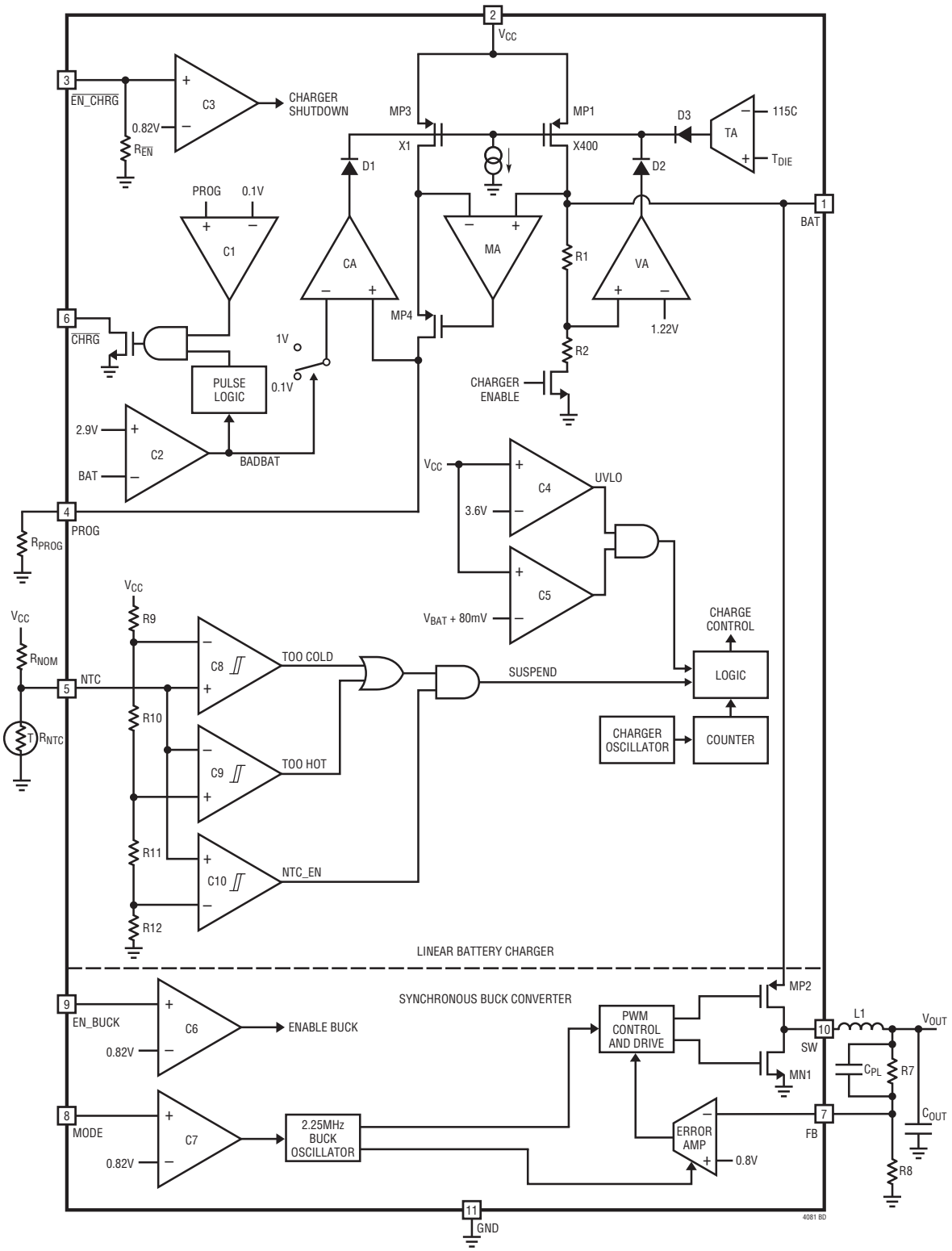
MODE (Pin 8): Burst Mode Enable Pin. Tie this pin high to force the LTC4081 regulator into Burst Mode operation for all load conditions. Tie this pin low to force constant-frequency mode operation for all load conditions. Do not float this pin.

EN_BUCK (Pin 9): Enable Input Pin for the Buck Regulator. Pull this pin high to enable the regulator, pull low to shut down. Do not float this pin.

SW (Pin 10): Switch Pin for the Buck Regulator. Minimize the length of the metal trace connected to this pin. Place the inductor as close to this pin as possible.

GND (Pin 11): Ground. This pin is the back of the Exposed Pad package and must be soldered to the PCB for electrical connection and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC4081 is a full-featured linear battery charger with an integrated synchronous buck converter designed primarily for handheld applications. The battery charger is capable of charging single-cell 4.2V Li-Ion batteries. The buck converter is powered from the BAT pin and has a programmable output voltage providing a maximum load current of 300mA. The converter and the battery charger can run simultaneously or independently of each other.

BATTERY CHARGER OPERATION

Featuring an internal P-channel power MOSFET, MP1, the battery charger uses a constant-current/constant-voltage charge algorithm with programmable current. Charge current can be programmed up to 500mA with a final float voltage of 4.2V ±0.5%. The $\overline{CHRG}$ open-drain status output indicates when C/10 has been reached. No blocking diode or external sense resistor is required; thus, the basic charger circuit requires only two external components. An internal charge termination timer adheres to battery manufacturer safety guidelines. Furthermore, the LTC4081 battery charger is capable of operating from a USB power source.

A charge cycle begins when the voltage at the V_{CC} pin rises above 3.6V and approximately 82mV above the BAT pin voltage, a 1% program resistor is connected from the PROG pin to ground, and the $\overline{EN_CHRG}$ pin is pulled below the shutdown threshold (V_{IL}).

When the BAT pin approaches the final float voltage of 4.2V, the battery charger enters constant-voltage mode and the charge current begins to decrease. When the current drops to 10% of the full-scale charge current, an internal comparator turns off the N-channel MOSFET driving the $\overline{CHRG}$ pin, and the pin becomes high impedance.

An internal thermal limit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 115°C. This feature protects the LTC4081 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without the risk of damaging the LTC4081 or external components. Another benefit of the thermal limit is that charge current can be set according to typical, rather than worst-case, ambient temperatures for a given application with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

An internal timer sets the total charge time, t_{TIMER} (typically 4.5 hours). When this time elapses, the charge cycle terminates and the $\overline{CHRG}$ pin assumes a high impedance state even if C/10 has not yet been reached. To restart the charge cycle, remove the input voltage and reapply it or momentarily force the $\overline{EN_CHRG}$ pin above V_{IH}. A new charge cycle will automatically restart if the BAT pin voltage falls below V_{RECHRG} (typically 4.1V).

Constant-Current/Constant-Voltage/Constant-Temperature

The LTC4081 battery charger uses a unique architecture to charge a battery in a constant-current, constant-voltage and constant-temperature fashion. Three of the amplifier feedback loops shown control the constant-current, CA, constant-voltage, VA, and constant-temperature, TA modes (see Block Diagram). A fourth amplifier feedback loop, MA, is used to increase the output impedance of the current source pair, MP1 and MP3 (note that MP1 is the internal P-channel power MOSFET). It ensures that the drain current of MP1 is exactly 400 times the drain current of MP3.

Amplifiers CA and VA are used in separate feedback loops to force the charger into constant-current or constant-voltage mode, respectively. Diodes D1 and D2 provide priority to either the constant-current or constant-voltage loop, whichever is trying to reduce the charge current the most. The output of the other amplifier saturates low which effectively removes its loop from the system. When in constant-current mode, CA servos the voltage at the PROG pin to be precisely 1V. VA servos its non-inverting input to 1.22V when in constant-voltage mode and the internal resistor divider made up of R1 and R2 ensures that the battery voltage is maintained at 4.2V. The PROG pin voltage gives an indication of the charge current anytime in the charge cycle, as discussed in “Programming Charge Current” in the Applications Information section.

If the die temperature starts to creep up above 115°C due to internal power dissipation, the transconductance amplifier, TA, limits the die temperature to approximately 115°C by reducing the charge current. Diode D3 ensures that TA does not affect the charge current when the die

OPERATION

temperature is below 115°C. In thermal regulation, the PROG pin voltage continues to give an indication of the charge current.

In typical operation, the charge cycle begins in constant-current mode with the current delivered to the battery equal to $400V/R_{PROG}$. If the power dissipation of the LTC4081 results in the junction temperature approaching 115°C, the amplifier (TA) will begin decreasing the charge current to limit the die temperature to approximately 115°C. As the battery voltage rises, the LTC4081 either returns to full constant-current mode or enters constant-voltage mode straight from constant-temperature mode.

Battery Charger Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors the V_{CC} input voltage and keeps the battery charger off until V_{CC} rises above 3.6V and approximately 82mV above the BAT pin voltage. The 3.6V UVLO circuit has a built-in hysteresis of approximately 0.6V, and the 82mV automatic shutdown threshold has a built-in hysteresis of approximately 50mV. During undervoltage lockout conditions, maximum battery drain current is 5µA and maximum supply current is 10µA.

Undervoltage Charge Current Limiting (UVCL)

The battery charger in the LTC4081 includes undervoltage charge current limiting that prevents full charge current until the input supply voltage reaches approximately 300mV above the battery voltage (ΔV_{UVCL1}). This feature is particularly useful if the LTC4081 is powered from a supply with long leads (or any relatively high output impedance). See Applications Information section for further details.

Trickle Charge and Defective Battery Detection

At the beginning of a charge cycle, if the battery voltage is below 2.9V, the battery charger goes into trickle charge mode, reducing the charge current to 10% of the programmed current. If the low battery voltage persists for one quarter of the total time (1.125 hr), the battery is assumed to be defective, the charge cycle terminates and the $\overline{CHRG}$ pin output pulses at a frequency of 2Hz with a 75% duty cycle. If, for any reason, the battery voltage rises above 2.9V, the charge cycle will be restarted. To restart the charge cycle (i.e., when the dead battery is replaced with a discharged battery less than 2.9V), the charger must be reset by removing the input voltage and reapplying it or temporarily pulling the $\overline{EN_CHRG}$ pin above the shutdown threshold.

Battery Charger Shutdown Mode

The LTC4081's battery charger can be disabled by pulling the $\overline{EN_CHRG}$ pin above the shutdown threshold (V_{IH}). In shutdown mode, the battery drain current is reduced to about 2µA and the V_{CC} supply current to about 5µA provided the regulator is off. When the input voltage is not present, the battery charger is in shutdown and the battery drain current is less than 5µA.

$\overline{CHRG}$ Status Output Pin

The charge status indicator pin has three states: pull-down, pulsing at 2Hz (see Trickle Charge and Defective Battery Detection and Battery Temperature Monitoring) and high impedance. The pull-down state indicates that the battery charger is in a charge cycle. A high impedance state indicates that the charge current has dropped below 10% of the full-scale current or the battery charger is disabled. When the timer runs out (4.5 hrs), the $\overline{CHRG}$ pin is also forced to the high impedance state. If the battery charger is not in constant-voltage mode when the charge current is forced to drop below 10% of the full-scale current by UVCL, $\overline{CHRG}$ will stay in the strong pull-down state.

Charge Current Soft-Start

The LTC4081's battery charger includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to full-scale current over a period of approximately 180µs. This has the effect of minimizing the transient current load on the power supply during start-up.

Timer and Recharge

The LTC4081's battery charger has an internal charge termination timer that starts when the input voltage is greater than the undervoltage lockout threshold and at least 82mV above BAT, and the battery charger is leaving shutdown.

OPERATION

At power-up or when exiting shutdown, the charge time is set to 4.5 hours. Once the charge cycle terminates, the battery charger continuously monitors the BAT pin voltage using a comparator with a 2ms filter time. When the average battery voltage falls below 4.1V (which corresponds to 80% – 90% battery capacity), a new charge cycle is initiated and a 2.25 hour timer begins. This ensures that the battery is kept at, or near, a fully charged condition and eliminates the need for periodic charge cycle initiations. The $\overline{CHRG}$ output assumes a strong pull-down state during recharge cycles until C/10 is reached or the recharge cycle terminates.

Battery Temperature Monitoring via NTC

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 1.

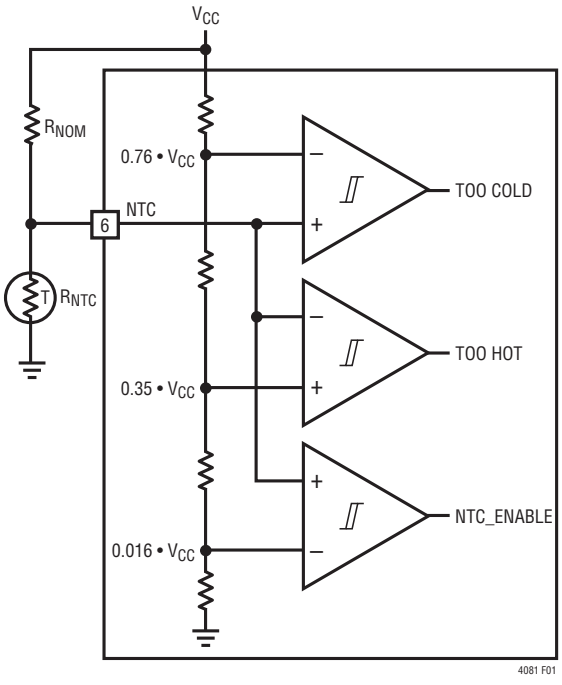


Figure 1. NTC Circuit Information

To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a resistor, R_{NOM}, from the NTC pin to V_{CC}. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (this value is 10k for a Vishay NTHS0603NO1N1002J thermistor). The LTC4081 goes into hold mode when the value of the NTC thermistor drops to 0.53 times the value of R_{NOM}, which corresponds to approximately 40°C, and when the value of the NTC thermistor increases to 3.26 times the value of R_{NOM}, which corresponds to approximately 0°C. Hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. For a Vishay NTHS0603NO1N1002J thermistor, this value is 32.6k which corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point.

When the charger is in Hold mode (battery temperature is either too hot or too cold) the $\overline{CHRG}$ pin pulses in a 2Hz, 25% duty cycle frequency unless the charge task is finished or the battery is assumed to be defective. If the NTC pin is grounded, the NTC function will be disabled.

SWITCHING REGULATOR OPERATION

The switching buck regulator in the LTC4081 can be turned on by pulling the EN_BUCK pin above V_{IH}. It has two user-selectable modes of operation: constant-frequency (PWM) mode and Burst Mode operation. The constant-frequency mode operation offers low noise at the expense of efficiency whereas the Burst Mode operation offers higher efficiency at light loads at the cost of increased noise, higher output voltage ripple, and less output current. A detailed description of different operating modes and different aspects of operation follow. Operations can best be understood by referring to the Block Diagram.

OPERATION

Constant-Frequency (PWM) Mode Operation

The switching regulator operates in constant-frequency (PWM) mode when the MODE pin is pulled below V_{IL}. In this mode, it uses a current mode architecture including an oscillator, an error amplifier, and a PWM comparator for excellent line and load regulation. The main switch MP2 (P-channel MOSFET) turns on to charge the inductor at the beginning of each clock cycle if the FB pin voltage is less than the 0.8V reference voltage. The current into the inductor (and the load) increases until it reaches the peak current demanded by the error amp. At this point, the main switch turns off and the synchronous switch MN1 (N-channel MOSFET) turns on allowing the inductor current to flow from ground to the load until either the next clock cycle begins or the current reduces to the zero current (I_{ZERO}) level.

Oscillator: In constant-frequency mode, the switching regulator uses a dedicated oscillator which runs at a fixed frequency of 2.25MHz. This frequency is chosen to minimize possible interference with the AM radio band.

Error Amplifier: The error amplifier is an internally compensated transconductance (g_m) amplifier with a g_m of 65 µmhos. The internal 0.8V reference voltage is compared to the voltage at the FB pin to generate a current signal at the output of the error amplifier. This current signal represents the peak inductor current required to achieve regulation.

PWM Comparator: Lossless current sensing converts the PMOS switch current signal to a voltage which is summed with the internal slope compensation signal. The PWM comparator compares this summed signal to determine when to turn off the main switch. The switch current sensing is blanked for ~12ns at the beginning of each clock cycle to prevent false switch turn-off.

Burst Mode Operation

Burst Mode operation can be selected by pulling the MODE pin above V_{IH}. In this mode, the internal oscillator is disabled, the error amplifier is converted into a comparator monitoring the FB voltage, and the inductor current swings between a fixed I_{PEAK} (~100mA) and I_{ZERO} (35mA) irrespective of the load current as long as the FB pin voltage is less than or equal to the reference voltage of 0.8V. Once V_{FB} is greater than 0.8V, the control logic shuts off both switches along with most of the circuitry and the regulator is said to enter into SLEEP mode. In SLEEP mode, the regulator only draws about 20µA from the BAT pin provided that the battery charger is turned off. When the output voltage droops about 1% from its nominal value, the regulator wakes up and the inductor current resumes swinging between I_{PEAK} and I_{ZERO}. The output capacitor recharges and causes the regulator to re-enter the SLEEP state if the output load remains light enough. The frequency of this intermittent burst operation depends on the load current. That is, as the load current drops further, the regulator turns on less frequently. Thus Burst Mode operation increases the efficiency at light loads by minimizing the switching and quiescent losses. However, the output voltage ripple increases to about 2%.

To minimize ripple in the output voltage, the current limits for both switches in Burst Mode operation are reduced to about 20% of their values in the constant-frequency mode. Also the zero current of the synchronous switch is changed to about 35mA thereby preventing reverse conduction through the inductor. Consequently, the regulator can only deliver approximately 67mA of load current while in Burst Mode operation. Any attempt to draw more load current will cause the output voltage to drop out of regulation.

Current Limit

To prevent inductor current runaway, there are absolute current limits (I_{LIM}) on both the PMOS main switch and the NMOS synchronous switch. These limits are internally set at 520mA and 700mA respectively for PWM mode. If the peak inductor current demanded by the error amplifier ever exceeds the PMOS I_{LIM}, the error amplifier will be ignored and the inductor current will be limited to PMOS I_{LIM}. In Burst Mode operation, the PMOS current limit is reduced to 100mA to minimize output voltage ripple.

Zero Current Comparator

The zero or reverse current comparator monitors the inductor current to the output and shuts off the synchronous rectifier when this current reduces to a predetermined value (I_{ZERO}). In fixed frequency mode, this is set to

OPERATION

negative 15mA meaning that the regulator allows the inductor current to flow in the reverse direction (from the output to ground through the synchronous rectifier) to a maximum value of 15mA. This is done to ensure that the regulator is able to regulate at very light loads without skipping any cycles thereby keeping output voltage ripple and noise low at the cost of efficiency.

However, in Burst Mode operation, I_{ZERO} is set to positive 35mA meaning that the synchronous switch is turned off as soon as the current through the inductor to the output decreases to 35mA in the discharge cycle. This preserves the charge on the output capacitor and increases the overall efficiency at light loads.

Soft-Start

The LTC4081 switching regulator provides soft-start in both modes of operation by slowly charging an internal capacitor. The voltage on this capacitor, in turn, slowly ramps the current limits of both switches from a low value to their respective maximum values over a period of about 400µs. The soft-start capacitor is discharged completely whenever the regulator is disabled.

Short-Circuit Protection

In the event of a short circuit at the output or during start-up, V_{OUT} will be near zero volts. Since the downward slope of the inductor current is ~V_{OUT}/L, the inductor current may not get a chance to discharge enough to avoid a runaway situation. Because the current sensing is blanked for ~12ns at the beginning of each clock cycle, inductor current can build up to a dangerously high level over a number of cycles even if there is a hard current limit on the main PMOS switch. This is why the switching regulator in the LTC4081 also monitors current through the synchronous NMOS switch and imposes a hard limit on it. If the inductor current through the NMOS switch at the end of a discharge cycle is not below this limit, the regulator skips the next charging cycle thereby preventing inductor current runaway.

Switching Regulator Undervoltage Lockout

Whenever V_{BAT} is less than 2.7V, an undervoltage lockout circuit keeps the regulator off, preventing unreliable operation. However, if the regulator is already running and the battery voltage is dropping, the undervoltage comparator does not shut down the regulator until V_{BAT} drops below 2.5V.

Dropout Operation

When the BAT pin voltage approaches V_{OUT}, the duty cycle of the switching regulator approaches 100%. When V_{BAT} is approximately equal to V_{OUT}, the regulator is said to be in dropout. In dropout, the main switch (MP2) stays on continuously with the output voltage being equal to the battery voltage minus the voltage drops across the main switch and the inductor.

Global Thermal Shutdown

The LTC4081 includes a global thermal shutdown which shuts off the entire device (battery charger and switching regulator) if the die temperature exceeds 160°C. The LTC4081 resumes normal operation once the temperature drops approximately 14°C.

APPLICATIONS INFORMATION

BATTERY CHARGER

Programming Charge Current

The battery charge current is programmed using a single resistor from the PROG pin to ground. The charge current is 400 times the current out of the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = 400 \bullet \frac{1V}{I_{BAT}}, I_{BAT} = 400 \bullet \frac{1V}{R_{PROG}}$$

The charge current out of the BAT pin can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 400$$

Stability Considerations

The LTC4081 battery charger contains two control loops: constant-voltage and constant-current. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 4.7µF capacitor with a 0.2Ω to 1Ω series resistor from BAT to GND is required to keep ripple voltage low when the battery is disconnected.

In constant-current mode, the PROG pin voltage is in the feedback loop, not the battery voltage. Because of the additional pole created by PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

Average, rather than instantaneous, battery current may be of interest to the user. For example, when the switching regulator operating in low current mode is connected in parallel with the battery, the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses. In such a case, a simple RC filter can be used on the PROG pin to measure the average battery current as shown in Figure 2. A 10k resistor has been added between the PROG pin and the filter capacitor to ensure stability.

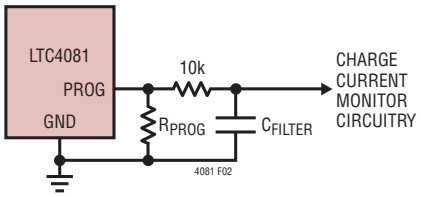


Figure 2. Isolating Capacitive Load on PROG Pin and Filtering

Undervoltage Charge Current Limiting (UVCL)

USB powered systems tend to have highly variable source impedances (due primarily to cable quality and length). A transient load combined with such impedance can easily trip the UVLO threshold and turn the battery charger off unless undervoltage charge current limiting is implemented.

Consider a situation where the LTC4081 is operating under normal conditions and the input supply voltage begins to sag (e.g. an external load drags the input supply down). If the input voltage reaches V_{UVCL} (approximately 300mV above the battery voltage, ΔV_{UVCL}), undervoltage charge current limiting will begin to reduce the charge current in an attempt to maintain ΔV_{UVCL} between V_{CC} and BAT. The LTC4081 will continue to operate at the reduced charge current until the input supply voltage is increased or voltage mode reduces the charge current further.

Operation from Current Limited Wall Adapter

By using a current limited wall adapter as the input supply, the LTC4081 can dissipate significantly less power when programmed for a current higher than the limit of the wall adapter.

APPLICATIONS INFORMATION

Consider a situation where an application requires a 200mA charge current for a discharged 800mAh Li-Ion battery. If a typical 5V (non-current limited) input supply is available then the peak power dissipation inside the part can exceed 300mW.

Now consider the same scenario, but with a 5V input supply with a 200mA current limit. To take advantage of the supply, it is necessary to program the LTC4081 to charge at a current greater than 200mA. Assume that the LTC4081 charger is programmed for 300mA (i.e., R_{PROG} = 1.33kΩ) to ensure that part tolerances maintain a programmed current higher than 200mA. Since the battery charger will demand a charge current higher than the current limit of the input supply, the supply voltage will collapse to the battery voltage plus 200mA times the on-resistance of the internal PFET. The on-resistance of the battery charger power device is approximately 0.7Ω with a 5V supply. The actual on-resistance will be slightly higher due to the fact that the input supply will have collapsed to less than 5V. The power dissipated during this phase of charging is approximately 30mW. That is a ten times improvement over the non-current limited supply power dissipation.

USB and Wall Adapter Power

Although the LTC4081 allows charging from a USB port, a wall adapter can also be used to charge Li-Ion batteries. Figure 3 shows an example of how to combine wall adapter and USB power inputs. A P-channel MOSFET, MP1, is used to prevent back conducting into the USB port when a wall adapter is present and Schottky diode, D1, is used to prevent USB power loss through the 1k pull-down resistor.

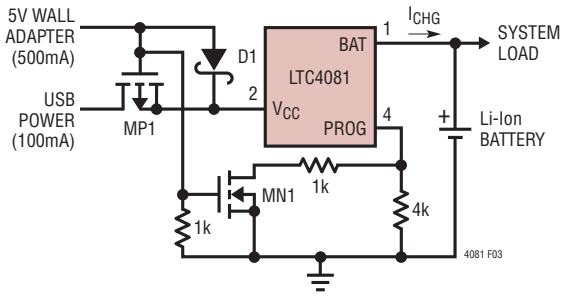


Figure 3. Combining Wall Adapter and USB Power

Typically a wall adapter can supply significantly more current than the current-limited USB port. Therefore, an N-channel MOSFET, MN1, and an extra program resistor can be used to increase the charge current when the wall adapter is present.

Power Dissipation

The conditions that cause the LTC4081 battery charger to reduce charge current through thermal feedback can be approximated by considering the total power dissipated in the IC. For high charge currents, the LTC4081 power dissipation is approximately:

$$P_D = (V_{CC} - V_{BAT}) \bullet I_{BAT} + P_{D_BUCK}$$

Where P_D is the total power dissipated within the IC, V_{CC} is the input supply voltage, V_{BAT} is the battery voltage, I_{BAT} is the charge current and P_{D_BUCK} is the power dissipation due to the regulator. P_{D_BUCK} can be calculated as:

$$P_{D_BUCK} = V_{OUT} \bullet I_{OUT} \left(\frac{1}{\eta} - 1 \right)$$

Where V_{OUT} is the regulated output of the switching regulator, I_{OUT} is the regulator load and η is the regulator efficiency at that particular load.

It is not necessary to perform worst-case power dissipation scenarios because the LTC4081 will automatically reduce the charge current to maintain the die temperature at approximately 115°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$T_A = 115°C - P_D\theta_{JA}$

$T_A = 115°C - (V_{CC} - V_{BAT}) \bullet I_{BAT} \bullet \theta_{JA}$ if the regulator is off.

Example: Consider the extreme case when an LTC4081 is operating from a 6V supply providing 250mA to a 3V Li-Ion battery and the regulator is off. The ambient temperature above which the LTC4081 will begin to reduce the 250mA charge current is approximately:

$T_A = 115°C - (6V - 3V) \bullet (250mA) \bullet 43°C/W$

$T_A = 115°C - 0.75W \bullet 43°C/W = 115°C - 32.25°C$

$T_A = 82.75°C$

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If there is more power dissipation due to the regulator, the thermal regulation will begin at a somewhat lower temperature. In the above circumstances, the LTC4081 can be used above 82.75°C, but the charge current will be reduced from 250mA. The approximate current at a given ambient temperature can be calculated:

$$I_{BAT} = \frac{115°C - T_A}{(V_{CC} - V_{BAT}) \bullet \theta_{JA}}$$

Using the previous example with an ambient temperature of 85°C, the charge current will be reduced to approximately:

$$I_{BAT} = \frac{115°C - 85°C}{(6V - 3V) \bullet 43°C/W} = \frac{30°C}{129°C/A} = 232.6mA$$

Furthermore, the voltage at the PROG pin will change proportionally with the charge current as discussed in the Programming Charge Current section.

V_{CC} Bypass Capacitor

Many types of capacitors can be used for input bypassing; however, caution must be exercised when using multi-layer ceramic capacitors. Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the battery charger input to a live power source. Adding a 1Ω series resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients. For more information, refer to Application Note 88.

Thermistors

The LTC4081 NTC trip points are designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's "R-T Curve 1." The Vishay NTHS0603N01N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 1" characteristic in a variety of sizes. Furthermore, any thermistor whose ratio of R_{COLD} to R_{HOT} is about 5 will also work (Vishay Dale R-T Curve 1 shows a ratio of R_{COLD} to R_{HOT} of 3.266/0.5325 = 6.13).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 1." Using different R-T curves, such as Vishay Dale "R-T Curve 2", is also possible. This curve, combined with LTC4081 internal thresholds, gives temperature trip points of approximately 0°C (falling) and 40°C (rising), a delta of 40°C. This delta in temperature can be moved in either direction by changing the value of R_{NOM} with respect to R_{NTC}. Increasing R_{NOM} will move both trip points to higher temperatures. To calculate R_{NOM} for a shift to lower temperature for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{3.266} \bullet R_{NTC} \text{ at } 25°C$$

where R_{COLD} is the resistance ratio of R_{NTC} at the desired cold temperature trip point. If you want to shift the trip points to higher temperatures use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.5325} \bullet R_{NTC} \text{ at } 25°C$$

where R_{HOT} is the resistance ratio of R_{NTC} at the desired hot temperature trip point.

Here is an example using a 100k R-T Curve 2 thermistor from Vishay Dale. The difference between the trip points is 40°C, from before, and we want the cold trip point to be 0°C, which would put the hot trip point at 40°C. The R_{NOM} needed is calculated as follows:

$$R_{NOM} = \frac{R_{COLD}}{3.266} \bullet R_{NTC} \text{ at } 25°C$$

$$= \frac{2.816}{3.266} \bullet 10k = 8.62k$$

The nearest 1% value for R_{NOM} is 8.66k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 40°C respectively. To extend the delta

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between the cold and hot trip points, a resistor, R1, can be added in series with R_{NTC} (see Figure 4). The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{3.266 - 0.5325}$$

$$R_1 = \left(\frac{0.5325}{3.266 - 0.5325} \right) \bullet (R_{COLD} - R_{HOT}) - R_{HOT}$$

where R_{NOM} is the value of the bias resistor and R_{HOT} and R_{COLD} are the values of R_{NTC} at the desired temperature trip points. Continuing the example from before with a desired trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{3.266 - 0.5325} = \frac{10k \bullet (2.816 - 0.4086)}{3.266 - 0.5325}$$

$$= 8.8k,\ 8.87k \text{ is the nearest 1\% value.}$$

$$R_1 = 10k \bullet \left(\frac{0.5325}{3.266 - 0.5325} \right) \bullet (2.816 - 0.4086) - 0.4086$$

$$= 604\Omega,\ 604 \text{ is the nearest 1\% value.}$$

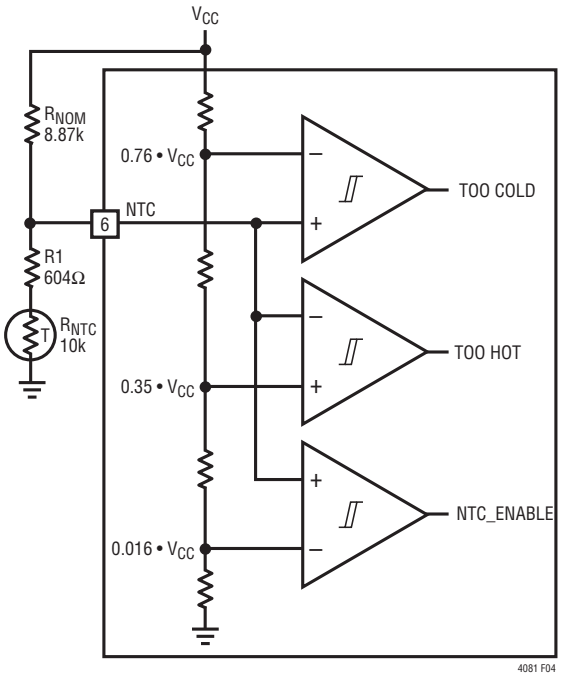

Figure 4. NTC Circuits

NTC Trip Point Error

When a 1% resistor is used for R_{HOT}, the major error in the 40°C trip point is determined by the tolerance of the NTC thermistor. A typical 100k NTC thermistor has ±10% tolerance. By looking up the temperature coefficient of the thermistor at 40°C, the tolerance error can be calculated in degrees centigrade. Consider the Vishay NTHS0603N01N1003J thermistor, which has a temperature coefficient of –4%/°C at 40°C. Dividing the tolerance by the temperature coefficient, ±5%/(4%/°C) = ±1.25°C, gives the temperature error of the hot trip point.

The cold trip point error depends on the tolerance of the NTC thermistor and the degree to which the ratio of its value at 0°C and its value at 40°C varies from 6.14 to 1. Therefore, the cold trip point error can be calculated using the tolerance, TOL, the temperature coefficient of the thermistor at 0°C, TC (in %/°C), the value of the thermistor at 0°C, R_{COLD}, and the value of the thermistor at 40°C, R_{HOT}. The formula is:

$$\text{Temperature Error}(°C) = \frac{\left(\frac{1+TOL}{6.14} \bullet \frac{R_{COLD}}{R_{HOT}} - 1 \right) \bullet 100}{TC}$$

For example, the Vishay NTHS0603N01N1003J thermistor with a tolerance of ±5%, TC of –5%/°C and R_{COLD}/R_{HOT} of 6.13, has a cold trip point error of:

$$\text{Temperature Error}(°C) = \frac{\left(\frac{1+0.05}{6.14} \bullet 6.13 - 1 \right) \bullet 100}{-5}$$

$$= -0.95°C,\ 1.05°C$$

SWITCHING REGULATOR

Setting the Buck Converter Output Voltage

The LTC4081 regulator compares the FB pin voltage with an internal 0.8V reference to generate an error signal at the output of the error amplifier. A voltage divider from

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V_{OUT} to ground (as shown in the Block Diagram) programs the output voltage via FB using the formula:

$$V_{OUT} = 0.8V \bullet \left[1 + \frac{R7}{R8} \right]$$

Keeping the current low (<5µA) in these resistors maximizes efficiency, but making them too low may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop. To improve the frequency response, a phase-lead capacitor (C_{PL}) of approximately 10pF can be used. Great care should be taken to route the FB line away from noise sources, such as the inductor or the SW line.

Inductor Selection

The value of the inductor primarily determines the current ripple in the inductor. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_{OSC} \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is ΔI_L = 0.3 • I_{LIM}, where I_{LIM} is the peak switch current limit. The largest ripple current occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L \geq \frac{V_{OUT}}{f_0 \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

For applications with V_{OUT} = 1.8V, the above equation suggests that an inductor of at least 6.8µH should be used for proper operation.

Many different sizes and shapes of inductors are available from numerous manufacturers. To maximize efficiency, choose an inductor with a low DC resistance. Keep in mind that most inductors that are very thin or have a very small volume typically have much higher core and DCR losses and will not give the best efficiency. Also choose an inductor with a DC current rating at least 1.5 times larger than the peak inductor current limit to ensure that the inductor does not saturate during normal operation. To minimize radiated noise use a toroid or shielded pot core inductor in ferrite or permalloy materials. Table 1 shows a list of several inductor manufacturers.

Table 1. Recommended Surface Mount Inductor Manufacturers

Coilcraft	www.coilcraft.com
Sumida	www.sumida.com
Murata	www.murata.com
Toko	www.tokoam.com

Input and Output Capacitor Selection

Since the input current waveform to a buck converter is a square wave, it contains very high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass the BAT pin which is the input for the converter. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on BAT directly controls the amount of input voltage ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple.

To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass V_{OUT}. A typical value for this capacitor is 4.7µF.

Multilayer Ceramic Chip Capacitors (MLCC) typically have exceptional ESR performance. MLCCs combined with a carefully laid out board with an unbroken ground plane will yield very good performance and low EMI emissions.

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There are several types of ceramic capacitors with considerably different characteristics. Y5V ceramic capacitors have apparently higher packing density but poor performance over their rated voltage or temperature ranges. Under given voltage and temperature conditions, X5R and X7R ceramic capacitors should be compared directly by case size rather than specified value for a desired minimum capacitance. Some manufacturers provide excellent data on their websites about achievable capacitance. Table 2 shows a list of several ceramic capacitor manufacturers.

Table 2. Recommended Ceramic Capacitor Manufacturers

Taiyo Yuden	www.t-yuden.com
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com

Board Layout Considerations

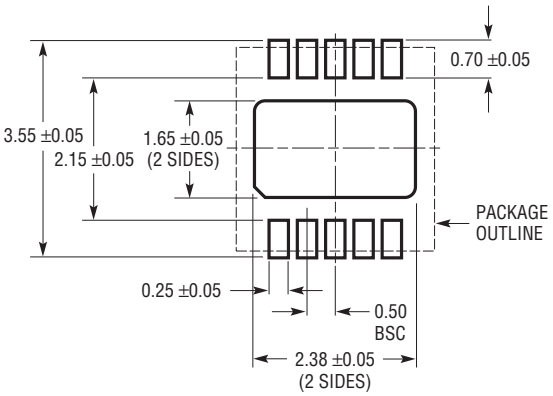
To be able to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the LTC4081's package has a good thermal contact to the PC board ground. Correctly soldered to a 2500mm^2 double-sided 1 oz. copper board, the LTC4081 has a thermal resistance of approximately 43°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistance far greater than 43°C/W.

Furthermore due to its high frequency switching circuitry, it is imperative that the input capacitor, BAT pin capacitor, inductor, and the output capacitor be as close to the LTC4081 as possible and that there is an unbroken ground plane under the LTC4081 and all of its high frequency components.

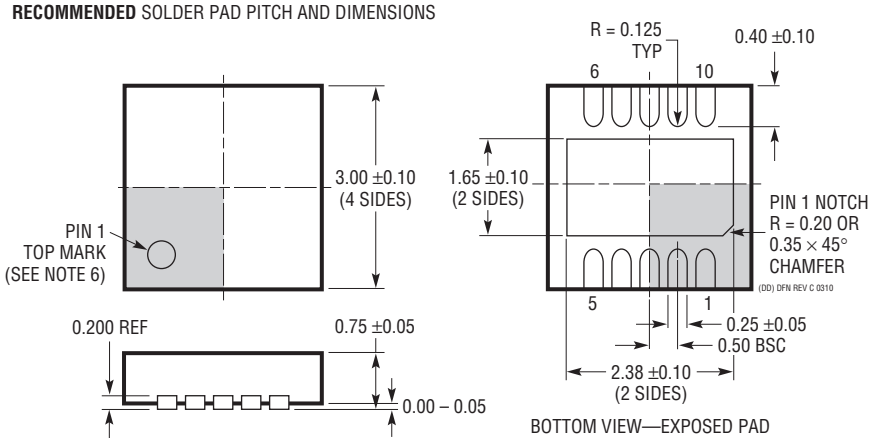
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/15	Modified Typical Application diagrams	1, 24

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