High Efficiency Battery Charger/USB Power Manager with Regulated Output Voltage

FEATURES

- **Switching Regulator Makes Optimal Use of Limited Power Available from USB Port to Charge Battery and Power Application**
- **180mΩ Internal Ideal Diode Plus External Ideal Diode Controller Seamlessly Provide Low Loss Power Path When Input Power is Limited or Unavailable**
- **Automatic Charge Current Reduction Maintains 3.6V Minimum V_{OUT}**
- Full Featured Li-Ion/Polymer Battery Charger
- V_{BUS} Operating Range: 4.25V to 5.5V (7V Absolute Maximum—Transient)
- 1.2A Maximum Input Current Limit
- 1.5A Maximum Charge Current with Thermal Limiting
- Bat-Track™ Adaptive Output Control
- Slew Control Reduces Switching EMI
- Low Profile (0.75mm) 14-Lead 4mm × 3mm DFN Package

APPLICATIONS

- Media Players
- Digital Cameras
- GPS
- PDAs
- Smart Phones

DESCRIPTION

The LTC®4088-1/LTC4088-2 is a high efficiency USB PowerPath™ controller and Li-Ion/Polymer battery charger. It includes a synchronous switching input regulator, a full-featured battery charger and an ideal diode. Designed specifically for USB applications, the LTC4088-1/LTC4088-2's switching regulator automatically limits its input current to either 100mA, 500mA or 1A via logic control. The LTC4088-1 powers-up with the charger off; the LTC4088-2 powers-up with the charger on.

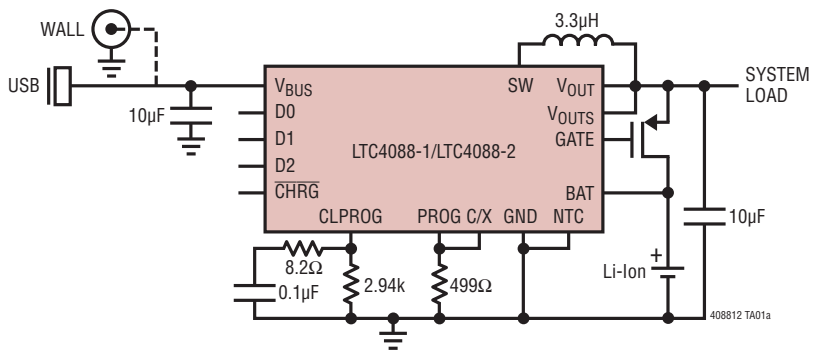
The switching input stage provides power to V_{OUT} where power sharing between the application circuit and the battery charger is managed. Charge current is automatically reduced to maintain a regulated 3.6V V_{OUT} during low-battery conditions. As the battery is charged, V_{OUT} tracks V_{BAT} for high efficiency charging. This feature allows the LTC4088-1/LTC4088-2 to provide more power to the application and eases thermal issues in constrained applications.

An ideal diode ensures that system power is available from the battery when the input current limit is reached or if the USB or wall supply is removed.

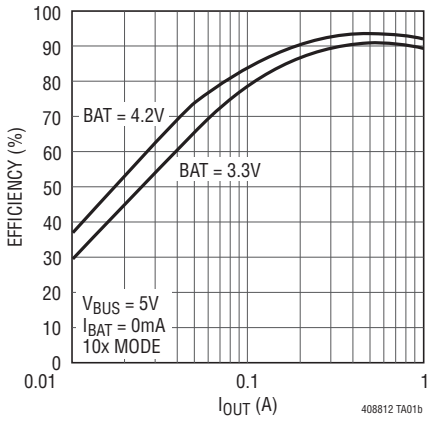
The LTC4088-1/LTC4088-2 is available in the low profile 14-Lead 4mm × 3mm × 0.75mm DFN surface mount package.

TYPICAL APPLICATION

High Efficiency Battery Charger/USB Power Manager



Switching Regulator Efficiency to System Load (P_{OUT}/P_{BUS})

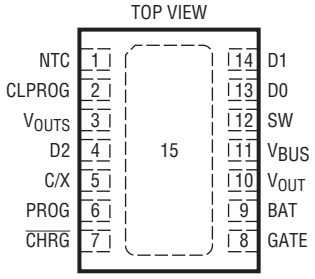


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{BUS} (Transient) t < 1ms, Duty Cycle < 1% .. –0.3V to 7V
V_{BUS} (Static), BAT, $\overline{CHRG}$, NTC, D0, D1, D2 ..... –0.3V to 6V
I_{CLPROG} 3mA
I_{PROG}, $I_{C/X}$ 2mA
$I_{\overline{CHRG}}$ 75mA
I_{OUT} 2A
I_{SW} 2A
I_{BAT} 2A
Maximum Operating Junction Temperature ..... 125°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4088EDE-1#PBF	LTC4088EDE-1#TRPBF	40881	14-Lead (4mm x 3mm x 0.75mm) Plastic DFN	–40°C to 85°C
LTC4088EDE-2#PBF	LTC4088EDE-2#TRPBF	40882	14-Lead (4mm x 3mm x 0.75mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part markings, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, R_{CLPROG} = 2.94k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
V_{BUS}	Input Supply Voltage		●	4.35		5.5	V
$I_{BUS(LIM)}$	Total Input Current	1x Mode	●	92	97	100	mA
		5x Mode	●	445	470	500	mA
		10x Mode	●	815	877	1000	mA
		Low Power Suspend Mode	●	0.32	0.39	0.5	mA
		High Power Suspend Mode	●	1.6	2.05	2.5	mA
I_{BUSQ} (Note 4)	Input Quiescent Current	1x Mode			6		mA
		5x Mode			14		mA
		10x Mode			14		mA
		Low Power Suspend Mode			0.038		mA
		High Power Suspend Mode			0.038		mA
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1x Mode			224		mA/mA
		5x Mode			1133		mA/mA
		10x Mode			2140		mA/mA
		Low Power Suspend Mode			11.3		mA/mA
		High Power Suspend Mode			59.4		mA/mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, R_{CLPROG} = 2.94k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OUT}	V_{OUT} Current Available Before Discharging Battery	1x Mode, BAT = 3.3V 5x Mode, BAT = 3.3V 10x Mode, BAT = 3.3V Low Power Suspend Mode High Power Suspend Mode		 0.26 1.6	135 672 1251 0.32 2.04	 0.41 2.46	mA mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x, 5x, 10x Modes Suspend Modes			1.188 100		V mV
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.95	4.30 4.00	4.35	V V
V_{DUVLO}	V_{BUS} to BAT Differential Undervoltage Lockout	Rising Threshold Falling Threshold			200 50		mV mV
V_{OUT}	V_{OUT} Voltage	1x, 5x, 10x Modes, 0V < BAT ≤ 4.2V, I_{OUT} = 0mA, Battery Charger Off		3.5	BAT + 0.3	4.7	V
		USB Suspend Modes, I_{OUT} = 250µA		4.5	4.6	4.7	V
f_{OSC}	Switching Frequency			1.8	2.25	2.7	MHz
R_{PMOS}	PMOS On Resistance				0.18		Ω
R_{NMOS}	NMOS On Resistance				0.30		Ω
I_{PEAK}	Peak Inductor Current Clamp	1x, 5x Modes 10x Mode			2 3		A A
R_{SUSP}	Suspend LDO Output Resistance				15		Ω
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage	 0°C ≤ T_A ≤ 85°C		4.179 4.165	4.200 4.200	4.221 4.235	V V
I_{CHG}	Constant-Current Mode Charge Current	R_{PROG} = 1k R_{PROG} = 5k		980 196	1030 206	1080 220	mA mA
I_{BAT}	Battery Drain Current	V_{BUS} > V_{UVLO}, PowerPath Switching Regulator On, Battery Charger Off, I_{OUT} = 0µA			3.5	5	µA
		V_{BUS} = 0V, I_{OUT} = 0µA (Ideal Diode Mode)			23	35	µA
V_{PROG}	PROG Pin Servo Voltage				1.000		V
$V_{PROG,TRKL}$	PROG Pin Servo Voltage in Trickle Charge	BAT < V_{TRKL}			0.100		V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1031		mA/mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.7	2.85	3.0	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				135		mV
V_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–80	–100	–120	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts When V_{BAT} = V_{FLOAT}		3.2	4.0	4.8	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.4	0.5	0.6	Hour
$I_{C/X}$	Battery Charge Current at Programmed End of Charge Indication	$R_{C/X}$ = 1k $R_{C/X}$ = 5k		85	100 20	115	mA mA
$V_{C/X}$	C/X Threshold Voltage				100		mV
$h_{C/X}$	Battery Charge Current Ratio to C/X				1031		mA/mA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			65	100	mV
$I_{\overline{CHRG}}$	$\overline{CHRG}$ Pin Input Current	BAT = 4.5V, $V_{\overline{CHRG}}$ = 5V			0	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, R_{CLPROG} = 2.94k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)	I_{BAT} = 200mA			0.18		Ω
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		75.0	76.5 1.5	78.0	$\%V_{BUS}$ $\%V_{BUS}$
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		33.4	34.9 1.5	36.4	$\%V_{BUS}$ $\%V_{BUS}$
V_{DIS}	NTC Disable Threshold Voltage	Falling Threshold Hysteresis		0.7	1.7 50	2.7	$\%V_{BUS}$ mV
I_{NTC}	NTC Leakage Current	V_{NTC} = V_{BUS} = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage Detection	I_{OUT} = 10mA V_{BUS} = 0V, I_{OUT} = 10mA			15 2		mV mV
$R_{DROPOUT}$	Internal Diode On-Resistance, Dropout	I_{OUT} = 200mA			0.18		Ω
I_{MAX}	Diode Current Limit			2			A
Logic (D0, D1, D2)							
V_{IL}	Input Low Voltage					0.4	V
V_{IH}	Input High Voltage			1.2			V
I_{PD}	Static Pull-Down Current	V_{PIN} = 1V			2		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

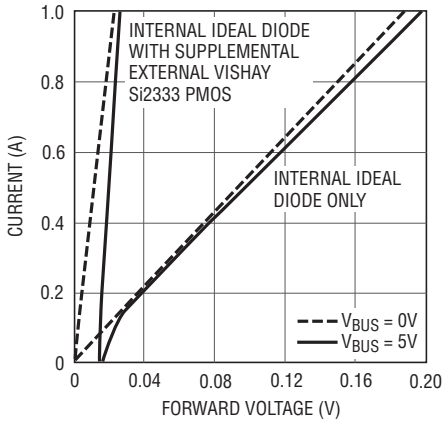
Note 2: The LTC4088E-1/LTC4088E-2 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC4088E-1/ LTC4088E-2 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

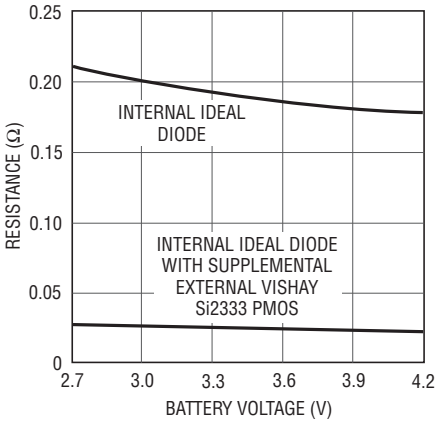
Note 4: Total input current is the sum of quiescent current, I_{BUSQ}, and measured current given by $V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

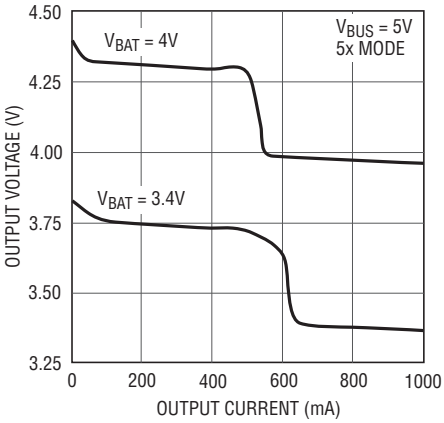
Ideal Diode V-I Characteristics



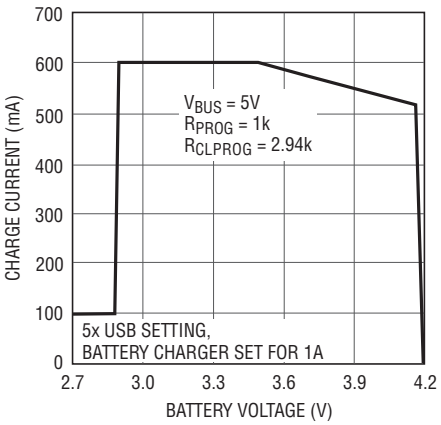
Ideal Diode Resistance vs Battery Voltage



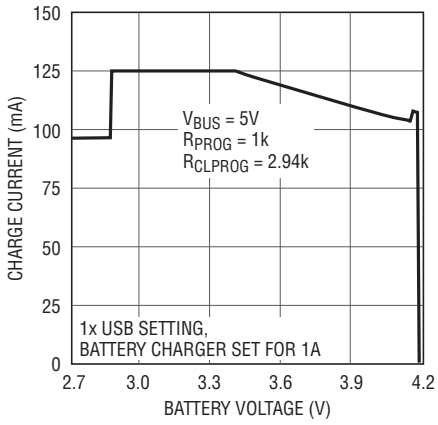
Output Voltage vs Output Current (Battery Charger Disabled)



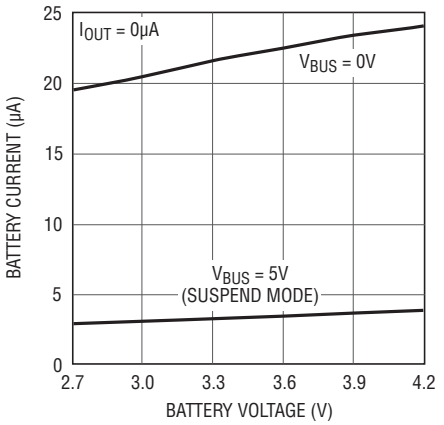
USB Limited Battery Charge Current vs Battery Voltage



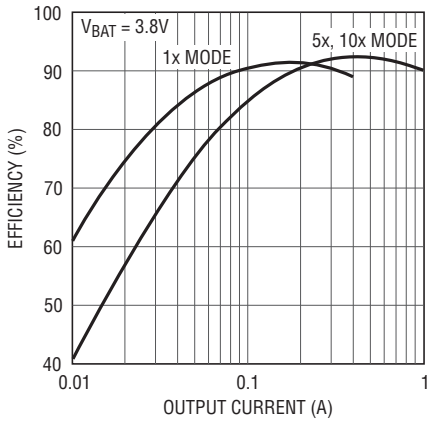
USB Limited Battery Charge Current vs Battery Voltage



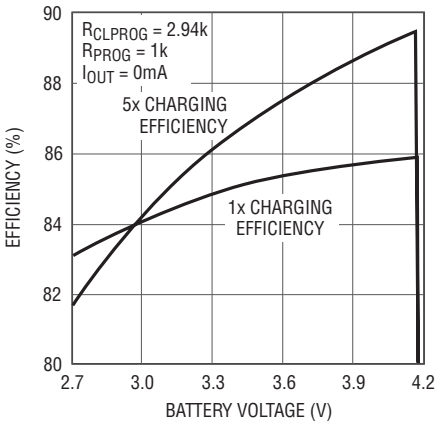
Battery Drain Current vs Battery Voltage



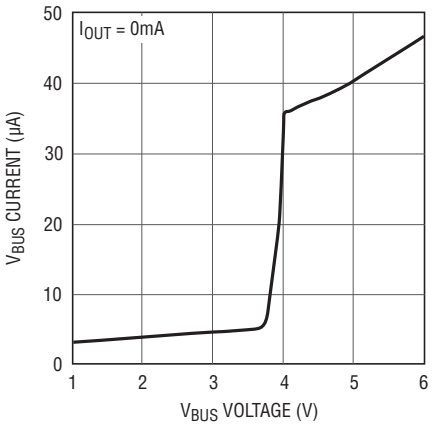
PowerPath Switching Regulator Efficiency vs Output Current



Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{BUS})

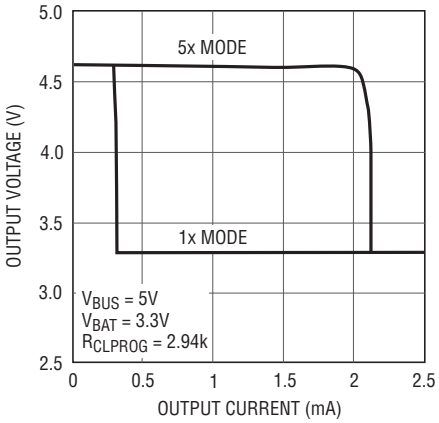


V_{BUS} Current vs V_{BUS} Voltage (Suspend)



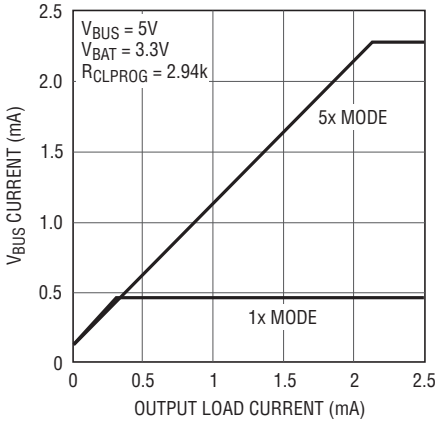
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage vs Output Current in Suspend



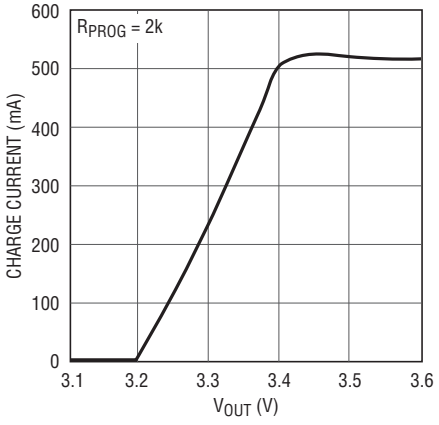
408812 G10

V_{BUS} Current vs Output Current in Suspend



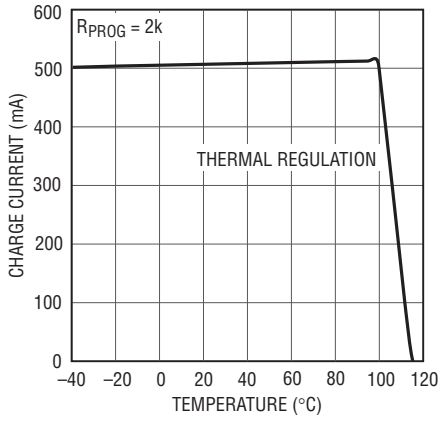
408812 G11

Battery Charge Current vs V_{OUT}



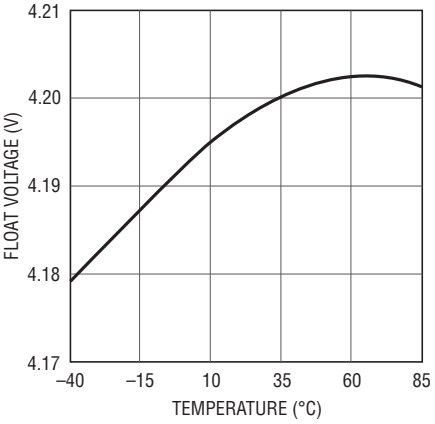
408812 G12

Battery Charge Current vs Temperature



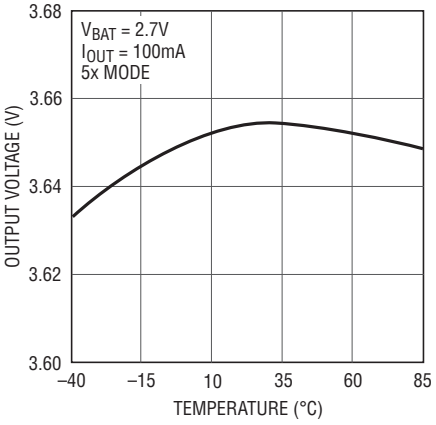
408812 G13

Battery Charger Float Voltage vs Temperature



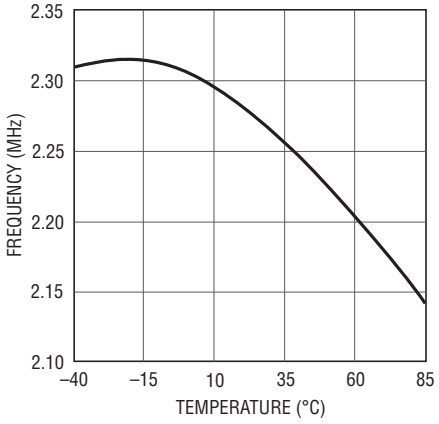
408812 G14

Low-Battery (Instant-On) Output Voltage vs Temperature



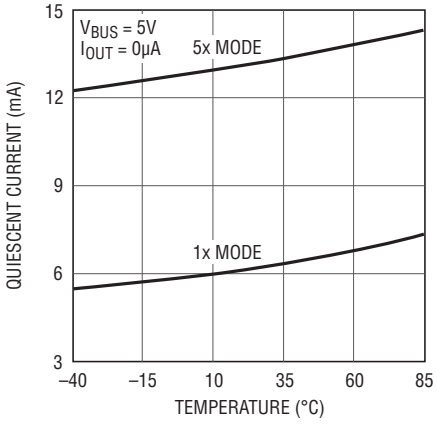
408812 G15

Oscillator Frequency vs Temperature



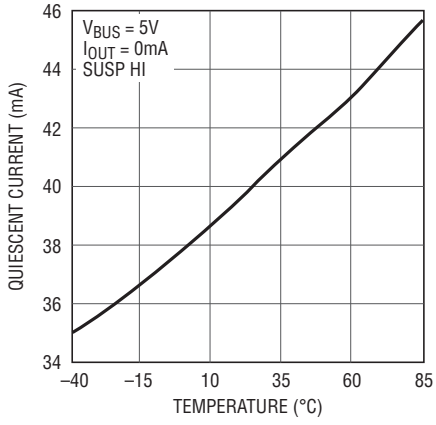
408812 G16

V_{BUS} Quiescent Current vs Temperature



408812 G17

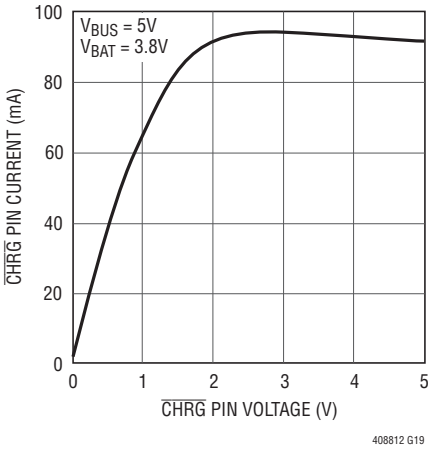
Quiescent Current in Suspend vs Temperature



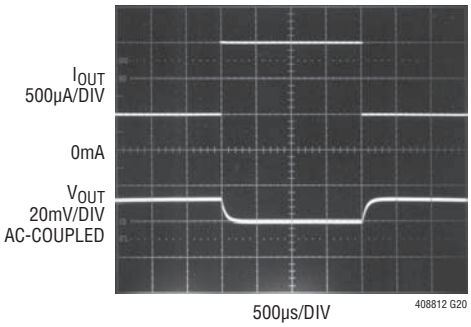
408812 G18

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

$\overline{CHRG}$ Pin Current vs Voltage (Pull-Down State)



Suspend LDO Transient Response (500µA to 1mA)



PIN FUNCTIONS

NTC (Pin 1): Input to the NTC Thermistor Monitoring Circuits. The NTC pin connects to a negative temperature coefficient thermistor which is typically co-packaged with the battery pack to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from V_{BUS} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

CLPROG (Pin 2): USB Current Limit Program and Monitor Pin. A 1% resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin. A precise fraction of the input current, h_{CLPROG}, is sent to the CLPROG pin when the high side switch is on. The switching regulator delivers power until the CLPROG pin reaches 1.188V. Therefore, the current drawn from V_{BUS} will be limited to an amount given by h_{CLPROG} and R_{CLPROG}. There are several ratios for h_{CLPROG} available, two of which correspond to the 500mA and 100mA USB specifications. A multilayer ceramic averaging capacitor is also required at CLPROG for filtering.

V_{OUTS} (Pin 3): Output Voltage Sense. The V_{OUTS} pin is used to sense the voltage at V_{OUT} when the PowerPath switching regulator is in operation. V_{OUTS} should always be connected directly to V_{OUT}.

D2 (Pin 4): Mode Select Input Pin. D2, in combination with the D0 pin and D1 pin, controls the current limit and battery charger functions of the LTC4088-1/LTC4088-2. The LTC4088-1 and LTC4088-2 differ only in the functionality of the D2 pin default (0, 0, 0) state (see Table 1). This pin is pulled low by a weak current sink.

C/X (Pin 5): End of Charge Indication Program Pin. This pin is used to program the current level at which a completed charge cycle is indicated by the $\overline{CHRG}$ pin.

PROG (Pin 6): Charge Current Program and Charge Current Monitor Pin. Connecting a 1% resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current by using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1031$$

PIN FUNCTIONS

$\overline{\text{CHRG}}$ (Pin 7): Open-Drain Charge Status Output. The $\overline{\text{CHRG}}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{\text{CHRG}}$: charging, not charging (or float charge current less than programmed end of charge indication current), unresponsive battery and battery temperature out of range. $\overline{\text{CHRG}}$ is modulated at 35kHz and switches between a low and a high duty cycle for easy recognition by either humans or microprocessors. $\overline{\text{CHRG}}$ requires a pull-up resistor and/or LED to provide indication.

GATE (Pin 8): Ideal Diode Amplifier Output. This pin controls the gate of an external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT.

BAT (Pin 9): Single Cell Li-Ion Battery Pin. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger.

V_{OUT} (Pin 10): Output voltage of the switching PowerPath controller and input voltage of the battery charger. The majority of the portable product should be powered from V_{OUT}. The LTC4088-1/LTC4088-2 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor.

V_{BUS} (Pin 11): Input voltage for the switching PowerPath controller. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

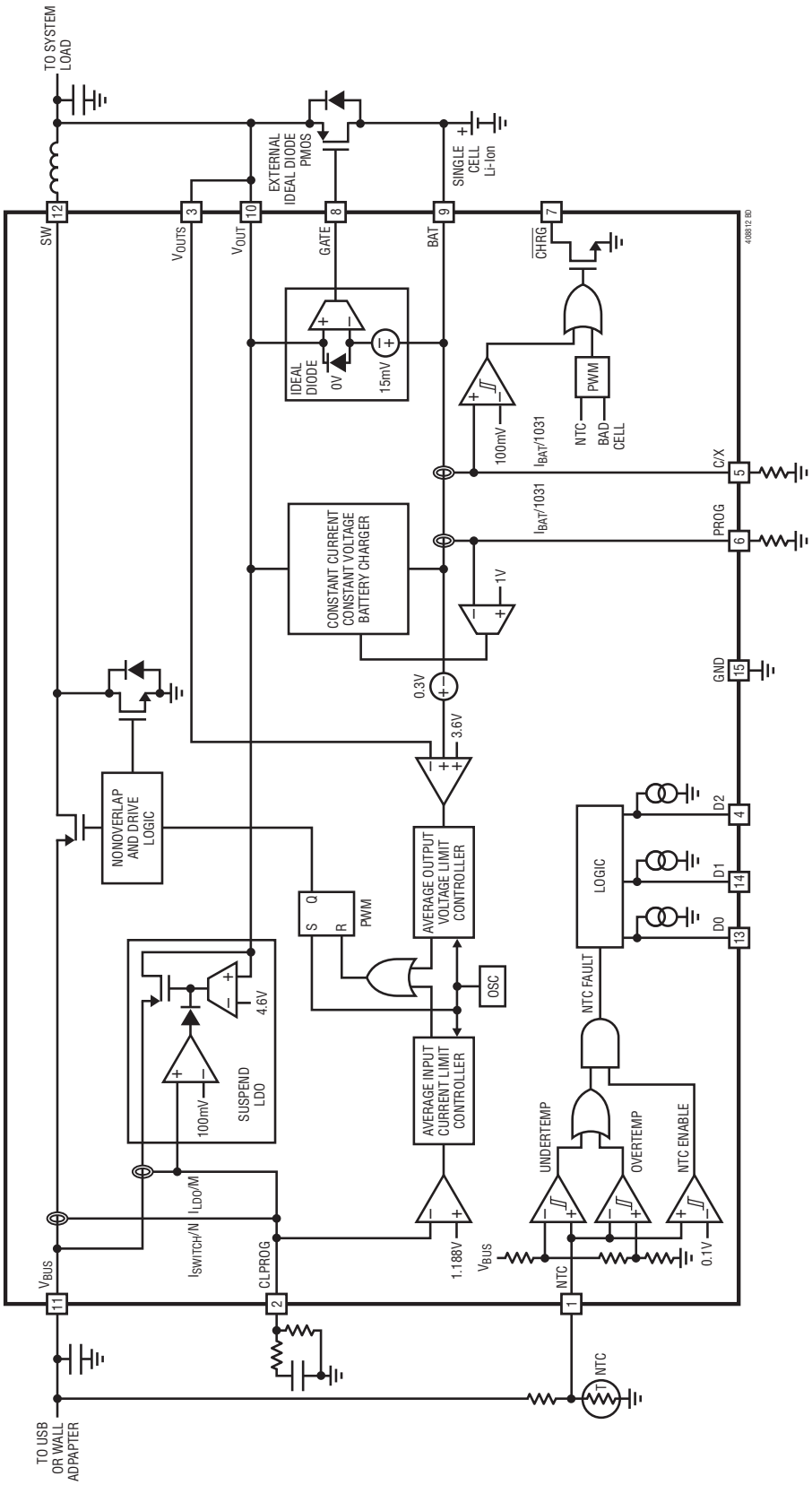
SW (Pin 12): The SW pin delivers power from V_{BUS} to V_{OUT} via the step-down switching regulator. An inductor should be connected from SW to V_{OUT}. See the Applications Information section for a discussion of inductance value and current rating.

D0 (Pin 13): Mode Select Input Pin. D0, in combination with the D1 pin and the D2 pin, controls the current limit and battery charger functions of the LTC4088-1/LTC4088-2 (see Table 1). This pin is pulled low by a weak current sink.

D1 (Pin 14): Mode Select Input Pin. D1, in combination with the D0 pin and the D2 pin, controls the current limit and battery charger functions of the LTC4088-1/LTC4088-2 (see Table 1). This pin is pulled low by a weak current sink.

Exposed Pad (Pin 15): GND. Must be soldered to the PCB to provide a low electrical and thermal impedance connection to ground.

BLOCK DIAGRAM



OPERATION

Introduction

The LTC4088-1/LTC4088-2 includes a PowerPath controller, battery charger, internal ideal diode, external ideal diode controller and a SUSPEND LDO. Designed specifically for USB applications, the PowerPath controller incorporates a precision average input current limited step-down switching regulator to make maximum use of the allowable USB power. Because power is conserved, the LTC4088-1/LTC4088-2 allows the load current on V_{OUT} to exceed the current drawn by the USB port without exceeding the USB load specifications.

The switching regulator and battery charger communicate to ensure that the average input current never exceeds the USB specifications.

The ideal diodes from BAT to V_{OUT} guarantee that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}.

Finally, to prevent battery drain when a device is connected to a suspended USB port, an LDO from V_{BUS} to V_{OUT} provides either low power or high power suspend current to the application.

Input Current Limited Step Down Switching Regulator

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant frequency step-down switching regulator. To meet the USB maximum load specification, the switching regulator contains a measurement and control system that ensures that the average input current remains below the level programmed at CLPROG. V_{OUT} drives the combination of the external load and the battery charger.

If the combined load does not cause the switching power supply to reach the programmed input current limit, V_{OUT} will track approximately 0.3V above the battery voltage. By keeping the voltage across the battery charger at this low level, power lost to the battery charger is minimized. Figure 1 shows the power path components.

If the combined external load plus battery charge current is large enough to cause the switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable USB current, the USB specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load current at V_{OUT} exceeds the programmed power from V_{BUS}, load current will be drawn from the battery via the ideal diodes even when the battery charger is enabled.

The current at CLPROG is a precise fraction of the V_{BUS} current. When a programming resistor and an averaging

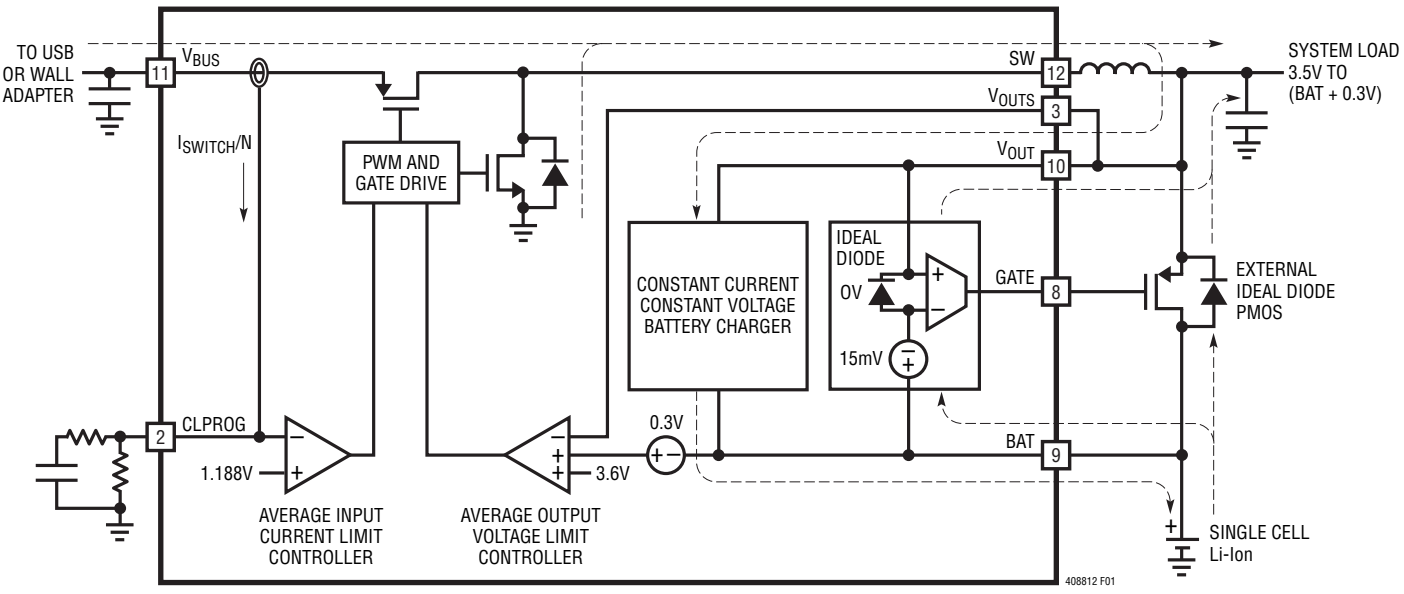


Figure 1

OPERATION

capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. As the input current approaches the programmed limit, CLPROG reaches 1.188V and power delivered by the switching regulator is held constant. Several ratios of current are available which can be set to correspond to USB low and high power modes with a single programming resistor.

The input current limit is programmed by various combinations of the D0, D1 and D2 pins as shown in Table 1. The switching input regulator can also be deactivated (USB Suspend).

The average input current will be limited by the CLPROG programming resistor according to the following expression:

$$I_{VBUS} = I_{BUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet (h_{CLPROG} + 1)$$

where I_{BUSQ} is the quiescent current of the LTC4088-1/LTC4088-2, V_{CLPROG} is the CLPROG servo voltage in current limit, R_{CLPROG} is the value of the programming resistor and h_{CLPROG} is the ratio of the measured current at V_{BUS} to the sample current delivered to CLPROG. Refer to the Electrical Characteristics table for values of h_{CLPROG}, V_{CLPROG} and I_{BUSQ}. Given worst-case circuit tolerances, the USB specification for the average input current in 1x or 5x mode will not be violated, provided that R_{CLPROG} is 2.94k or greater.

Table 1 shows the available settings for the D0, D1 and D2 pins.

Table 1. Controlled Input Current Limit

D0	D1	4088-1 D2	4088-2 D2	CHARGER STATUS	$I_{BUS(LIM)}$
0	0	0	1	Off	100mA (1x)
0	0	1	0	On	100mA (1x)
0	1	0	1	Off	500mA (5x)
0	1	1	0	On	500mA (5x)
1	0	0	1	Off	1A (10x)
1	0	1	0	On	1A (10x)
1	1	0	1	Off	2.5mA (Susp High)
1	1	1	0	Off	500µA (Susp Low)

Notice that when D0 is high and D1 is low, the switching regulator is set to a higher current limit for increased charging and power availability at V_{OUT}. These modes will typically be used when there is line power available from a wall adapter.

While not in current limit, the switching regulator's Bat-Track feature will set V_{OUT} to approximately 300mV above the voltage at BAT. However, if the voltage at BAT is below 3.3V, and the load requirement does not cause the switching regulator to exceed its current limit, V_{OUT} will regulate at a fixed 3.6V as shown in Figure 2. This will allow a portable product to run immediately when power is applied without waiting for the battery to charge.

If the load does exceed the current limit at V_{BUS}, V_{OUT} will range between the no-load voltage and slightly below the battery voltage, indicated by the shaded region of Figure 2.

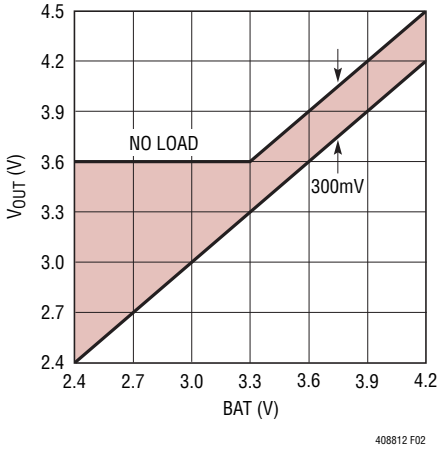


Figure 2. V_{OUT} vs BAT

For very low-battery voltages, the battery charger acts like a load and, due to limited input power, its current will tend to pull V_{OUT} below the 3.6V "Instant On" voltage. To prevent V_{OUT} from falling below this level, an undervoltage circuit automatically detects that V_{OUT} is falling and reduces the battery charge current as needed. This reduction ensures that load current and voltage are always prioritized and yet delivers as much battery charge current as possible. (See Over Programming the Battery Charger in the Applications Information section).

The voltage regulation loop compensation is controlled by the capacitance on V_{OUT}. An MLCC capacitor of 10µF is required for loop stability. Additional capacitance beyond this value will improve transient response.

OPERATION

Ideal Diode from BAT to V_{OUT}

The LTC4088-1/LTC4088-2 has an internal ideal diode as well as a controller for an external ideal diode. Both the internal and the external ideal diodes are always on and will respond quickly whenever V_{OUT} drops below BAT.

If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diodes. Furthermore, if power to V_{BUS} (USB or wall power) is removed, then all of the application power will be provided by the battery via the ideal diodes. The ideal diodes will be fast enough to keep V_{OUT} from drooping with only the storage capacitance required for the switching regulator. The internal ideal diode consists of a precision amplifier that activates a large on-chip MOSFET transistor whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFET will be in full conduction. An external P-channel MOSFET transistor should be added from BAT to V_{OUT}. The GATE pin of the LTC4088-1/LTC4088-2 drives the gate of the external P-channel MOSFET transistor for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the GATE pin can control an external P-channel MOSFET transistor having an on-resistance of 30mΩ or lower. When V_{BUS} is unavailable, the forward voltage of the ideal diode amplifier will be reduced from 15mV to nearly zero.

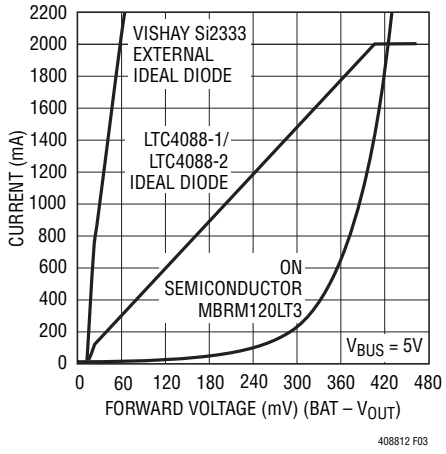


Figure 3. Ideal Diode V-I Characteristics

Suspend LDO

The LTC4088-1/LTC4088-2 provides a small amount of power to V_{OUT} in SUSPEND mode by including an LDO from V_{BUS} to V_{OUT}. This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the switching converter is disabled. To remain compliant with the USB specification, the input to the LDO is current limited so that it will not exceed the low power or high power suspend specification. If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the battery via the ideal diodes. The suspend LDO sends a scaled copy of the V_{BUS} current to the CLPROG pin, which will servo to approximately 100mV in this mode. Thus, the high power and low power suspend settings are related to the levels programmed by the same resistor for 1x and 5x modes.

V_{BUS} Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the switching regulator off until V_{BUS} rises above the rising UVLO threshold (4.3V). If V_{BUS} falls below the falling UVLO threshold (4V), system power at V_{OUT} will be drawn from the battery via the ideal diodes. The voltage at V_{BUS} must also be higher than the voltage at BAT by approximately 170mV for the switching regulator to operate.

Battery Charger

The LTC4088-1/LTC4088-2 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out of temperature charge pausing.

OPERATION

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates, via the $\overline{CHRG}$ pin, that the battery was unresponsive.

Once the battery voltage is above V_{TRKL}, the charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1031V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. Once the voltage on the battery reaches the pre-programmed float voltage of 4.200V, the charger will regulate the battery voltage there and the charge current will decrease naturally. Once the charger detects that the battery has reached 4.200V, the 4-hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

Once the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.1V). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, it will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.5ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS} is removed and then replaced) or if the charger is momentarily disabled using the D2 pin.

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1031th of the battery charge current is delivered to PROG, which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1031 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1031V}{I_{CHG}},\ I_{CHG} = \frac{1031V}{R_{PROG}}$$

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the *actual* charge current delivered to the battery. The charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1031$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than the programmed current, I_{CHG}, due to limited input power available and prioritization to the system load drawn from V_{OUT}.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ which include charging, not charging (or float charge current less than programmed end of charge indication current), unresponsive battery and battery temperature out of range.

The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

OPERATION

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either a DC signal of ON for charging, OFF for not charging or it is switched at high frequency (35kHz) to indicate the two possible faults. While switching at 35kHz, its duty cycle is modulated at a slow rate that can be recognized by a human.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, as determined by the criteria set by the C/X pin, the $\overline{CHRG}$ pin is released (Hi-Z). The $\overline{CHRG}$ pin does not respond to the C/X threshold if the LTC4088-1/LTC4088-2 is in V_{BUS} current limit. This prevents false end of charge indications due to insufficient power available to the battery charger. If a fault occurs while charging, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking". Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for machine recognition.

Table 2 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 2. $\overline{CHRG}$ Signal

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLES
Charging	0Hz	0Hz (Low Z)	100%
I_{BAT} < C/X	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	6.25% or 93.75%
Bad Battery	35kHz	6.1Hz at 50%	12.5% or 87.5%

Notice that an NTC fault is represented by a 35kHz pulse train whose duty cycle toggles between 6.25% and 93.75% at a 1.5Hz rate. A human will easily recognize the 1.5Hz rate as a "slow" blinking which indicates the out of range battery temperature while a microprocessor will be able to decode either the 6.25% or 93.75% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below 2.85V for 1/2 hour), the $\overline{CHRG}$ pin gives the battery fault indication. For this fault, a human would easily recognize the frantic 6.1Hz "fast" blink of the LED while a microprocessor would be able to decode either the 12.5% or 87.5% duty cycles as a bad cell fault.

Because the LTC4088-1/LTC4088-2 is a 3-terminal PowerPath product, system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the bad cell threshold voltage within the bad cell timeout period. In this case the battery charger will falsely indicate a bad cell. System software may then reduce the load and reset the battery charger to try again.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and take a new duty cycle reading.

C/X Determination

The current exiting the C/X pin represents 1/1031th of the battery charge current. With a resistor from C/X to ground that is X/10 times the resistor at the PROG pin, the $\overline{CHRG}$ pin releases when the battery current drops to C/X. For example, if C/10 detection is desired, $R_{C/X}$ should be made equal to R_{PROG}. For C/20, $R_{C/X}$ would be twice R_{PROG}. The current threshold at which $\overline{CHRG}$ will change state is given by:

$$I_{BAT} = \frac{V_{C/X}}{R_{C/X}} \bullet 1031$$

With this design, C/10 detection can be achieved with only one resistor rather than a resistor for both the C/X pin and the PROG pin. Since both of these pins have 1/1031 of the battery charge current in them, their voltages will be equal when they have the same resistor value. Therefore, rather than using two resistors, the C/X pin and the PROG pin can be connected together and the resistors can be paralleled to a single resistor of 1/2 of the program resistor.

OPERATION

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in the Block Diagram.

To use this feature, connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from V_{BUS} to NTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). A 100k thermistor is recommended since thermistor current is not measured by the LTC4088-1/LTC4088-2 and will have to be considered for USB compliance.

The LTC4088-1/LTC4088-2 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k (for a Vishay "Curve 1" thermistor, this corresponds to approximately 40°C). If the battery charger is in constant voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4088-1/LTC4088-2 is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For a Vishay "Curve 1" thermistor, this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC4088-1/LTC4088-2 from excessive temperature due to high power operation or high ambient thermal conditions, and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC4088-1/LTC4088-2 or external components. The benefit of the LTC4088-1/LTC4088-2 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

Shutdown Mode

The input switching regulator is enabled whenever V_{BUS} is above the UVLO voltage and the LTC4088-1/LTC4088-2 is not in one of the two USB suspend modes (500µA or 2.5mA).

The ideal diode is enabled at all times and cannot be disabled.

APPLICATIONS INFORMATION

CLPROG Resistor and Capacitor

As described in the Step-Down Input Regulator section, the resistor on the CLPROG pin determines the average input current limit in each of the six current limit modes. The input current will be comprised of two components, the current that is used to drive V_{OUT} and the quiescent current of the switching regulator. To ensure that the USB specification is strictly met, both components of input current should be considered. The Electrical Characteristics table gives the typical values for quiescent currents in all settings as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a precision resistor should be used.

An averaging capacitor is required in parallel with the resistor so that the switching regulator can determine the average input current. This capacitor also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.47µF or larger. Alternatively, faster transient response may be obtained with 0.1µF in series with 8.2Ω.

Choosing the Inductor

Because the average input current circuit does not measure reverse current (i.e., current from V_{OUT} to V_{BUS}), current reversal in the inductor at light loads will contribute an error to the V_{BUS} current measurement. The error is conservative in that if the current reverses, the voltage at CLPROG will be higher than what would represent the actual average input current drawn. The current available for charging and the system load is thus reduced. The USB specification will not be violated.

This reduction in available V_{BUS} current will happen when the peak-peak inductor ripple is greater than twice the average current limit setting. For example, if the average current limit is set to 100mA, the peak-peak ripple should not exceed 200mA. If the input current is less than 100mA, the measurement accuracy may be reduced, but it does not affect the average current loop since it will not be in regulation.

The LTC4088-1/LTC4088-2 includes a current-reversal comparator which monitors inductor current and disables the synchronous rectifier as current approaches zero. This comparator will minimize the effect of current reversal on the average input current measurement. For some low inductance values, however, the inductor current may reverse slightly. This value depends on the speed of the comparator in relation to the slope of the current waveform, given by V_L/L, where V_L is the voltage across the inductor (approximately $–V_{OUT}$) and L is the inductance value.

An inductance value of 3.3µH is a good starting value. The ripple will be small enough for the regulator to remain in continuous conduction at 100mA average V_{BUS} current. At lighter loads the current-reversal comparator will disable the synchronous rectifier at a current slightly above 0mA. As the inductance is reduced from this value, the part will enter discontinuous conduction mode at progressively higher loads. Ripple at V_{OUT} will increase, directly proportionally to the magnitude of inductor ripple. Transient response, however, will be improved. The current mode controller controls inductor current to exactly the amount required by the load to keep V_{OUT} in regulation. A transient load step requires the inductor current to change to a new level. Since inductor current cannot change instantaneously, the capacitance on V_{OUT} delivers or absorbs the difference in current until the inductor current can change to meet the new load demand. A smaller inductor changes its current more quickly for a given voltage drive than a larger inductor, resulting in faster transient response. A larger inductor will reduce output ripple and current ripple, but at the expense of reduced transient performance (or more C_{VOUT} required) and a physically larger inductor package size.

The input regulator has an instantaneous peak current clamp to prevent the inductor from saturating during transient load or start-up conditions. The clamp is designed so that it does not interfere with normal operation at high loads with reasonable inductor ripple. It will prevent inductor current runaway in case of a shorted output.

The DC winding resistance and AC core losses of the inductor will affect efficiency, and therefore available output power. These effects are difficult to characterize and vary by application. Some inductors which may be suitable for this application are listed in Table 3.

APPLICATIONS INFORMATION

Table 3. Recommended Inductors for the LTC4088-1/LTC4088-2

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC DB318C	3.3 3.3	2.26 1.55	0.034 0.070	5 × 5 × 3 3.8 × 3.8 × 1.8	Toko www.toko.com
WE-TPC Type M1	3.3	1.95	0.065	4.8 × 4.8 × 1.8	Würth Elektronik www.we-online.com
CDRH6D12 CDRH6D38	3.3 3.3	2.2 3.5	0.0625 0.020	6.7 × 6.7 × 1.5 7 × 7 × 4	Sumida www.sumida.com

V_{BUS} and V_{OUT} Bypass Capacitors

The style and value of capacitors used with the LTC4088-1/LTC4088-2 determine several important parameters such as regulator control-loop stability and input voltage ripple. Because the LTC4088-1/LTC4088-2 uses a step-down switching power supply from V_{BUS} to V_{OUT}, its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass V_{BUS}. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on V_{BUS} directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple. The USB specification allows a maximum of 10µF to be connected directly across the USB power bus. If additional capacitance is required for noise performance, a soft-connect circuit may be required to limit inrush current and avoid excessive transient voltage drops on the bus (see Figure 5).

To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass V_{OUT}. The output capacitor is used in the compensation of the switching regulator. At least 10µF with low ESR are required on V_{OUT}. Additional capacitance will improve load transient performance and stability.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

There are several types of ceramic capacitors available each having considerably different characteristics. For example, X7R ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors have the highest packing density, but must be used with caution, because of their extreme nonlinear characteristic of capacitance versus voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal and DC bias as is expected in-circuit. Many vendors specify the capacitance verse voltage with a $1V_{RMS}$ AC test signal and, as a result, over state the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

Overprogramming the Battery Charger

The USB high power specification allows for up to 2.5W to be drawn from the USB port. The switching regulator transforms the voltage at V_{BUS} to just above the voltage at BAT with high efficiency, while limiting power to less than the amount programmed at CLPROG. The charger should be programmed (with the PROG pin) to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, it will reduce charge current until the system load on V_{OUT} is satisfied and the V_{BUS} current limit is satisfied. Programming the

APPLICATIONS INFORMATION

charger for more current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal power dissipation within the charger.

Alternate NTC Thermistors and Biasing

The LTC4088-1/LTC4088-2 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay "Curve 1" thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N01N1003, used in the following examples, has a nominal value of 100k and follows the Vishay "Curve 1" resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the Thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT} = Ratio of $R_{NTC|COLD}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 4a)

R1 = Optional temperature range adjustment resistor (see Figure 4b)

The trip points for the LTC4088-1/LTC4088-2's temperature qualification are internally programmed at 0.349 • V_{BUS} for the hot threshold and 0.765 • V_{BUS} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM} + R_{NTC|HOT}} \bullet V_{BUS} = 0.349 \bullet V_{BUS}$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM} + R_{NTC|COLD}} \bullet V_{BUS} = 0.765 \bullet V_{BUS}$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.536 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.25 \bullet R_{NOM}$$

By setting R_{NOM} equal to R25, the above equations result in r_{HOT} = 0.536 and r_{COLD} = 3.25. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the non-linear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the *desired* hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can

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be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in "temperature gain" of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 4b. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose:

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k:

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 4b and results in an upper trip point of 45°C and a lower trip point of 0°C.

USB Inrush Limiting

The USB specification allows at most 10µF of downstream capacitance to be hot-plugged into a USB hub. In most LTC4088-1/LTC4088-2 applications, 10µF should be enough to provide adequate filtering on V_{BUS}. If more capacitance is required, the following circuit can be used to soft-connect additional capacitance.

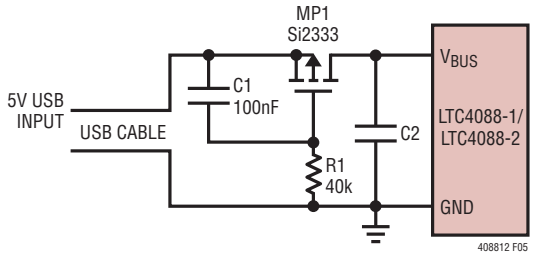
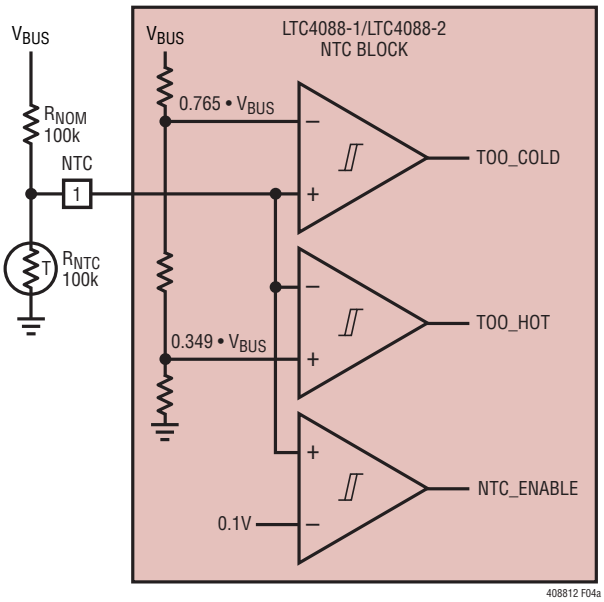
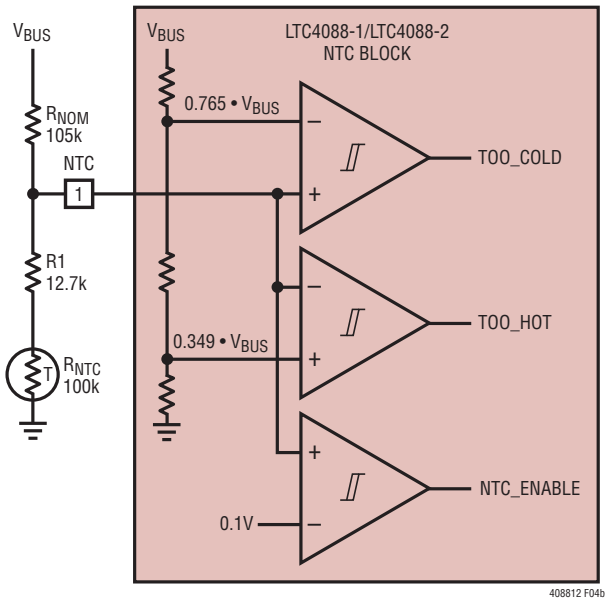


Figure 5. USB Soft-Connect Circuit



(a)



(b)

Figure 4. NTC Circuits

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In this circuit, capacitor C1 holds MP1 off when the cable is first connected. Eventually the bottom plate of C1 discharges to GND, applying increasing gate support to MP1. The long time constant of R1 and C1 prevent the current from building up in the cable too fast, thus dampening out any resonant overshoot.

Voltage overshoot on V_{BUS} may sometimes be observed when connecting the LTC4088-1/LTC4088-2 to a lab power supply. This overshoot is caused by long leads from the power supply to V_{BUS}. Twisting the wires together from the supply to V_{BUS} can greatly reduce the parasitic inductance of these long leads, and keep the voltage at V_{BUS} to safe levels. USB cables are generally manufactured with the power leads in close proximity, and thus fairly low parasitic inductance.

Board Layout Considerations

The Exposed Pad on the backside of the LTC4088-1/LTC4088-2 package must be securely soldered to the PC board ground. This is the only ground pin in the package, and it serves as the return path for both the control circuitry and the synchronous rectifier.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitor, inductor, and output capacitor be as close to the LTC4088-1/LTC4088-2 as possible and that there be an *unbroken* ground plane under the LTC4088-1/LTC4088-2 and all of its external high frequency components. High frequency currents, such as the input current on the LTC4088-1/LTC4088-2, tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur (see Figure 6). There should be a group of vias directly under the grounded backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (layer 2).

The GATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an additional offset to the ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{OUT} connected metal, which should generally be less than one volt higher than GATE.

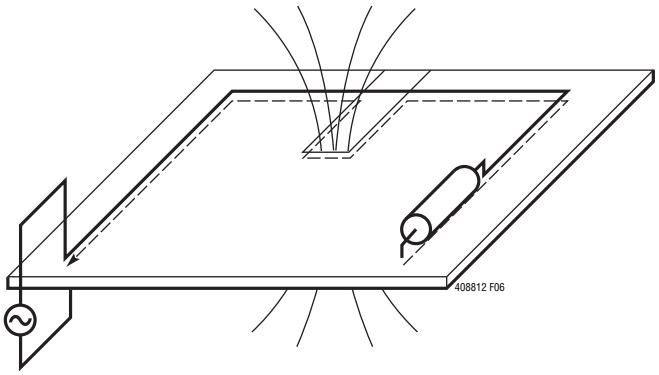

Figure 6. Ground Currents Follow Their Incident Path at High Speed. Slices in the Ground Plane Cause High Voltage and Increased Emissions

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Battery Charger Stability Considerations

The LTC4088-1/LTC4088-2's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND.

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

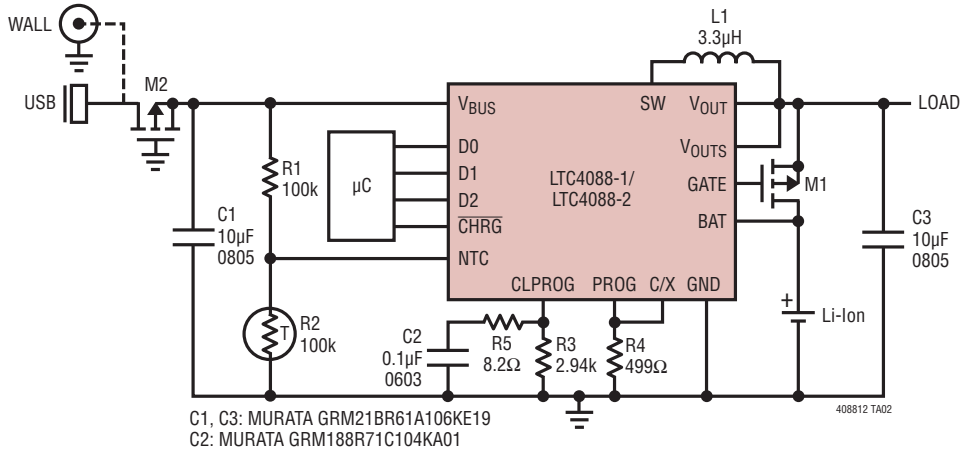
Furthermore, a 4.7µF capacitor in series with a 0.2Ω to 1Ω resistor from BAT to GND is required to prevent oscillation when the battery is disconnected.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

TYPICAL APPLICATION

High Efficiency Battery Charger/USB Power Manager with NTC Qualified Charging and Reverse Input Protection

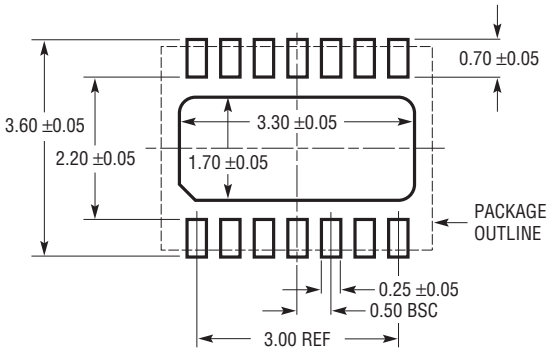


C1, C3: MURATA GRM21BR61A106KE19
C2: MURATA GRM188R71C104KA01
L1: COILCRAFT LPS4018-332MLC
M1, M2: SILICONIX Si2333
R2: VISHAY-DALE NTHS0603N01N1003

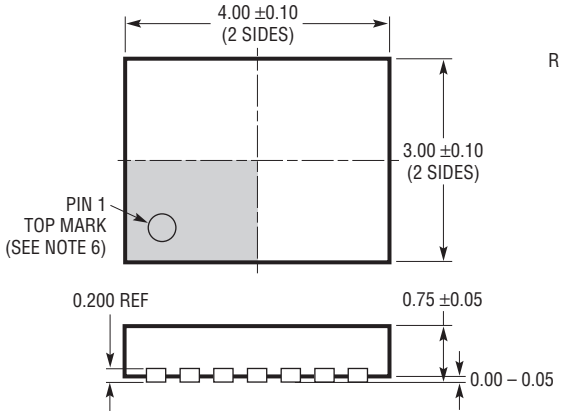
PACKAGE DESCRIPTION

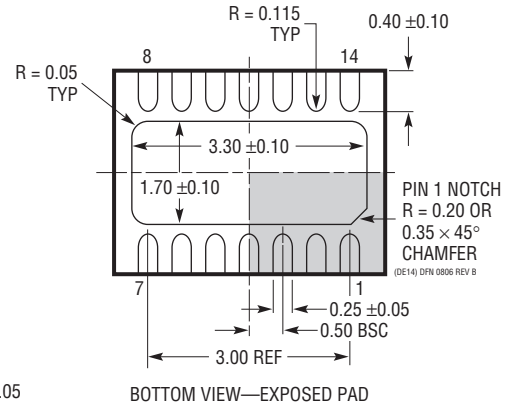
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	05/12	Clarified USB Limited Battery Charge Current curves.	5
		Clarified thermistor part number.	18, 21