Hot Swap Controller with Power-Up Timeout

FEATURES

- **Allows Safe Board Insertion and Removal from a Live Backplane**
- **Controls Supply Voltages from 2.5V to 16.5V**
- **Adjustable Soft-Start with Inrush Current Limiting**
- **Fast Turn-Off Time**
- **No External Gate Capacitor is Required**
- **Power Good Input with Adjustable Timer and Glitch Filter**
- Power-Up Timeout Circuit Interfaces with External Supply Monitors
- Dual Level Overcurrent Fault Protection
- Automatic Retry or Latched Mode Operation
- High Side Drive for an External N-Channel FET
- MS10 Package

APPLICATIONS

- Electronic Circuit Breaker
- Hot Board Insertion and Removal
- Self-Isolating Hot Swap Boards

DESCRIPTION

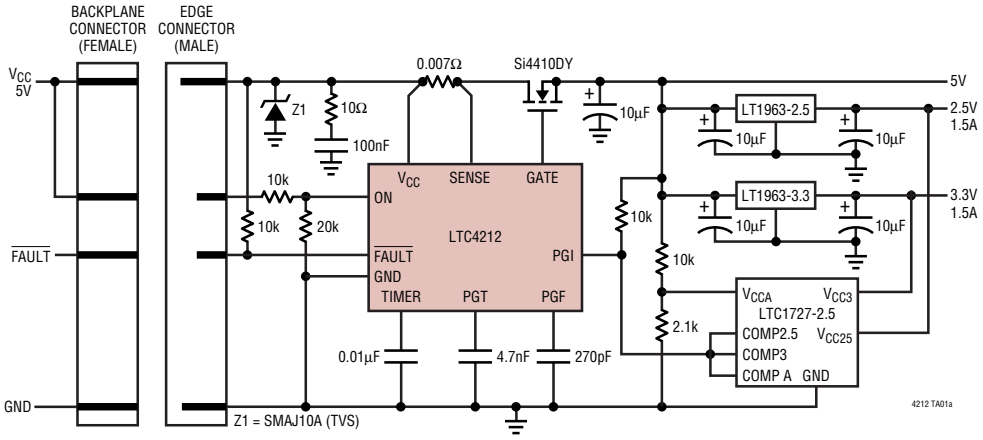
The LTC®4212 is a Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. An internal high side switch driver controls the gate of an external N-channel MOSFET for supply voltages ranging from 2.5V to 16.5V. The LTC4212 provides soft-start and inrush current limiting during the start-up period. It features a power-up timeout circuit that disconnects the system supply when the onboard supplies do not enter into regulation within an adjustable timeout period. The controller interfaces with external supply monitor ICs or directly with the PGOOD pin of a DC/DC converter. After normal power-up, a programmable power good glitch filter can be enabled to filter out short term dips in the supplies.

Two current limit comparators provide dual level overcurrent circuit breaker protection. The slow comparator trips at V_{CC} – 50mV and activates in 18µs. The fast comparator trips at V_{CC} – 150mV and typically responds in 500ns.

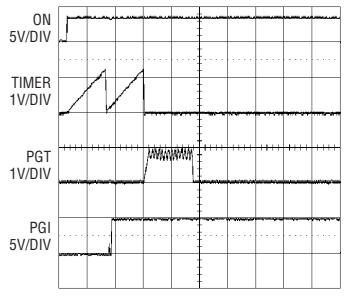
The LTC4212 can be configured for both latchoff and autoretry applications and is available in a 10-pin MSOP package.

TYPICAL APPLICATION

Hot Swap Controller with Power Good Function



Power-Up Waveforms

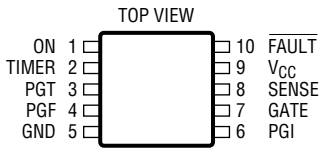


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 17V
Input Voltages
  ON, PGI ..... –0.3V to 17V
  SENSE ..... –0.3V to (V_{CC} + 0.3V)
  TIMER, PGT, PGF .....–0.3V to 2V
Output Voltages
  GATE ..... Internally Limited (Note 3)
  $\overline{FAULT}$ ..... –0.3V to 17V
Operating Temperature Range
  LTC4212C ..... 0°C to 70°C
  LTC4212I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 200°C/W

ORDER PART NUMBER
LTC4212CMS LTC4212IMS
MS PART MARKING
LTC5 LTC6

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Supply Voltage Range		●	2.5		16.5	V
I_{CC}	V_{CC} Supply Current	ON = High, TIMER = Low	●		1	1.5	mA
V_{LKO}	Internal V_{CC} Undervoltage Lockout	V_{CC} Low-to-High Transition	●	2.13	2.34	2.47	V
V_{LKOHST}	V_{CC} Undervoltage Lockout Hysteresis				110		mV
I_{INON}	ON Input Current	V_{ON} = V_{CC} or GND			±1	±10	µA
I_{LEAK}	$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 15V, Pull-Down Device Off	●		±0.1	±2.5	µA
I_{INPGI}	PGI Pin Input Current	V_{PGI} = V_{CC} or GND			±1	±10	µA
$I_{INSENSE}$	SENSE Input Current	V_{SENSE} = V_{CC} or GND			±1	±10	µA
$V_{CB(FAST)}$	SENSE Trip Voltage (V_{CC} – V_{SENSE})	Fast Comparator Trips	●	130	150	170	mV
$V_{CB(SLOW)}$	SENSE Trip Voltage (V_{CC} – V_{SENSE})	Slow Comparator Trips	●	40	50	60	mV
I_{GATEUP}	GATE Pull-Up Current	Charge Pump On, V_{GATE} ≤ 0.2V	●	–12.5	–10	–7.5	µA
$I_{GATEDOWN}$	Normal GATE Pull-Down Current	ON Low	●	130	200	270	µA
	Fast GATE Pull-Down Current	$\overline{FAULT}$ Latched and Circuit Breaker Tripped or in UVLO, V_{GATE} = 15V			50		mA
ΔV_{GATE}	External N-Channel Gate Drive	V_{GATE} – V_{CC} (For V_{CC} = 2.5V)	●	4.0		8	V
		V_{GATE} – V_{CC} (For V_{CC} = 2.7V)	●	4.5		8	V
		V_{GATE} – V_{CC} (For V_{CC} = 3.3V)	●	5.0		10	V
		V_{GATE} – V_{CC} (For V_{CC} = 5V)	●	10		16	V
		V_{GATE} – V_{CC} (For V_{CC} = 12V)	●	10		18	V
		V_{GATE} – V_{CC} (For V_{CC} = 15V), (Note 3)	●	8		15	V
V_{GATEOV}	GATE Overvoltage Lockout Threshold		●	0.08	0.2	0.3	V
V_{ONHI}	ON Threshold High		●	1.23	1.316	1.39	V
V_{ONLO}	ON Threshold Low		●	0.4	0.455	0.5	V
V_{PGI}	Power Good Input Threshold		●	1.20	1.236	1.26	V
V_{PGIHST}	Power Good Input Hysterisis				28		mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PGFHI}	Power Good Glitch Filter High Threshold		●	1.20	1.236	1.26	V
V_{PGFHST}	Power Good Glitch Filter Hysterisis	(Note 4)			40		mV
V_{PGTHI}	Power Good Timer High Threshold		●	0.928	0.952	0.976	V
V_{PGTLO}	Power Good Timer Low Threshold		●	0.640	0.657	0.680	V
$V_{PGT\Delta V}$	Power Good Timer Delta Threshold		●	0.283	0.295	0.304	V
I_{PGT}	Power Good Timer Pin Current	Power Good Timer On, C_{PGT} Charging, PGT = 0.65V Power Good Timer On, C_{PGT} Discharging, PGT = 0.95V Power Good Timer Off, PGT = 1.5V	● ● 	−5.61 4.63 	−5.1 5.2 5	−4.59 5.77 	µA µA mA
I_{PGF}	Power Good Glitch Filter Pin Current	Power Good Glitch Filter On, C_{PGF} Charging Power Good Timer Off, PGF = 1.5V	● 	−5.61 	-5.1 5	−4.49 	µA mA
I_{TMR}	TIMER Current	Timer On, V_{TIMER} = 1V Timer Off, TIMER = 1.5V	● 	−2.5 	−2 5	−1.5 	µA mA
V_{TMR}	TIMER Threshold	TIMER Low to High TIMER High to Low	● ●	1.20 0.15	1.236 0.200	1.26 0.40	V V
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Threshold	Latched Off Threshold, $\overline{FAULT}$ High to Low	●	1.20	1.236	1.26	V
$V_{\overline{FAULT}HST}$	$\overline{FAULT}$ Threshold Hysteresis				50		mV
$V_{OL\overline{FAULT}}$	Output Low Voltage	$I_{\overline{FAULT}}$ = 1.6mA	●		0.14	0.4	V
t_{TO}	Power Good Time-Out	C_{PGT} =10nF, PGT = 0.1V to $\overline{FAULT}$ Low	●	16.3	18.16	20	ms
$t_{\overline{FAULT}LO}$	Power Good Input Low at Time-Out to GATE Discharging	End of 14th PGT Cycle			1		µs
$t_{\overline{FAULT}VG}$	Valid Power Good Glitch to GATE Discharging	PGF > 1.26V			1.5		µs
$t_{\overline{FAULT}FC}$	FAST COMP Trip to GATE Discharging	V_{CB} = 0mV to 200mV Step	●		500	700	ns
$t_{\overline{FAULT}SC}$	SLOW COMP Trip to GATE Discharging	V_{CB} = 0mV to 100mV Step	●	10	18	30	µs
$t_{EXT\overline{FAULT}}$	$\overline{FAULT}$ Low to GATE Discharging	V_{FAULT} = 5V to 0V	●	1	3	5	µs
t_{RESET}	Circuit Breaker Reset Delay Time	ON Low to $\overline{FAULT}$ High	●		120	250	µs
t_{OFF}	Turn-Off Time	ON Low to GATE Off			10		µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All current into device pins are positive; all current out of device pins are negative; all voltages are referenced to ground unless otherwise specified.

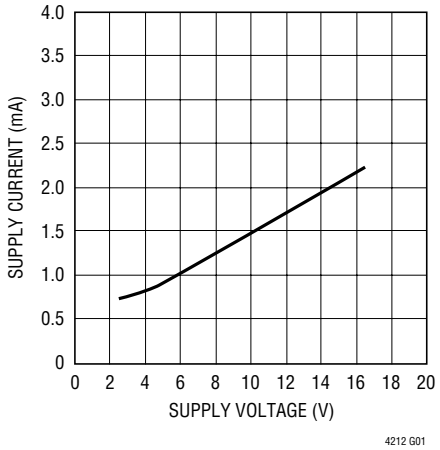
Note 3: An internal clamp limits the GATE pin to a minimum of 10V above V_{CC}. Driving this pin to voltages beyond the clamp may damage the part. If a lower GATE pin voltage is desired, use an external zener diode. The GATE capacitance must be <0.15µF at maximum V_{CC}.

Note 4: Guaranteed by design and not tested in production.

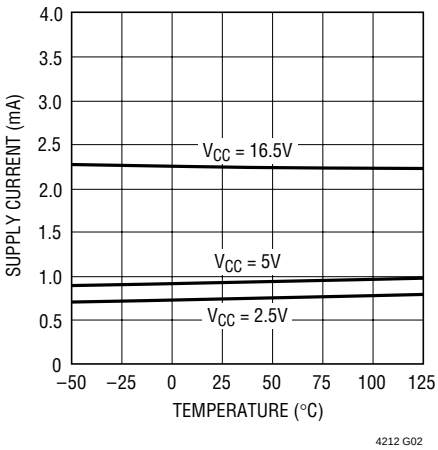
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted.

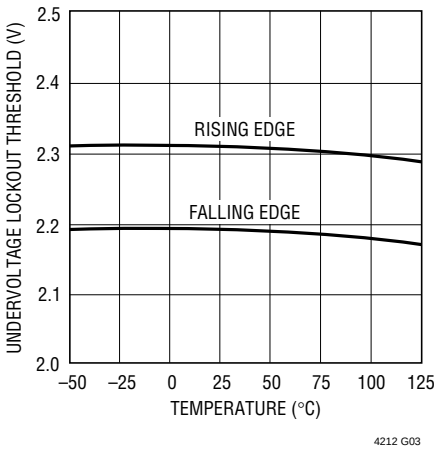
Supply Current vs Supply Voltage



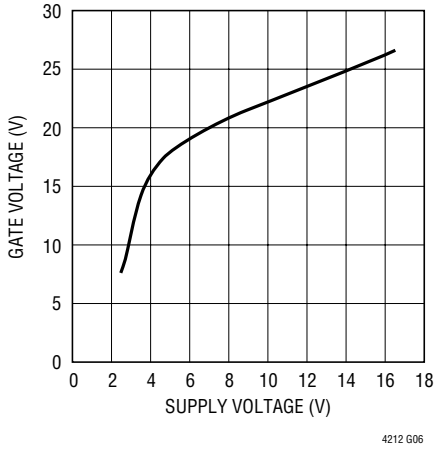
Supply Current vs Temperature



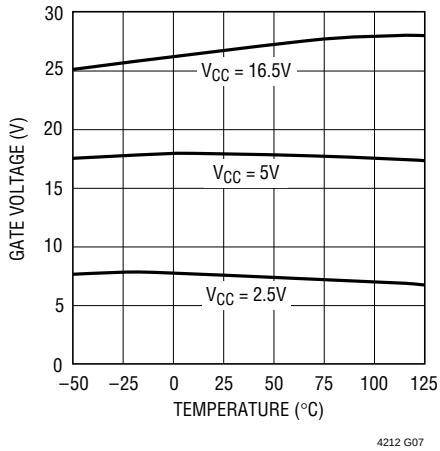
Undervoltage Lockout Threshold vs Temperature



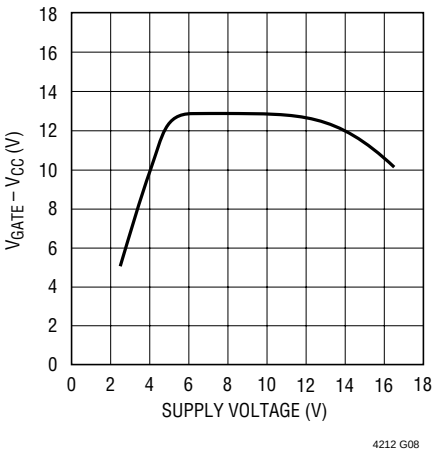
GATE Voltage vs Supply Voltage



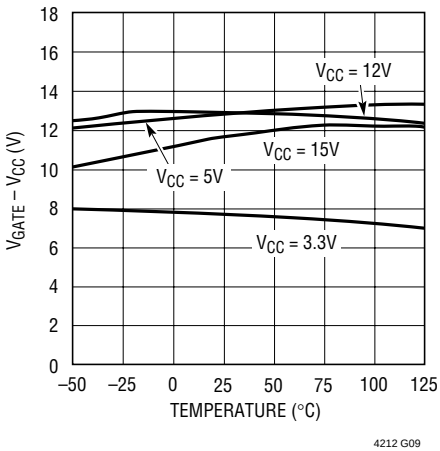
GATE Voltage vs Temperature



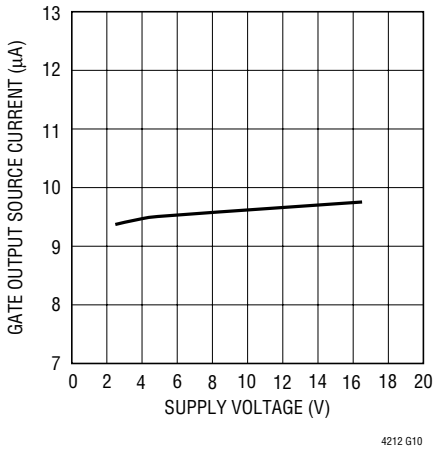
$V_{GATE} - V_{CC}$ vs Supply Voltage



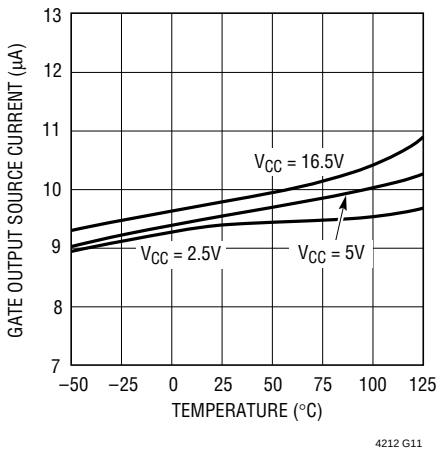
$V_{GATE} - V_{CC}$ vs Temperature



GATE Output Source Current vs Supply Voltage



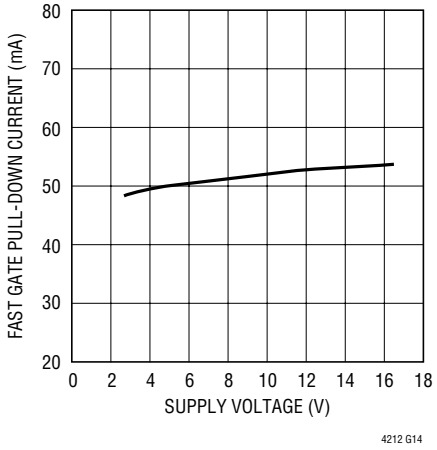
GATE Output Source Current vs Temperature



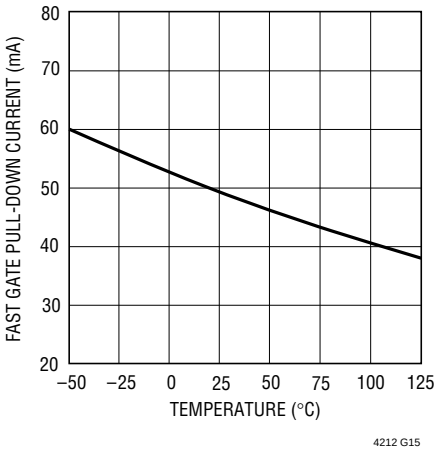
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted.

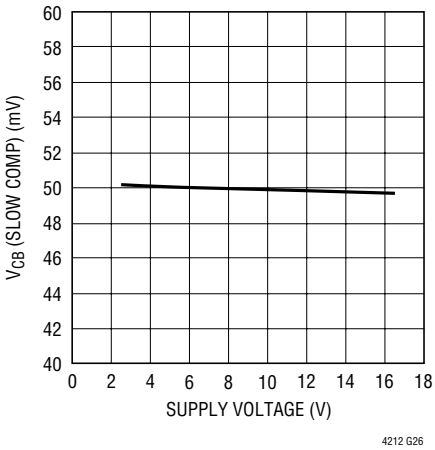
Fast GATE Pull-Down Current vs Supply Voltage



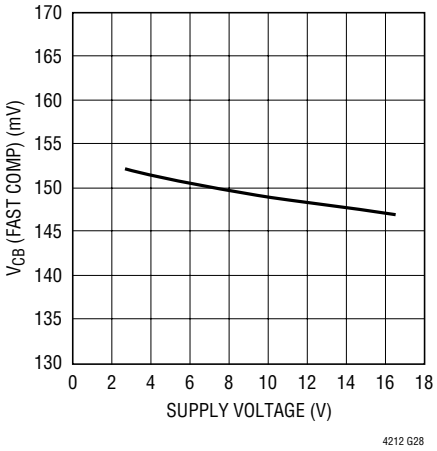
Fast GATE Pull-Down Current vs Temperature



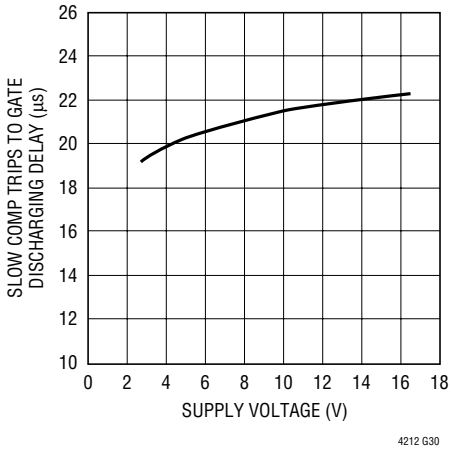
V_{CB} (SLOW COMP) vs Supply Voltage



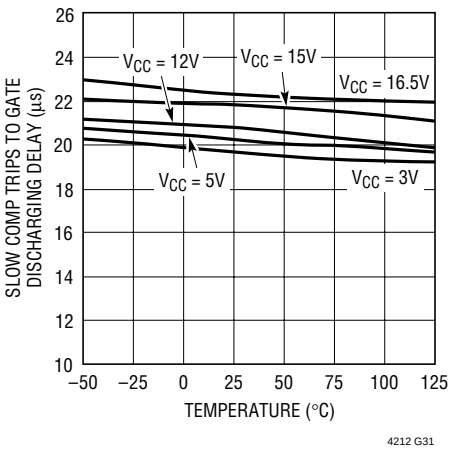
V_{CB} (FAST COMP) vs Supply Voltage



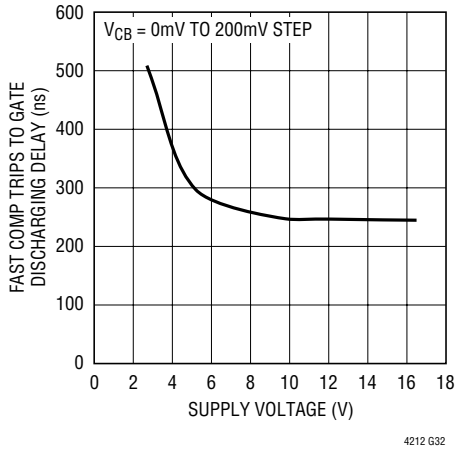
SLOW COMP Trips to GATE Discharging Delay vs Supply Voltage



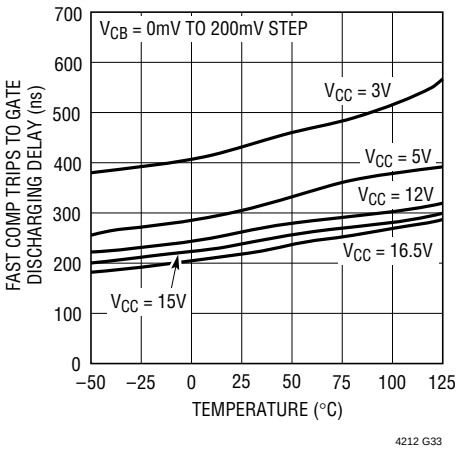
SLOW COMP Trips to GATE Discharging Delay vs Temperature



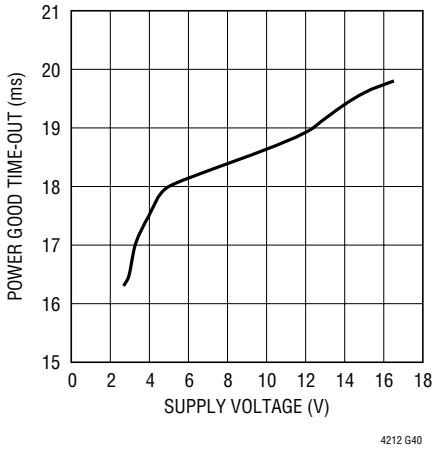
FAST COMP Trips to GATE Discharging Delay vs Supply Voltage



FAST COMP Trips to GATE Discharging Delay vs Temperature



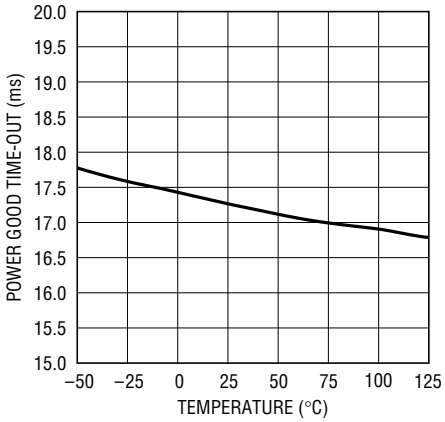
Power Good Timeout vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

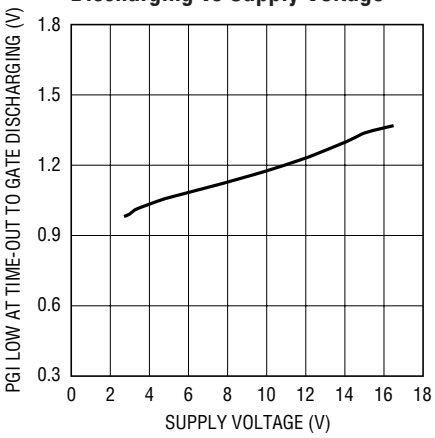
Specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted.

Power Good Timeout vs Temperature



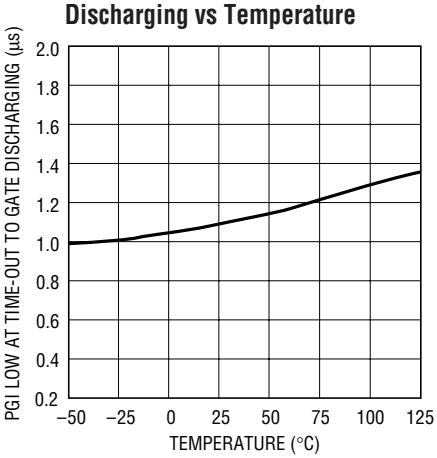
4212 G41

PGI Low at Timeout to GATE Discharging vs Supply Voltage



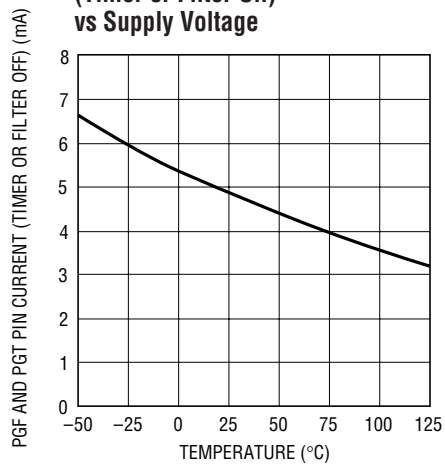
4212 G44

PGI Low at Timeout to GATE Discharging vs Temperature



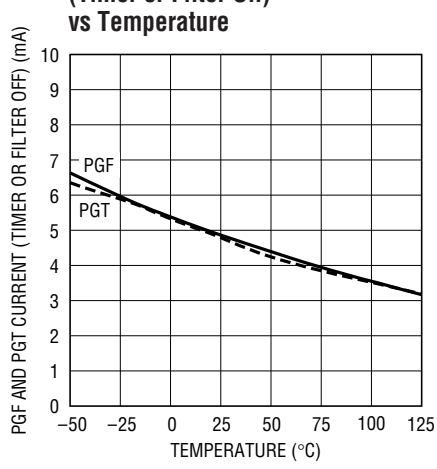
4212 G45

PGF and PGT Pin Current (Timer or Filter Off) vs Supply Voltage



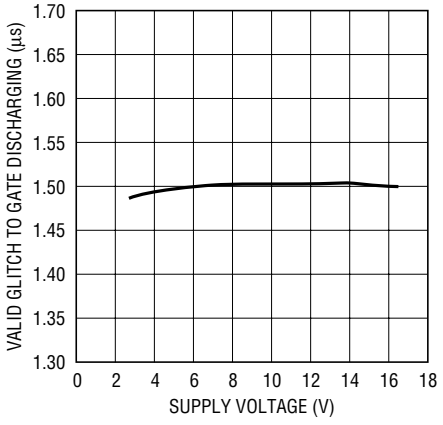
4212 G50

PGF and PGT Pin Current (Timer or Filter Off) vs Temperature



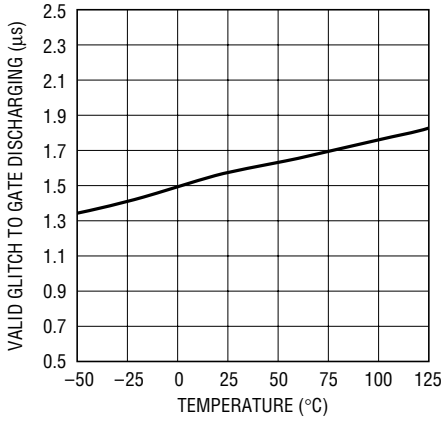
4212 G51

Valid Glitch to GATE Discharging vs Supply Voltage



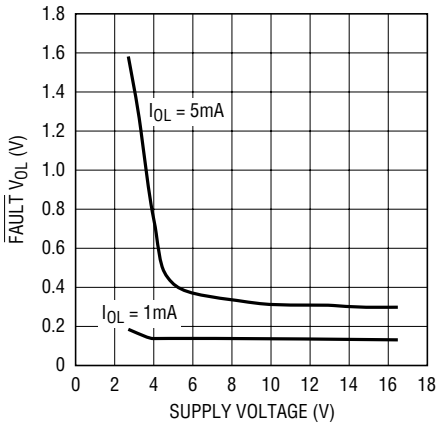
4212 G52

Valid Glitch to GATE Discharging vs Temperature



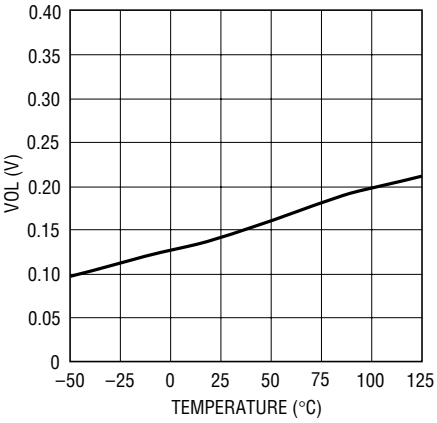
4212 G53

$\overline{FAULT}$ V_{OL} vs Supply Voltage



4212 G54

$\overline{FAULT}$ V_{OL} vs Temperature

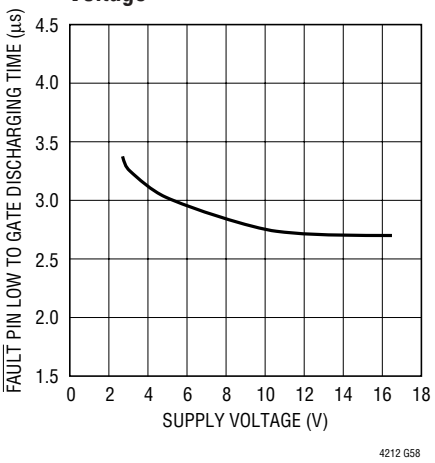


4212 G55

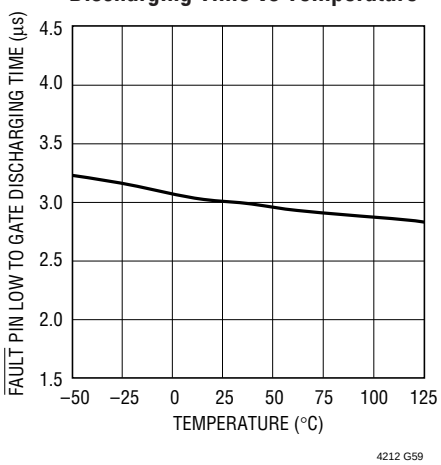
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are T_A = 25°C. V_{CC} = 5V, unless otherwise noted.

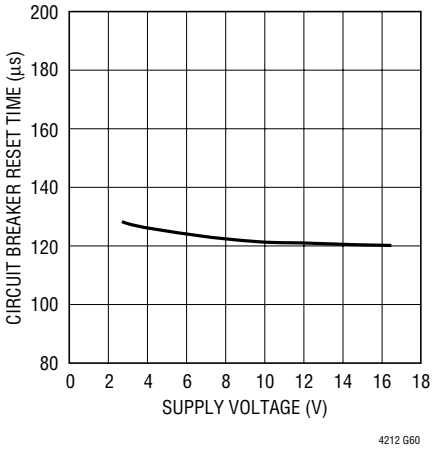
$\overline{FAULT}$ Pin Low to GATE Discharging Time vs Supply Voltage



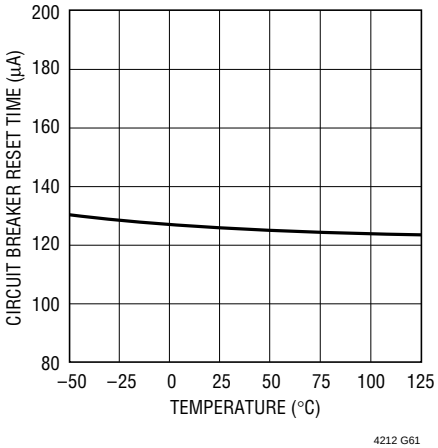
$\overline{FAULT}$ Pin Low to GATE Discharging Time vs Temperature



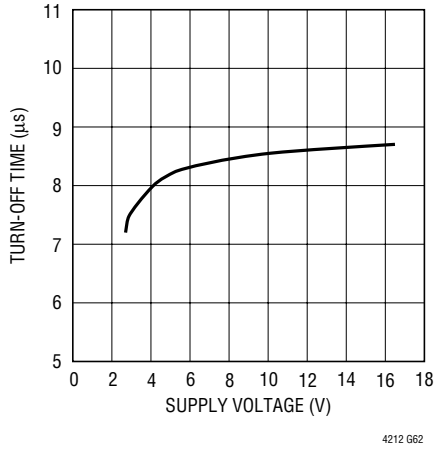
Circuit Breaker RESET Time vs Supply Voltage



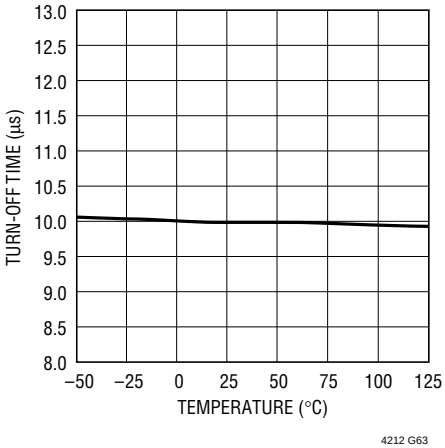
Circuit Breaker RESET Time vs Temperature



Turn-Off Time vs Supply Voltage



Turn-Off Time vs Temperature



PIN FUNCTIONS

ON (Pin 1): On/Off Control Input. The ON pin is used to enable and disable LTC4212 operation and reset internal logic and the electronic circuit breaker (ECB). It must be pulled high (>1.316V) to start the first system timing cycle. If the ON pin is pulled low (<0.455V typical) for more than 10µs, the internal logic is reset and the GATE pin is pulled down by a 200µA current to turn off the external FET. If the ON pin is pulled low for more than 120µs, the electronic circuit breaker is reset. This pin is tied to a resistive divider in latch-off applications or to the $\overline{FAULT}$ pin and an external RC circuit in auto-retry applications.

TIMER (Pin 2): System Timer Input. An external capacitor (C_{TIMER}) connected from this pin to ground determines the duration of the first and second system timing cycles. The first timing cycle allows time for the board to be inserted properly. During the second timing cycle, a soft-start circuit controls the gate of the external N-channel FET to limit inrush currents from the backplane supply.

PGT (Pin 3): Power Good Timer Input. An external capacitor (C_{PGT}) connected from this pin to ground sets the power good time-out period. This is the maximum time allowed for externally monitored DC/DC converters to power-up into regulation and pull the PGI pin high. The nominal time-out cycle is 1.81s/µF and begins from the end of the second system timing cycle. This pin is pulled to ground by an internal switch when the power good timer is disabled or when the ECB is tripped.

PGF (Pin 4): Power Good Glitch Filter Input. An external capacitor (C_{PGF}) connected from this pin to ground determines the power good glitch filter delay. The glitch filter is enabled if the externally monitored DC/DC converters are powered up within the power good time-out period (see Pin 3). If the PGI pin goes low for longer than the filter delay, the ECB is tripped.

GND (Pin 5): Device Ground Connection. Connect this pin to the system's analog ground plane.

PGI (Pin 6): Power Good Input Pin. This pin is used by the power good circuit to sense the open drain $\overline{RST}$ output or comparator outputs of an external supply monitor IC or the PGOOD output of a DC/DC converter. It requires an external pull-up resistor to a voltage above the $V_{\overline{FAULT}}$ threshold 1.236V. When the power good timer times out (see Pin 3), PGI must be high to avoid tripping the ECB and to enable the power good glitch filter.

GATE (Pin 7): Gate Output Pin. The output signal at this pin is the high side gate drive for the external N-channel FET pass transistor.

As shown in the Block Diagram, an internal charge pump supplies a 10µA gate current and sufficient gate voltage to drive the external FET for supply voltages from 2.5V to 16.5V. The internal charge pump and zener clamps at the charge pump output determine the gate drive voltage ($\Delta V_{GATE} = V_{GATE} - V_{CC}$). The charge pump produces a minimum 4V of ΔV_{GATE} for supplies in the range of 2.5V < V_{CC} < 4.75V. For V_{CC} > 4.75V, the ΔV_{GATE} is limited by zener clamp Z1 connected between the charge pump output and the V_{CC} pin. The ΔV_{GATE} is typically at 12V and with guaranteed minimum value of 10V. For V_{CC} > 15V, the zener clamp Z2 sets the limitation for ΔV_{GATE}. Z2 clamps the gate voltage to ground to 28V typically. The minimum Z2's clamp voltage is 23V. This effectively sets ΔV_{GATE} to 8V minimum.

SENSE (Pin 8): Circuit Breaker Set Pin. With a sense resistor placed in the power path between V_{CC} and SENSE, the LTC4212's electronic circuit breaker trips if the voltage across the sense resistor exceeds the thresholds set internally for the SLOW COMP and the FAST COMP, as shown in the Block Diagram. The threshold for the SLOW COMP is $V_{CB(SLOW)}$ = 50mV, and the electronic circuit breaker trips if the voltage across the sense resistor exceeds 50mV for 18µs.

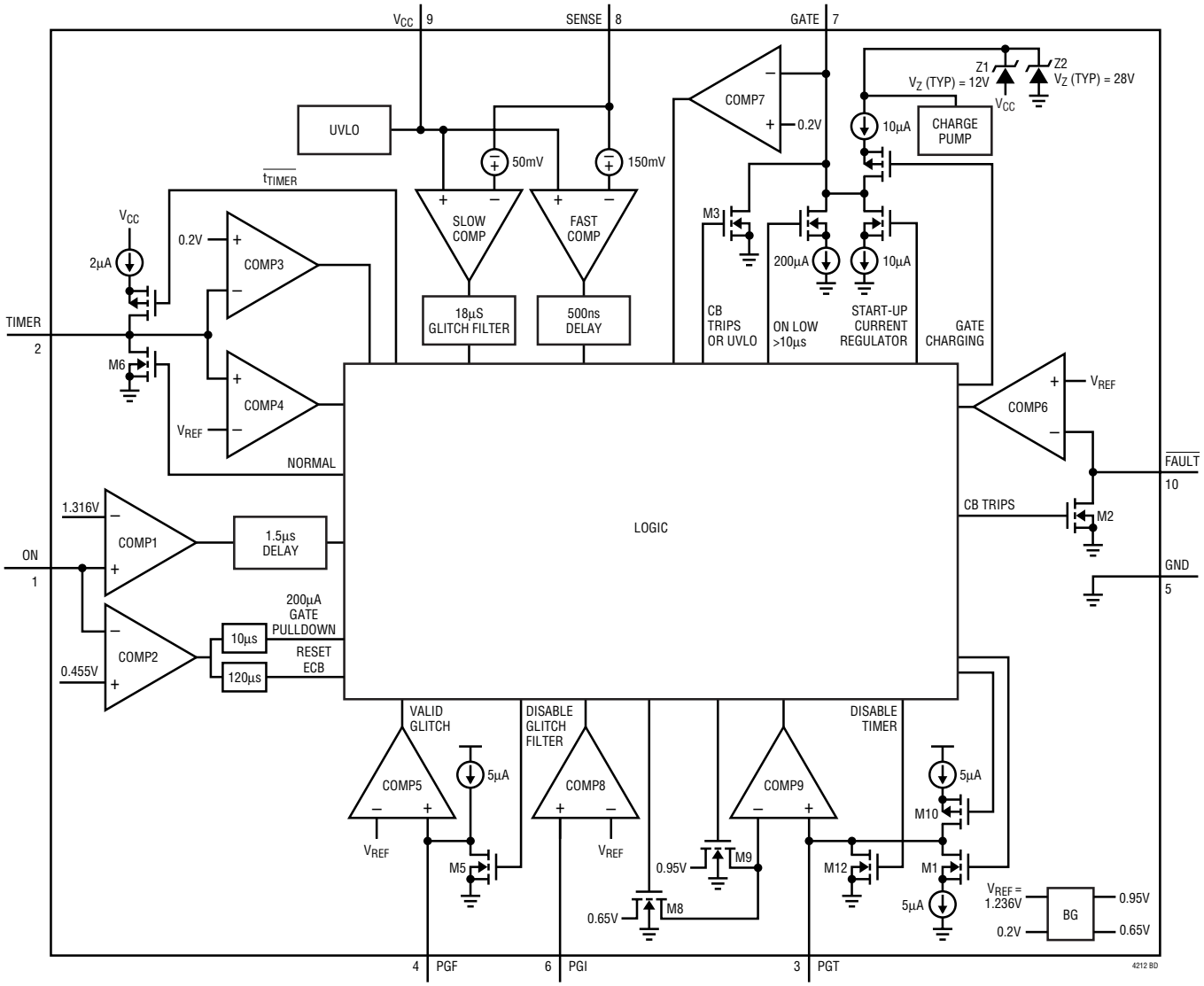
Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for the FAST COMP is set at $V_{CB(FAST)}$ = 150mV, and the circuit breaker trips if the voltage across the sense resistor exceeds 150mV for more than 500ns. To disable the electronic circuit breaker, connect the V_{CC} and SENSE pins together.

V_{CC} (Pin 9): This is the positive supply input to the LTC4212. The LTC4212 operates from 2.5V < V_{CC} < 16.5V, and the supply current is typically 1mA. An internal undervoltage lockout circuit disables the device until the voltage at V_{CC} exceeds 2.34V.

PIN FUNCTIONS

$\overline{\text{FAULT}}$ (Pin 10): Open Drain $\overline{\text{FAULT}}$ Output or External $\overline{\text{FAULT}}$ Input. If the FAST COMP, SLOW COMP or the power good circuit trips the ECB, the $\overline{\text{FAULT}}$ pin is latched low. The $\overline{\text{FAULT}}$ pin is an open drain output and is typically connected by a 10k pull-up resistor to V_{CC}. An external circuit can also trip the ECB by driving $\overline{\text{FAULT}}$ below 1.236V (typical).

BLOCK DIAGRAM



OPERATION

Hot Circuit Insertion

When circuit boards are inserted into or removed from live backplanes, the supply bypass capacitors can draw huge transient currents from the backplane power bus as they charge. The transient current can cause permanent damage to the connector pins as well as cause glitches on the system supply, causing other boards in the system to reset.

The LTC4212 is designed to turn a printed circuit board's supply voltages ON and OFF in a controlled manner, allowing the circuit board to be safely inserted or removed from a live backplane.

Output Voltage Monitor

Unlike other LTC Hot Swap controller products, the LTC4212 does not have an FB pin and monitors onboard DC/DC converters via an external power supply monitor IC such as the LTC1326-2.5 or the LTC1727. This allows several DC/DC converters to be monitored at the same time. The LTC4212's PGI or power good input pin is used to monitor the $\overline{RST}$ or comparator outputs of the monitor IC and it can also be tied directly to the PGOOD pin of a DC/DC converter.

Undervoltage Lockout

The LTC4212's internal power-on reset circuit initializes the start-up procedure and ensures the IC is in the proper state if the input supply voltage exceeds 2.34V. If the supply voltage falls below 2.23V, the LTC4212 is in undervoltage lockout (UVLO) mode, and the GATE pin is pulled low. Since the UVLO circuitry uses hysteresis, the LTC4212 restarts after the supply voltage rises above 2.34V and the ON pin goes high.

In addition, users can utilize the ON comparator (COMP1) or the $\overline{FAULT}$ comparator (COMP6) to effectively set up a higher undervoltage lockout level. Figure 1 shows the external resistive divider for the ON pin to adjust the system's undervoltage lockout voltage. The system will enter the plug-in cycle after the ON pin rises above 1.316V. The resistive divider sets the circuit to turn on when V_{CC} reaches around 79% of its final value. If a different turn on V_{CC} voltage is desired change the resistive divider ratio accordingly. The $\overline{FAULT}$ comparator can also be used to set a higher undervoltage lockout voltage. If the $\overline{FAULT}$ comparator is used for this purpose, the system will wait for the input voltage to increase above the level set by the user before starting the second timing cycle. Also, if the input voltage drops below the set level in normal operating mode, the electronic circuit breaker (ECB) trips and the user must cycle the ON pin or V_{CC} to restart the system.

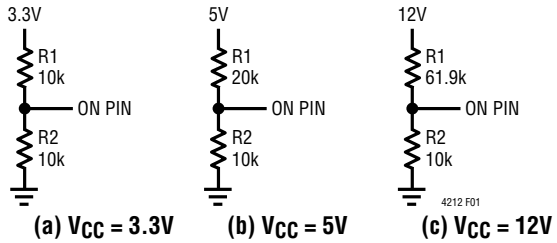


Figure 1. ON Pin Sets the Undervoltage Lockout Voltage Externally

System Timing

System timing for the LTC4212 is generated by the TIMER circuitry (see the Block Diagram). If the LTC4212's internal timing circuit is off, an internal N-channel FET connects the TIMER pin to GND. If the timing circuit is enabled, an internal 2µA current source is then connected to the TIMER pin to charge C_{TIMER} at a rate given by Equation 1:

$$C_{TIMER}\ Charge\text{-}Up\ Rate = \frac{2\mu A}{C_{TIMER}} \quad (1)$$

When the TIMER pin voltage reaches COMP4's threshold of 1.236V, the TIMER pin is reset to GND. Equation 2 gives an expression for the timer period:

$$t_{TIMER} = 1.236V \bullet \frac{C_{TIMER}}{2\mu A} \quad (2)$$

As a design aid, the LTC4212's timer period as a function of the C_{TIMER} using standard values from 3.3nF to 0.33µF is shown in Table 1.

The C_{TIMER} value is vital to ensure a proper start-up and reliable operation. This timing period should not be excessive as an output short can occur at start-up causing the external MOSFET to overheat. A good starting point is to

OPERATION

set C_{TIMER} = 10nF and adjust its value accordingly to suit the specific applications.

Table 1. t_{TIMER} vs C_{TIMER}

C_{TIMER}	t_{TIMER}
0.0033µF	2.0ms
0.0047µF	2.9ms
0.0068µF	4.2ms
0.0082µF	5.1ms
0.01µF	6.2ms
0.015µF	9.3ms
0.022µF	13.6ms
0.033µF	20.4ms
0.047µF	29.0ms
0.068µF	42.0ms
0.082µF	50.7ms
0.1µF	61.8ms
0.15µF	92.7ms
0.22µF	136ms
0.33µF	204ms

Power-Up Timeout Circuit

The power-up timeout circuit has two functions. During power-up, it trips the circuit breaker if the DC/DC converters on the board do not power-up and do not enter regulation on time. After normal power-up, it is configured to trip the circuit breaker if any of the converters exit regulation for longer than a programmable delay. Once the circuit breaker is tripped, the LTC4212 is latched off and the board is disconnected from the system supply. The ON pin must be taken low for 120µs to reset the circuit breaker and then high to reconnect the board to the backplane supply.

The power-up timeout circuit uses three pins: PGI or power good input pin, PGT or power good timer pin and PGF or power good filter pin. It is enabled at the end of the second system timing cycle, provided that the $\overline{FAULT}$ pin is high. Prior to being enabled or if $\overline{FAULT}$ is low, the PGT and PGF pins are pulled to GND by internal N-channel FETs, M5 and M12 respectively. When enabled, the power-up timeout circuit starts the power good timer, which generates a time-out period before the PGI pin is sampled.

Power Good Timer

The timer consists of COMP9, M8-M12, two 5µA current sources and 0.65V and 0.95V threshold voltages for COMP9.

The PGI pin is normally connected to the $\overline{RST}$ output pin or comparator outputs of an external supply monitor IC or to the PGOOD pin of a DC/DC converter and drives a comparator, COMP8 which has a threshold voltage of 1.236V and 28mV of hysterisis. The $\overline{RST}$ and PGOOD pins are typically open drain pins and require an external pull-up resistor. The upper end of the resistor must be connected to a voltage greater than the upper threshold of the PGI comparator (1.236V).

A capacitor, C_{PGT}, connected from the PGT pin to ground programs the time-out period generated by the power good timer according to Equation 3. Table 2 shows the power good time-out periods for a list of standard capacitor values.

$$t_{TIMEOUT} = 1.81\Omega \bullet C_{PGT} \quad (3)$$

Two 5µA current sources are switched in and out to charge and discharge C_{PGT} between 0.65V and 0.95V for 14 cycles.

Table 2. $t_{TIMEOUT}$ vs C_{PGT}

C_{PGT}	$t_{TIMEOUT}$
3.3nF	5.97ms
4.7nF	8.51ms
6.8nF	12.3ms
8.2nF	14.8ms
0.01µF	18.1ms
0.022µF	39.8ms
0.033µF	59.7ms
0.047µF	85.1ms
0.068µF	123ms
0.082µF	148ms
0.1µF	181ms
0.22µF	136ms
0.33µF	398ms
0.47µF	851ms
0.68µF	1230ms
0.82µF	1480ms
1µF	1810ms

OPERATION

Since the PGT is pulled to GND by M12 before the power good circuit is enabled, the first positive ramp at the PGT pin starts from 0V instead of the 0.65V for the subsequent 13 cycles.

Power Good Time-Out

At the end of the time-out period, the PGI pin is sampled. M12 is turned on to discharge C_{PGT} to ground. If the PGI pin is low when sampled, the DC/DC converters have not entered into regulation on time and the power good circuit trips the circuit breaker to latch off the board. If PGI is high when sampled, the converters powered up into regulation on time and the board is left powered up. The power good glitch filter is enabled and it monitors the PGI pin for a low, an indication that at least one DC/DC converter has dropped out of regulation. The glitch filter rejects low pulses shorter than a programmable period.

Power Good Glitch Filter

A glitch filter consisting of COMP5, M5 and a 5µA current source rejects PGI low pulses that are shorter than the duration programmed by an external capacitor, C_{PGF}, connected from the PGF pin to GND.

Once the glitch filter is enabled, M5 is switched off whenever PGI goes low. This allows an internal 5µA current source to charge the capacitor at the PGF pin. If PGI stays low for long enough, the voltage at the PGF pin rises above the upper threshold of COMP5 (1.236V) and causes the power good circuit to trip the circuit breaker. For a given C_{PGF} capacitance connected between PGF and GND, the minimum low PGI pulse width needed to trip the circuit breaker is given by:

$$t_{PGF} = 1.236V \bullet (C_{PGF})/5\mu A + 5\mu s \quad (4)$$

An internal 5pF capacitor and stray MSOP-10 package capacitance sets t_{PGF} to 5µs nominal when C_{PGF} is omitted. Table 3 shows t_{PGF} values for various standard capacitors. Tying the PGF pin to ground prevents the power good glitch filter from tripping the circuit breaker after normal power-up.

Table 3. t_{PGF} vs C_{PGF}

C_{PGF}	t_{PGF}
—	5µs
10pF	7.5µs
22pF	10.4µs
33pF	13.2µs
47pF	16.6µs
68pF	21.8µs
82pF	25.2µs
100pF	29.7µs
220pF	59.3µs
330pF	86.6µs
470pF	121.2µs
680pF	173µs
820pF	208µs
1nF	252µs

Soft-Start or Inrush Current Control

The LTC4212 monitors the load current by sensing the voltage (V_{CC} – V_{SENSE}) developed across an external sense resistor (R_{SENSE}) connected between the V_{CC} and SENSE pins. During the second timing cycle (see Normal Operating Sequence) a soft-start circuit turns on the external N-channel FET gradually to keep inrush currents in check. The soft-start circuit monitors and servos the voltage across R_{SENSE} to 50mV by either connecting a 10µA pull-up current source to the GATE pin when the voltage across R_{SENSE} is less than 50mV or discharging it with a 10µA pull-down current source when the voltage rises above 50mV. Therefore, the inrush current from the backplane supply is limited to:

$$I_{LIMIT(SOFTSTART)} = 50mV/R_{SENSE} \quad (5)$$

For example, $I_{LIMIT(SOFTSTART)} = 5A$ when $R_{SENSE} = 0.01\Omega$.

Assuming that the voltage across the sense resistor does not exceed 50mV, the voltage at the GATE pin rises at rate given by:

$$V_{GATE} \text{ Slew Rate} = dV_{GATE}/dt = 10\mu A/C_{GATE} \quad (6)$$

where, C_{GATE} = Power MOSFET gate input capacitance (C_{ISS}).

For example, an Si4410DY (a 30V N-channel power MOSFET) exhibits an approximate C_{GATE} of 3300pF at

OPERATION

V_{GS} = 10V. From Equation 6, the slew rate is calculated to be 3.03V/ms.

The inrush current being delivered to the load while the GATE pin is ramping depends on C_{LOAD} and C_{GATE}. The external N-channel MOSFET acts as a source follower so that its source (load) voltage ramps up at the same rate as the GATE pin. The output current component for capacitor charging is given by Equation 7:

$$I_{INRUSH} = C_{LOAD} \bullet dV_{GATE}/dt = 10\mu A \bullet C_{LOAD}/C_{GATE} \quad (7)$$

where, C_{LOAD} is the total capacitance at the load side of the MOSFET. For example, if C_{GATE} = 3300pF and C_{LOAD} = 2000µF, the inrush current charging C_{LOAD} is 6.06A. Note that the soft-start circuit will servo the inrush to $I_{LIMIT(SOFTSTART)}$ or 5A in this example and dV_{GATE}/dt will be lower than calculated from Equation 6.

Frequency Compensation at Soft-Start

If the external MOSFET's gate input capacitance (C_{ISS}) is greater than 600pF, no external gate capacitor is required at GATE to stabilize the internal current-limiting loop during soft-start. Otherwise, connect a gate capacitor between the GATE pin and ground to increase the total gate capacitance to be equal to or above 600pF. The servo loop that controls the external MOSFET during current limiting has a unity-gain frequency of about 105kHz and phase margin of 80° for external MOSFET gate input capacitances of up to 2.5nF.

Electronic Circuit Breaker

The LTC4212 features an electronic circuit breaker function that protects against supply overvoltage, externally-generated fault conditions, shorts or excessive load current conditions and power good faults. If the circuit breaker trips, the GATE pin is immediately pulled to ground, the external N-channel MOSFET is quickly turned OFF and $\overline{FAULT}$ is latched low.

The circuit breaker trips whenever the voltage across the sense resistor exceeds two different levels, set by the LTC4212's SLOW COMP and FAST COMP thresholds (see Block Diagram). The SLOW COMP trips the circuit breaker if the voltage across the SENSE resistor ($V_{CC} – V_{SENSE} = V_{CB}$) is greater than 50mV for 18µs. The FAST COMP trips the circuit breaker to protect against fast load overcurrents if the transient voltage across the sense resistor is greater than 150mV for 500ns.

The timing diagram of Figure 2 illustrates when the LTC4212's electronic circuit breaker is armed. After the first timing cycle, the LTC4212's FAST COMP is armed at Time Point 6. This ensures that the system is protected against a short-circuit condition during the second timing cycle after C_{LOAD} has been fully charged. At Time Point 8, SLOW COMP is armed when the internal control loop is disengaged.

The timing diagram in Figure 4 illustrates the operation of the LTC4212 when the load current conditions exceed the threshold of SLOW COMP ($V_{CB(SLOW)}$ > 50mV).

Circuit Breaker Reset

Referring to the Block Diagram, the ON pin drives two internal comparators, COMP1 and COMP2. COMP1 is referenced to 1.236V and has a hysterisis of 80mV. COMP2 is referenced to 0.5V and has a hysterisis of 45mV. The outputs of the two comparators drive an internal flip-flop to generate a typical high and low ON pin threshold of 1.31V and 0.455V respectively.

If the voltage at the ON pin is driven below 0.455V for more than 10µs, all internal control logic except the circuit breaker is reset. A 200µA pull-down current source is connected to the GATE pin to pull it down gradually. Holding the ON pin below 0.455V for 120µs or longer, resets the circuit breaker. Following reset, the ON pin must be taken above 1.316V to start a power-up sequence.

Normal Operating Sequence

Figure 2 illustrates the normal power-up sequence for two different applications. The PGI ($\overline{RST}$) and PGF ($\overline{RST}$) waveforms are valid for applications which use the PGI pin to monitor the $\overline{RST}$ output of a supply monitor IC. The PGI (PGOOD) and PGF (PGOOD) waveforms refer to applications that tie the PGI pin to the PGOOD output of a DC/DC converter. All other waveforms in Figure 2 are common to both applications. The PGI and PGF waveforms for applications that connect PGI pin to the

OPERATION

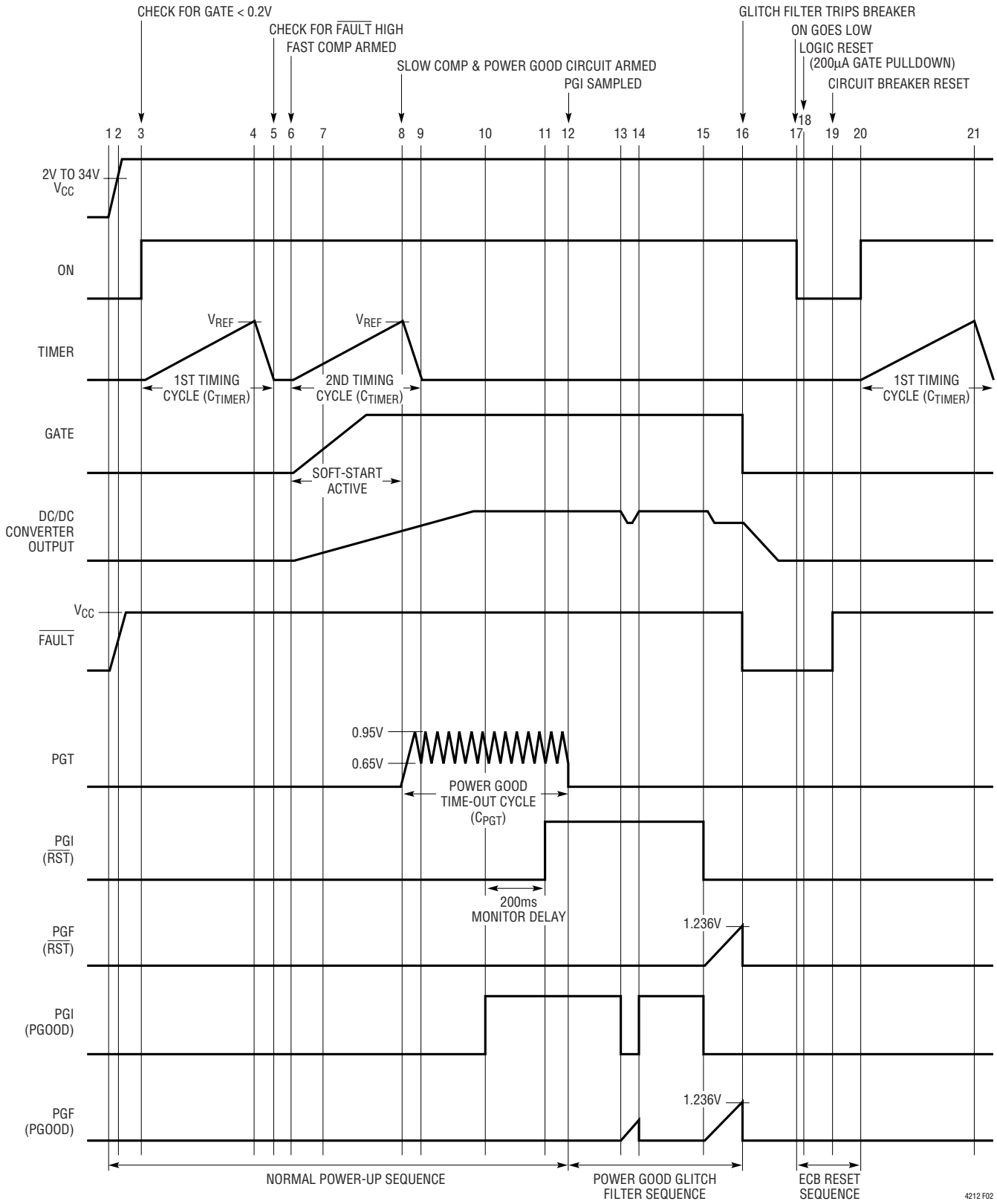


Figure 2. Normal Power-Up, Power Good Glitch Filter and ECB Reset Sequences

OPERATION

comparator outputs of a supply monitor such as the LTC1727 are similar to PGI (PGOOD) and PGF (PGOOD).

First Timing Cycle

When the PC board makes contact with the backplane (Time Point 1), V_{CC} starts to rise. While V_{CC} < 2.23V, the LTC4212 is in UVLO mode. The GATE pin is pulled to ground by a 200µA current source to shut off the external N-channel MOSFET and the TIMER, PGT and PGF pins are all pulled low by internal N-channel FETs M6, M5 and M12. When V_{CC} rises above the UVLO threshold of 2.34V (Time Point 2), the LTC4212 waits for the ON pin to go high (> 1.316V) and checks that the GATE is low (V_{GATE} < 0.2V) before initiating the first timing cycle (Time Point 3).

The first timing cycle begins with the TIMER pin up at a rate given by Equation 1. At Time Point 4 (the timing period programmed by C_{TIMER}), the TIMER pin voltage equals V_{TMR} = 1.236V. Next the TIMER pin is pulled down by M6 to Time Point 5 where V_{TMR} = 0.2V. At Time Point 5, the LTC4212 checks that the $\overline{FAULT}$ pin voltage is high ($V_{\overline{FAULT}}$ > 1.236V) before initiating the second timing cycle. If $\overline{FAULT}$ is forced low externally, the second timing cycle will not start and the external N-channel FET stays OFF.

Second Timing Cycle

At the beginning of the second timing cycle (Time Point 6), the LTC4212 FAST COMP is armed and the soft-start circuit is enabled. The GATE pin is ramped up at a rate given by Equation 6. If the inrush current from the backplane supply (Equation 7) is large enough to cause the voltage drop across the sense resistor to exceed 50mV, the soft-start circuit activates to regulate the inrush current (Equation 5). The soft-start circuit continues to operate until Time Point 8 when the TIMER pin voltage equals V_{TMR} = 1.236V again. At Time Point 8, SLOW COMP is armed and the power good circuit is enabled.

When the power good circuit is enabled, M12, the internal N-channel FET shorting the PGT pin to ground is switched OFF and the power good timer started. The DC/DC converters enter regulation at Time Point 10. In applications where the PGI pin is connected to the PGOOD pin of a DC/DC converter, PGI is pulled high shortly after the converter enters into regulation (see PGI (PGOOD) waveform). In applications where PGI monitors the $\overline{RST}$ output of a supply monitor like the LTC1326-2.5, the $\overline{RST}$ and therefore the PGI pins are held low for another 200ms until Time Point 11 (see PGI ($\overline{RST}$) waveform). At Time Point 12, the power good circuit samples the PGI pin. During normal power-up, PGI will go high before Time Point 12. The power good circuit disables and resets the power good timer and M12 is turned ON to pull PGT to ground. The power good glitch filter is then enabled to monitor the PGI pin.

Power Good Glitch Filter Sequence

The power good glitch filter sequence is also shown in Figure 2 from Time Points 12 through 16. When the glitch filter is enabled, M5, the internal N-channel FET that shorts the PGF pin to GND is switched OFF whenever PGI is low. This allows the C_{PGF} capacitor to be charged by an internal 5µA current source towards 1.236V. If the PGF pin voltage exceeds 1.236V, the power good circuit trips the circuit breaker to latch the part off. Tying PGF to GND disables the glitch filter and prevents the power good from tripping the circuit breaker after Time Point 12.

For supply monitors such as the LTC1326-2.5, the glitch filter is less useful. The comparators in the LTC1326-2.5 that monitor the DC/DC converters have a typical propagation delay of 13µs. If any of the monitored supplies leave regulation for more than 13µs, the $\overline{RST}$ signal will be pulled low until 200ms after all the supplies re-enter regulation. The net effect is that the LTC1326-2.5 performs the glitch filtering and rejects pulses shorter than 13µs. The PGOOD output of a DC/DC converter does not have the 200ms delay of the LTC1326-2.5. Thus any low PGOOD pulse will immediately cause C_{PGF} to be charged towards 1.236V (Time Points 13 and 14). C_{PGF} values can be selected to reject low pulses that are shorter than some desired pulse width.

Some supply monitor ICs such as the LTC1727 provide access to the outputs of comparators monitoring the DC/DC converters as well as the $\overline{RST}$ output. The comparator outputs track the converter output voltages. If the LTC4212 PGI pin is used to monitor the output of a comparator rather than the $\overline{RST}$ output of the LTC1727, C_{PGF} can be selected to reject low pulses shorter than a desired pulse width.

OPERATION

Electronic Circuit Breaker (ECB) Reset Sequence

The ECB reset sequence is shown in Figure 2 from Time Points 17 through 19. At Time Point 17, the ON pin is taken low. Ten microseconds later at Time Point 18, the internal logic is reset and a 200µA source is connected to the GATE pin to pull the pin to ground. 120µs after ON goes low (Time Point 19), the ECB is reset. When the ON pin is taken high at Time Point 20 a new first timing cycle is started. If the time from Time Point 17 to Time Point 18 is less than 120µs, the ECB is not reset and taking the ON pin high at Time Point 20 will not start a new first timing cycle.

Power Good Timeout Fault Sequence

Figure 3 shows a power-up sequence in which the DC/DC converters do not enter regulation on time and the power good trips the ECB. The sequence is the same as for the normal power-up in Figure 2 until Time Point 12 when the power good timer times out and the PGI pin is sampled. Since PGI is low, the power good circuit trips the ECB. The GATE pin is pulled to ground immediately to disconnect power to the board and the $\overline{\text{FAULT}}$ pin is latched to a low state. The PGT and PGF pins are pulled to GND internally by N-channel FETs. To reconnect the board to the backplane supply, the ON pin must be taken low for at least 120µs to reset the ECB and then high again to start a new first timing cycle.

Overcurrent Fault Sequence

Figure 4 shows a power-up sequence with SLOW COMP tripping the ECB. At the beginning of the second timing cycle (Time Point 6), the GATE pin is connected to the soft-start circuit and FAST COMP is armed but it does not usually trip the ECB due to the action of the soft-start circuit on the GATE pin. The soft-start circuit regulates the voltage across the R_{SENSE} resistor to 50mV. At Time Point 8, the soft-start circuit is disconnected. A 10µA current source pulls the GATE pin up and SLOW COMP is armed. If a short occurs and the voltage across R_{SENSE} jumps above 50mV for more than 18µs but is less than 150mV, SLOW COMP trips the ECB (Time Point 10). If the voltage across R_{SENSE} jumps above 150mV for 500ns or more, FAST COMP will trip the ECB.

When the ECB trips, the GATE pin is driven to GND immediately to shut off the external N-channel FET and disconnect the board from the backplane supply. The $\overline{\text{FAULT}}$ pin is latched to a low state and the power good circuit is reset. The PGT and PGF pins are shorted to ground by internal N-channel FETs. In order to reset the fault latch, the ON pin must be taken low for more than 120µs (Time Points 12 to 14). After that, taking the ON pin high (Time Point 15) starts a new power-up sequence.

Autoretry Sequence

Once the circuit breaker trips, the LTC4212 can be configured to autoretry that is attempt to reconnect the backplane supply automatically. Both $\overline{\text{FAULT}}$ and ON pins are tied together to an external pull-up resistor to V_{CC} (R_{AUTO}) and to a delay capacitor (C_{AUTO}) as shown in Figure 5.

Figure 6 shows two autoretry sequences caused by a persistent short. When the circuit breaker trips (Time Point 9), an internal N-channel FET at the $\overline{\text{FAULT}}$ pin is turned on to pull the pin low. This discharges the autoretry capacitor, C_{AUTO} towards ground. When the ON pin voltage drops below 0.455V for 10µs (from Time Point 10), internal logic is reset and a 200µA current source is connected to the GATE pin. The GATE pin is already pulled down to ground at Time Point 9. The circuit breaker is not reset so that the $\overline{\text{FAULT}}$ pin continues to discharge C_{AUTO}. After the ON pin has dropped below 0.455V for more than 120µs (Time Point 11), the circuit breaker is reset. The N-channel FET at the $\overline{\text{FAULT}}$ pin is switched off and the pull-up resistor at the ON pin starts to charge C_{AUTO} towards the upper 1.316V threshold of the ON pin. Once the ON pin voltage rises above 1.316V, the first timing cycle is started. The total cooling off period for the external N-channel FET starts at Time Point 9 when the circuit breaker trips to Time Point 15 when the second timing cycle is started.

OPERATION

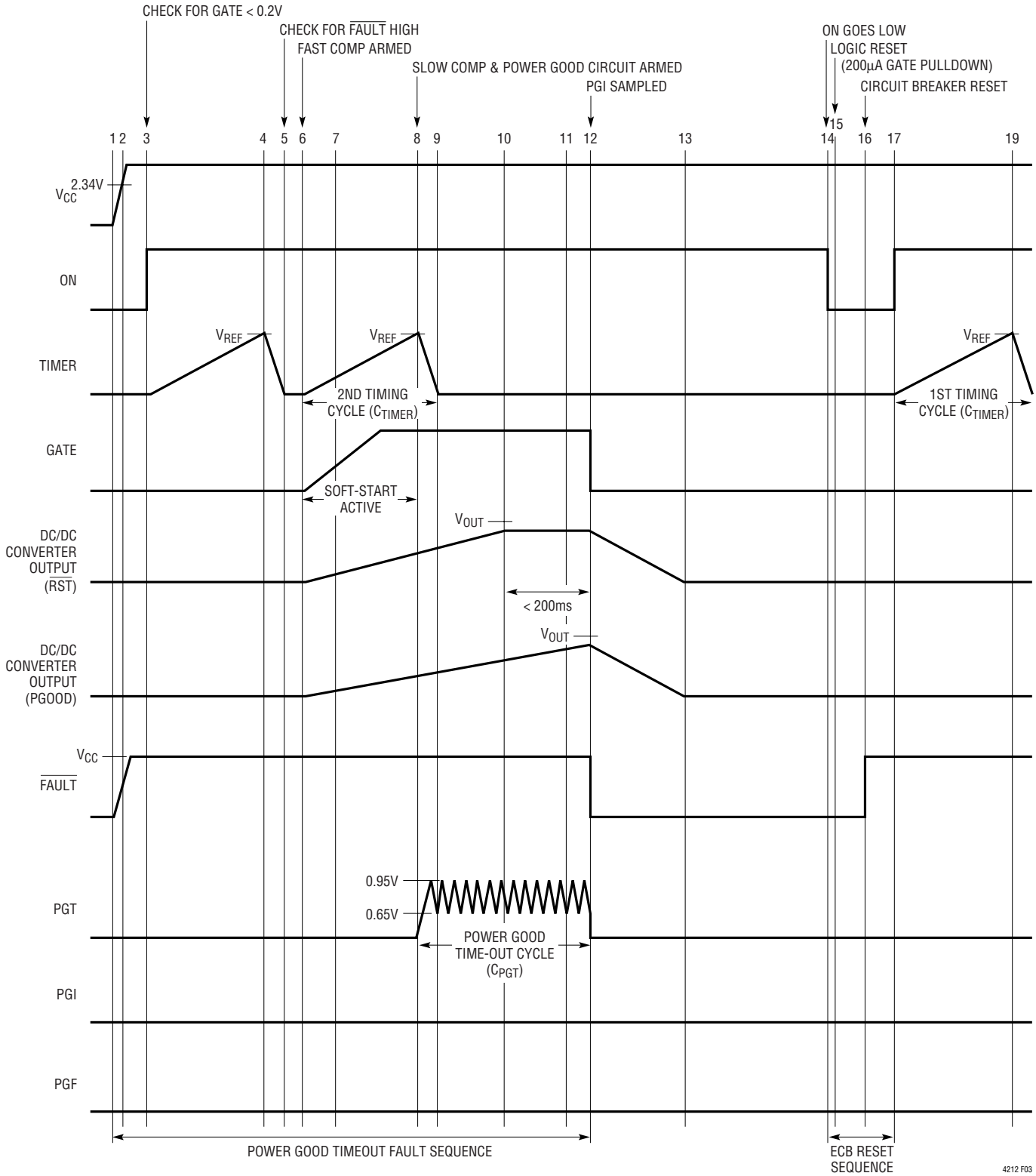


Figure 3. Power Good Time-Out Fault and ECB Reset Sequence

OPERATION

It consists of the time the $\overline{FAULT}$ pin takes to discharge C_{AUTO} (Time Points 9 to 10), the 120µs needed to reset the circuit breaker (Time Points 9 to 11), the time it takes the pull-up resistor at the ON pin to charge C_{AUTO} above 1.316V (Time Points 11 to 12) and the elapsed time before the external N-channel starts to conduct during the second timing cycle (Time Points 12 to 16).

Sense Resistor Considerations

The fault current level at which the LTC4212's internal electronic circuit breaker trips is determined by a sense resistor connected between the LTC4212's V_{CC} and SENSE pins and two separate trip points. The first trip point is set

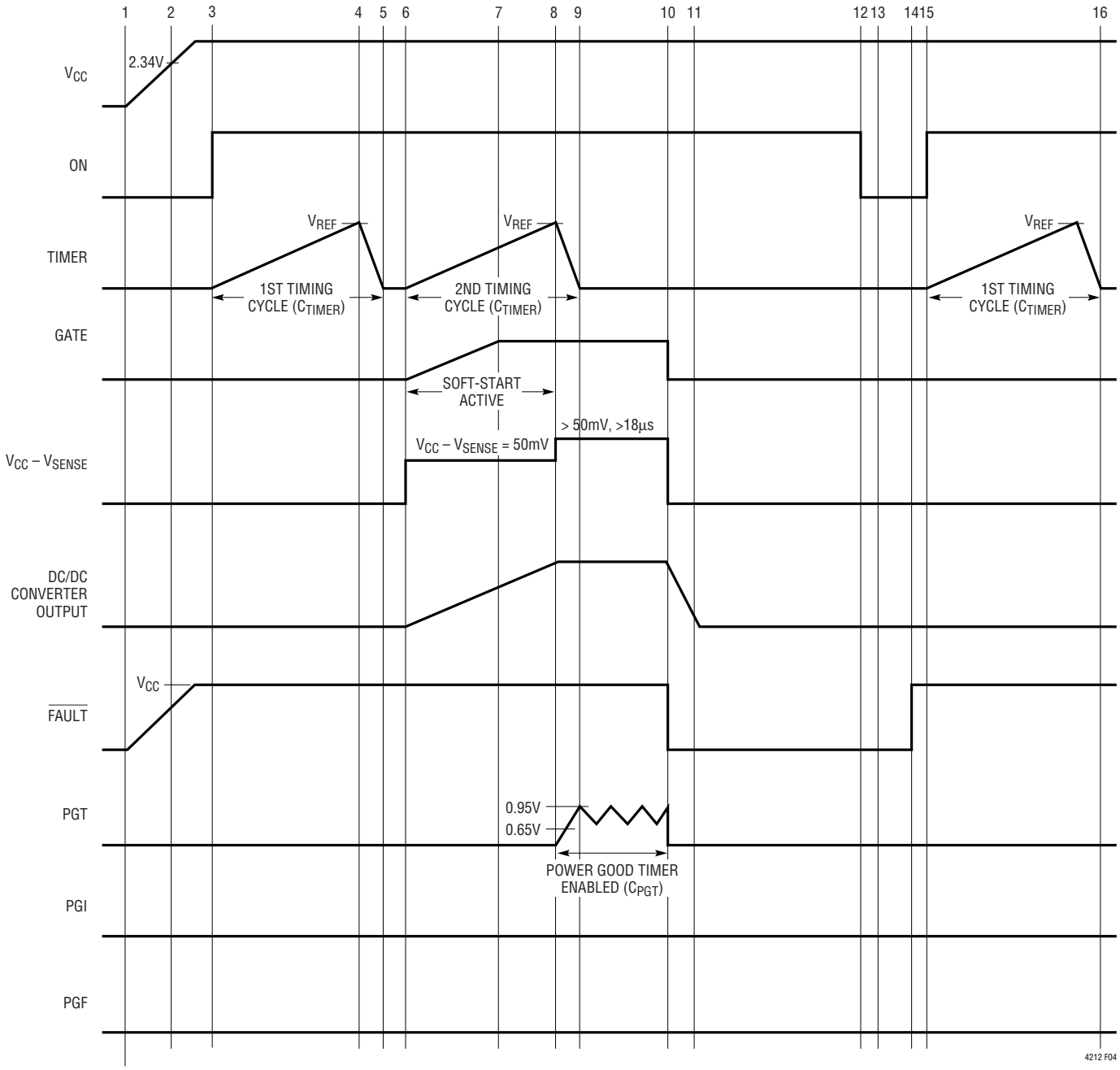


Figure 4. Power-Up with Overcurrent, Slow Comparator Trips the Circuit Breaker

OPERATION

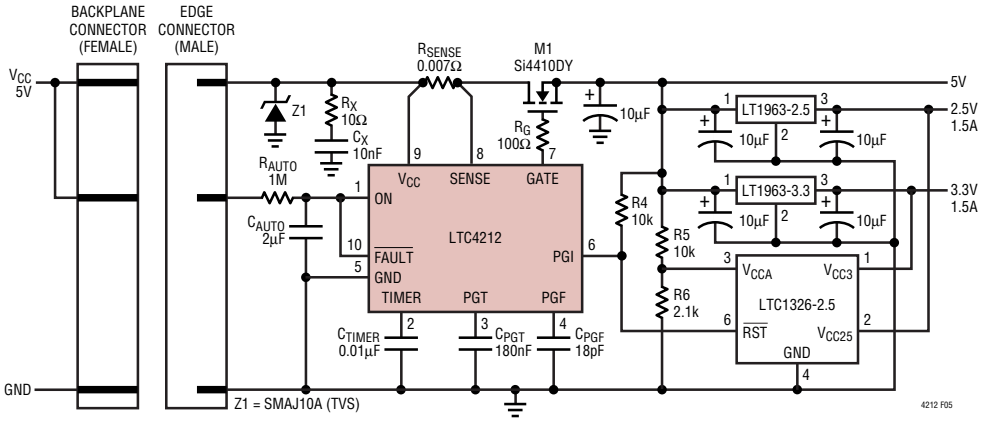


Figure 5. LTC4212 Autoretry Application

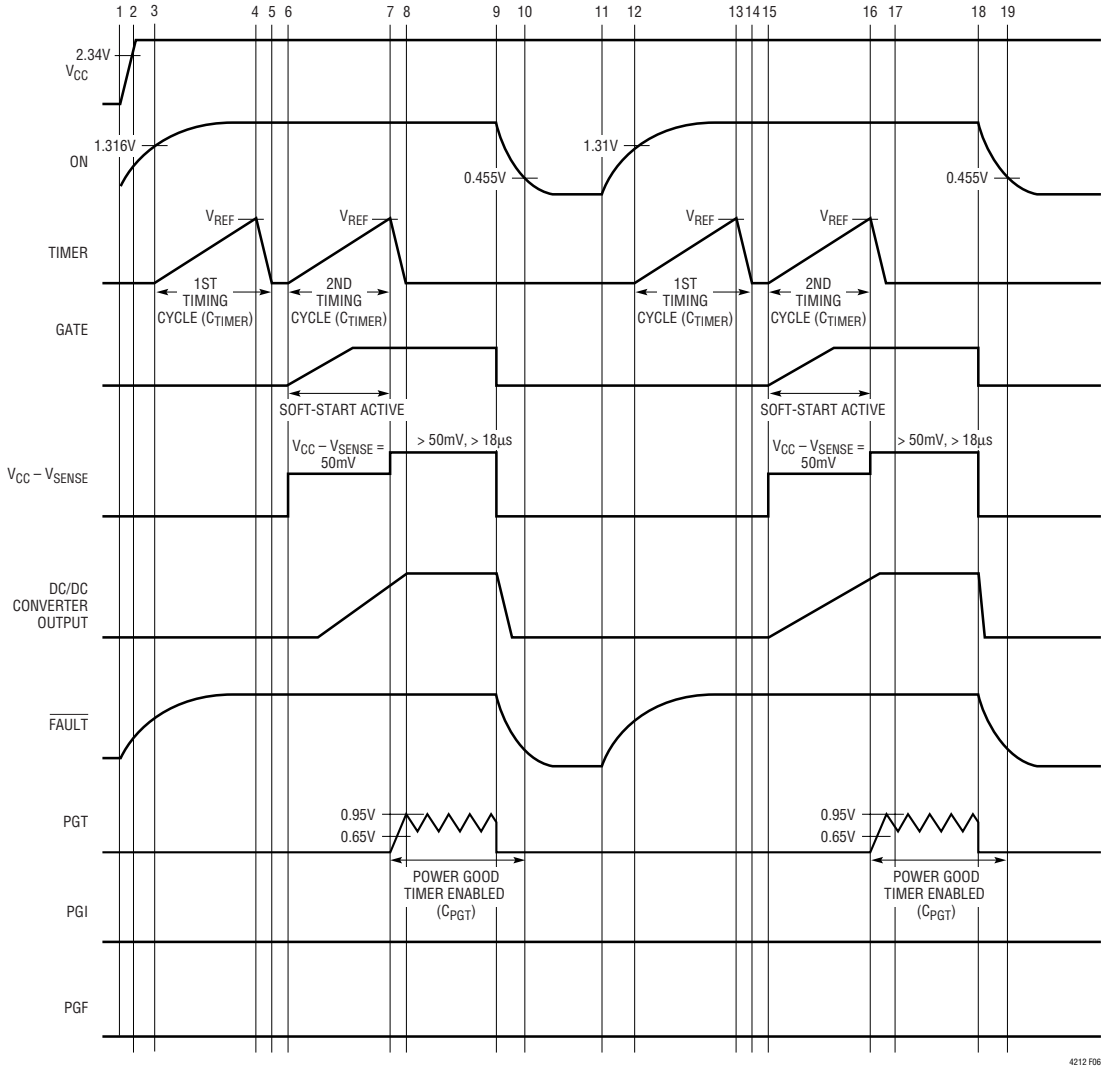


Figure 6. Autoretry Sequence

OPERATION

by the SLOW COMP's threshold, $V_{CB(SLOW)}$ = 50mV, and occurs should a load current fault condition exist for more than 18µs. The current level at which the electronic circuit breaker trips is given by Equation 8:

$$I_{TRIP(SLOW)} = \frac{V_{CB(SLOW)}}{R_{SENSE}} = \frac{50mV}{R_{SENSE}} \quad (8)$$

The second trip point is set by the FAST COMP's threshold, $V_{CB(FAST)}$ = 150mV, and occurs during fast load current transients that exist for 500ns or longer. The current level at which the circuit breaker trips in this case is given by Equation 9:

$$I_{TRIP(FAST)} = \frac{V_{CB(FAST)}}{R_{SENSE}} = \frac{150mV}{R_{SENSE}} \quad (9)$$

As a design aid, the currents at which electronic circuit breaker trips for common values for R_{SENSE} are shown in Table 4.

Table 4. $I_{TRIP(SLOW)}$ and $I_{TRIP(FAST)}$ vs R_{SENSE}

R_{SENSE}	$I_{TRIP(SLOW)}$	$I_{TRIP(FAST)}$
0.005Ω	10A	30A
0.006Ω	8.3A	25A
0.007Ω	7.1A	21A
0.008Ω	6.3A	19A
0.009Ω	5.6A	17A
0.01Ω	5A	15A

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4212's V_{CC} and SENSE pins are strongly recommended. The drawing in Figure 7 illustrates the correct way of making connections between the LTC4212 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips. Table 5 in the Appendix lists sense resistors that can be used with the LTC4212's circuit breaker.

Calculating Circuit Breaker Trip Current

For a selected R_{SENSE} value, the nominal load current that trips the circuit breaker is given by Equation 10:

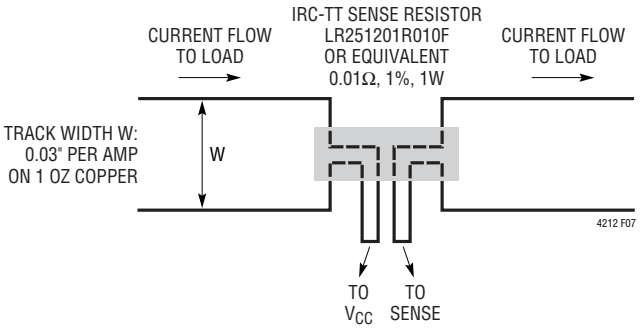


Figure 7. Making PCB Connections to the Sense Resistor

$$I_{TRIP(NOM)} = \frac{V_{CB(NOM)}}{R_{SENSE(NOM)}} = \frac{50mV}{R_{SENSE(NOM)}} \quad (10)$$

The minimum load current that trips the circuit breaker is given by Equation 11.

$$I_{TRIP(MIN)} = \frac{V_{CB(MIN)}}{R_{SENSE(MAX)}} = \frac{40mV}{R_{SENSE(MAX)}} \quad (11)$$

where

$$R_{SENSE(MAX)} = R_{SENSE(NOM)} \bullet \left[1 + \left(\frac{R_{TOL}}{100}\right)\right]$$

The maximum load current that trips the circuit breaker is given in Equation 12.

$$I_{TRIP(MAX)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}} = \frac{60mV}{R_{SENSE(MIN)}} \quad (12)$$

where

$$R_{SENSE(MIN)} = R_{SENSE(NOM)} \bullet \left[1 - \left(\frac{R_{TOL}}{100}\right)\right]$$

OPERATION

For example:

If a sense resistor with 7mΩ ±5% R_{TOL} is used for current limiting, the nominal trip current $I_{TRIP(NOM)}$ = 7.1A. From Equations 11 and 12, $I_{TRIP(MIN)}$ = 5.4A and $I_{TRIP(MAX)}$ = 9.02A respectively.

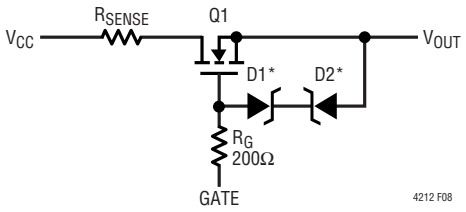
For proper operation and to avoid the circuit breaker tripping unnecessarily, the minimum trip current ($I_{TRIP(MIN)}$) must exceed the circuit's maximum operating load current. For reliability purposes, the operation at the maximum trip current ($I_{TRIP(MAX)}$) must be evaluated carefully. If necessary, two resistors with the same R_{TOL} can be connected in parallel to yield an $R_{SENSE(NOM)}$ value that fits the circuit requirements.

Power MOSFET Selection Criteria

To start the power MOSFET selection process, choose the maximum drain-to-source voltage, $V_{DS(MAX)}$, and the maximum drain current, $I_{D(MAX)}$ of the MOSFET. The $V_{DS(MAX)}$ rating must exceed the maximum input supply voltage (including surges, spikes, ringing, etc.) and the $I_{D(MAX)}$ rating must exceed the maximum short-circuit current in the system during a fault condition. In addition, consider three other key parameters: 1) the required gate-source (V_{GS}) voltage drive, 2) the voltage drop across the drain-to-source on resistance, $R_{DS(ON)}$ and 3) the maximum junction temperature rating of the MOSFET.

Power MOSFETs are classified into two categories: standard MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 10V) and logic-level MOSFETs ($R_{DS(ON)}$ specified at V_{GS} = 5V). The absolute maximum rating for V_{GS} is typically ±20V for standard MOSFETs. However, the V_{GS} maximum rating for logic-level MOSFETs ranges from ±8V to ±20V depending upon the manufacturer and the specific part number. The LTC4212's GATE overdrive as a function of V_{CC} is illustrated in the Typical Performance curves. Logic-level MOSFETs are recommended for low supply voltage applications and standard MOSFETs can be used for applications where supply voltage is greater than 4.75V.

Note that in some applications, the gate of the external MOSFET can discharge faster than the output voltage when the circuit breaker is tripped. This causes a negative V_{GS} voltage on the external MOSFET. Usually, the selected external MOSFET should have a $\pm V_{GS(MAX)}$ rating that is higher than the operating input supply voltage to ensure that the external MOSFET is not destroyed by a negative V_{GS} voltage. In addition, the $\pm V_{GS(MAX)}$ rating of the MOSFET must be higher than the gate overdrive voltage. Lower $\pm V_{GS(MAX)}$ rating MOSFETs can be used with the LTC4212 if the GATE overdrive is clamped to a lower voltage. The circuit in Figure 8 illustrates the use of zener diodes to clamp the LTC4212's GATE overdrive signal if lower voltage MOSFETs are used.



*USER SELECTED VOLTAGE CLAMP
(A LOW BIAS CURRENT ZENER DIODE IS RECOMMENDED)
1N4688 (5V)
1N4692 (7V): LOGIC-LEVEL MOSFET
1N4695 (9V)
1N4702 (15V): STANDARD-LEVEL MOSFET

Figure 8. Optional Gate Clamp for Lower $V_{GS(MAX)}$ MOSFETs

The $R_{DS(ON)}$ of the external pass transistor should be low to make its drain-source voltage (V_{DS}) a small percentage of V_{CC}. At a V_{CC} = 2.5V, V_{DS} + V_{RSENSE} = 0.1V yields 4% error at the output voltage. This restricts the choice of MOSFETs to very low $R_{DS(ON)}$. At higher V_{CC} voltages, the V_{DS} requirement can be relaxed in which case MOSFET package dissipation (P_D and T_J) may limit the value of $R_{DS(ON)}$. Table 6 lists some power MOSFETs that can be used with the LTC4212.

For reliable circuit operation, the maximum junction temperature ($T_{J(MAX)}$) for a power MOSFET should not exceed the manufacturer's recommended value. This includes normal mode operation, start-up, current-limit and autoretry mode in a fault condition. Under normal conditions the junction temperature of a power MOSFET is given by Equation 13:

MOSFET Junction Temperature,

$$T_{J(MAX)} \leq T_{A(MAX)} + \theta_{JA} \bullet P_D \quad (13)$$

OPERATION

where

$P_D = (I_{LOAD})^2 \bullet R_{DS(ON)}$

θ_{JA} = junction-to-ambient thermal resistance

$T_{A(MAX)}$ = maximum ambient temperature

If a short circuit happens during start-up, the external MOSFET can experience a big single pulse energy. This is especially true if the applications only employed a small gate capacitor or no gate capacitor at all. Consult the safe operating area (SOA) curve of the selected MOSFET to ensure that the $T_{J(MAX)}$ is not exceeded during start-up.

Using Staggered Pin Connectors

The LTC4212 can be used on either a printed circuit board or on the backplane side of the connector. Printed circuit board edge connectors with staggered pins are recommended as the insertion and removal of circuit boards do sequence the pin connections. Supply voltage and ground connections on the printed circuit board should be wired to the edge connector's long pins or blades. Control and status signals (like $\overline{FAULT}$ and ON) passing through the card's edge connector should be wired to short length pins or blades.

PCB Connection Sense

There are a number of ways to use the LTC4212's ON pin to detect whether the printed circuit board has been fully seated in the backplane before the LTC4212 commences a start-up cycle.

An example is shown in the schematic on the front page of this data sheet. In this case, the LTC4212 is mounted on the PCB and a 20k/10k resistive divider is connected to the ON pin. On the edge connector, R1 is wired to a short pin. Until the connectors are fully mated, the ON pin is held low, keeping the LTC4212 in an off state. Once the connectors are mated, the resistive divider is connected to V_{CC}, V_{ON} > 1.316V and the LTC4212 begins a start-up cycle.

PCB Layout Considerations

For proper operation of the LTC4212's circuit breaker function, a 4-wire Kelvin connection to the sense resistors is highly recommended. In Hot Swap applications where load currents can reach 10A or more, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately 0.54mΩ/square, track resistances add up quickly in high current applications. Thus, to keep PCB track resistance and temperature rise to a minimum, PCB track width must be appropriately sized. Consult Appendix A of LTC Application Note 69 for details on sizing and calculating trace resistances as a function of copper thickness.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1 ounce copper foil plating, a good starting point is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

APPENDIX

Table 5 lists some current sense resistors that can be used with the circuit breaker. Table 6 lists some power MOSFETs that are available. Table 7 lists the web sites of several manufacturers. Since this information is subject to change, please verify the part numbers with the manufacturer.

Table 5. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R050	0.05Ω 0.5W 1% Resistor	IRC-TT
2A	LR120601R025	0.025Ω 0.5W 1% Resistor	IRC-TT
2.5A	LR120601R020	0.02Ω 0.5W 1% Resistor	IRC-TT
3.3A	WSL2512R015F	0.015Ω 1W 1% Resistor	Vishay-Dale
5A	LR251201R010F	0.01Ω 1.5W 1% Resistor	IRC-TT
10A	WSR2R005F	0.005Ω 2W 1% Resistor	Vishay-Dale

APPENDIX

Table 6. N-Channel Selection Guide

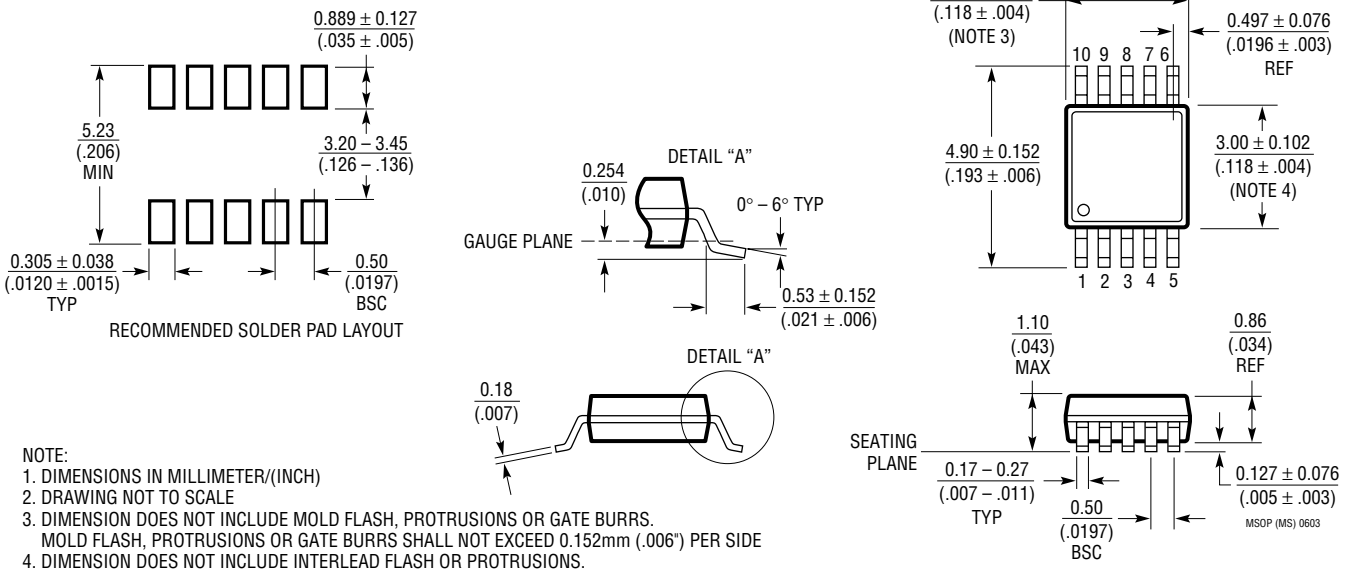
CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	MMDF3N02HD	Dual N-Channel SO-8 $R_{DS(ON)}$ = 0.1Ω, C_{ISS} = 455pF	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8 $R_{DS(ON)}$ = 0.025Ω, C_{ISS} = 1130pF	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.028Ω, C_{ISS} = 1570pF	ON Semiconductor
10 to 20	MTB75N05HD	Single N-Channel DD Pak $R_{DS(ON)}$ = 0.0095Ω, C_{ISS} = 2600pF	ON Semiconductor

Table 7. Manufacturers' Web Sites

MANUFACTURER	WEB SITE
TEMIC Semiconductor	www.temic.com
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
Harris Semiconductor	www.semi.harris.com
IRC-TT	www.irctt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

PACKAGE DESCRIPTION

MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX